RAiO

RA8815

128x33 Character/Graphic LCD Driver Specification

Version 2.1

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1. General Description

The RA8815 is a Dot-Matrix LCD Driver which supports both character and graphic mode. It built-in a 256Kbyte character ROM that consists of Chinese, English and ASCII fonts. The embedded 528Byte display RAM supports up to 128x33 dots LCD panel. The RA8815 also provides a scrolling buffer memory for scrolling functions. It supports up, down, left and right scrolling features, and all of the scrolling are execute by hardware.

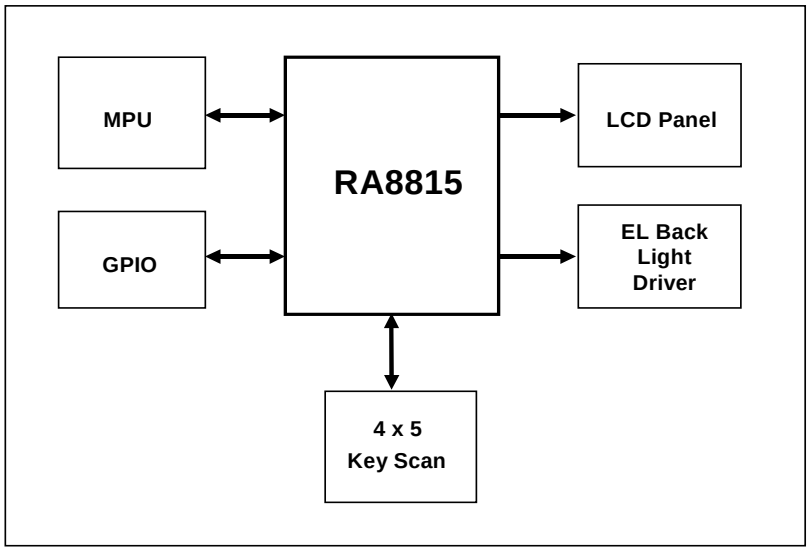
In character mode, the RA8815 supports Chinese BIG5 code or GB code. The system(MPU) does not need take a lot of time to show the Chinese font in graphic mode. It also provides small ASCII(8x8) and big ASCII(8x16) font for English character, Japanese, European and Latin. The RA8815 integrates many powerful hardware that including Contrast adjustment, 4x5 Key-Scan, eight General Purpose I/O and EL Backlight signals for EL driver.

The RA8815 is a high integration chip of LCD Controller. It reduce a lot of time for system develop, and save much cost for hardware system that due to it provides many features for related LCD display application.

2. Feature

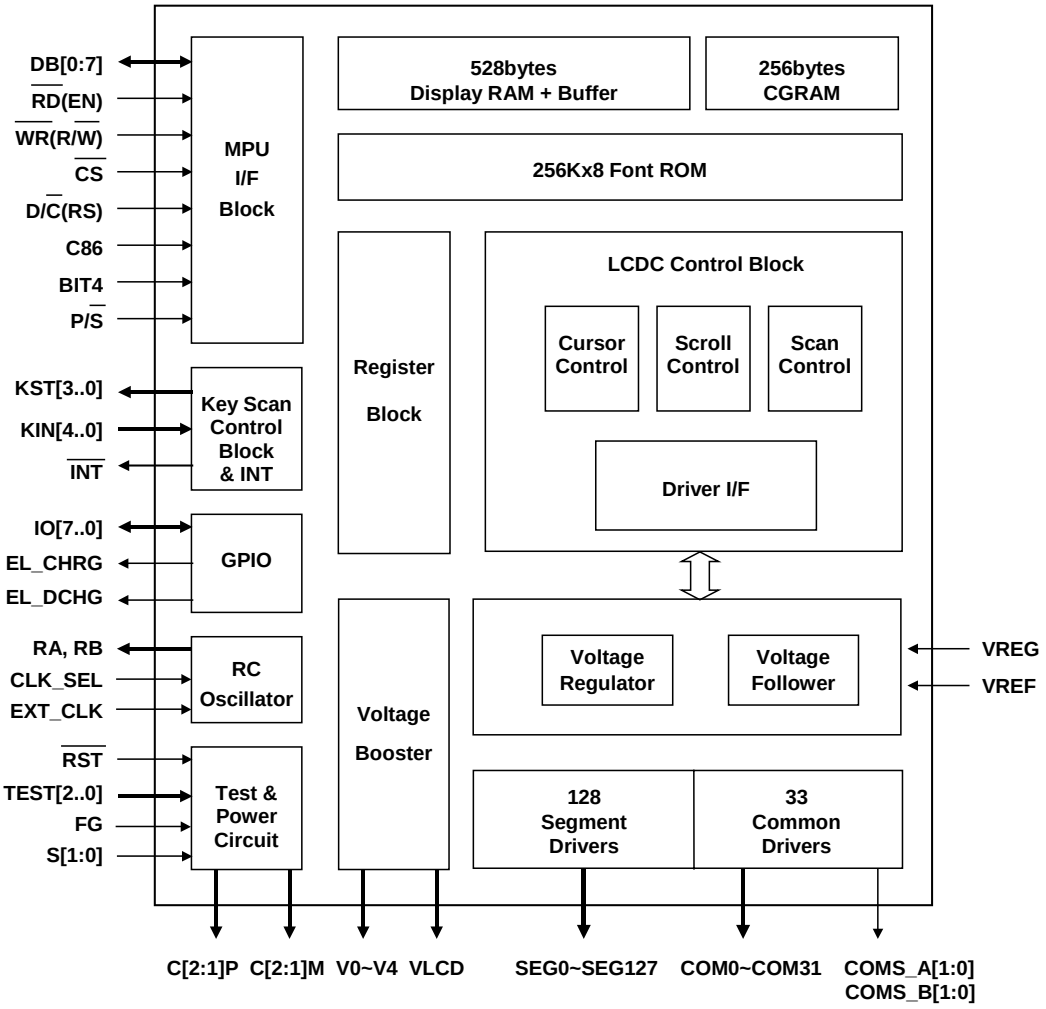
- Support both Character and Graphic Mode
- Support 8080/6800 8/4-bit Parallel Interface and 3-wire/4-wire Serial Interface
- Built-in 256KB Font ROM: Chinese, English, ASCII, Japanese, Latin, Latin-ext A, Latin-ext B
- Support ASCII 8x8/8x16 Half Size Font, 16x16 Full Size Chinese Font
- Support Maximum 128Seg x 33Com LCD Panel. 2 x 8 Chinese Fonts(16x16), or 4 x 16 English Fonts(8x8)
- Built-in 528 Bytes Display RAM and 354Byte Scrolling Buffer
- Built-in 256Byte SRAM for Create Font
- Built-in 2X~3X(Voltage Booster), Voltage Regulator, Voltage Follower
- Support 1/33 Duty, 1/6~1/4 Bias Panel
- Eight General Purpose I/O
- Built-in 4x5 Key Scan Circuit
- Support Horizontal/Vertical Scrolling Functions
- Provide Signals for EL Driver
- Provide 32-Steps Contrast Adjust
- Build-in RC Oscillator
- Voltage Operation : Chip → 2.5~3.6V, COG Module → 2.7~3.8V
- Package : Gold Bump Die

3. System Block Diagram



4. Block Diagram

The RA8815 is consist of Display RAM, 256Kbyte Font ROM, Command Registers, LCD Controller, LCD Driver, Voltage Booster, Voltage Regulator, MPU Interface and Key-Scan circuit.



5. Pin Definition

5-1 MPU Interface

Pin Name	I/O	Description
DB[7..0] DB0: SCK DB1: SDA/SDO DB2: RS/SDI DB3: $\overline{CS}$ DB[7:6]: SMOD	I/O	**Data Bus** When the MPU use parallel mode and 8-bit then all of the DB[7:0] are valid. When use 4-bit then only DB[4:0] are valid, and DB[7:4] have to keep floating. When P/$\overline{S}$ is "0", then the interface between MPU and RA8815 is Serial Mode. The pins DB[7:6](SMOD[1:0]) are used to select which serial mode:

		SMOD : Serial Mode --- 0 X : 3-Wire, SCK, SDA, $\overline{CS}$ are used. 1 0 : 4-Wire, SCK, SDA, RS, $\overline{CS}$ are used. 1 1 : 4-Wire, SCK, SDO, SDI, $\overline{CS}$ are used. In serial mode, all of the related signals are defined by DB[3:0]: SCK(DB0) : Serial Clock. SDA(DB1) : Bi-direction Mode Serial Data. SDO(DB1) : Data Out. RS(DB2) : Memory/Register Cycle Select. SDI(DB2) : Serial Data In. $\overline{CS}$(DB3) : Chip Select, active low. The unused pin must keep NC for serial mode.
$\overline{RD}$ EN	I	**Read Control or Enable** When use 8080 series interface, $\overline{RD}$ is the read signal and active low. When use 6800 series interface, EN is the Enable signal and active high. This pin must keep NC for serial mode.
$\overline{WR}$ R/$\overline{W}$	I	**Write Control or Read-Write Control** When use 8080 series interface, $\overline{WR}$ is the write signal and active low. When use 6800 series interface, this pin is R/$\overline{W}$, active high for read cycle and active low for write cycle. This pin must keep NC for serial mode.
D/$\overline{C}$ RS	I	**Data/Command Select or Register Select)** When use 8080 series interface, this is Data or Command signal. When D/$\overline{C}$ is “0”, means Register Cycle(or Command Cycle). When D/$\overline{C}$ is “1”, means Data Access Cycle(Data Cycle). When use 6800 series interface, this is the RS signal. When RS is “0”, means Register Cycle and “1” means Data Access Cycle. This pin must keep NC for serial mode.
$\overline{CS}$	I	**Chip Select** This is a chip enable for RA8815. This pin must keep NC for serial mode.
$\overline{INT}$	O	**Interrupt Signal** This is an interrupt output for MPU. Active low。
C86	I	**MPU Select** C86 = 0 ➔ The MPU interface is 8080 series. C86 = 1 ➔ The MPU interface is 6800 series(Default). This pin must keep NC for serial mode.
BIT4	I	**Data Bit Select** BIT4 = 0➔ The parallel mode is use 8-bit data bus. BIT4 = 1➔ The parallel mode is use 4-bit data bus(Default). This pin must keep NC for serial mode.

P/$\overline{S}$	I	**Parallel/Serial Select** P/$\overline{S}$ = 0 ➔ The MPU interface is serial mode(Default). See the setting of DB[7:6]. P/$\overline{S}$ = 1 ➔ The MPU interface is parallel mode.

5-2 LCD Panel Interface

Pin Name	I/O	Description
SEG0 ~ SEG127	O	**Segment Signals for Panel**
COM0 ~ COM31	O	**Common Signals for Panel**
COMS_A[1:0] COMS_B[1:0]	O	**Icon Common Signals for Panel**
DUM_L DUM_R	O	**Dummy PAD**

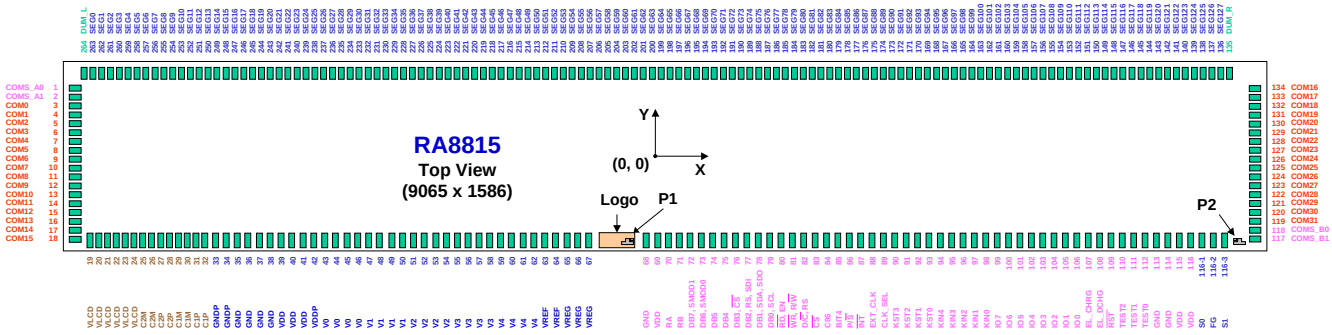
5-.3 Clock and Power

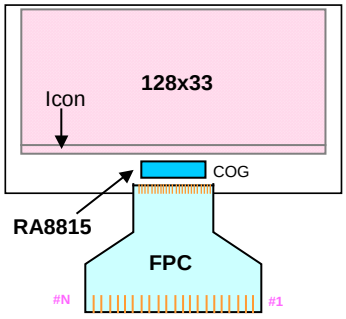
Pin Name	I/O	Description
RA, RB	I	**Resister Input** These are used to connect a resistor for internal oscillator.
V0~V4	O	**Voltage Source of LCD Driver** The relationship of the power is VLCD>VREG≧V0≧V1≧V2≧V3≧V4≧VSS。
C1P, C1M	I	**Capacitor Input** These are used to connect a capacitor for internal Booster.
C2P, C2M	I	**Capacitor Input** These are used to connect a capacitor for internal Booster.
VLCD	O	**Booster Output**
VREF	I	**Reference Voltage Input** This is the refeence voltage input when use an external regulator.
VREG	I	**Voltage Regulator Output** When the internal voltage regulator is disable, this pin is connect to VLCD and used to generate V0~V4.
CLK_SEL	I	**Clock Select** This pin is used to select the clock source. When CLK_SEL “1”, the clock is generated by internal oscillator and the external resistor that connect on RA and RB. When CLK_SEL is “0”, the system clock is drive by external pin - EXT_CLK.
EXT_CLK	I	**External Clock** When CLK_SEL is “0”, this pin is the external clock input. When CLK_SEL is “1”, this pin do not used and has to connect VDD or GND.
VDD VDDP	P	**VDD Power**
GND GNDP	P	**Ground**

5-4 Misc.

Pin Name	I/O	Description
KST[3..0]	O	**Key Strobe Output**
KIN[4..0]	I	**Key Data Input**
IO[7..0]	I/O	**General Purpose I/O**
EL_CHRG	O	**EL Charge Signal**
EL_DCHG	O	**EL Discharge Signal**
$\overline{RST}$	I	**Reset**
TEST[2..0] S[1:0], FG	I	**Test Pins** These pins must keep NC for normal mode.

6. Pad and Package





COG Module