NOVATEK
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Data Sheet

NT7607

16 Characters X 3 Lines + 80 icons

STN LCD Controller/Driver

V2.0

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Revision History

NT7607 Specification Revision History		
Version	**Content**	**Date**
1.0	Released	Oct 2006
2.0	Add ROM code table of D06.	Dec 2006

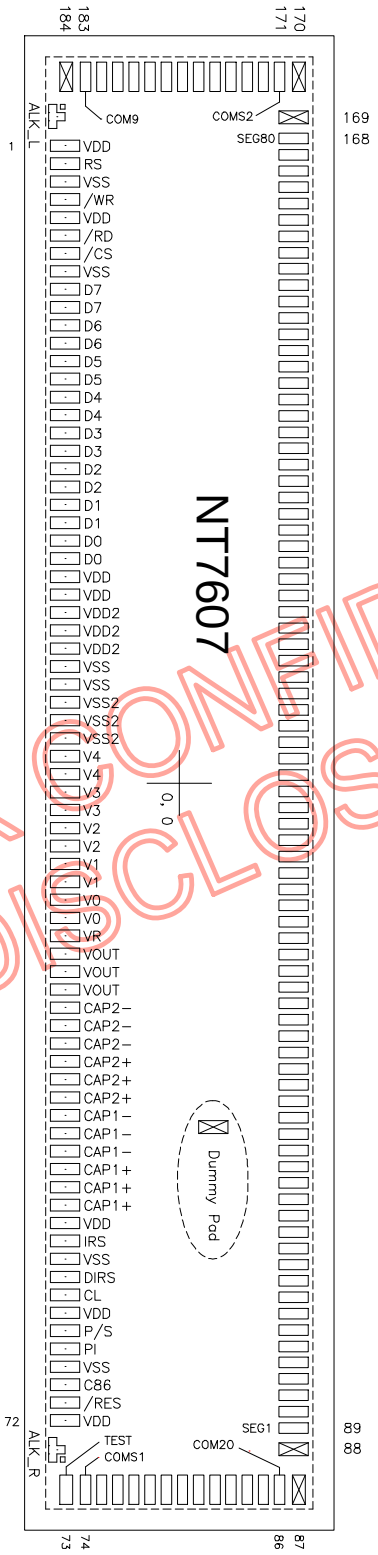
Features

- Single-chip LCD controller / driver
  - 26 common outputs
  - 80 segment outputs
- Applicable display panel
  - 2-line x 16 characters + 80 icons (1/17 duty)
  - 3-line x 16 characters + 80 icons (1/25 duty)
- 5 x 7 character format plus cursor; 5 x 8 for user defined symbols
- Character Generator ROM (CGROM)
  - 10,240 bits (256 characters x 5 x 8 dots)
  - Custom CGROM is also available
- Character Generator RAM (CGRAM): 320 bits (8 characters x 5 x 8 dots)
- Display Data RAM (DDRAM): 512 bits (16 characters x 4 lines x 8)
- Segment Icon Ram (ICONRAM): 80 bits (80 icons)
- Versatile functions provided on chip: Return home, Display control, Power save, Power control, etc.
- COM / SEG bi-directional (4-type LCD application available)
- On-chip oscillator requires no external components (external clock also possible)
- 2X / 3X DC-DC converter generation of LCD supply voltage
- Voltage regulator with electronic volume for contrast control (32 steps)
- Voltage follower & bias circuit
- Very low current consumption (VDD, VDD2 = 3.0 V):
  - Sleep mode: < 5 µA
  - Normal mode: < 80 µA
- Power supply voltage: VDD=1.8~3.6V, VDD2 = 2.4~3.6V
- Display supply voltage range (VLCD = V0 - VSS): VLCD = 4.0 to 7.0 V
- 80 / 67 Hz frequency selection of frame rate
- No busy check or no execution waiting time
- 4-bit or 8-bit parallel bus: 6800 and 8080
- Serial interface: 3-wire / 4-wire SPI
- CMOS process
- Available in COG form

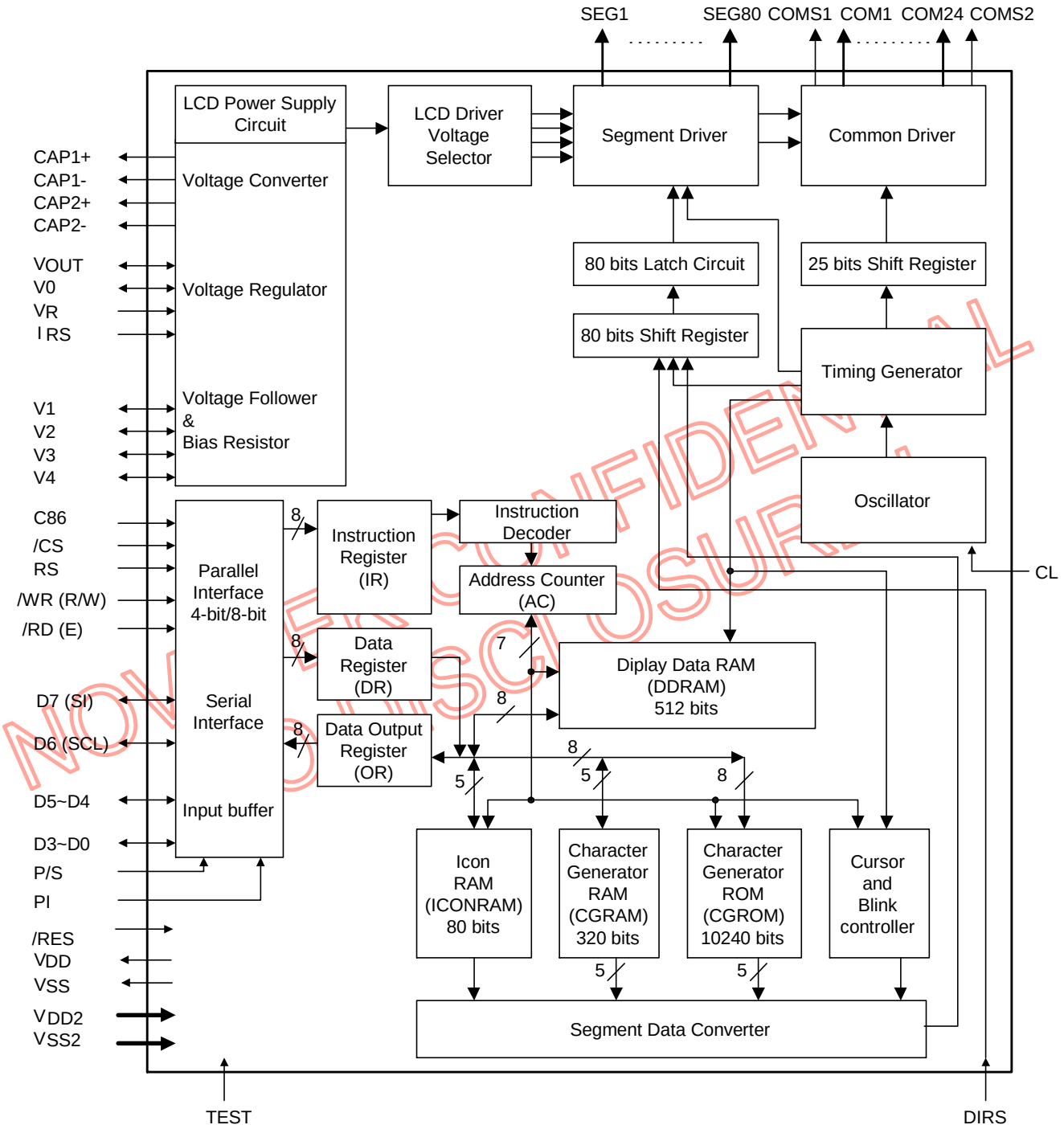
General Description

The NT7607 is a low power CMOS LCD controller and driver designed to drive a dot matrix LCD display of 2-line or 3-line by 16 characters with 5 × 8-dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower system current consumption. The NT7607 interfaces to most micro-controllers via a 4-bit / 8-bit parallel bus or via the 3SPI / 4SPI serial interface. The chip contains a character generator and displays alphanumeric character.

Pad Configuration



Block Diagram



Pad Descriptions

Power Supply

Pad No.	Designation	I/O	Description
25, 26	VDD	P	1.8 ~ 3.6 V power supply input for digital circuit
30, 31	VSS	P	Digital ground
1, 5, 61, 66, 72	VDD	O	1.8 ~ 3.6 V power supply output for pad option
3, 8, 63, 69	VSS	O	Ground output for pad option
27~29	VDD2	P	2.4 ~ 3.6 V power supply input for analog circuit
32~34	VSS2	P	Analog ground
43, 44 41, 42 39, 40 37, 38 35, 36	V0 V1 V2 V3 V4	P	LCD driver supply voltages. The voltage determined by LCD cell is impedance-converted by a resistive driver or an operation amplifier for application. Voltages should be the following relationship: V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS2 When the on-chip operating power circuit is on, the following voltages are given to V1 to V4 by the on-chip power circuit. Voltage selection is performed by the Set LCD Bias instruction.

LCD bias	V1	V2	V3	V4
1/4 bias	3/4 V0	2/4 V0		1/4 V0
1/5 bias	4/5 V0	3/5 V0	2/5 V0	1/5 V0

LCD Driver Supply

Pad No.	Designation	I/O	Description
55~57	CAP1-	O	Capacitor 1- pad for internal DC/DC voltage converter
58~60	CAP1+	O	Capacitor 1+ pad for internal DC/DC voltage converter
49~51	CAP2-	O	Capacitor 2- pad for internal DC/DC voltage converter
52~54	CAP2+	O	Capacitor 2+ pad for internal DC/DC voltage converter
46~48	VOUT	I/O	DC/DC voltage converter output.
45	VR	I	Voltage adjustment pad. Applies voltage between V0 and VSS using a resistive divider.

System Bus Connection Pads

Pad No.	Designation	I/O	Description
62	IRS	I	This terminal selects the resistors for the V0 voltage level adjustment. IRS = "H", Use the internal resistors IRS = "L", Do not use the internal resistors The V0 voltage level is regulated by an external resistive voltage divider attached to the VR terminal.
65	CL	I	External clock input. It must be fixed to "H" or "L" when the internal oscillation circuit is used. In case of the external clock mode, CL is used as the clock and OS bit should be OFF.
68	PI	I	Interface data length selection pin for parallel data input PI = "L": 4-bit data input mode. PI = "H": 8-bit data input mode.
70	C86	I	This is the MPU interface switch terminal. C86 = "L": 8080 Series MPU interface. C86 = "H": 6800 Series MPU interface.
67	P/S	I	This is the parallel data input/serial data input switch terminal. P/S = "L": Serial data input. P/S = "H": Parallel 4-bit / 8-bit data input. When P/S = "L", D0 to D5 are HZ. D0 to D5 may be "H" or "L" /RD (E) and /WR (R/W) are fixed to either "H" or "L". With serial data input, RAM display data reading is not supported.
64	DIRS	I	SEG direction selection input DIRS = "L": SEG1, SEG2, ……SEG79, SEG80 DIRS = "H": SEG80, SEG79, ……SEG2, SEG1
7	/CS	I	This is the chip select signal. When /CS = "L", then the chip select becomes active, and data/instruction I/O is enabled
71	/RES	I	When /RES is set to "L", the settings are initialized. The reset operation is performed by the /RES signal level.
6	/RD (E)	I	When connected to an 8080 Series MPU, it is low active. This pad is connected to the /RD signal of the 8080 MPU, and the NT7607 data bus is in an output status when this signal is "L". When connected to a 6800 Series MPU, this is active HIGH. This is used as an enable clock input of the 6800 series MPU.
4	/WR (R/W)	I	When connected to an 8080 Series MPU, this is low active. This terminal connects to the 8080 Series MPU /WR signal. The signals on the data bus are latched at the rising edge of the /WR signal. When connected to a 6800 Series MPU: This is the read/write control signal input terminal. R/W = "L": Write. R/W = "H": Read.

System Bus Connection Pads (continued)

Pad No.	Designation	I/O	Description
2	RS	I	Register selects signal input. RS = “L”: selects the instruction register RS = “H”: selects the data register
24~17 16~13 11, 12 9, 10	D0 ~ D3 D4 ~ D5 D6 (SCL) D7 (SI)	I/O	When 8-bit bus mode (P/S = “H” and PI = “H”), D0 ~ D7 are used as bi-directional data bus that connects to an 8-bit MPU data bus. When 4-bit bus mode (P/S = “H” and PI = “L”), D4 ~ D7 are used as bi-directional data bus that connects to a 4bit MPU data bus. And in this case D0 ~ D3 pins are not used and must always be fixed “H” or “L”. When the serial interface is selected (P/S = “L”), then D7 serves as the serial data input terminal (SI) and D6 serves as the serial clock input terminal (SCL). At this time, D0 to D5 are must always be fixed “H” or “L”. When the chip select is inactive, D0 to D7 are set to HZ.

System Bus Connection

Pad No.	Designation	I/O	Description
89~168	SEG1 ~ 80	O	Segment signal output for LCD display
75~86 172~183	COM1 ~ 24	O	Common signal output for LCD display.
74, 171	COMS1, COMS2	O	Common signal output for icon display COMS1 and COMS2 are the same signal, but name is different.

Dummy Pads

Pad No.	Designation	I/O	Description
87	Dummy1	-	Dummy pads. No connection for user.
88	Dummy2	-	
169	Dummy3	-	
170	Dummy4	-	
184	Dummy5	-	

Test Pad

Pad No.	Designation	I/O	Description
73	TEST	I	Test pad. No connection for user.

Functional Descriptions

Microprocessor Interface

NT7607 has two kinds of interface type with MPU: parallel mode, serial mode. Parallel or serial mode is selected by P/S pad. In parallel mode, 4-bit data bus or 8-bit data bus is selected by PI pad, and 6800 or 8080 MPU mode is selected by C86 pad.

Interface type selection

The NT7607 can transfer data via 4-bit bi-directional data bus (D7 to D4) / 8-bit bi-directional data bus (D7 to D0) or via serial data input (SI).
When high or low is selected for the parity of P/S pad, either 4-bit/ 8-bit parallel data input or serial data input can be selected. When serial data input is selected, the RAM data cannot be read out.

Table 1. Parallel or Serial MPU Interface according to P/S

P/S	C86	PI	Type	/CS	RS	/RD (E)	/WR (R/W)	D7	D6	D5, D4	D3 to D0
L	L	-	3-wire SPI	/CS	-	-	-	SI	SCL	-	-
	H	-	4-wire SPI	/CS	RS	-	-	SI	SCL	-	-
H	L	L	8080 series 4-bit	/CS	RS	/RD	/WR	D7 to D4			-
	L	H	8080 series 8-bit	/CS	RS	/RD	/WR	D7 to D0			
	H	L	6800 series 4-bit	/CS	RS	E	R/W	D7 to D4			-
	H	H	6800 series 8-bit	/CS	RS	E	R/W	D7 to D0			

Note: "-" must always be fixed "H" or "L".

Parallel Input (P/S is high)

When the NT7607 selects parallel input (P/S = high), the 4-bit or 8-bit parallel input mode can be selected by causing the PI pad to go high or low.

When the NT7607 selects parallel input (P/S = high), the 8080 series microprocessor or 6800 series microprocessor can be selected by causing the C86 pad to go high or low.
The NT7607 identifies the data bus signal according to RS, /RD (E) and /WR (R/W) signals.

Table 2. Parallel Interface Read/Write Status

C86	1		0		Function
Control	6800 processor		8080 processor		
RS	E	R/W	/RD	/WR	
0	1	1	0	1	Reads status
0	1	0	1	0	Writes instruction data
1	1	1	0	1	Reads display data
1	1	0	1	0	Writes display data

Serial Interface (P/S is low)

When the serial interface has been selected (P/S = “L”) then when the chip is in active state (/CS = “L”) the serial data input (SI) and the serial clock input (SCL) can be received. The serial data is read from the serial data input pin in the rising edge of the serial clocks D7, D6 through D0, in this order.
At the rising edge of the 8th serial clock, the serial data (D7 – D0) is converted into 8 bit bus mode data. The RS input of the DR/IR selection is latched in the rising edge of eighth serial clock (SCL) for the processing.

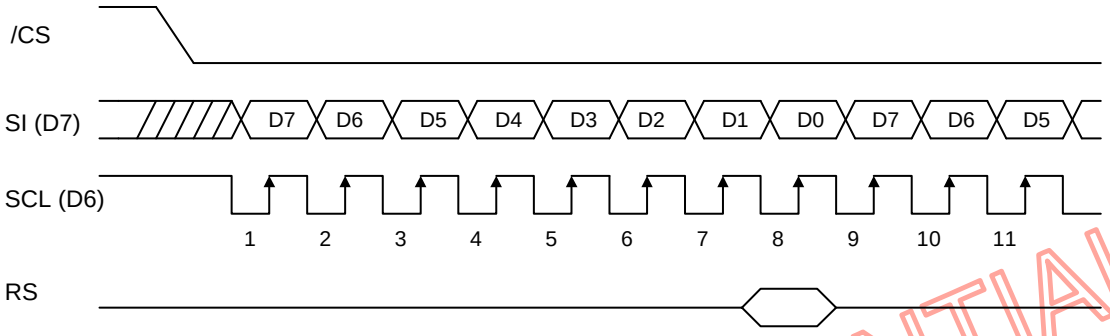


Figure 1. Diagram of 4-wire Serial Data Transfer

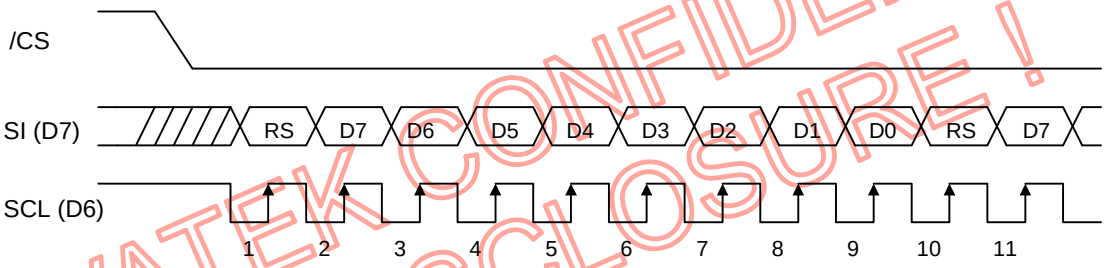


Figure 2. Diagram of 3-wire Serial Data Transfer

Note:
1. When the chip is not active, the shift registers and the counter is reset to their initial states.
2. Reading is not possible while in serial interface mode.
3. Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend the operation be rechecked on the actual equipment.

Chip Select Inputs

The NT7607 has one chip select pads. /CS can interface to a microprocessor when /CS is low . When this pads are set to high, D0 to D7 are high impedance and RS, /RD (E), /WR (R/W) inputs are disabled.

Registers

The NT7607 has three 8-bit registers, an Instruction Register (IR), and Data Register (DR) and an output data register (OR).

During writing operation, the Register Select signal (RS) determines which register will be accessed. The instruction registers stores instruction codes and address information for the Display Data RAM (DDRAM), Character Generator RAM (CGRAM) and Segment Icon RAM (ICONRAM).

During reading operation, output data register (OR) is used. The output data register temporarily stores data to be read from the DDRAM, CGRAM and ICONRAM and one of these RAM are selected by RAM address setting instruction. After RAM address setting, first reading is a dummy cycle in 8-bit bus mode. The valid data comes from second reading. In 4-bit bus mode, after RAM address setting, first and second reading is dummy cycles. The valid data comes from third reading. The dummy read make the address counter (AC) increased by 1.So it is recommended to set address again before writing, The instruction read cycle is not supported and it is regarded as a no operation cycle.

In 4-bit bus mode, it is needed to transfer 4-bit data (through D7~ D4) by two times .The high order bits (for 8-bit mode D7~D4) are written before the low order bits (for 8-bit mode D3~D0) in write and low order bits (for 8-bit mode D3~D0) are read before the high order bits (8-bit mode D3~D0) in read transaction. The D0~D3 pins are fixed “H” or “L” in this 4-bits bus mode. After /RES resets, NT7607 considers first 4-bit data from MPU as high order bits.

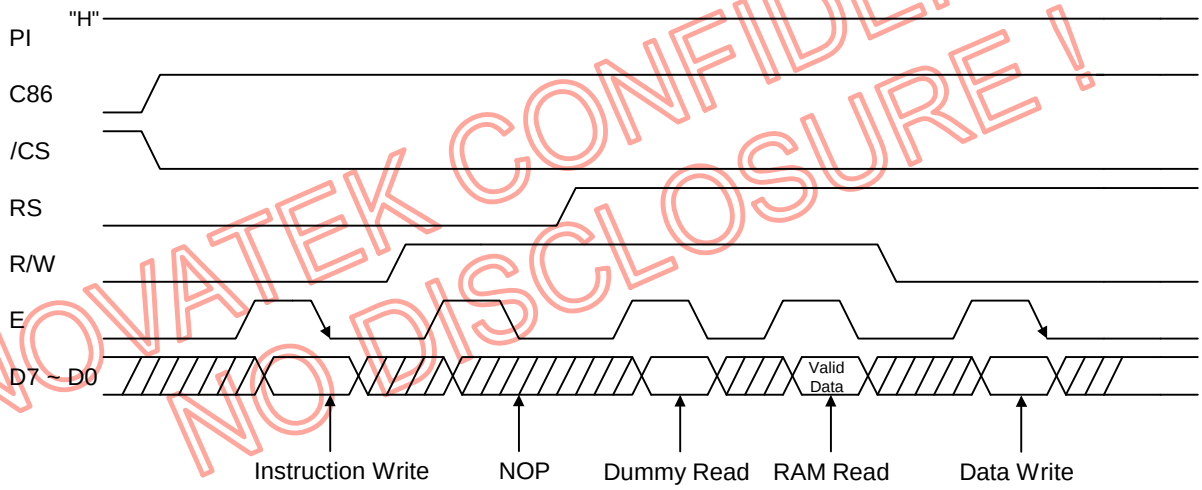


Figure 3. Diagram of 8-bit Parallel Bus Mode Data Transfer (6800 MPU Mode)

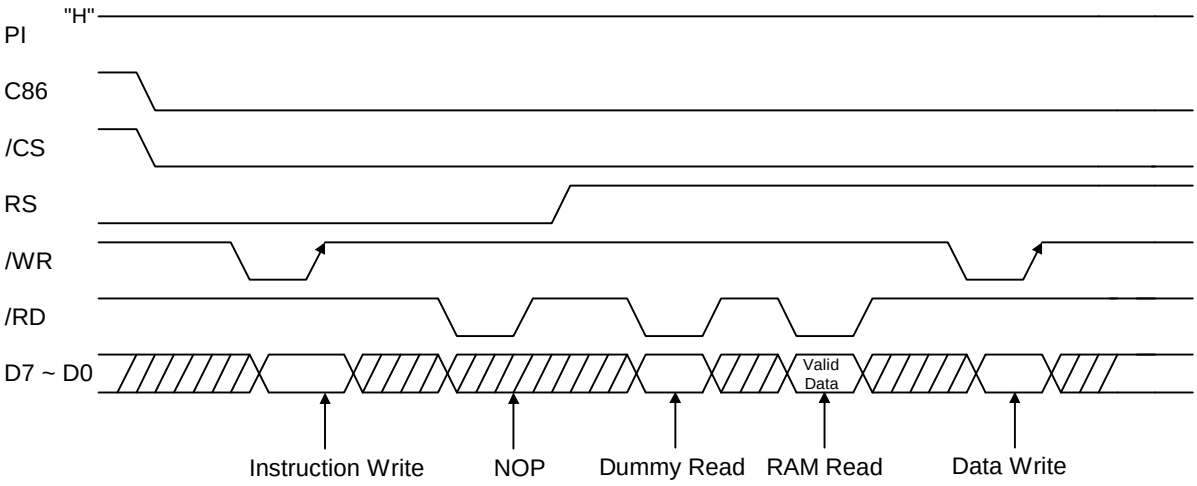


Figure 4. Diagram of 8-bit Parallel Bus Mode Data Transfer (8080 MPU Mode)

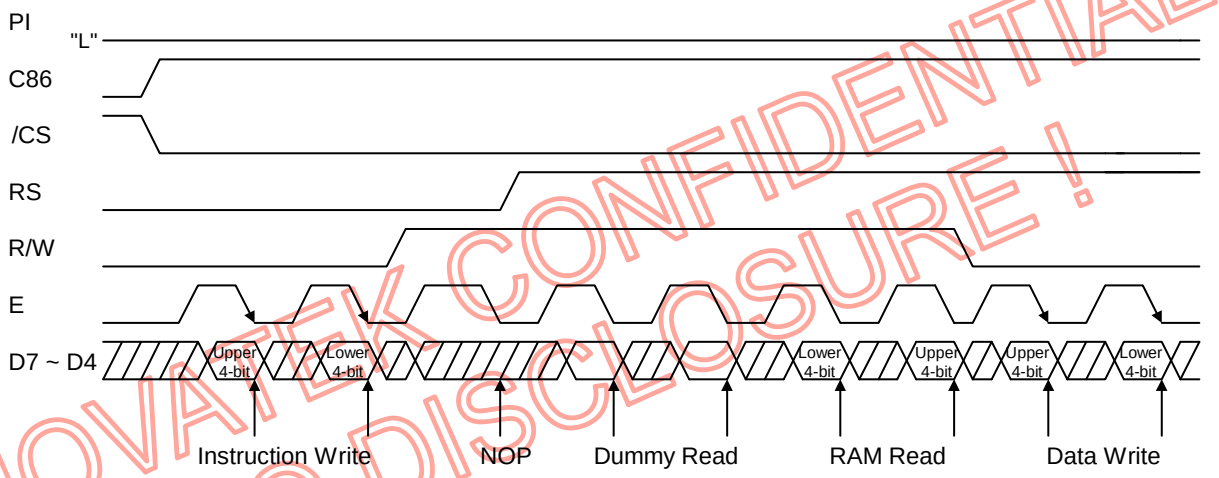


Figure 5. Diagram of 4-bit Parallel Bus Mode Data Transfer (6800 MPU Mode)

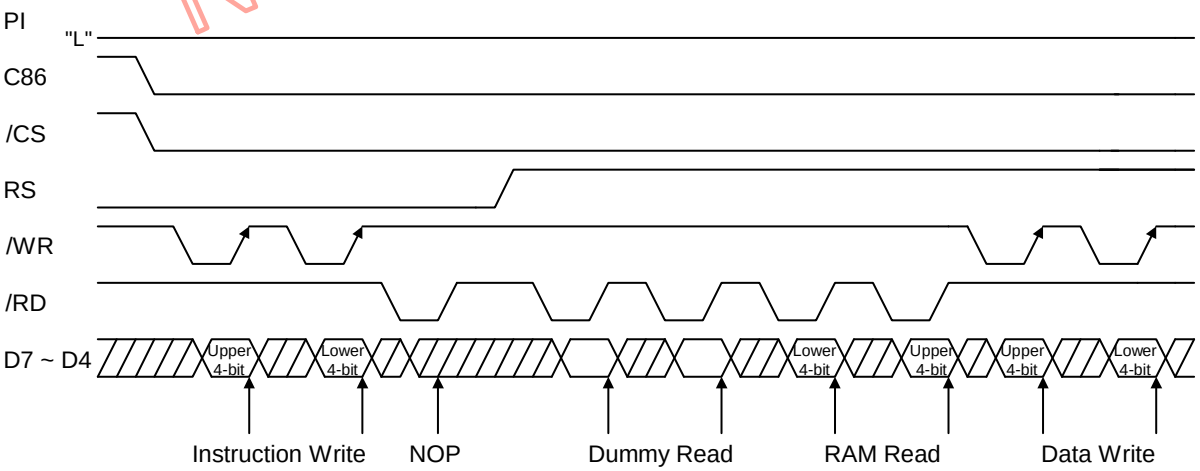


Figure 6. Diagram of 4-bit Parallel Bus Mode Data Transfer (8080 MPU Mode)

Address Counter (AC)

The address counter assigns addresses to the DDRAM CGRAM and ICONRAM for reading and writing and is set by the instructions ‘CGRAM address set’, ‘DDRAM address set’ and ‘ICONRAM address set’. After a read/write operation, the address counter is automatically incremented by 1.
The address counter content are only one and stores the address among DDRAM / CGRAM / ICONRAM.

Display Data RAM (DDRAM)

The DDRAM stores up to 64 characters of display data represented by 8-bit character codes. DDRAM address is set in the address counter (AC) as a hexadecimal number.

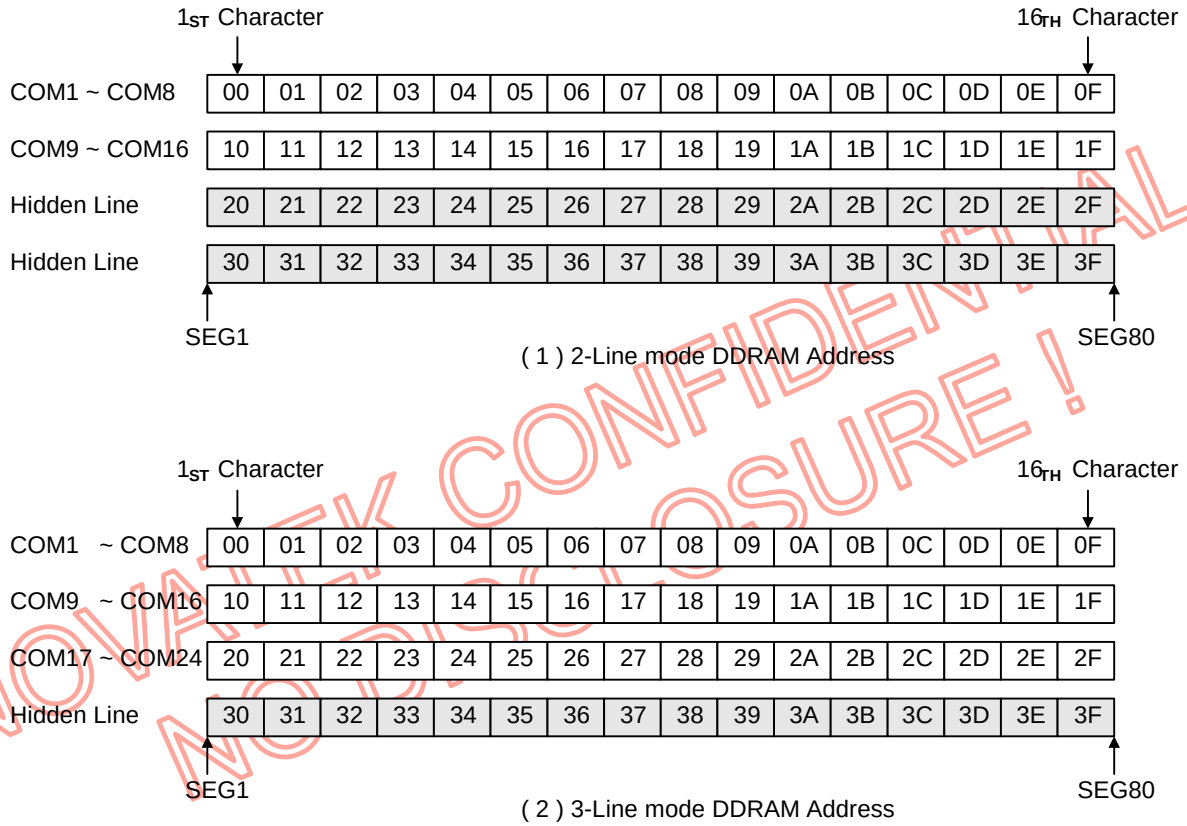


Figure 7. DDRAM Address

Character Generator ROM (CGROM)

The Character Generator ROM generates 256 character patterns in a 5 × 8-dot format from 8-bit character codes. The CG bit of the instruction table selects the 8 characters (00H ~ 07H) of CGROM or CGRAM. Table 3 shows the character set that is currently implemented.
User can define self-CGROM through changing MASK ROM.

Table 3-1. Character Standard Code in CGROM (D01)

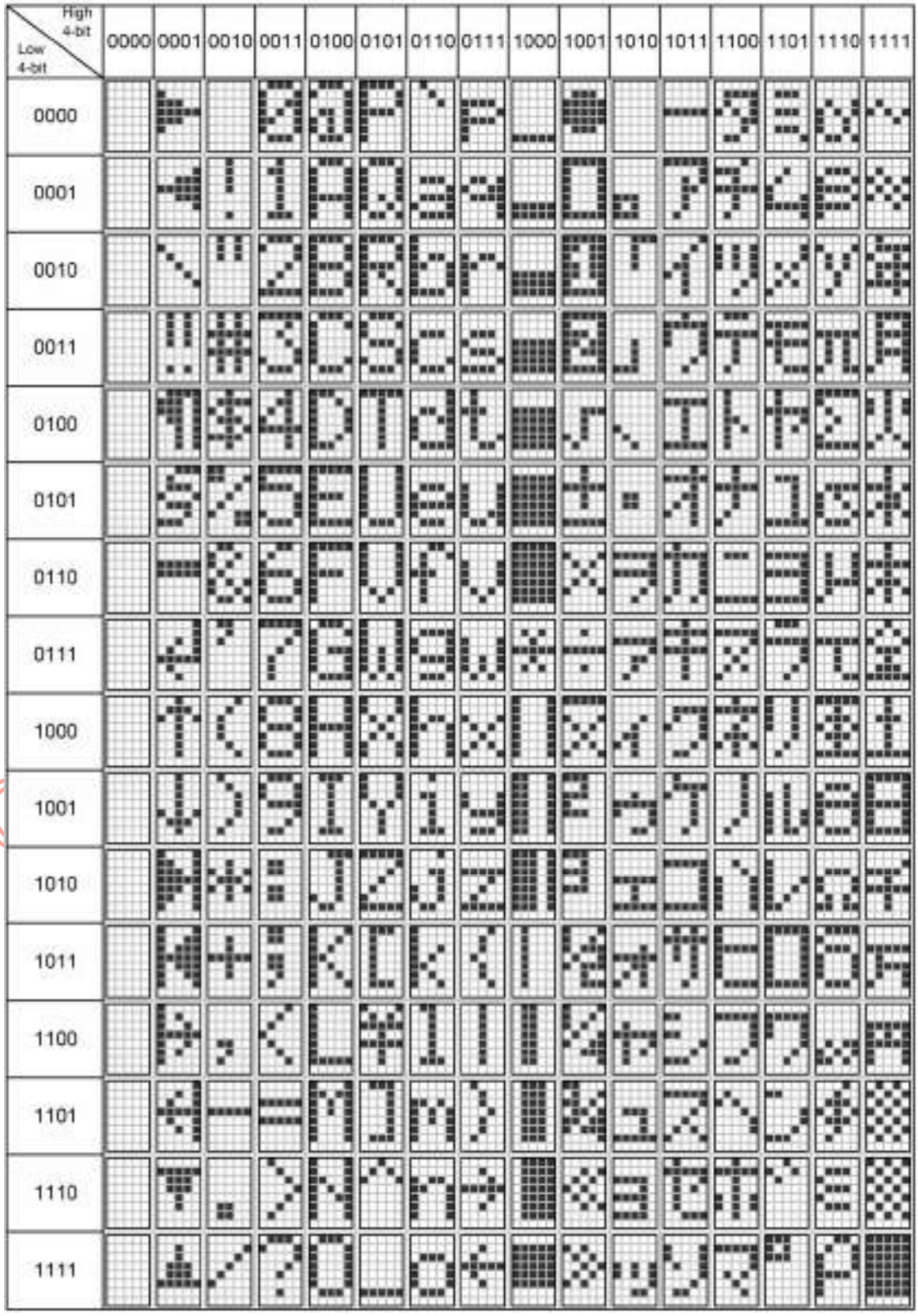
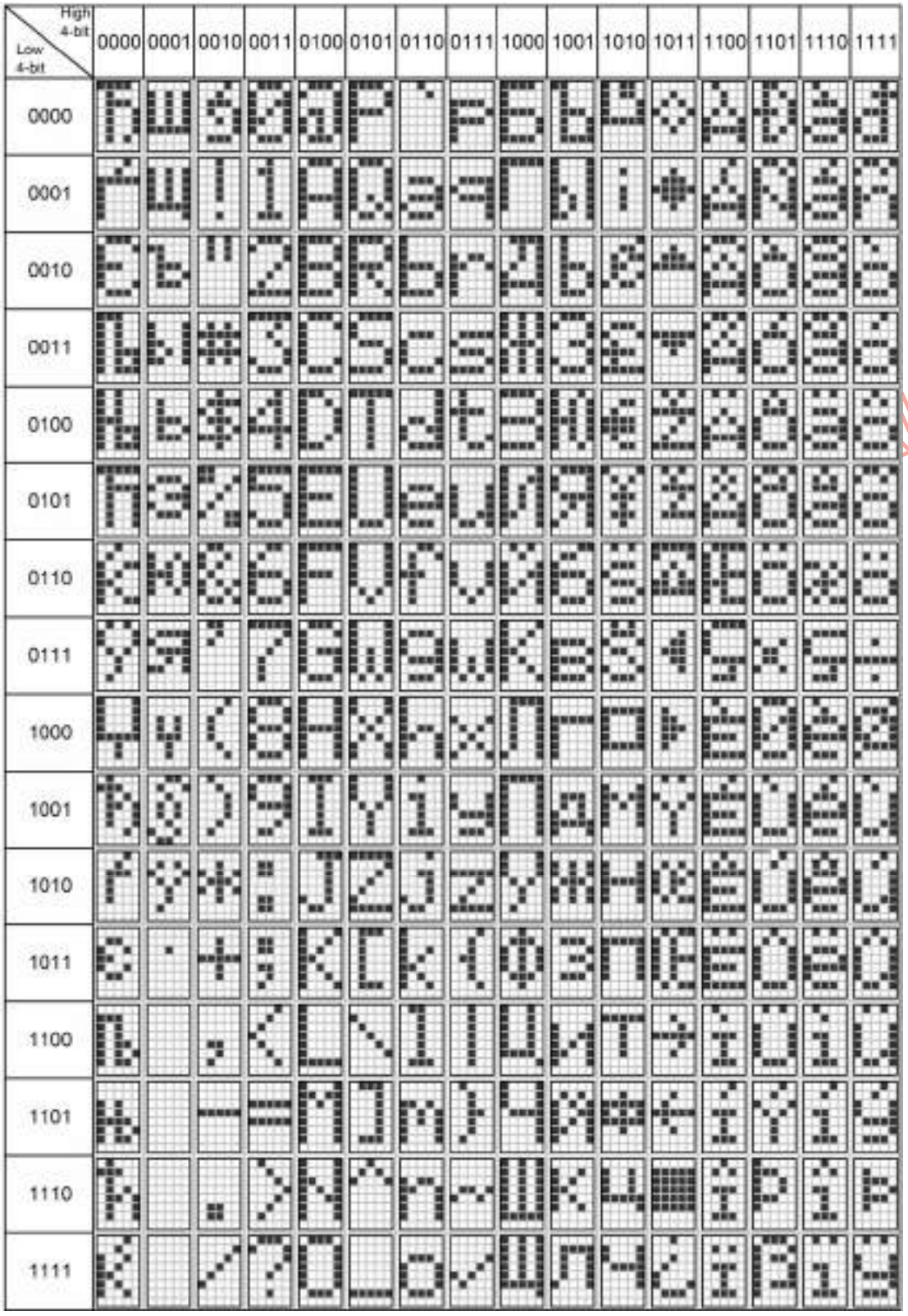


Table 3-2. Character Standard Code in CGROM (D06)



Character Generator RAM (CGRAM)

CGRAM has up to 5 × 8 dot 8 characters. By writing font data to CGRAM, use defined character can be used. CGRAM can be written regardless of CG bit.

Table 4. Relationship between CGRAM addresses data and display patterns

Character codes (DDRAM data)								DD / CGRAM address							CGRAM data (example)										Pattern No.
Higher Order bits					Lower			Higher Order bits					Lower		Character patterns					Character code					
D7	D6	D5	D4	D3	D2	D1	D0	A6	A5	A4	A3	A2	A1	A0	4	3	2	1	0	4	3	2	1	0	
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0						0	1	0	1	0	Pattern 0
												0	0	1						1	0	1	0	1	
												0	1	0						0	1	0	1	0	
			(00H)									0	1	1						1	0	1	0	1	
												1	0	0						0	1	0	1	0	
												1	0	1						1	0	1	0	1	
												1	1	0						0	1	0	1	0	
												1	1	1						1	0	1	0	1	
0	0	0	0	0	0	0	1	1	0	0	1	0	0	0						0	0	0	0	0	Pattern 1
												0	0	1						1	1	1	1	1	
												0	1	0						0	0	0	0	0	
			(01H)									0	1	1						1	1	1	1	1	
												1	0	0						0	0	0	0	0	
												1	0	1						1	1	1	1	1	
												1	1	0						0	0	0	0	0	
												1	1	1						1	1	1	1	1	
0	0	0	0	0	0	1	0	1	0	1	0	0	0	0						0	1	0	1	0	Pattern 2
												0	0	1						0	1	0	1	0	
												0	1	0						0	1	0	1	0	
			(02H)									0	1	1						0	1	0	1	0	
												1	0	0						0	1	0	1	0	
												1	0	1						0	1	0	1	0	
												1	1	0						0	1	0	1	0	
												1	1	1						0	1	0	1	0	
0	0	0	0	0	0	1	1	1	0	1	1	0	0	0						0	1	1	1	0	Pattern 3
												0	0	1						1	0	1	0	1	
												0	1	0						1	1	0	1	1	
			(03H)									0	1	1						1	0	1	0	1	
												1	0	0						0	1	1	1	0	
												1	0	1						1	1	1	1	1	
												1	1	0						1	1	1	1	1	
												1	1	1						1	1	1	1	1	
0	0	0	0	0	1	0	0	1	1	0	0	0	0	0						1	1	0	1	1	Pattern 4
												0	0	1						1	0	0	0	1	
												0	1	0						0	0	0	0	0	
			(04H)									0	1	1						1	0	0	0	1	
												1	0	0						1	1	0	1	1	
												1	0	1						1	1	1	1	1	
												1	1	0						1	1	1	1	1	
												1	1	1						1	1	1	1	1	
0	0	0	0	0	1	0	1	1	1	0	1	0	0	0						1	1	1	1	1	Pattern 5
												0	0	1						1	1	1	1	1	
												0	1	0						0	0	0	0	0	
			(05H)									0	1	1						0	0	0	0	0	
												1	0	0						1	1	1	1	1	
												1	0	1						1	1	1	1	1	
												1	1	0						0	0	0	0	0	
												1	1	1						0	0	0	0	0	

Table 4. Relationship between CGRAM addresses data and display patterns (Continued)

Character codes (DDRAM data)								DD / CGRAM address							CGRAM data (example)										Pattern No.
Higher			Order bits				Lower	Higher			Order bits			Lower	Character patterns					Character code					
D7	D6	D5	D4	D3	D2	D1	D0	A6	A5	A4	A3	A2	A1	A0	4	3	2	1	0	4	3	2	1	0	
0	0	0	0	0	1	1	0	1	1	1	0	0	0	0						0	0	1	1	0	Pattern 6
												0	0	1						0	0	1	1	0	
												0	1	0						0	0	1	1	0	
			(06H)									0	1	1						0	0	1	1	0	
												1	0	0						0	0	1	1	0	
												1	0	1						0	0	1	1	0	
												1	1	0						0	0	1	1	0	
												1	1	1						0	0	1	1	0	
0	0	0	0	0	1	1	1	1	1	1	1	0	0	0						0	0	0	0	0	Pattern 7
												0	0	1						1	0	0	0	1	
												0	1	0						1	1	0	1	1	
			(07H)									0	1	1						1	0	0	0	1	
												1	0	0						0	0	0	0	0	
												1	0	1						1	0	0	0	1	
												1	1	0						1	1	0	1	1	
												1	1	1						1	1	1	1	1	

Segment ICON RAM (ICONRAM)

The ICONRAM has segment control data and segment pattern data. COMS1 and COMS2 are the same signals, but the name is different. The number of icons is 80.

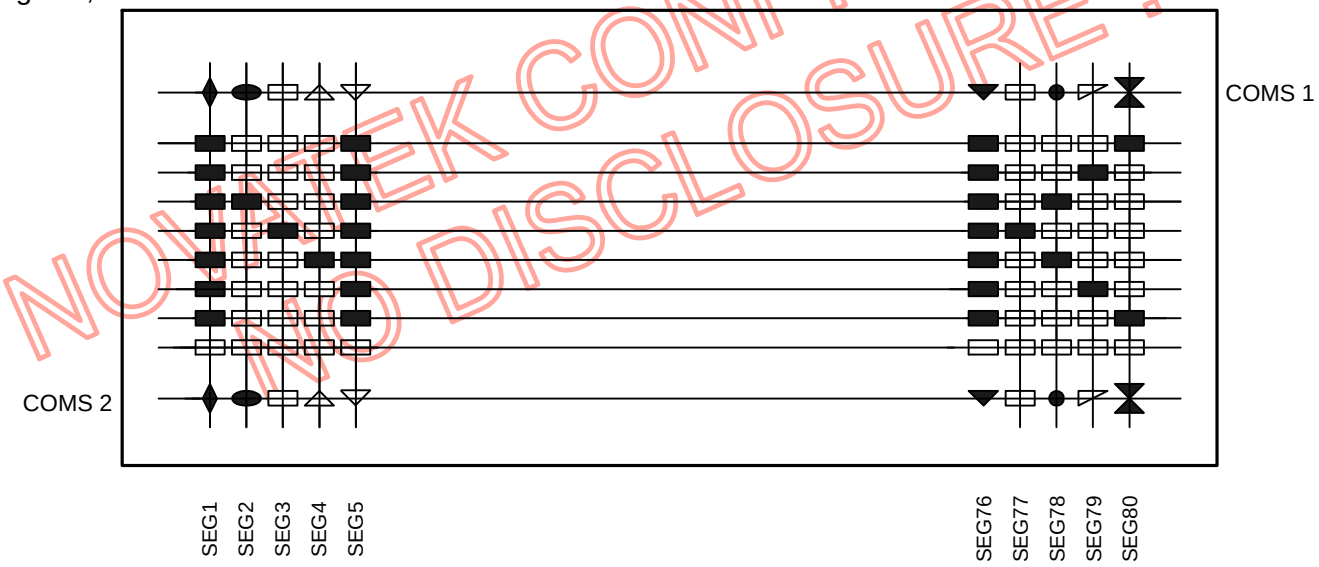


Figure 8. Relationship between ICONRAM and Icon Display

Table 5. Relationship between ICONRAM addresses data and display patterns

ICONRAM address	ICONRAM Bits							
	D7	D6	D5	D4	D3	D2	D1	D0
00H	-	-	-	S1	S2	S3	S4	S5
01H	-	-	-	S6	S7	S8	S9	S10
.	.	.	.	.	.	.	.	.
0EH	-	-	-	S71	S72	S73	S74	S75
0FH	-	-	-	S76	S77	S78	S79	S80

Note: "-" Don't care.

Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required and the CL pad must be connected to "H" or "L" when the internal oscillation circuit is used. In case of the external clock mode, CL is used as the clock and OS bit should be OFF.

Frame frequency (Frame Frequency Select Bit OFF)

- 1/17 Duty (2-line mode)

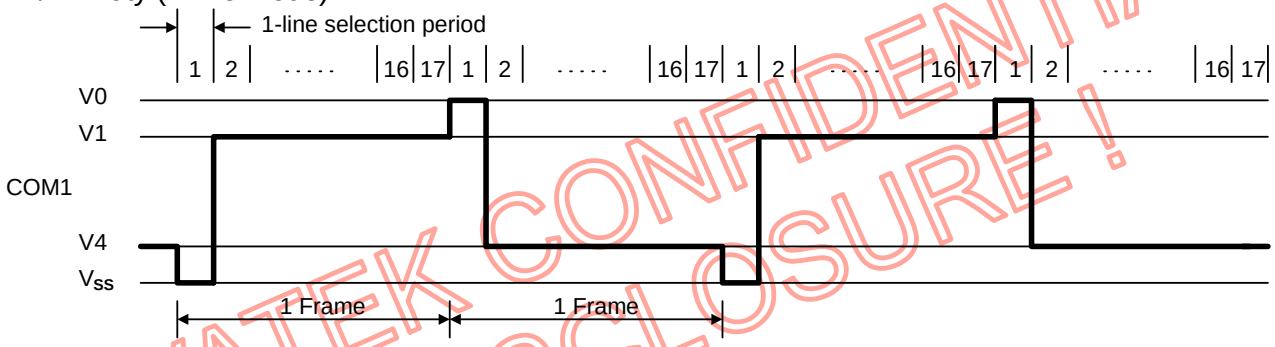


Figure 9. 2-Line Mode Frame Frequency

1-line Selection Period = 16 clocks
One Frame = 16 × 17 × 46.0 µs = 12.5 ms (1 Clock = 46.0µs at Fosc = 21.76 KHz)
Frame Frequency = 1/12.5 ms = 80 Hz

- 1/25 Duty (3-line mode)

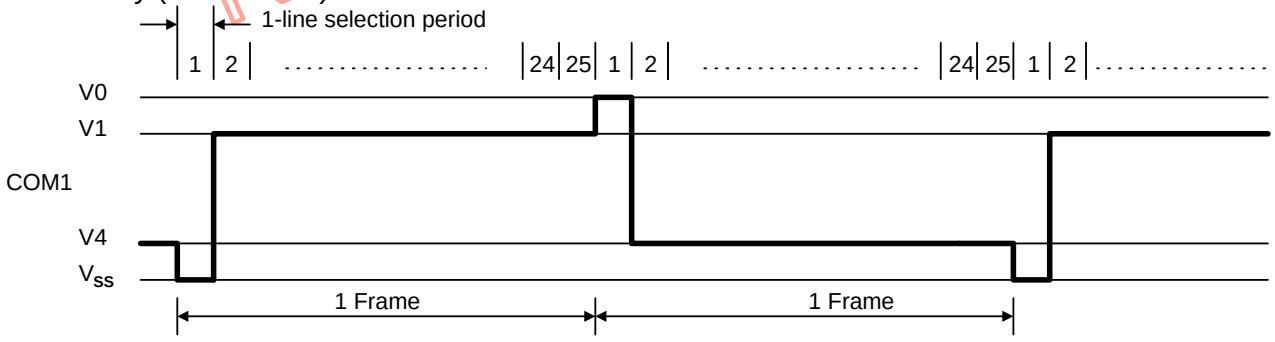


Figure 10. 3-Line Mode Frame Frequency

1-line Selection Period = 16 clocks
One Frame = 16 × 25× 31.25 µs = 12.5 ms (1 Clock = 31.25µs at Fosc = 32 KHz)
Frame Frequency = 1/12.5 ms = 80 Hz

Sleep mode (Power Save Bit ON, Oscillation Bit OFF)

NT7607 provides with sleep mode for saving power consumption during standby period.
To enter the sleep mode, the power circuit and oscillation circuit should be turned off by using the power save instruction and the power control instruction. This mode helps to save power consumption by reducing current to reset level.

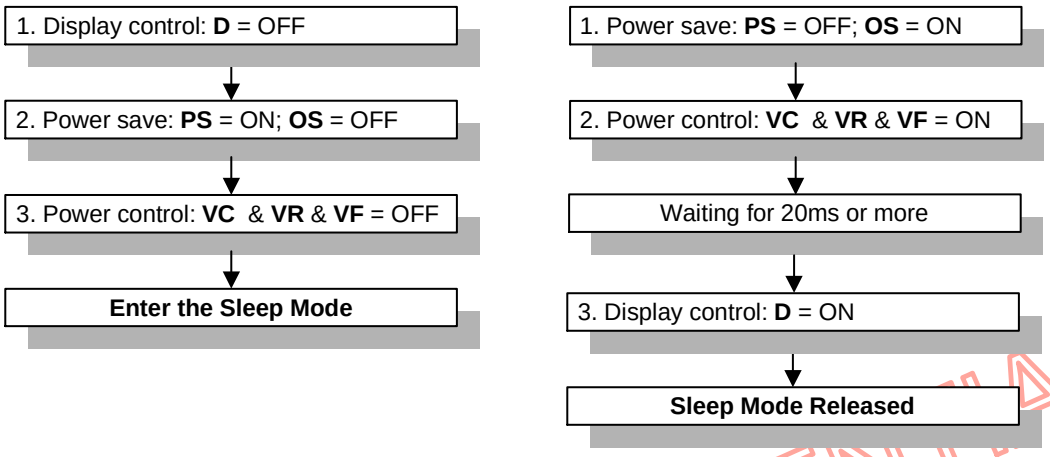


Figure 11. Sleep Mode Set or Release by Instructions

1. Liquid Crystal Display Output
   COM1 ~ COM24, COMS1, COMS2: VSS level. SEG1 ~ SEG80: VSS level
2. Data written in DDRAM, CGRAM, ICONRAM and registers are remained as previous value.
3. Operation mode is retained the same as it was prior to execution of the sleep mode.
   All internal circuits are stopped.
4. Power Circuit and Oscillation Circuit.
   The build-in power supply circuit and oscillation circuit are turned off by power save instruction and power control instruction.

LCD common and segment drivers

The NT7607 contains 26 common and 80 segment drivers, which connect the appropriate LCD bias voltages in sequence to the display in accordance with the data to be displayed. COMS1 and COMS2 drive the icon common. The bias voltages and the timing are selected automatically when the number of lines in the display is selected.

Table 6. SEG Data Shift Direction

DIRS pad	SEG data shift direction
L	SEG1, SEG2, SEG3, ……;·SEG78, SEG79, SEG80
H	SEG80, SEG79, SEG78, ……;·SEG3, SEG2, SEG1

Table 7. COM Data Shift Direction

Line mode	S	COM data shift direction
2-Line mode	0 (left)	COM1, COM2, ……,·COM16, COMS1 (COMS2)
	1 (right)	COMS1 (COMS2), COM16, ……,·COM2, COM1
3-Line mode	0 (left)	COM1, COM2, ……,·COM24, COMS1 (COMS2)
	1 (right)	COMS1 (COMS2), COM24, ……,·COM2, COM1

LCD supply voltage generator

The power supply circuits are low-power consumption power supply circuits that generate the voltage levels required for the liquid crystal drivers. They comprise DC-DC converter circuits, voltage regulator circuits, and voltage follower circuits. The power supply circuits can turn the Booster circuits, the voltage regulator circuits, and the voltage follower circuits ON or OFF independently through the use of the Power Control Set instruction. Consequently, it is possible to make an external power supply and the internal power supply function somewhat in parallel. Table 8 shows the Power Control Set Instruction 3-bit data control function, and Table 9 shows reference combinations.

Table 8. The Control Details of Each Bit of the Power Control Set Instruction

Item	Status "1"	Status "0"
VC: DC-DC converter (V/C) circuit control bit	ON	OFF
VR: Voltage regulator circuit (V/R) control bit	ON	OFF
VF: Voltage follower circuit (V/F) control bit	ON	OFF

Table 9. LCD Power Supply Combinations

Use Settings	VC	VR	VF	Voltage converter circuit	Voltage regulator circuit	Voltage follower circuit	External voltage input	Step-up voltage system terminal
Only the internal power supply is used	1	1	1	ON	ON	ON	VDD2	Used
Only the V regulator circuit and the V/F circuit are used	0	1	1	OFF	ON	ON	VOUT, VDD2	Open
Only the V/F circuit is used	0	0	1	OFF	OFF	ON	V0, VDD2	Open
Only the external power supply is used	0	0	0	OFF	OFF	OFF	V0 to V4, VDD2	Open

*The "step-up system terminals" refer CAP1+, CAP1-, CAP2+ and CAP2-.

*While other combinations, not shown above, are also possible, these combinations are not recommended because they have no practical use.

The Voltage DC-DC Converter Circuits

Using the step-up voltage circuits equipped within the NT7607 chips it is possible to product 2X, 3X Step-up of the VDD2 - VSS voltage levels. VOUT is generated from the voltage converter. And this conversion voltage is used in the build-in Voltage Regulator circuit. Figure 12 shows the application circuit of 2-time and 3-time DC-DC converter.

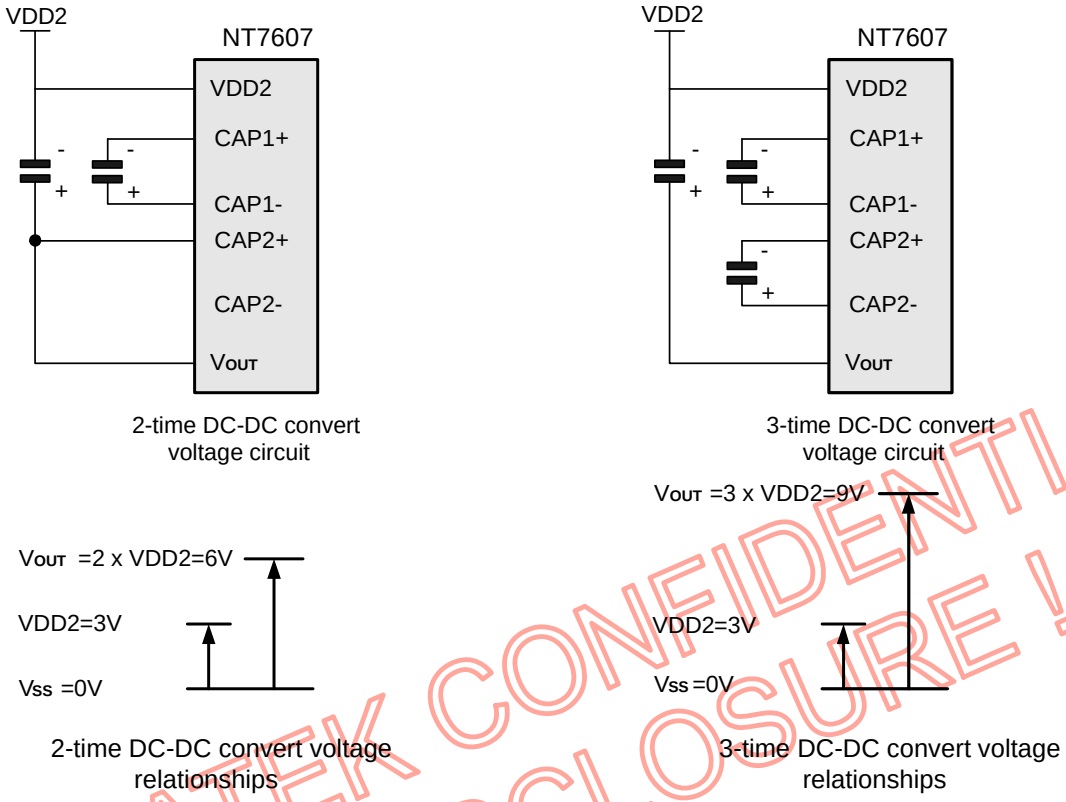


Figure 12. Voltage DC-DC Converter Circuit and Output

The Voltage regulator circuit

The step-up voltage generated at V_{OUT} outputs the liquid crystal driver voltage V0 through the voltage regulator circuit. Because the NT7607 chips have an internal high-accuracy fixed voltage power supply with a 32-level electronic volume function and external resistors for the V0 voltage regulator.
Moreover, the internal VREF of voltage regulator has the temperature compensation function, and the temperature coefficient is about 0.0%/°C.

Using External Resistors to Adjust V0 Voltage Regulator

Through the use of the V0 voltage regulator external resistors and the electronic volume function the liquid crystal power supply voltage V0 can be controlled (with adding two external resistors: Ra and Rb), making it possible to adjust the liquid crystal display brightness. The V0 voltage can be calculated using equation A-1 over the range where V0 < VOUT.

$V0 = (1+Rb/Ra)*V_{EV} = (1+Rb/Ra)* (1-\alpha/150)*VREF$ (Equation A-1)

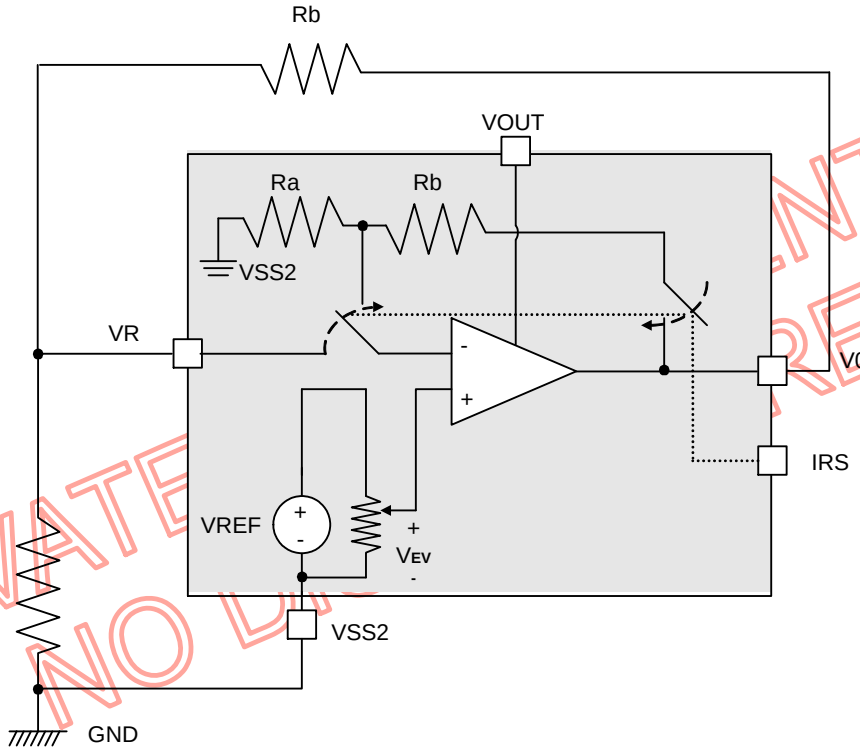


Figure 13. Voltage Regulator and Electronic Contrast Control Circuit

VREF is the IC internal fixed voltage supply, and its voltage at Ta = 25°C is as shown in Table 10.

Table 10. Voltage VREF Selection

Equipment Type	Thermal Gradient	Units	VREF
Internal power Supply	-0.05	%/°C	2.0V

α is set to 1 level of 32 possible levels by the electronic volume function depending on the data set in the 5-bit electronic volume register. Table 11 shows the value for α depending on the electronic volume register settings. Rb/Ra is the V0 voltage regulator internal resistor ratio, and can be set to 4 different

levels through the V0 voltage regulator internal resistor ratio set command. The (1+Rb/Ra) ratio assumes the values shown in Table 12 depending on the 2bit data settings in the V0 voltage regulator internal resistor ratio register.

Table 11. Electronic Contrast Control

D7	D6	D5	D4	D3	D2	D1	D0	α	V_0	Contrast
-	-	-	0	0	0	0	0	0 (default)	Maximum	High
-	-	-	0	0	0	0	1	1	:	:
-	-	-	0	0	0	1	0	2	:	:
				:			:	:	:	:
				:			:	:	:	:
-	-	-	1	1	1	1	0	30	:	:
-	-	-	1	1	1	1	1	31	Minimum	Low

Note: "-" Don't care.

V0 voltage regulator internal resistance ratio register value and (1+ Rb/Ra) ratio (Reference value)

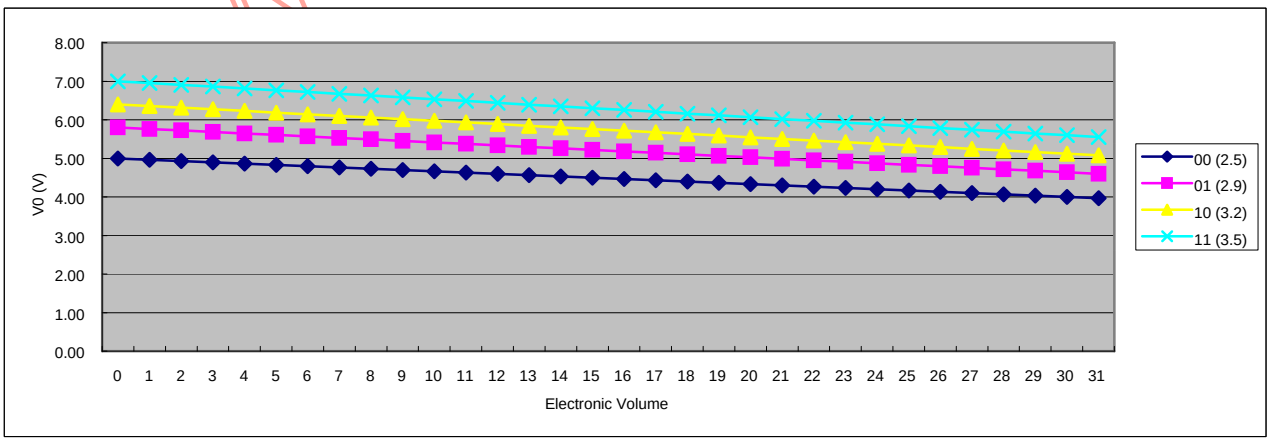
Table 12. Rb/Ra ratio

Register RR[1:0]								Equipment Type by Thermal Gradient [Units:%/°C]
D7	D6	D5	D4	D3	D2	D1	D0	-0.05
0	1	1	0	0	0	0	0	2.5
0	1	1	0	0	0	0	1	2.9 (default)
0	1	1	0	0	0	1	0	3.2
0	1	1	0	0	0	1	1	3.5

The V0 voltage as a function of the V0 voltage regulator internal resistor ratio register and the electronic volume register.

Note: When selecting external Rb/Ra resistors, Ra+Rb should be greater than 1.5M.

Figure 14. The Contrast Curve of V0 Voltage with internal resistors



Setup example: When selecting Ta = 25°C and V0 = 5V for an NT7607 model on which internal resistor is used. The equation A-1, the following setup is enabled.

Table 13. Example of V0 Voltage Adjust

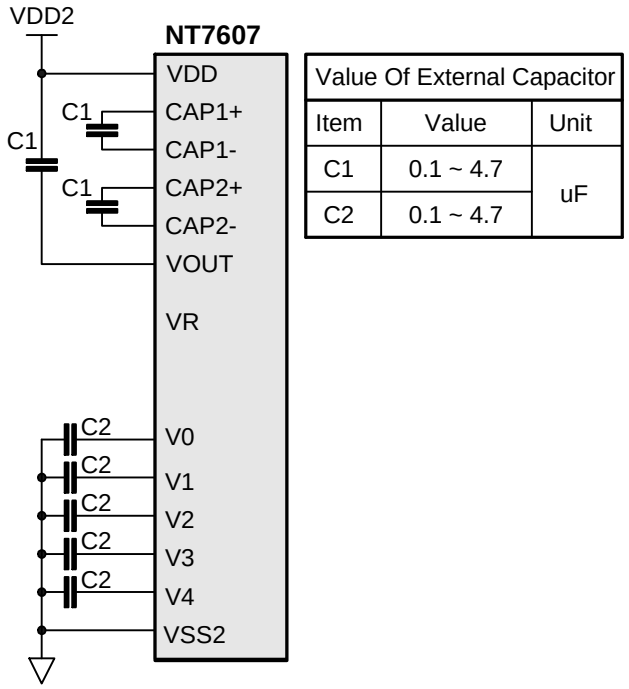
Contents	Register							
	D7	D6	D5	D4	D3	D2	D1	D0
Internal Rb/Ra ratio	0	1	1	0	0	0	0	1
Electronic Volume	0	0	0	1	0	1	0	1

- When the V0 voltage regulator internal resistors or the electronic volume function is used, it is necessary to at least set the voltage regulator circuit and the voltage follower circuit to an operating mode using the power control set commands. Moreover, it is necessary to provide a voltage from VOUT when the Booster circuit is OFF.
- The VR terminal is enabled only when the V0 voltage regulator internal resistors are not used (i.e. the IRS terminal = “L”). When the V0 voltage regulator internal resistors are used (i.e. when the IRS terminal = “H”), then the VR terminal is left open.
- Because the input impedance of the VR terminal is high, it is necessary to take into consideration short leads, shield cables, etc. to handle noise.

The Liquid Crystal Voltage Generator circuit (Volatage Follower & Bias)

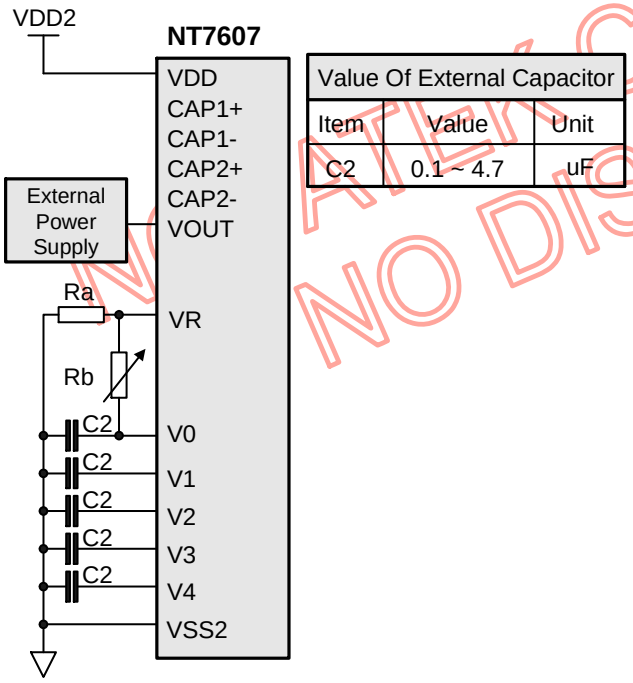
The V0 voltage is produced by a resistive voltage divider within the IC, and can be produced at the V1, V2, V3, and V4 voltage levels required for liquid crystal driving. Moreover, when the voltage follower changes the impedance, it provides V1, V2, V3, and V4 to the liquid crystal drive circuit. 1/4 bias or 1/5 bias for NT7607 can be selected by instruction.

Reference power supply circuit for driving LCD panel



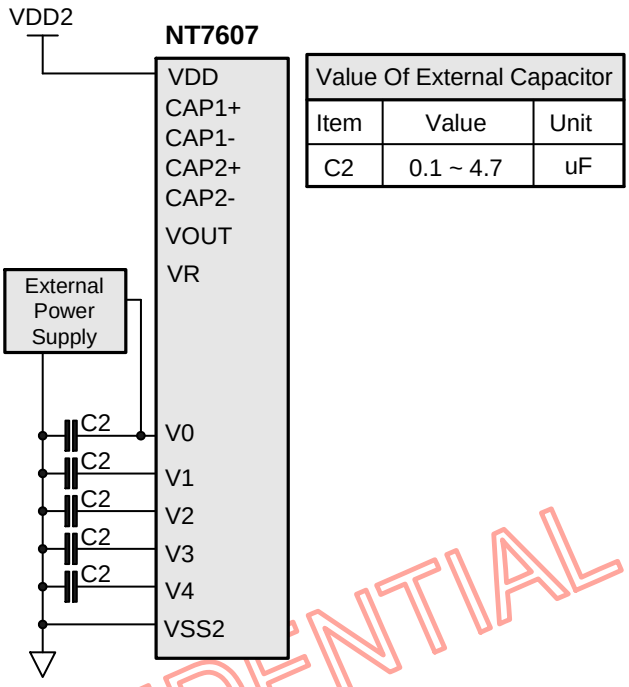
Value Of External Capacitor		
Item	Value	Unit
C1	0.1 ~ 4.7	uF
C2	0.1 ~ 4.7	

Figure 15. When using all LCD power circuits (VC, VR, VF = 111, IRS=VDD)



Value Of External Capacitor		
Item	Value	Unit
C2	0.1 ~ 4.7	uF

Figure 16. When not using voltage booster circuits (VC, VR, VF = 011, IRS=VSS)



Value Of External Capacitor		
Item	Value	Unit
C2	0.1 ~ 4.7	uF

Figure 17. When only using voltage follower (VC, VR, VF = 001)

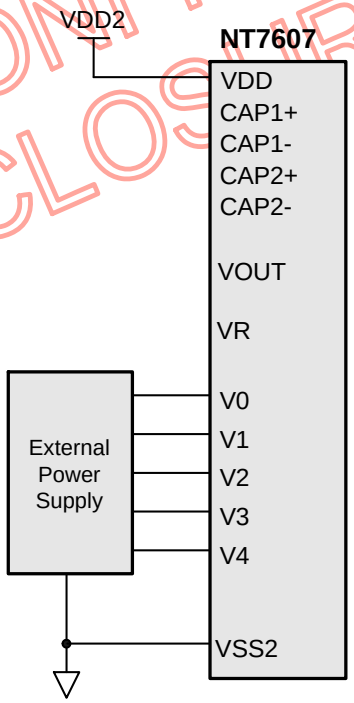


Figure 18. When not using internal LCD power supply circuits (VC, VR, VF = 000)

Power-on reset and Initial State

The NT7607 must be reset externally by /RES pin when power is turned on. The external reset is low active. After the reset the chip has the state shown in Table 14.

Table 14. State after reset

Function	Control bit state	Remarks
Display control set	D = 0	Display off
	C = 0	Cursor off
	B = 0	Cursor character blink off
Power save set	OS = 0	Oscillator off
	PS = 0	Power save off
Power control set	VC = 0	Voltage DC-DC converter OFF
	VR = 0	Voltage regulator OFF
	VF = 0	Voltage follower OFF
Function set	N = 0	2-line display
	S = 0	COM left shift
	CG = 0	CGRAM is not used. CGROM is used.
Return home	-	Address counter (AC) = 00H
V0 Regulator Internal Resistor Ratio Set	RR [1:0]=01	Internal resistor ratio (1+Rb/Ra) = 2.9
Electronic contrast control register	-	10H = (0,0,0,0,0)
Frame Frequency Select	FS=0	Frame Frequency = 80Hz
In case of 4-bit mode	-	NT7607 considers the first 4-bit data from MPU as the high order bits.

Note: If initialization is not done by /RES pin at application, unknown condition might result.

Commands

Only the Instruction Register (IR), the Data Register (DR) and output Data Register (OR) can be directly controlled by the MPU. Before internal operation, control information is stored temporarily in these registers, to allow interfacing to various types of MPU that operates at different speeds or to allow interface to peripheral control ICs.

Instruction set

1. Return Home

RS	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	0	0	0	0	0	0	1	-	02h to 03h

Return home instruction field makes cursor return home.
DDRAM address is set to 00H from AC and the cursor returns to 00H position. The contents of DDRAM are not changed

2. Double Height Mode

RS	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	0	0	0	0	1	0	DH2	DH1	08h to 0Bh

Double height mode instruction field selects double height line type.
When DH2 DH1 = 00: normal display (default)
01: COM1 ~ COM16 is a double height, COM17 ~ COM24 is normal
10:1) 2-line mode: normal display
2) 3-line mode:COM1 ~ COM8 is normal, COM9 ~ COM24 is a double height.
11: normal display

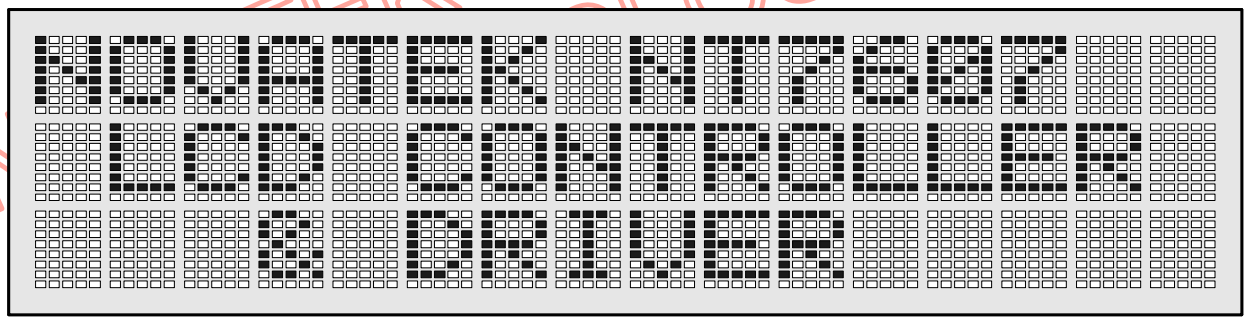


Figure 19. 3-Line Normal Mode Display (DH2, DH1 = 00)

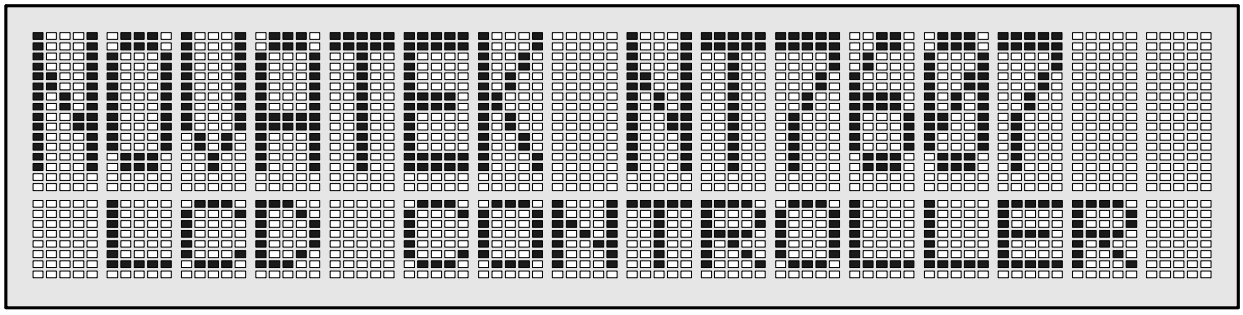


Figure 20. COM1 ~ COM16 is a Double Height Line, COM17 ~ COM24 is Normal (DH2, DH1 = 01)

Figure 21. COM1 ~ COM8 is Normal, COM9 ~ COM24 is a Double Height Line (DH2, DH1 = 10)

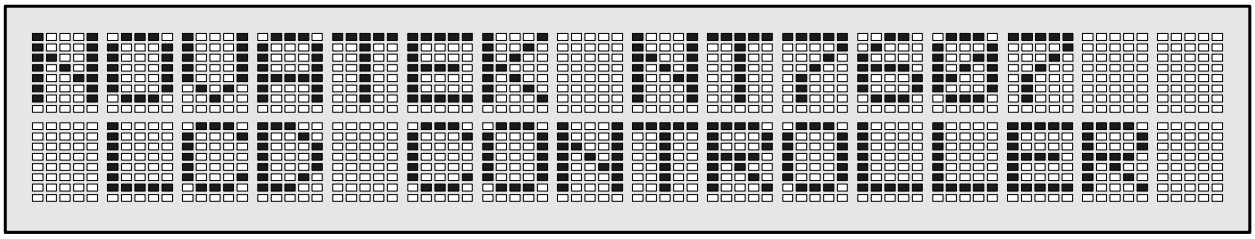


Figure 22. 2-Line Normal Mode Display (DH2, DH1 = 00)

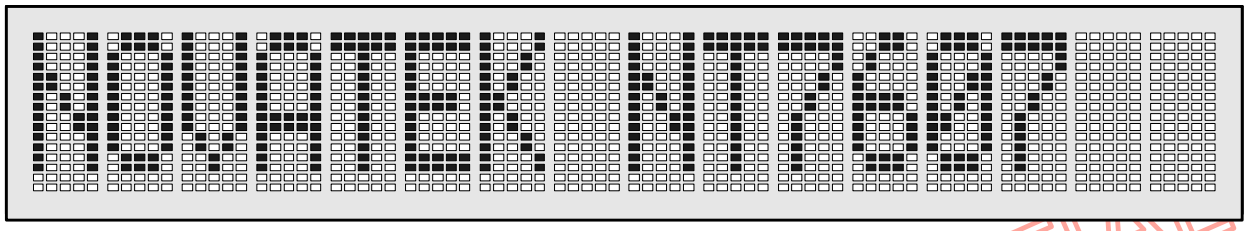


Figure 23. COM1 ~ COM16 is a Double Height Line (DH2, DH1 = 01)

3. Power Save Set

RS	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	0	0	0	0	1	1	OS	PS	0Ch to 0Fh

Power save instruction field is used to control the oscillator and set or to reset the power save mode.

OS: oscillator ON/OFF control bit
- When OS = “L”, oscillator is turned OFF (default)
- When OS = “H”, oscillator is turned ON.

PS: power save ON/OFF control bit
- When PS = “L”: power save is turned OFF (default).
- When PS = “H”: power save is turned ON.

4. Function Set

RS	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	0	0	0	1	0	N	S	CG	10h to 17h

N: display line mode instruction field selects 2-line or 3-line display mode
When N = “L”: 2-line display mode (default)
When N = “H”: 3-line display mode
S: data shift direction of common, S sets the shift direction of common display data
When S = “L”, COM left shift (default)
When S = “H”, COM right shift (Refer to Table 7)
CG: CGRAM enable bit
When CG = “L”, CGRAM is disable. CGROM (00H~07H) can be accessed and additional current consumption is saved by using this mode (default). (00H~07H = CGROM font display)
When CG = “H”, CGRAM can be accessed and you can use this RAM for eight special character area. (00H~07H = CGRAM font display)

5. Line Shift Mode

RS	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	0	0	0	1	1	0	LS2	LS1	18h to 1Bh

Line shift mode instruction field selects the DDRAM to be displayed in the first line.
When LS2, LS1 = 00: DDRAM line 1 shows at the first line of LCD (default).
01: DDRAM line 2 shows at the first line of LCD.
10: DDRAM line 3 shows at the first line of LCD.
11: DDRAM line 4 shows at the first line of LCD.

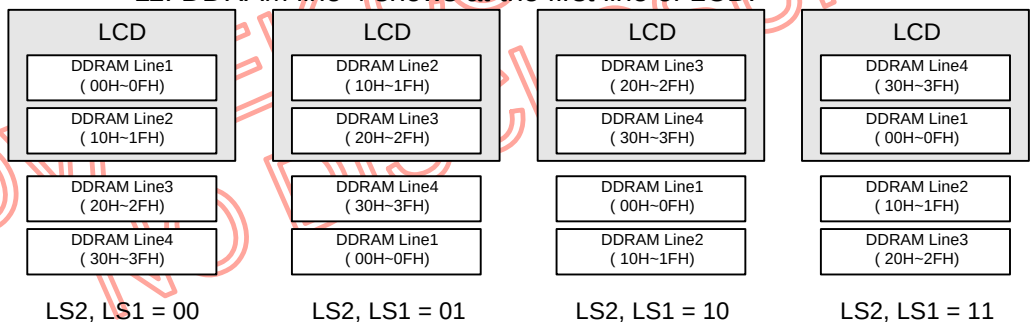


Figure 24. 2-Line Shift Mode Display at 2 Line LCD

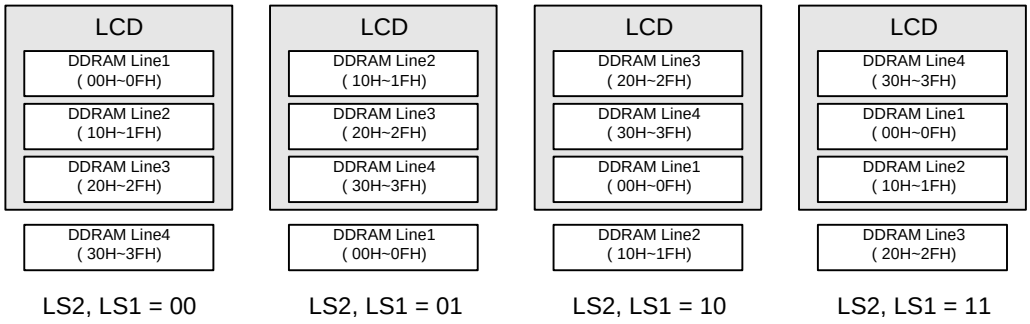


Figure 25. 3-Line Shift Mode Display at 3 Line LCD

6. Bias Control

RS	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	0	0	0	1	1	1	-	BS	1Ch to 1Fh

Bias Control instruction field sets LCD bias voltages generated internally.
BS: The bit is used when the internal voltage follower is ON
When BS = “L”: 1/5 bias (default)
When BS = “H”: 1/4 bias (V2 = V3)

7. Power Control Set

RS	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	0	0	1	0	0	VC	VR	VF	20h to 27h

Power Control instruction field sets voltage converter / regulator / follower ON / OFF.

VC: voltage converter circuit control bit
When VC = “L”: voltage booster is turned OFF (default)
When VC = “H”: voltage booster is turned ON

VR: voltage regulator circuit control bit
When VR = “L”: voltage regulator is turned OFF (default)
When VR = “H”: voltage regulator is turned ON

VF: voltage follower circuit control bit
When VF = “L”: voltage follower is turned OFF (default)
When VF = “H”: voltage follower ON

Note: The oscillation circuit must be turned on for the voltage converter circuit to be active.

8. Display Control

RS	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	0	0	1	0	1	C	B	D	28h to 2Fh

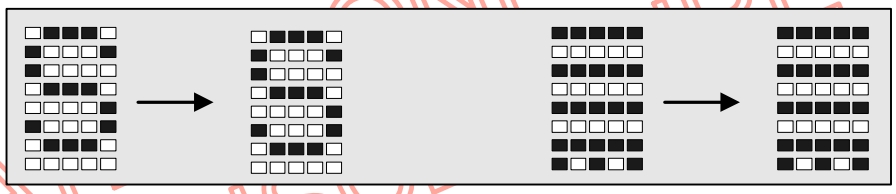
Display control instruction field controls cursor /blink/display ON/OFF.

C: cursor ON /OFF control bit
When C = “L”, cursor is disappeared in current display (default).
When C = “H”, cursor is turned ON.

B: cursor blink ON/OFF control bit
When C = “H” and B = “H”, NT7607 make LCD alternate between inverting display character and normal display character at the cursor position with about a half second.
On the contrary, if C = “L”, only a normal character is displayed regardless of “B” flag.
When B = “L”, blink is OFF (default).

D: display ON/OFF control bit
When D = “L”, Display is turned OFF. But display data are remained in DDRAM (default).
When D = “H”, Entire display in turned ON.

Table 15. Cursor Attributes

C	B	Display State
1	0	
1	1 Blinking Mode	
0	0 0	1 

9. DD/CG RAM Address Set

RS	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	80h to FFh

DD/CG RAM Address set instruction fields DDRAM/CGRAM address

Before writing / reading data into /from RAM, set address by RAM Address Set Instruction. Next when data are written / read in succession. The address is automatically increased by 1. For accessing DD/ CGRAM, the DD/CGRAM Address Set Instruction should be set before. After accessing 7FH, the address of AC is 00H.

The address range are 00H ~ 7FH.

Address	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00H	DDRAM line 1(00H ~ 0FH)															
10H	DDRAM line 2(10H ~ 1FH)															
20H	DDRAM line 3(20H ~ 2FH)															
30H	DDRAM line 4(30H ~ 3FH)															
40H	CGRAM (pattern 0)								CGRAM (pattern 1)							
50H	CGRAM (pattern 2)								CGRAM (pattern 3)							
60H	CGRAM (pattern 4)								CGRAM (pattern 5)							
70H	CGRAM (pattern 6)								CGRAM (pattern 7)							

10. ICONRAM Address Set

RS	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	0	1	0	IA4	IA3	IA2	IA1	IA0	40h to 5Fh

ICONRAM Address Set instruction fields ICONRAM / Registers address.
Before writing / reading data into /from ICON RAM, set the address by ICONRAM Address Set Instruction. Next when data are written / read in succession. The address is automatically increased by 1. For accessing ICONRAM, the ICONRAM Address Set Instruction should be set before. After accessing 0FH, the address of ICONRAM address is 00H.The ICONRAM address range are 00H ~ 1FH.
The 5 icons at a time can blink, if C and B bits of the display instructions are enabled. The blink attributes of ICON are same as the cursor blink.

Address	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00H	ICONRAM (00H ~ 0FH)															
10H	EV	TE	Reserved													

EV: electronic volume register (10H) ~ default (00000)
TE: test register (Do not use)(11H)

11. Write Data

RS	D7	D6	D5	D4	D3	D2	D1	D0	Hex
1	D7	D6	D5	D4	D3	D2	D1	D0	XX

The instruction field makes NT7607 write binary 8-bit data to DDRAM/CGRAM/ICONRAM or register. The RAM address to be written into is determined by previous DD/CGRAM Address Set instruction. After writing operation, the address is automatically increased by 1.

12. Read Data

RS	D7	D6	D5	D4	D3	D2	D1	D0	Hex
1	D7	D6	D5	D4	D3	D2	D1	D0	XX

DDRAM/CGRAM/ICONRAM data read instruction.
Each RAM is selected by address set instruction. And then you can read the RAM data. You can get correct RAM data from second read transaction. The first read data after setting RAM address is dummy data; so the correct RAM data come from the second read transaction. After reading operation, the address is increase by 1 automatically.

13. NOP

RS	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	0	0	0	0	0	0	0	0	00h

Non-Operation Instruction

14. V0 Regulator Internal Resistor Ratio Set

RS	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	0	1	1	0	0	0	RR1	RR0	60h to 63h

This command sets the V0 voltage regulator internal resistor ratio. For details, see explanation under “LCD supply voltage generator”.

Table 16. Rb/Ra Ratio

RR1	RR0	(1+Rb/Ra) Ratio
0	0	2.5
0	1	2.9 (default)
1	0	3.2
1	1	3.5

15. Frame Frequency Select

RS	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	0	1	1	0	1	0	0	FS	68h to 69h

FS	Frame Frequency
0	80Hz (Default)
1	67Hz

16. Test Instruction

RS	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	0	0	1	1	*	*	*	*	30h to 3Fh

This is the dedicate IC chip test instruction. It must not be used for normal operation.

Table 17. Instruction Table

Instruction	Code										Function
	RS	D7	D6	D5	D4	D3	D2	D1	D0	Hex	
Return Home	0	0	0	0	0	0	0	1	-	02h to 03h	DDRAM address is set to 00h from AC and the cursor returns to 00h position. The contents of DDRAM are not changed
Double Height Mode	0	0	0	0	0	1	0	DH2	DH1	08h to 0Bh	Double height mode DH2 DH1 = 00: normal display (default) 01: COM1 ~ COM16 is a double height. COM17 ~ COM24 is normal 10: 1) 2-line mode: normal display 2) 3-line mode: COM1 ~ COM8 is normal and COM9 ~ COM24 is a double height. 11: normal display
Power Save	0	0	0	0	0	1	1	OS	PS	0Ch to 0Fh	Power save/oscillation circuit ON/OFF OS = 0: oscillator OFF (default) OS = 1: oscillator ON PS = 0: power save OFF (default) PS = 1: power save ON
Function Set	0	0	0	0	1	0	N	S	CG	10h to 17h	Display line mode N = 0: 2-line display mode (default) N = 1: 3-line display mode Shifting direction of COM S = 0: 1) 2-line mode: COM1 ~ COM16 (default) 2) 3-line mode: COM1 ~ COM24 S = 1: 1) 2-line mode: COM16 ~ COM1 2) 3-line mode: COM24 ~ COM1 Select CGRAM or CGROM CG = 0: CGROM (default) CG = 1: CGRAM
Line Shift Mode	0	0	0	0	1	1	0	LS2	LS1	18h to 1Bh	Determination of the DDRAM line, which is displayed at the first line at LCD. LS2, LS1 = 00: DDRAM line 1 shows at (default) the first line of LCD. LS2, LS1 = 01: DDRAM line 2 shows at the first line of LCD. LS2, LS1 = 10: DDRAM line 3 shows at the first line of LCD. LS2, LS1 = 11: DDRAM line 4 shows at the first line of LCD.
Bias Control	0	0	0	0	1	1	1	-	BS	1Ch to 1Fh	Determination of Bias BS = 0: 1/5 bias (default) BS = 1: 1/4 bias

Table 17. Instruction Table (continued)

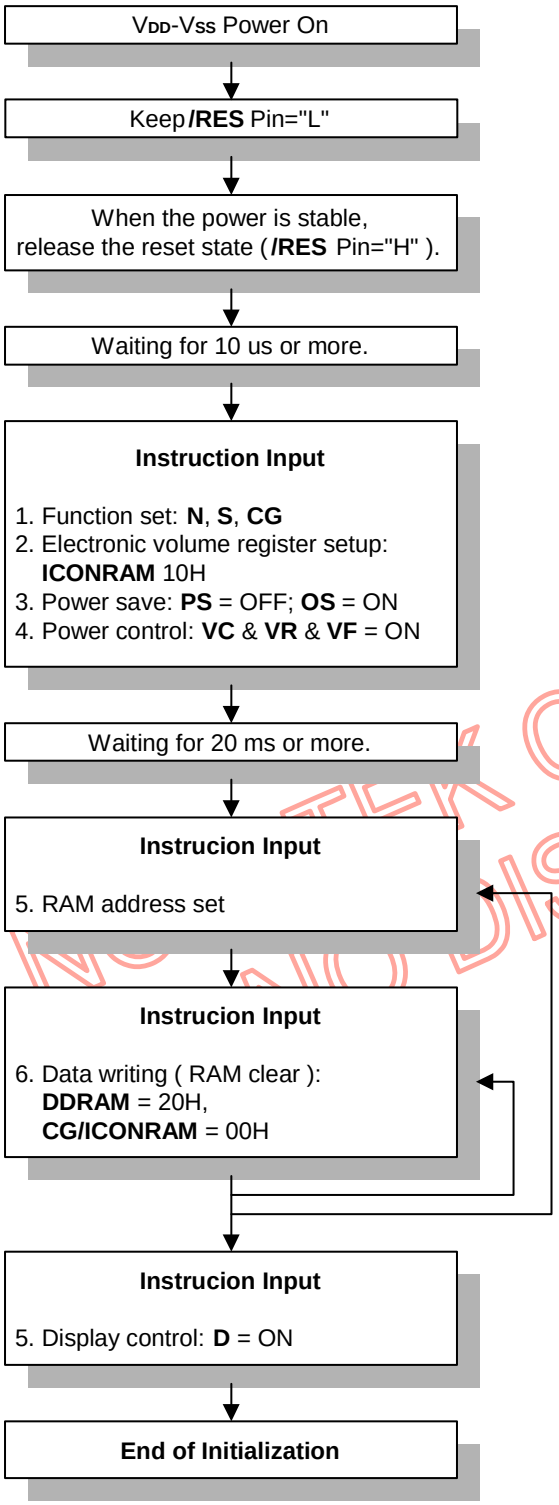
Instruction	Code										Function
	RS	D7	D6	D5	D4	D3	D2	D1	D0	Hex	
Power Control	0	0	0	1	0	0	VC	VR	VF	20h to 27h	LCD power control VC = 0: voltage converter OFF (default) VC = 1: voltage converter ON VR = 0: voltage regulator OFF (default) VR = 1: voltage regulator ON VF = 0: voltage follower OFF (default) VF = 1: voltage follower ON
Display Control	0	0	0	1	0	1	C	B	D	28h to 2Fh	Cursor/ blink /display ON/OFF C = 0: cursor OFF (default) 1: cursor ON B = 0: blink OFF (default) 1:blink ON D = 0: display OFF (default) 1:display ON
DD/CGRAM Address Set	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	80h to FFh	DDRAM/CGRAM Range: DDRAM 00h~3FH, CGRAM 40h~7FH
ICONRAM Address Set	0	0	1	0	IA4	IA3	IA2	IA1	IA0	40h to 5Fh	ICONRAM address, electronic volume and test byte address Range: ICONRAM 00H~0FH EV 10H (Electronic volume byte) TE 11H (Test byte)
Write Data	1	D7	D6	D5	D4	D3	D2	D1	D0	XX	Write DDRAM/CGRAM/ICONRAM
Read Data	1	D7	D6	D5	D4	D3	D2	D1	D0	XX	Read DDRAM/CGRAM/ICONRAM or register data
NOP	0	0	0	0	0	0	0	0	0	00h	Non-operation Instruction
V0 Regulator Internal Resistor Ratio Set	0	0	1	1	0	0	0	RR1	RR0	60h to 63h	Select internal resistor ratio Rb/Ra mode
Frame Frequency Select	0	0	1	1	0	1	0	0	FS	68h to 69h	Select the frame frequency
Test Instruction	0	0	0	1	1	*	*	*	*	30h to 3Fh	Don't use this Instruction

Note:1. "-" Don't care; "* "Don't use.

1. Instruction execution time depends on the internal process time of NT7607; therefore it is necessary to provide a time larger than one MPU interface cycle time (T_{CYC}) between executions of two successive instructions.

Instruction Description (for reference only)

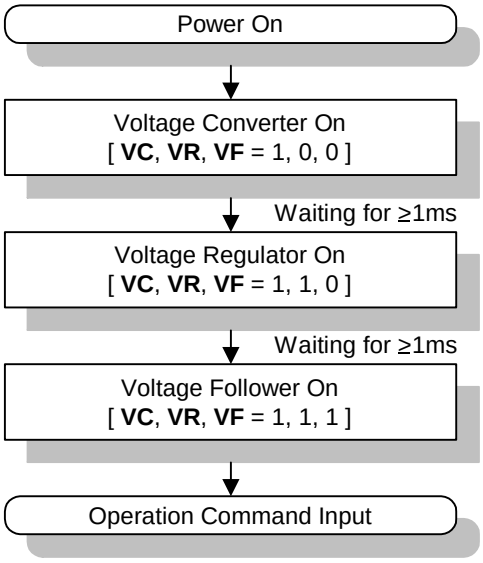
2. Initialization



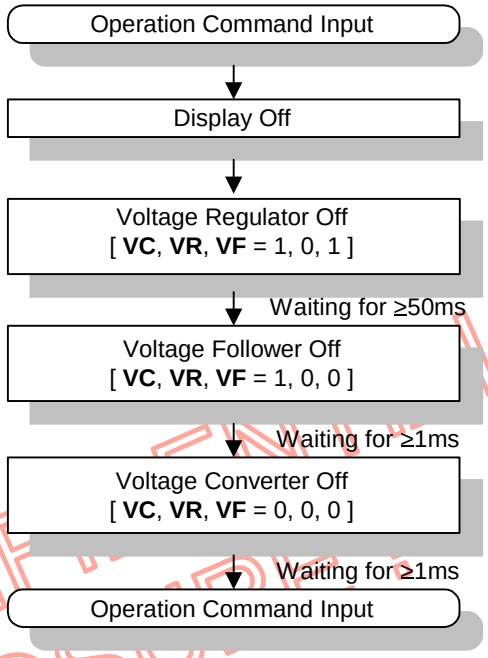
Note:
At command 5 and 6, the internal RAM should be cleared.
To clear DDRAM, set address at 00H (first DDRAM) and then write 20H (space character code) 64 times.
To clear CGRAM, set address at 40H (first CGRAM) and then write 00H (NULL data) 64 times.
To clear ICONRAM, set address at 00H (first ICONRAM) and then write 00H (NULL data) 16 times.

3. Recommendation of Power On/Off Sequence

Power On Sequence



Power Off Sequence



Absolute Maximum Rating

DC Supply Voltage (VDD, VDD2)..... –0.3V to +4.0V
DC Supply Voltage (VLCD, VOUT)..... –0.3V to +12.0V
Input Voltage (Vin)..... –0.3V to VDD
Operating Ambient Temperature ..... -40°C to +85°C
Storage Temperature ..... -55°C to +125°C

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

DC Characteristics (VSS=0V, VDD =1.8~3.6V, VDD2=2.4~3.6V, Ta=-40~85°C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition	
VDD	Operating Voltage	1.8	-	3.6	V		
VDD2	Operating Voltage	2.4	-	3.6	V		
VOUT	Converter output voltage	6.0	-	10.8	V	Ta = 25°C, C = 1µF	
VLCD	Voltage regulator operation voltage	4.0	-	7.0	V	VLCD = V0 - VSS	
IDD1	Dynamic current consumption 1	-	-	80	µA	Display operation, Internal resistor, VLCD = 6V, without load. No access from MPU.	
IDD2	Dynamic current consumption 2	-	-	500	µA	Access operation from MPU. (Fcyc = 200KHz)	
ISP	Sleep mode current consumption	-	-	5	µA	During power save mode, Ta = 25°C	
VIHC1	High-level input voltage	0.7×VDD	-	VDD	V	VDD=2.4~3.6V	RS, D0 ~ D7, /RD (E), /WR (R/W), /CS, CL, C86, P/S, PI, IRS and DIRS.
		0.8xVDD	-	VDD		VDD=1.8~2.4V	
VILC1	Low-level input voltage	VSS	-	0.3×VDD	V	VDD=2.4~3.6V	
		VSS	-	0.2xVDD		VDD=1.8~2.4V	
VIHC2	High-level input voltage	0.8×VDD	-	VDD	V	/RES pin is schmitt input.	
VILC2	Low-level input voltage	VSS	-	0.2×VDD	V		
VOHC	High-level output voltage	VDD - 0.4	-	-	V	IOH = -1mA (D0 ~ D7)	
VOLC	Low -level output voltage	-	-	VSS + 0.4	V	IOL = 1mA (D0 ~ D7)	

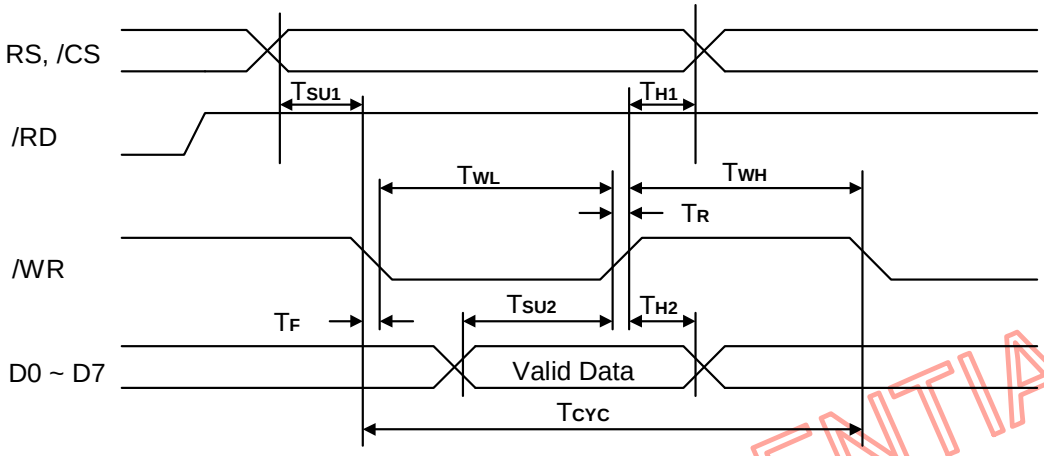
DC Characteristics (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
ILI	Input leakage current	-1.0	-	1.0	µA	VIN = VDD or VSS (RS, /RD (E), /WR (R/W), /CS, CL, C86, P/S,IRS, DIRS and /RES)
IHZ	HZ leakage current	-3.0	-	3.0	µA	When the D0 ~ D7 are in high impedance.
RON1	COM driver ON resistance	-	-	5	KΩ	IO = ±50 µA
RON2	SEG driver ON resistance	-	-	10	KΩ	IO = ±50 µA
FFR1	LCD Frame frequency 1	77	80	83	Hz	FS=0, TA = 25°C
FFR2	LCD Frame frequency 2	64	67	70	Hz	FS=1, TA = 25°C

Notes: Voltages V0≧V1≧V2≧V3≧V4≧VSS2 must always be satisfied.

AC Characteristics

1. System Buses Read/Write Characteristics (for 8080 Series MPU)
   - Write timing



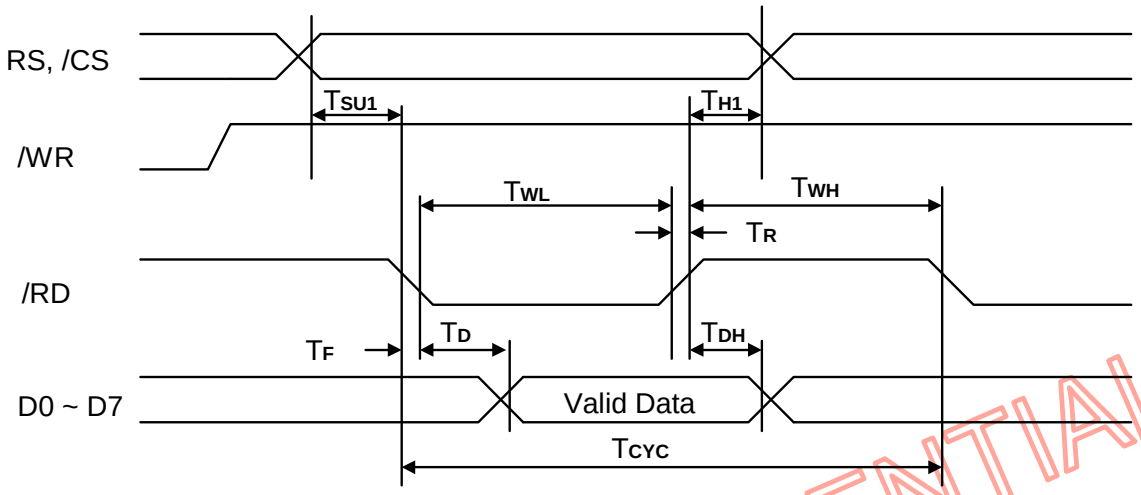
(VDD = 2.4 ~ 3.6V, Ta = -40 ~ 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T_{CYC}	/WR cycle time	240	-	-	ns	
T_R, T_F	Pulse rise / fall time	-	-	15	ns	
T_{WH}	/WR high pulse width	100	-	-	ns	
T_{WL}	/WR low pulse width	90	-	-	ns	
T_{SU1}	RS and /CS setup time	0	-	-	ns	
T_{H1}	RS and /CS hold time	0	-	-	ns	
T_{SU2}	Data setup time	40	-	-	ns	
T_{H2}	Data hold time	10	-	-	ns	

(VDD = 1.8 ~ 2.4V, Ta = -40 ~ 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T_{CYC}	/WR cycle time	400	-	-	ns	
T_R, T_F	Pulse rise / fall time	-	-	15	ns	
T_{WH}	/WR high pulse width	120	-	-	ns	
T_{WL}	/WR low pulse width	150	-	-	ns	
T_{SU1}	RS and /CS setup time	0	-	-	ns	
T_{H1}	RS and /CS hold time	0	-	-	ns	
T_{SU2}	Data setup time	80	-	-	ns	
T_{H2}	Data hold time	30	-	-	ns	

■ Read timing



(VDD = 2.4~ 3.6V, Ta = -40 ~ 85°C)

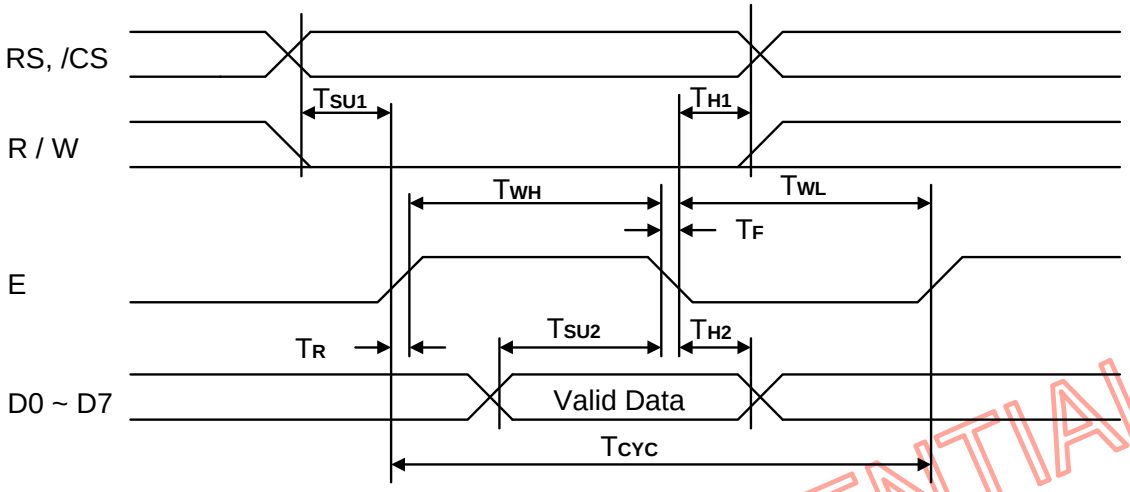
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T_{CYC}	/RD cycle time	240	-	-	ns	
T_R, T_F	Pulse rise / fall time	-	-	15	ns	
T_{WH}	/RD high pulse width	60	-	-	ns	
T_{WL}	/RD low pulse width	120	-	-	ns	
T_{SU}	RS and /CS setup time	0	-	-	ns	
T_{H1}	RS and /CS hold time	0	-	-	ns	
T_D	Data output delay time	50	-	140	ns	
T_{DH}	Data output hold time	5	-	50	ns	

(VDD = 1.8 ~ 2.4V, Ta = -40 ~ 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T_{CYC}	/RD cycle time	400	-	-	ns	
T_R, T_F	Pulse rise / fall time	-	-	25	ns	
T_{WH}	/RD high pulse width	150	-	-	ns	
T_{WL}	/RD low pulse width	120	-	-	ns	
T_{SU}	RS and /CS setup time	0	-	-	ns	
T_{H1}	RS and /CS hold time	0	-	-	ns	
T_D	Data output delay time	50	-	240	ns	
T_{DH}	Data output hold time	10	-	100	ns	

2. System Buses Read/Write Characteristics (for 6800 Series MPU)

■ Write timing



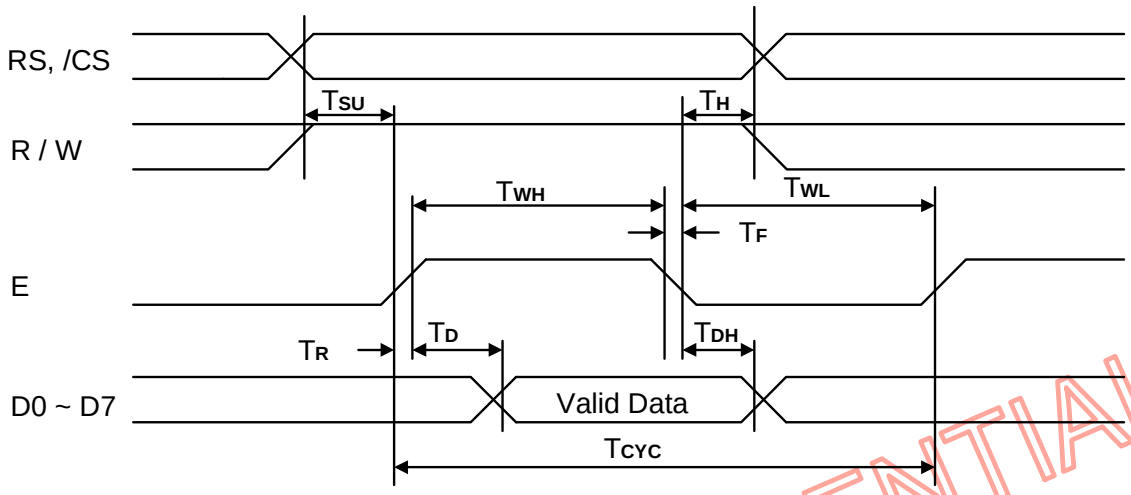
(VDD = 2.4 ~ 3.6V, Ta = -40 ~ 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T_{CYC}	E cycle time	240	-	-	ns	
T_R, T_F	Pulse rise / fall time	-	-	15	ns	
T_{WH}	E high pulse width	90	-	-	ns	
T_{WL}	E low pulse width	100	-	-	ns	
T_{SU1}	RS and /CS setup time	0	-	-	ns	
T_{H1}	RS and /CS hold time	0	-	-	ns	
T_{SU2}	Data setup time	40	-	-	ns	
T_{H2}	Data hold time	10	-	-	ns	

(VDD = 1.8 ~ 2.4V, Ta = -40 ~ 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T_{CYC}	E cycle time	400	-	-	ns	
T_R, T_F	Pulse rise / fall time	-	-	25	ns	
T_{WH}	E high pulse width	150	-	-	ns	
T_{WL}	E low pulse width	120	-	-	ns	
T_{SU1}	RS and /CS setup time	0	-	-	ns	
T_{H1}	RS and /CS hold time	0	-	-	ns	
T_{SU2}	Data setup time	80	-	-	ns	
T_{H2}	Data hold time	30	-	-	ns	

■ Read timing



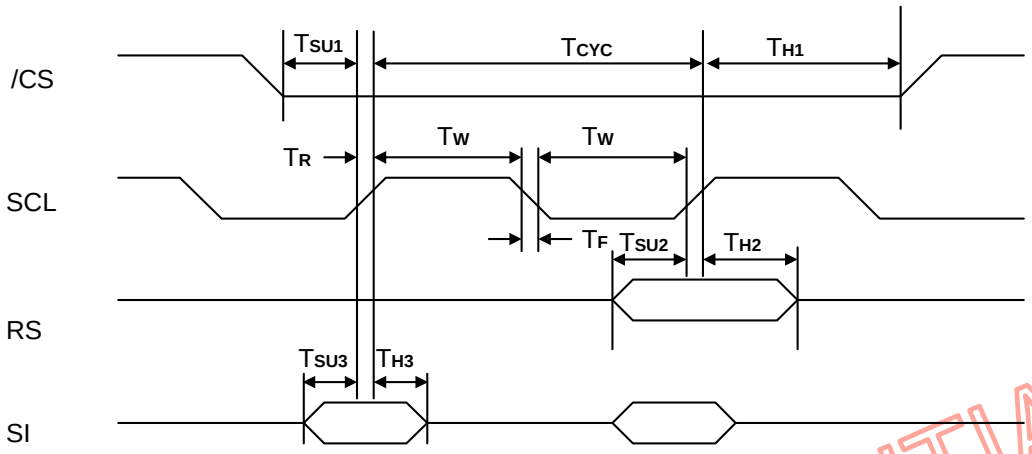
(VDD = 2.4~ 3.6 V, Ta = -40 ~ 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T_{CYC}	E cycle time	240	-	-	ns	
T_R, T_F	Pulse rise / fall time	-	-	15	ns	
T_{WH}	E high pulse width	120	-	-	ns	
T_{WL}	E low pulse width	60	-	-	ns	
T_{SU}	RS and /CS setup time	0	-	-	ns	
T_H	RS and /CS hold time	0	-	-	ns	
T_D	Data output delay time	50	-	140	ns	
T_{DH}	Data output hold time	5	-	50	ns	

(VDD = 1.8 ~ 2.4V, Ta = -40 ~ 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T_{CYC}	E cycle time	400	-	-	ns	
T_R, T_F	Pulse rise / fall time	-	-	25	ns	
T_{WH}	E high pulse width	150	-	-	ns	
T_{WL}	E low pulse width	120	-	-	ns	
T_{SU}	RS and /CS setup time	0	-	-	ns	
T_H	RS and /CS hold time	0	-	-	ns	
T_D	Data output delay time	50	-	240	ns	
T_{DH}	Data output hold time	10	-	100	ns	

3. Serial Interface Timing



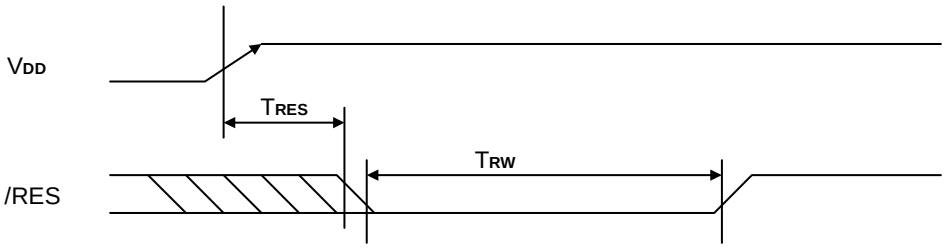
(VDD = 2.4 ~ 3.6 V, Ta = -40 ~ 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T_{CYC}	SCL clock cycle time	300	-	-	ns	
T_R, T_F	Pulse rise / fall time	-	-	15	ns	
T_W	SCL clock width (high to low)	120	-	-	ns	
T_{SU1}	/CS setup time	60	-	-	ns	
T_{H1}	/CS hold time	150	-	-	ns	
T_{SU2}	RS data setup time	75	-	-	ns	
T_{H2}	RS data hold time	60	-	-	ns	
T_{SU3}	SI data setup time	75	-	-	ns	
T_{H3}	SI data hold time	75	-	-	ns	

(VDD = 1.8 ~ 2.4V, Ta = -40 ~ 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T_{CYC}	SCL clock cycle time	400	-	-	ns	
T_R, T_F	Pulse rise / fall time	-	-	25	ns	
T_W	SCL clock width (high to low)	160	-	-	ns	
T_{SU1}	/CS setup time	80	-	-	ns	
T_{H1}	/CS hold time	200	-	-	ns	
T_{SU2}	RS data setup time	100	-	-	ns	
T_{H2}	RS data hold time	80	-	-	ns	
T_{SU3}	SI data setup time	100	-	-	ns	
T_{H3}	SI data hold time	100	-	-	ns	

4. Reset Timing



(VDD = 1.8 ~ 3.6 V, Ta = -40 ~ 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T_{RES}	Reset start time	50	-	-	ns	
T_{RW}	Reset low pulse width	5	-	-	µs	VDD=2.4~3.6V
		10	-	-		VDD=1.8~2.4V

Microprocessor Interface (for reference only)

1. 8080-series microprocessors

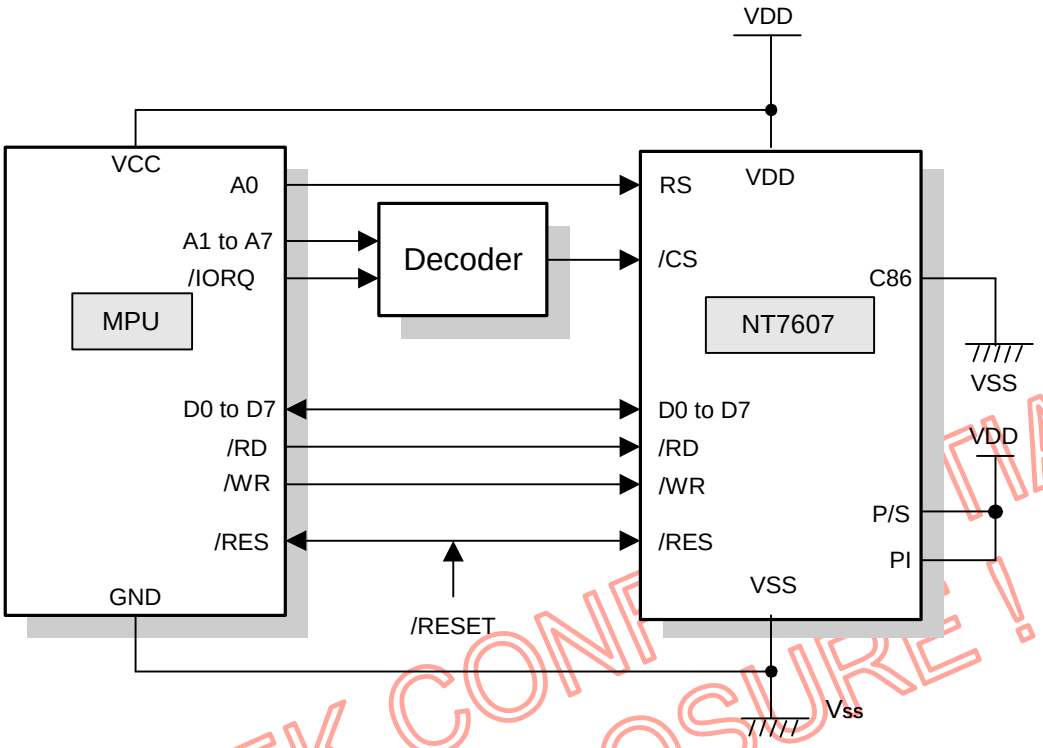


Figure 26

2. 6800-series microprocessors

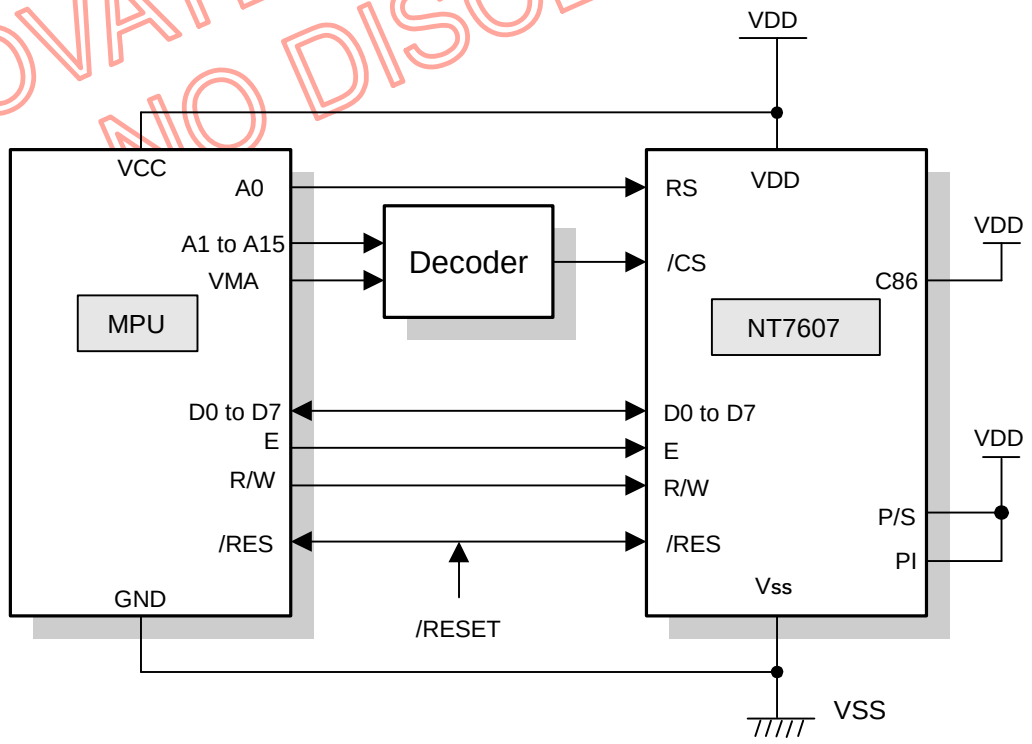
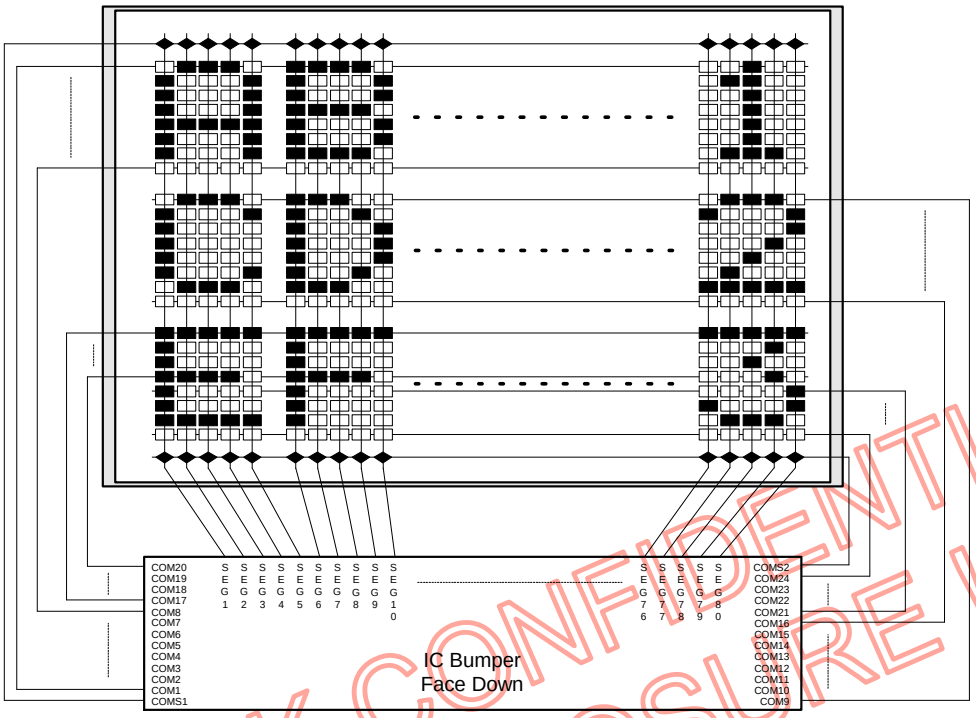


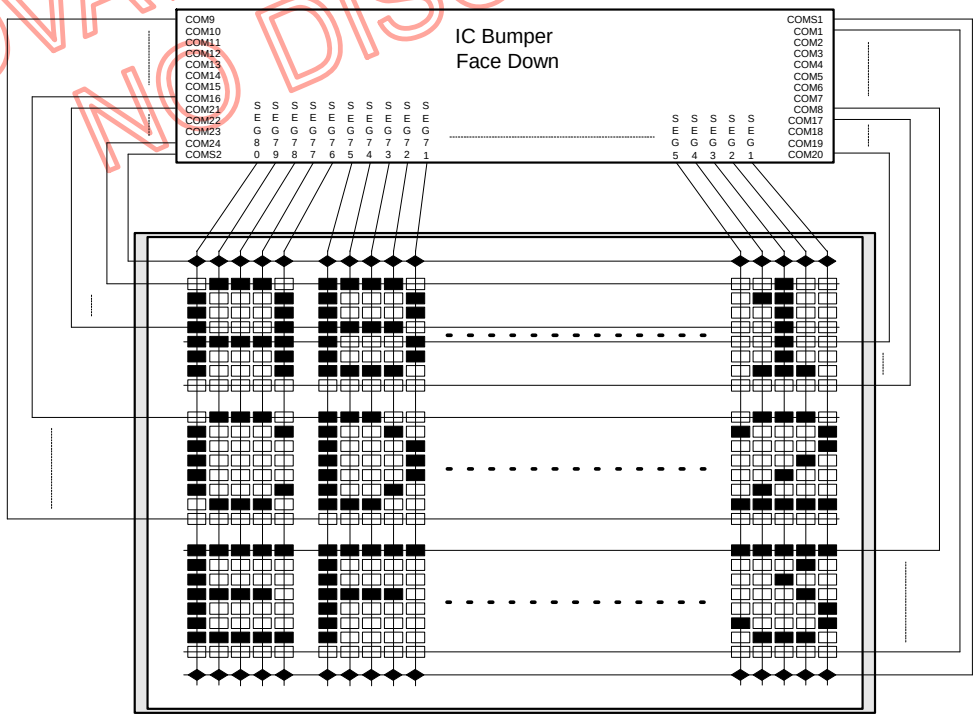
Figure 27

Application Information for LCD panel (for reference only)

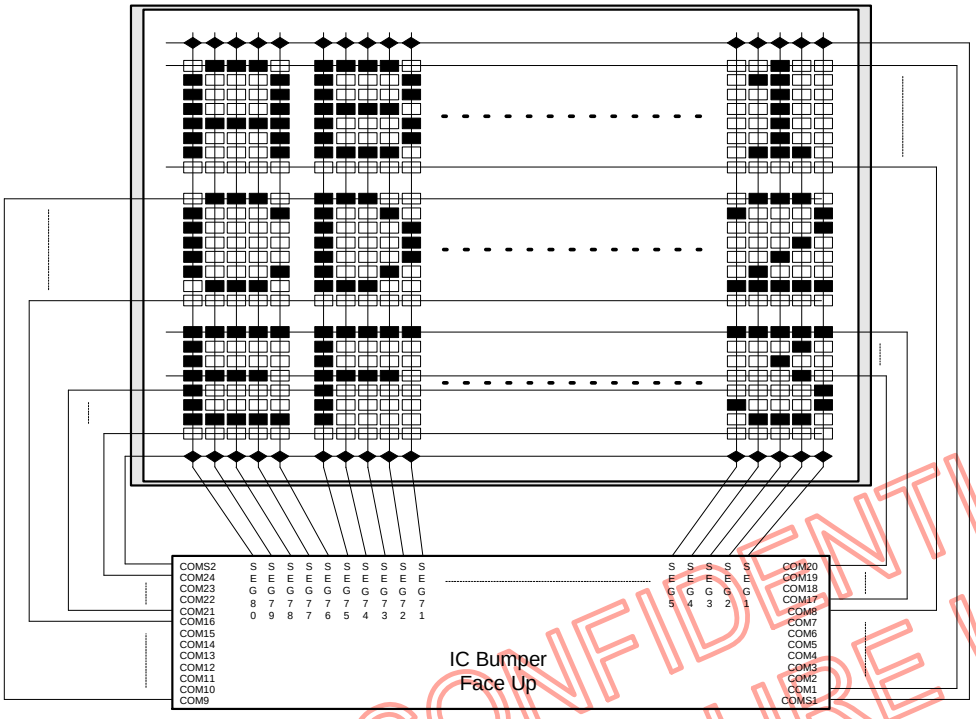
1. IC Bumper Face Down and Lower View (S bit = '0', DIRS = '0')



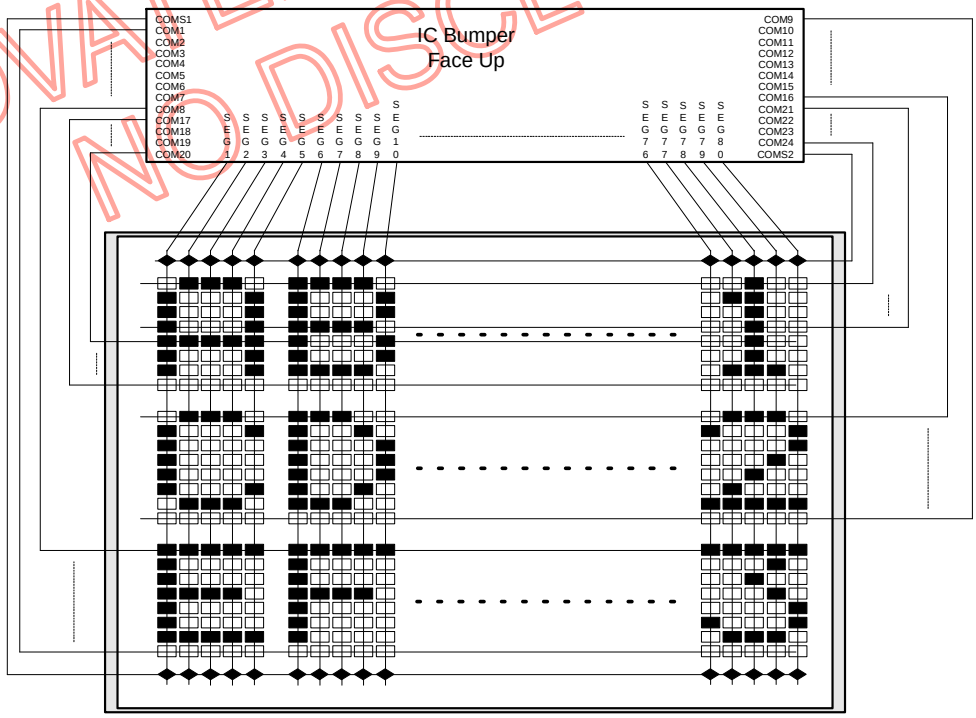
2. IC Bumper Face Down and Upper View (S bit = '1', DIRS = '1')



3. IC Bumper Face Up and Lower View (S bit = ’0’, DIRS = ’1’)



4. IC Bumper Face Up and Upper View (S bit = ’1’, DIRS = ’0’)

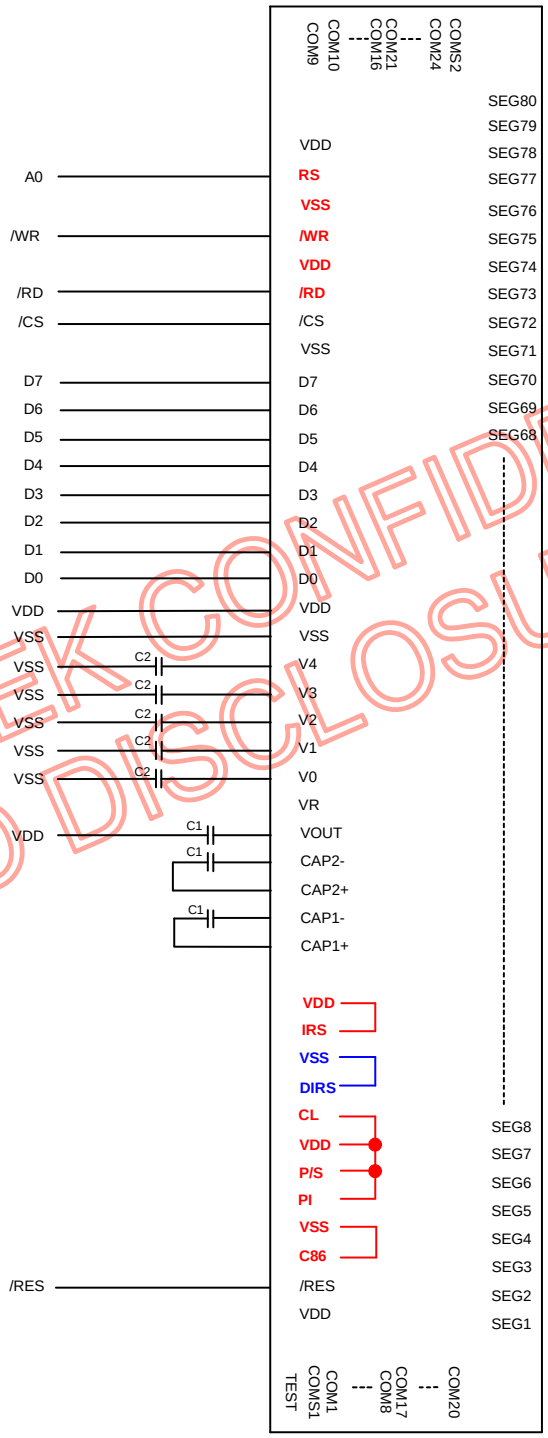


Application Information for Pin Connection to MPU (for reference only)

1. 8-bit 8080 MPU Mode:

   IRS=VDD: Internal resistors

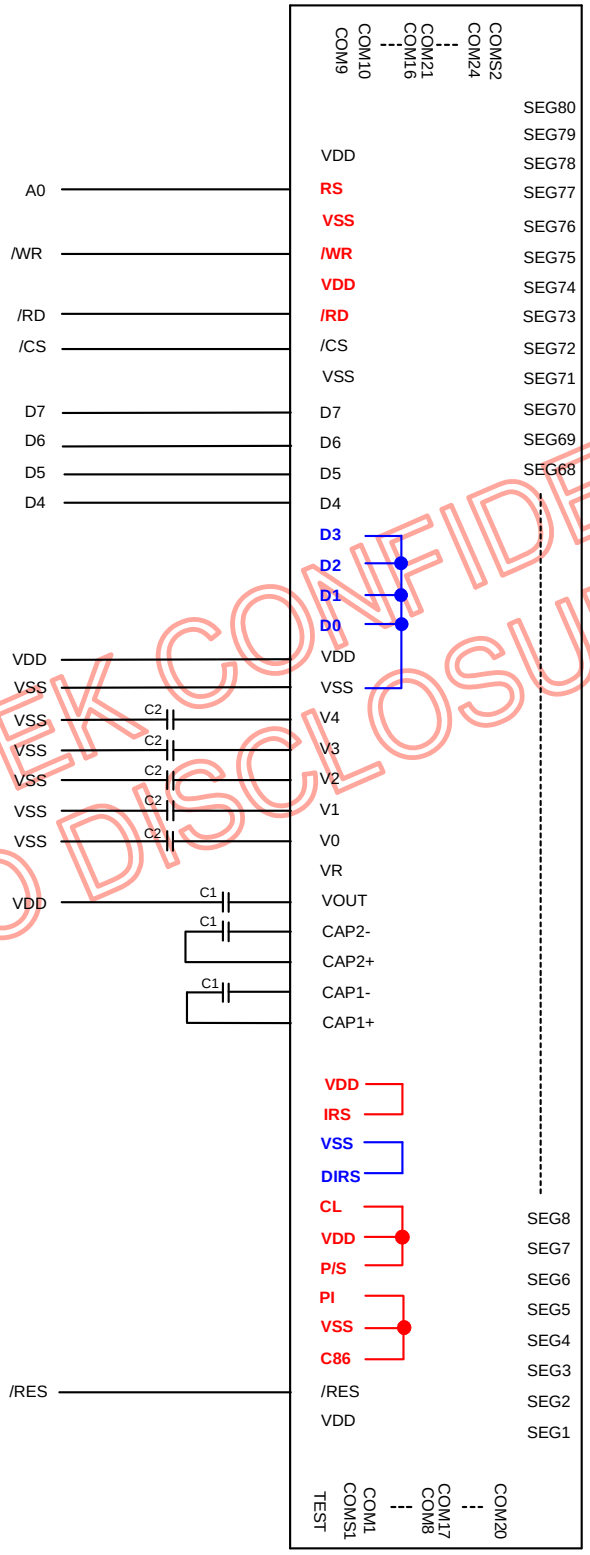
   DIRS=VSS: SEG DIR from SEG1 to SEG80



2. 4-bit 8080 MPU Mode:

IRS=VDD: Internal resistors

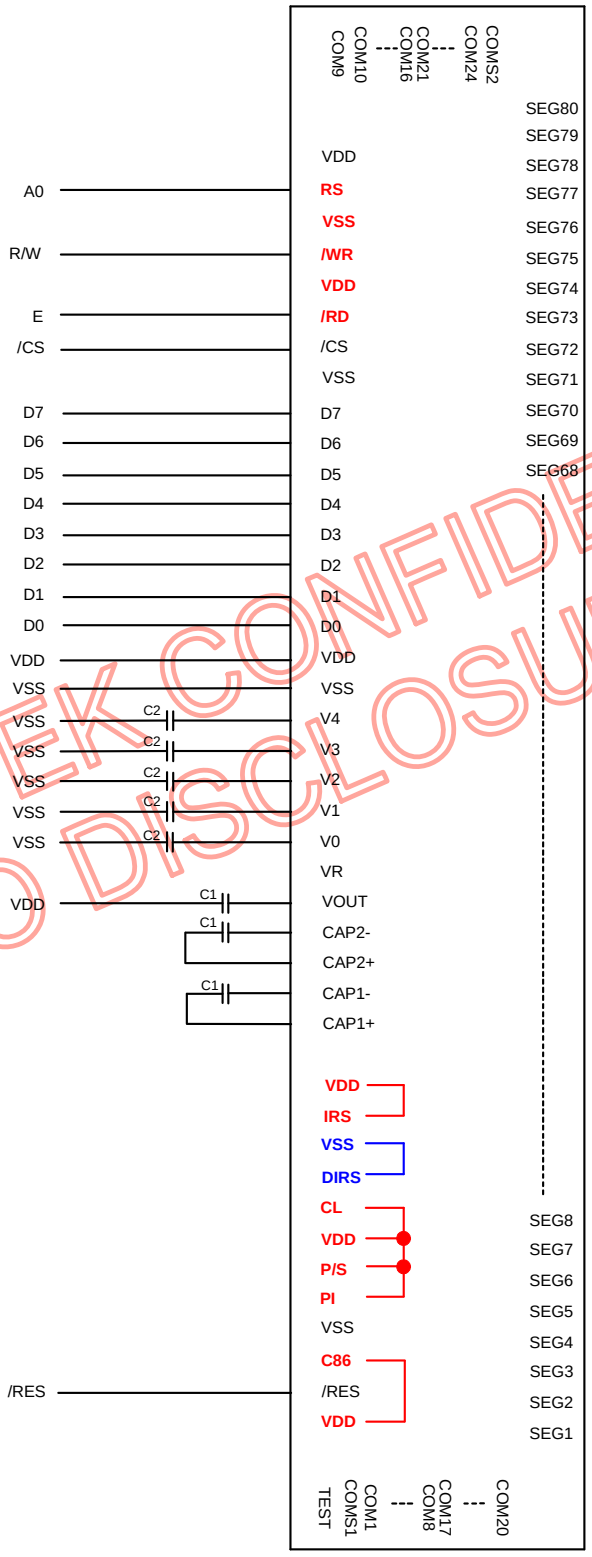
DIRS=VSS: SEG DIR from SEG1 to SEG80



3. 8-bit 6800 MPU Mode:

IRS=VDD: Internal resistors

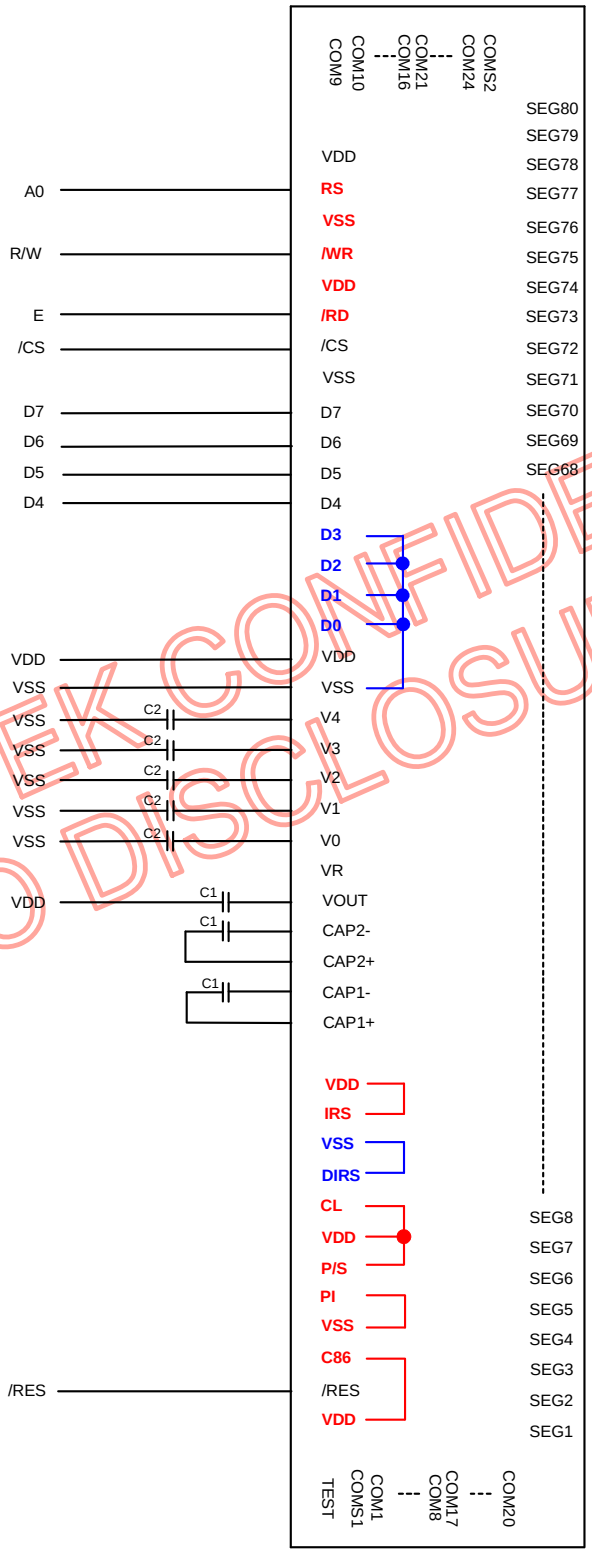
DIRS=VSS: SEG DIR from SEG1 to SEG80



4. 4-bit 6800 MPU Mode:

IRS=VDD: Internal resistors

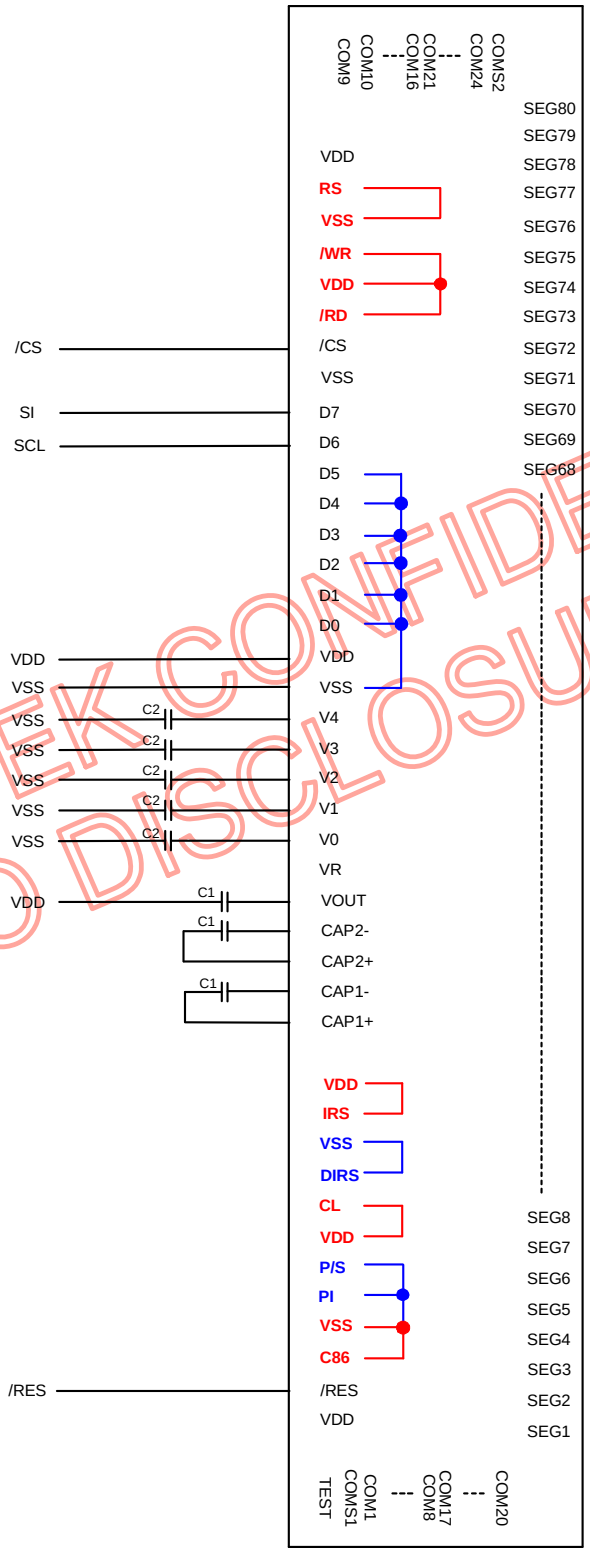
DIRS=VSS: SEG DIR from SEG1 to SEG80



5. 3SPI Serial Mode:

IRS=VDD: Internal resistors

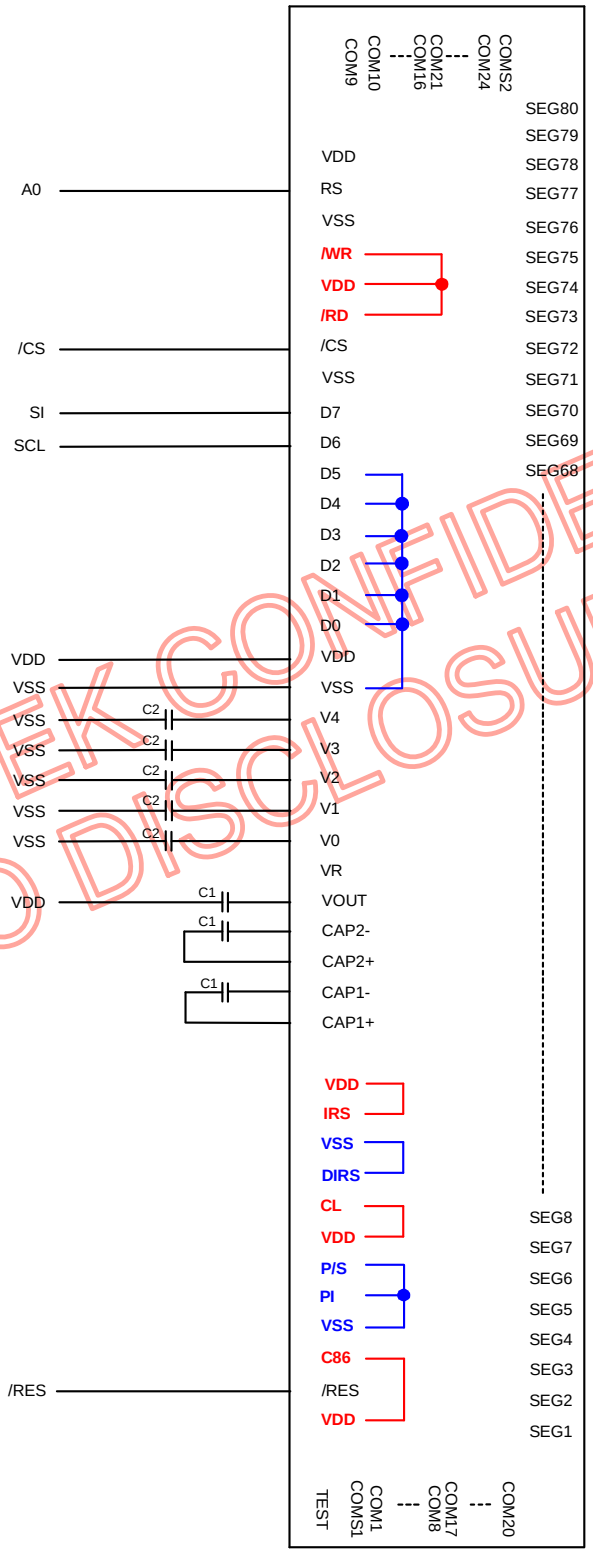
DIRS=VSS: SEG DIR from SEG1 to SEG80



6. 4SPI Serial Mode:

IRS=VDD: Internal resistors

DIRS=VSS: SEG DIR from SEG1 to SEG80



Application Notice

1. Power: 1.8V ≤ VDD ≤ 3.6V; 2.4V ≤ VDD2 ≤ 3.6V; VOUT ≤ 12V.
2. Make sure the VDD / VDD2 power near the IC side is larger than 1.8V / 2.4V. Please consider the path impedance (ITO / FPC / Heat seal impedance) from system power source to IC.
3. Use VDD (pad 25~29) for power supply input, and don't use VDD (pad 1, 5, 61, 66, 72) output for pad option to power supply input pad.
4. Use VSS (pad 30~34) for ground input, and don't use VSS (pad 3, 8, 63, 69) output for pad option to ground input pad.
5. It is better to use internal Regulator resistor (IRS = VDD).
6. Because the VR terminal input impedance is high, use short leads and shielded lines to reduce the noise coupling.
7. High resistance value of external resisters (Ra and Rb) can reduce the system power consumption: Ra > 500KΩand Rb > 500KΩ.
8. Use precise resistor for Ra and Rb, and you will get more accurate voltage of V0.
9. Keep TEST pad no connection.
10. Note that all capacitors must have proper capacitance and voltage rating. The capacitance of capacitors connected with VOUT, CAP1 and CAP2 are 0.1μF ~ 4.7μF; 0.1μF ~ 4.7μF for V0 ~ V4. Capacitors connected with V0 ~ V4 have to be the same capacitance. The voltage rating of capacitors connected to VOUT has to be more than 16V, more than 10V for V0 ~ V4 and 6V for CAP1 and CAP2.

Pads	Capacitor	Max. Rating
CAP1+, CAP1-	0.1μF ~ 4.7μF	6V
CAP2+, CAP2-	0.1μF ~ 4.7μF	6V
VOUT	0.1μF ~ 4.7μF	16V
V0 ~ V4	0.1μF ~ 4.7μF	10V

11. Add regulator capacitor (10uF) and high frequency capacitor (0.1uF) between VDD and VSS on user's board.
12. The reset pin of NT7607 is floating inside the IC. Please make sure the reset pin of the customer's system is in a fixed status ("H" or "L") while operating this pin.
13. If using serial mode, please make sure /RD, /WR and PI pads must be fixed "H" or "L".

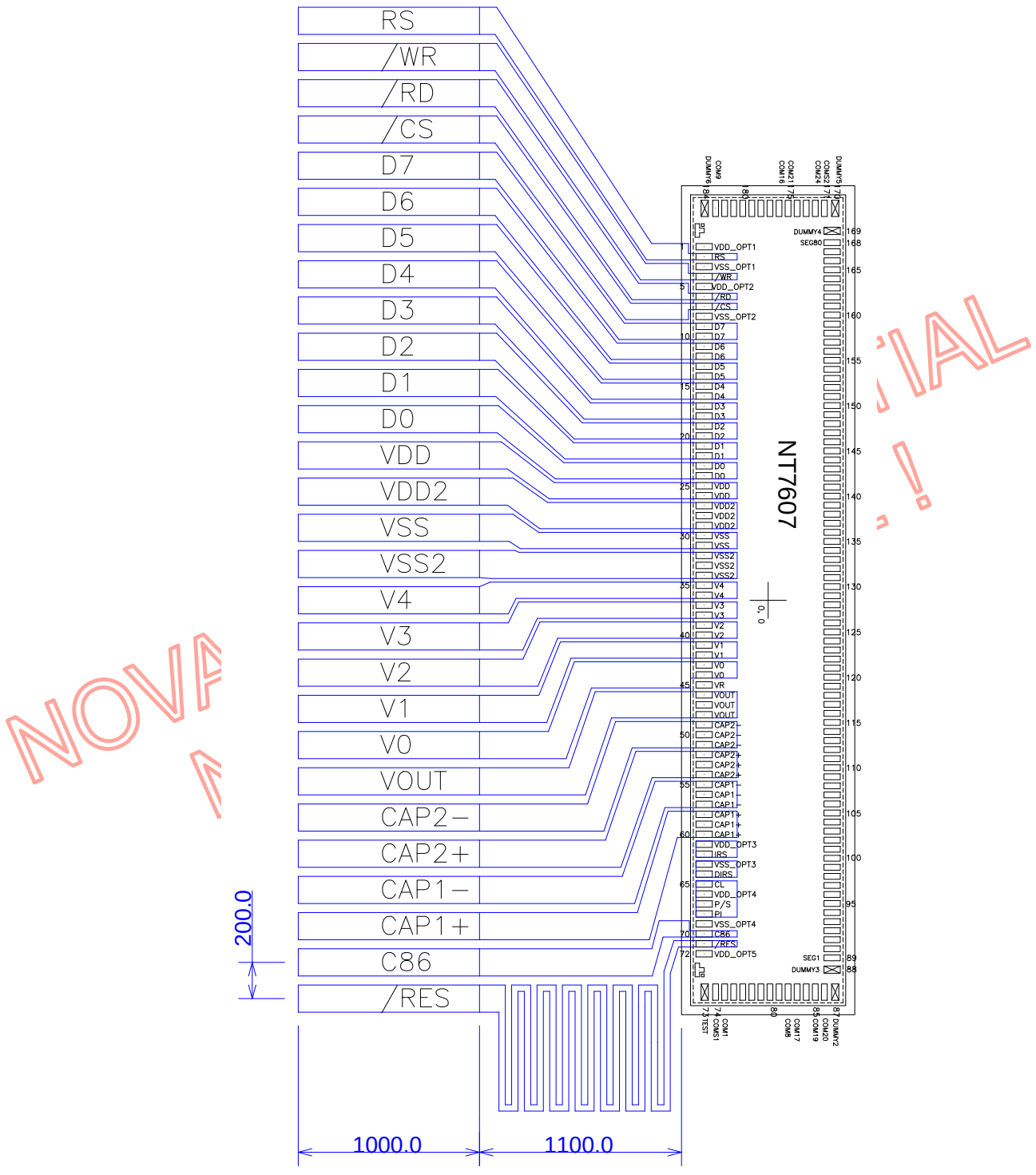
ITO Layout Notice

1. Specifically with COG application, it is important to reduce the resistance of the ITO path. To make the overall display performance of the LCM better, there are some suggestions for ITO layout described as below:
   a) Please keep the resistance of VDD (2) & VSS (2) path between PCB and corresponding pads of IC ≤ 200Ω. This value includes the ITO resistors' values, the FPC/Heat seal resistor; the ACF contact resistors between IC and Glass, Glass and FPC/Heat seal, FPC/Heat seal and PCB.
   b) Large resistance will reduce the efficiency of the voltage booster; the user should make the ITO resistance of charge pump pads as small as possible. The resistance of CAP1+, CAP1-, CAP2+, CAP2- and VOUT ≤ 300Ω; the resistance of V0 ~ V4 ≤ 300Ω.
   c) The value of the other pins of the interface ≤ 1KΩ (except the /RES pin).
   d) Make a long thin ITO line with an impedance of more than 4KΩand less than 10KΩbetween the RESET of interface and IC's /RES pads to work as a low-pass filter. With experience, it can filter some EMI and prevent the errors caused by ESD.

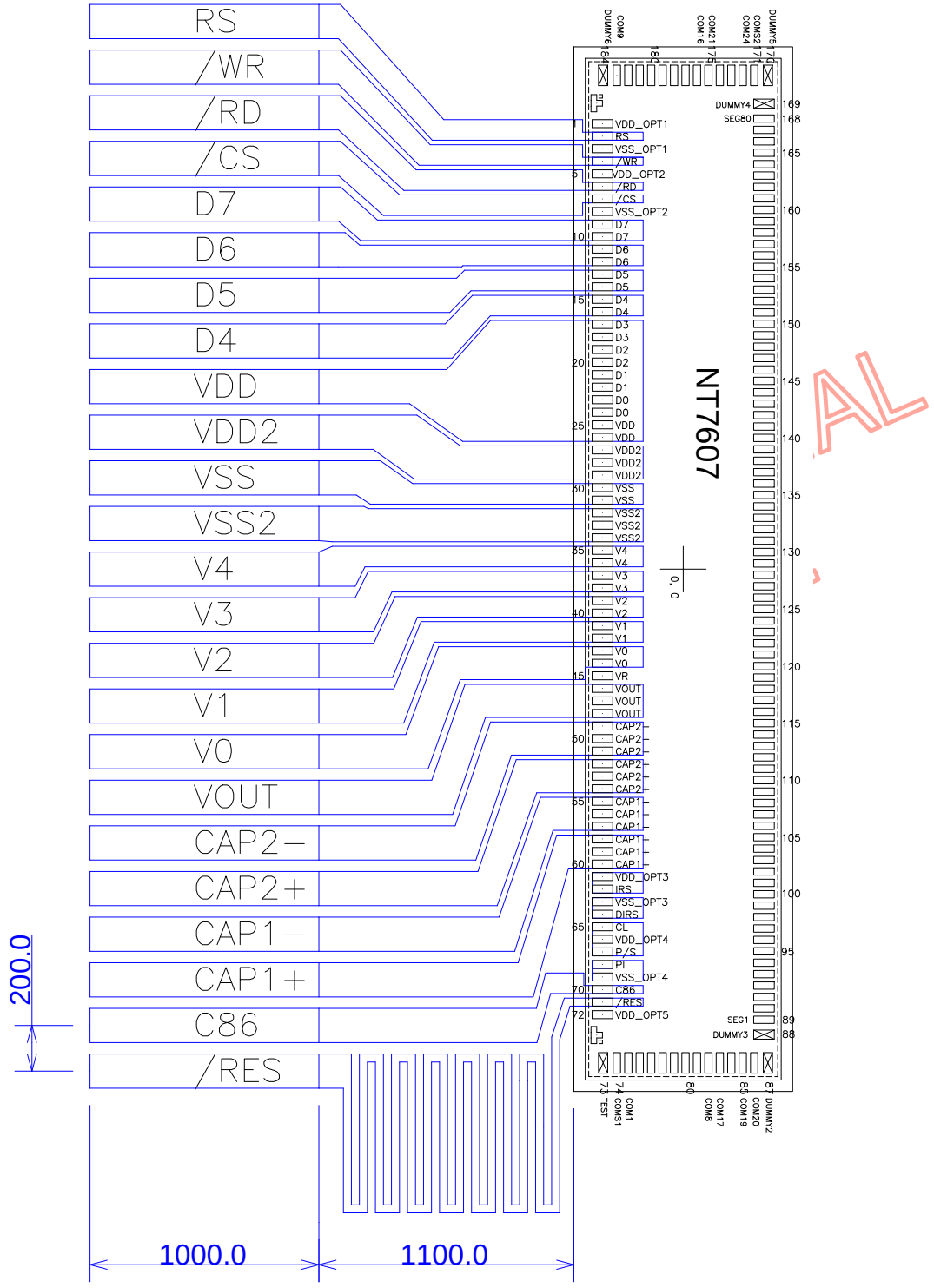
ITO Path	Max. Resistance
VDD, VDD2, VSS, VSS2	200Ω
CAP1+/-, CAP2+/-, VOUT	300Ω
V0 ~ V4, VR	300Ω
/RES	>4KΩ and <10KΩ
RS, /CS, /WR, /RD, D0 ~ D7	1KΩ

2. To meet the value demanded above while laying out ITO, users may accept the rules below:
   a) In order to keep the ITO resistance to a minimum, the pitch and position of the module connection to the outside should be selected to make the power lines go as straight as possible.
   b) The distance between NT7607 and FPC is the shorter as the better. Then the length of ITO will be the shortest and you can get a smaller resistor value.
   c) The ITO interface may fill the blank area on the LCD Panel to reduce the ITO resistance.

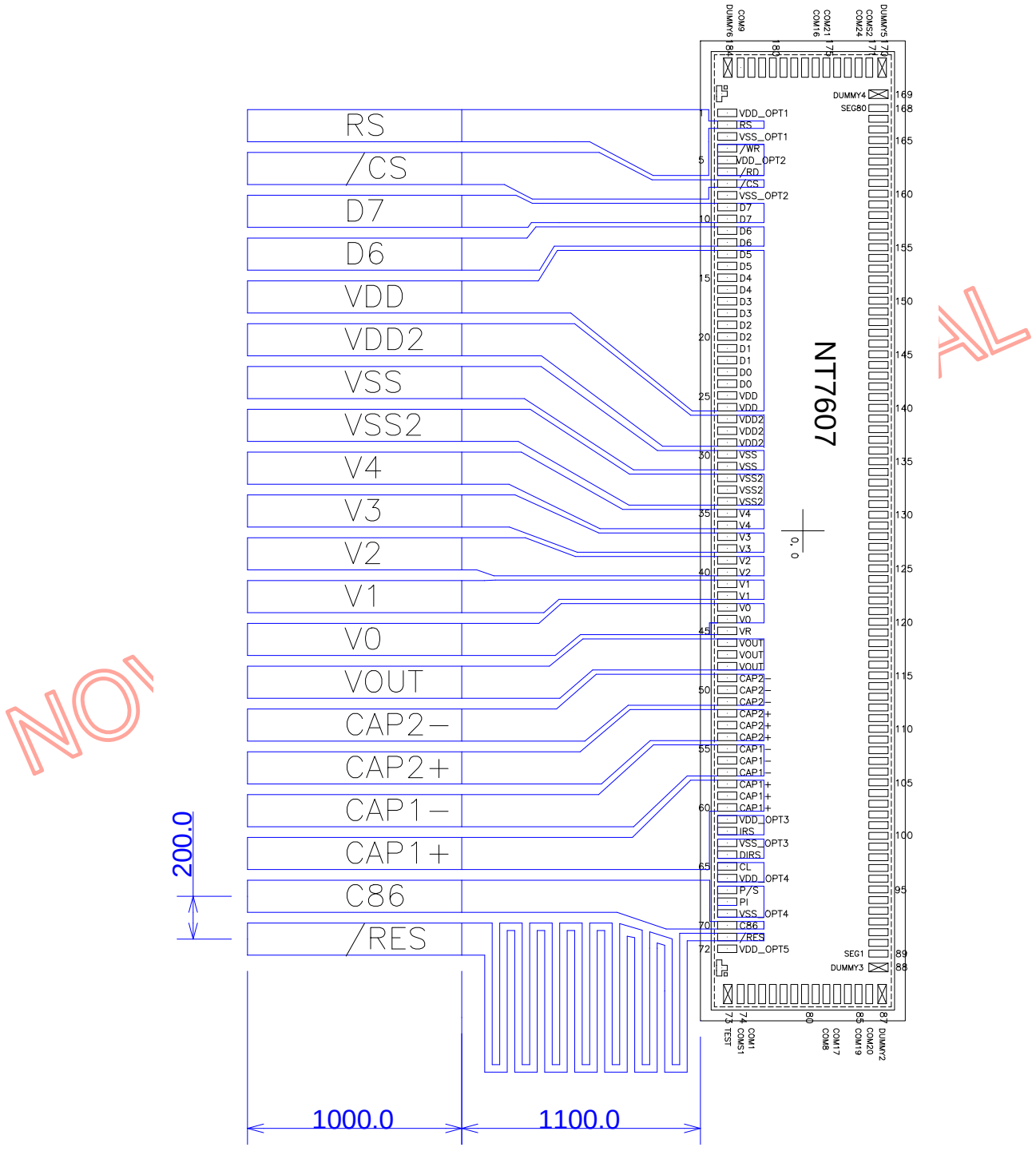
3. Reference the figures for ITO Layout:
   a) Figure 28 is ITO Layout for 8-bit parallel mode (Unit: μm)



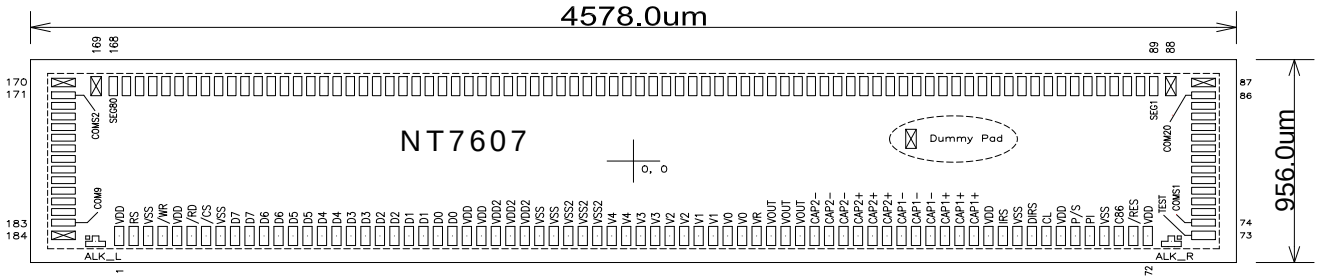
b) Figure 29 is ITO Layout for 4-bit parallel mode (Unit: μm)



c) Figure 30 is ITO Layout for Serial mode (Unit: μm)



Bonding Diagram



Unit: µm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	VDD	-1952.50	-353.00	31	VSS	-302.50	-353.00
2	RS	-1897.50	-353.00	32	VSS2	-247.50	-353.00
3	VSS	-1842.50	-353.00	33	VSS2	-192.50	-353.00
4	/WR	-1787.50	-353.00	34	VSS2	-137.50	-353.00
5	VDD	-1732.50	-353.00	35	V4	-82.50	-353.00
6	/RD	-1677.50	-353.00	36	V4	-27.50	-353.00
7	/CS	-1622.50	-353.00	37	V3	27.50	-353.00
8	VSS	-1567.50	-353.00	38	V3	82.50	-353.00
9	D7	-1512.50	-353.00	39	V2	137.50	-353.00
10	D7	-1457.50	-353.00	40	V2	192.50	-353.00
11	D6	-1402.50	-353.00	41	V1	247.50	-353.00
12	D6	-1347.50	-353.00	42	V1	302.50	-353.00
13	D5	-1292.50	-353.00	43	V0	357.50	-353.00
14	D5	-1237.50	-353.00	44	V0	412.50	-353.00
15	D4	-1182.50	-353.00	45	VR	467.50	-353.00
16	D4	-1127.50	-353.00	46	VOUT	522.50	-353.00
17	D3	-1072.50	-353.00	47	VOUT	577.50	-353.00
18	D3	-1017.50	-353.00	48	VOUT	632.50	-353.00
19	D2	-962.50	-353.00	49	CAP2-	687.50	-353.00
20	D2	-907.50	-353.00	50	CAP2-	742.50	-353.00
21	D1	-852.50	-353.00	51	CAP2-	797.50	-353.00
22	D1	-797.50	-353.00	52	CAP2+	852.50	-353.00
23	D0	-742.50	-353.00	53	CAP2+	907.50	-353.00
24	D0	-687.50	-353.00	54	CAP2+	962.50	-353.00
25	VDD	-632.50	-353.00	55	CAP1-	1017.50	-353.00
26	VDD	-577.50	-353.00	56	CAP1-	1072.50	-353.00
27	VDD2	-522.50	-353.00	57	CAP1-	1127.50	-353.00
28	VDD2	-467.50	-353.00	58	CAP1+	1182.50	-353.00
29	VDD2	-412.50	-353.00	59	CAP1+	1237.50	-353.00
30	VSS	-357.50	-353.00	60	CAP1+	1292.50	-353.00

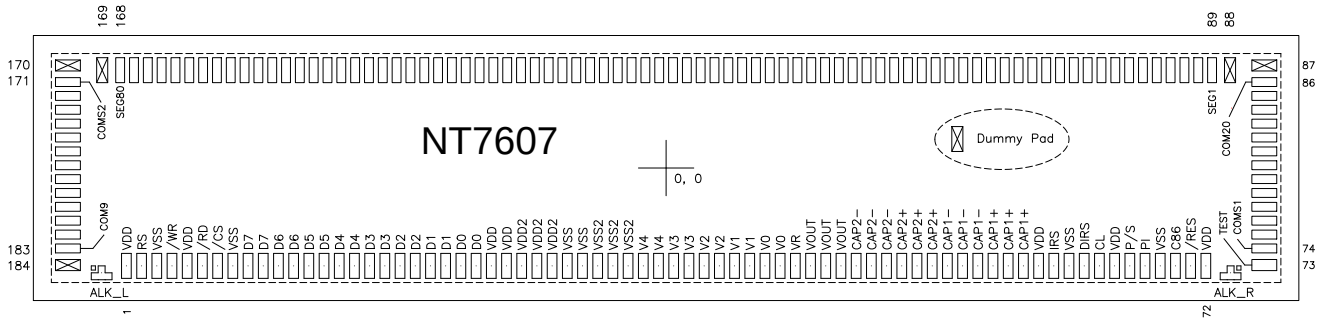
Bonding Diagram (continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
61	VDD	1347.50	-353.00	97	SEG9	1575.00	353.00
62	IRS	1402.50	-353.00	98	SEG10	1525.00	353.00
63	VSS	1457.50	-353.00	99	SEG11	1475.00	353.00
64	DIRS	1512.50	-353.00	100	SEG12	1425.00	353.00
65	CL	1567.50	-353.00	101	SEG13	1375.00	353.00
66	VDD	1622.50	-353.00	102	SEG14	1325.00	353.00
67	P/S	1677.50	-353.00	103	SEG15	1275.00	353.00
68	PI	1732.50	-353.00	104	SEG16	1225.00	353.00
69	VSS	1787.50	-353.00	105	SEG17	1175.00	353.00
70	C86	1842.50	-353.00	106	SEG18	1125.00	353.00
71	/RES	1897.50	-353.00	107	SEG19	1075.00	353.00
72	VDD	1952.50	-353.00	108	SEG20	1025.00	353.00
73	TEST	2164.00	-350.00	109	SEG21	975.00	353.00
74	COMS1	2164.00	-290.00	110	SEG22	925.00	353.00
75	COM1	2164.00	-240.00	111	SEG23	875.00	353.00
76	COM2	2164.00	-190.00	112	SEG24	825.00	353.00
77	COM3	2164.00	-140.00	113	SEG25	775.00	353.00
78	COM4	2164.00	-90.00	114	SEG26	725.00	353.00
79	COM5	2164.00	-40.00	115	SEG27	675.00	353.00
80	COM6	2164.00	10.00	116	SEG28	625.00	353.00
81	COM7	2164.00	60.00	117	SEG29	575.00	353.00
82	COM8	2164.00	110.00	118	SEG30	525.00	353.00
83	COM17	2164.00	160.00	119	SEG31	475.00	353.00
84	COM18	2164.00	210.00	120	SEG32	425.00	353.00
85	COM19	2164.00	260.00	121	SEG33	375.00	353.00
86	COM20	2164.00	310.00	122	SEG34	325.00	353.00
87	DUMMY1	2164.00	370.00	123	SEG35	275.00	353.00
88	DUMMY2	2040.00	353.00	124	SEG36	225.00	353.00
89	SEG1	1975.00	353.00	125	SEG37	175.00	353.00
90	SEG2	1925.00	353.00	126	SEG38	125.00	353.00
91	SEG3	1875.00	353.00	127	SEG39	75.00	353.00
92	SEG4	1825.00	353.00	128	SEG40	25.00	353.00
93	SEG5	1775.00	353.00	129	SEG41	-25.00	353.00
94	SEG6	1725.00	353.00	130	SEG42	-75.00	353.00
95	SEG7	1675.00	353.00	131	SEG43	-125.00	353.00
96	SEG8	1625.00	353.00	132	SEG44	-175.00	353.00

Bonding Diagram (continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
133	SEG45	-225.00	353.00	160	SEG72	-1575.00	353.00
134	SEG46	-275.00	353.00	161	SEG73	-1625.00	353.00
135	SEG47	-325.00	353.00	162	SEG74	-1675.00	353.00
136	SEG48	-375.00	353.00	163	SEG75	-1725.00	353.00
137	SEG49	-425.00	353.00	164	SEG76	-1775.00	353.00
138	SEG50	-475.00	353.00	165	SEG77	-1825.00	353.00
139	SEG51	-525.00	353.00	166	SEG78	-1875.00	353.00
140	SEG52	-575.00	353.00	167	SEG79	-1925.00	353.00
141	SEG53	-625.00	353.00	168	SEG80	-1975.00	353.00
142	SEG54	-675.00	353.00	169	DUMMY3	-2040.00	353.00
143	SEG55	-725.00	353.00	170	DUMMY4	-2164.00	370.00
144	SEG56	-775.00	353.00	171	COMS2	-2164.00	310.00
145	SEG57	-825.00	353.00	172	COM24	-2164.00	260.00
146	SEG58	-875.00	353.00	173	COM23	-2164.00	210.00
147	SEG59	-925.00	353.00	174	COM22	-2164.00	160.00
148	SEG60	-975.00	353.00	175	COM21	-2164.00	110.00
149	SEG61	-1025.00	353.00	176	COM16	-2164.00	60.00
150	SEG62	-1075.00	353.00	177	COM15	-2164.00	10.00
151	SEG63	-1125.00	353.00	178	COM14	-2164.00	-40.00
152	SEG64	-1175.00	353.00	179	COM13	-2164.00	-90.00
153	SEG65	-1225.00	353.00	180	COM12	-2164.00	-140.00
154	SEG66	-1275.00	353.00	181	COM11	-2164.00	-190.00
155	SEG67	-1325.00	353.00	182	COM10	-2164.00	-240.00
156	SEG68	-1375.00	353.00	183	COM9	-2164.00	-290.00
157	SEG69	-1425.00	353.00	184	DUMMY5	-2164.00	-350.00
158	SEG70	-1475.00	353.00	-	ALK_L	-2042.00	-378.00
159	SEG71	-1525.00	353.00	-	ALK_R	2042.00	-378.00

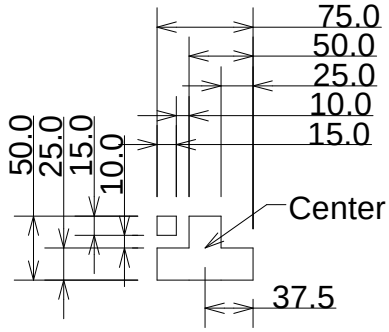
Package Information



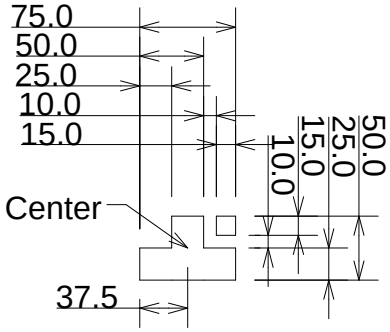
Pad Dimensions

Item	Pad No.	Size		Unit
		X	Y	
Chip size	-	4578.0	956.0	μm
Chip thickness	-	525		μm
Pad pitch	1~72	55		μm
	74~86, 89~168, 171~183	50		
	73~74, 86~87, 170~171, 183~184	60		
	88~89, 168~169	65		
Bump size	1~72	35	90	μm
	89~168	32	90	
	74~86, 171~183	90	32	
	88, 169	40	90	
	73, 87, 170, 184	90	40	
Bump height	All pads	15 ± 3		μm

Alignment Marks (Unit: μm)



ALK_L



ALK_R

Ordering Information

Part No.	Packages	CGROM Table
NT7607H-D01/3N	Gold Bump on Chip Tray	Refer to Table 3-1
NT7607H-D06/3N	Gold Bump on Chip Tray	Refer to Table 3-2

Cautions

1. The contents of this document will be subjected to change without notice.
2. Precautions against light projection:
   Light has the effect of causing the electrons of semiconductor to move; so light projection may change the characteristics of semiconductor devices. For this reason, it is necessary to take account of effective protection measures for the packages (such as COB, COG, TCP and COF, etc.) causing chip to be exposed to a light environment in order to isolate the projection of light on any part of the chip, including top, bottom and the area around the chip.
   Observe the following instructions in using this product:
   a. During the design stage, it is necessary to notice and confirm the light sensitivity and preventive measures for using IC on substrate (PCB, Glass or Film) or product.
   b. Test and inspect the product under an environment free of light source penetration.
   c. Confirm that all surfaces around the IC will not be exposed to light source.