NOVATEK
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Data Sheet

NT7573

132RGB X 132 RAM-Map STN LCD Controller/Driver for 65K Colors

V0.03

Preliminary

Features

- 132RGB x 132-dot graphics display LCD controller/driver for 65,536 STN colors
- RAM capacity: 132 x 16 x 132 = 278,784 bits
- 8-bit/16-bit parallel bus interface for both 8080 and 6800 series, 3-wire/4-wire Serial Peripheral Interface (SPI)
- 65,536 colors can be displayed at the same time by PWM and FRC
- Data output scan direction controlled by software commands
  - Shift change of common drivers
  - RAM addressing direction control (vertical and horizontal)
- Power supply voltage:
  - VDDIO = 1.2 ~ 3.6 V (power supply for interface circuit)
  - VDD = 1.65 ~ 1.95 V (power supply for digital circuit)
  - VIN1/VIN1A//VIN1R = 2.4 ~ 3.6 V (power supply for 1st booster circuit, VM Amp and regulator.)
  - V1 = 2.0 ~ 3.3 V (power supply for Segment Driver)
  - VCC-VEE = 19.8 V Max.(power supply for Common Driver)
- On chip LCD driving voltage generator or external power supply selectable
- 256-step contrast adjuster and on chip voltage follower
- Programmable drive duty ratios (1/33, 1/66, 1/96, 1/108, 1/120, 1/132) and bias values (1/4~1/6)
- Programmable partial display, screen scrolling
- N-block inversion AC liquid-crystal drive
- On chip oscillation and hardware reset
- Multi-Time Programming (2 times) for V1 voltage
- Available in COG form
- CMOS process

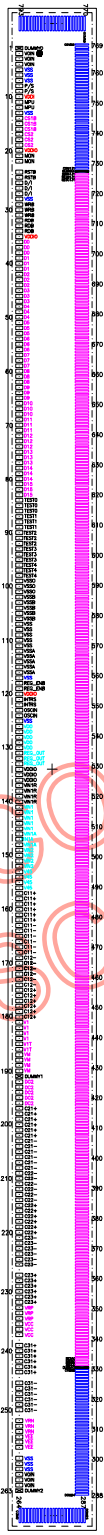
General Description

The NT7573 is a single-chip LCD controller/driver LSI for color-graphics, which displays 132 x 132-dot graphics for 65,536 STN colors. It accepts display data through 8-bit/16-bit parallel (8080 or 6800 series) or serial (3-wire or 4-wire) interface directly sent from a µC and stores it in an on-chip display data RAM.

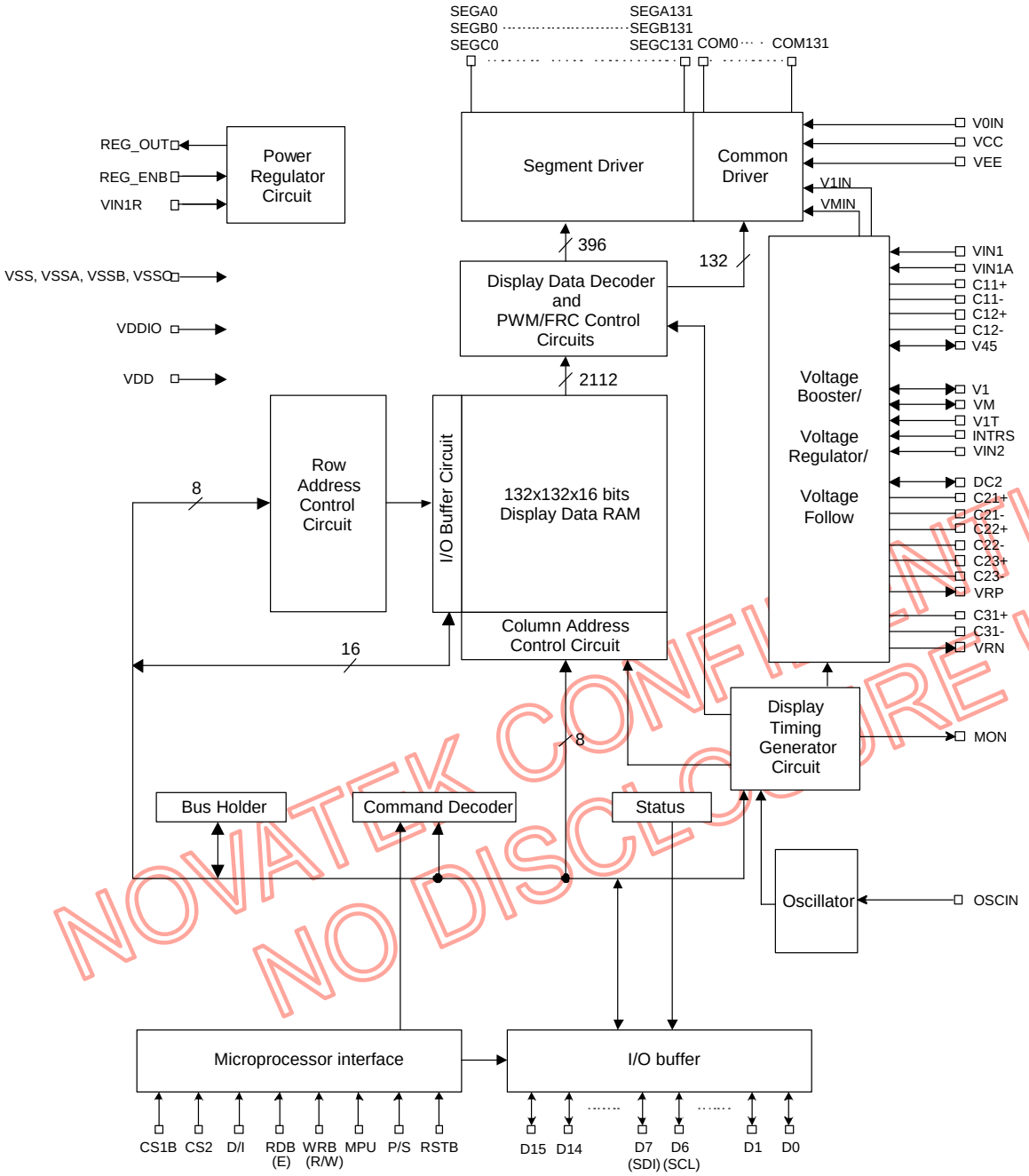
The NT7573 contains 132 common output circuits and 132 x 3 segment output circuits. The capacity of the on-chip display data RAM is 132 x 132 x 16 bits and every 16-bit corresponds to one pixel (include RGB) LCD panel. It generates an LCD drive signal independent of the MPU clock.

No external operation clock is required for RAM read/write operations. Accordingly, this driver can be operated with a minimum current consumption. It can implement a high-performance handy display system with minimum current consumption and the smallest LSI configuration.

Pad Configuration



Block Diagram



Pad Descriptions

Power Supply

Pad No.	Designation	I/O	Description
134~136	VDDIO	Supply	Main power supply
10, 20, 35, 120	VDDIO	O	Main power supply for pad option
126~130	VDD	Supply	Power supply for internal digital and DDRAM block This pin is connected to REG_OUT with stabilization capacitor When internal regulator is not used, connect VDD to VDDIO
5~7, 257~259, 107~111	VSS	Supply	Ground. All pads must be connected to ground
112~116	VSSA		
102~106	VSSB		
99~101	VSSO		
13, 28, 117, 125	VSS	O	Ground for pad option
137~140	VIN1R	Supply	Internal regulator power supply
141~145	VIN1	I	Power supply for 1st booster circuit and VM amplifier
146~148	VIN1A		
149~152	VIN2	I	Power supply for DC2 amplifier
153~156	V45	O	1st booster output pin, and Multi-Time Programming pin
		I	Power supply for V1 (1st booster off)
181~184	V1	O	LCD segment high driving voltage output
		I	LCD segment high driving voltage input (OP AMP off)
187~190	VM	O	LCD common non-selected driving voltage output
		I	LCD common non-selected driving voltage input (OP AMP off)
192~196	DC2	O	Power output pin for 2nd booster circuit input
		I	Power supply for 2nd booster circuit (OP AMP off)
2~4, 260~262	V0IN	I	LCD segment low driving voltage input
233~235	VRP	O	LCD common high selected driving voltage output
236~238	VCC	I	LCD common high selected driving voltage input
251~253	VRN	O	LCD common low selected driving voltage output
254~256	VEE	I	LCD common low selected driving voltage input

Power Supply (continuous)

Pad No.	Designation	I/O	Description
157~162, 163~168, 169~174, 175~180	C11+, C11-, C12-, C12+	O	External capacitor connection pins used for 1st booster circuit
197~202, 203~208, 209~214, 215~220, 221~226, 227~232	C21+, C21-, C22-, C22+, C23+, C23-	O	External capacitor connection pins used for 2nd booster circuit
239~244, 245~250	C31+, C31-	O	External capacitor connection pins used for 3rd booster circuit
185, 186	V1T	I	Thermistor resistor connection pin

Note: The IN / OUT settings of V45, DC2, V1, VM are controlled by DC/DC and AMP ON/OFF Set command.

* Make sure of the relationship of LCD driving voltage as follows:
  (1) VCC > V1 > VM > V0IN (=VSS) > VEE
  (2) VCC - VM = VM - VEE, V1 - VM = VM - V0IN

LCD Driver Pads

Pad No.	Designation	I/O	Description
333~728	SEGA0 ~ SEGA131	O	Segment signal outputs for LCD display (Red or Blue)
	SEGB0 ~ SEGB131	O	Segment signal outputs for LCD display (Green)
	SEGC0 ~ SEGC131	O	Segment signal outputs for LCD display (Blue or Red)
265~288, 290~331, 730~771, 773~796	COM0~23 COM24~65 COM131~90 COM89~66	O	Common signal outputs for LCD display

Configuration Pads

Pad No.	Designation	I/O	Description
121, 122	INTRS	I	External resistor select for temperature compensation circuit INTRS =”L” : external resistor mode INTRS =”H” : internal resistor mode

System Bus Connection

Pad No.	Designation	I/O	Description
23, 24	RSTB	I	Reset input pin. When RSTB is set to “L”, the settings are initialized.
8, 9	P/S	I	MPU interface select pin. When P/S is ”H” MPU = ”L”: 8080 series MPU interface MPU = ”H”: 6800 series MPU interface When P/S is ”L” MPU = ”L”: 3 pin SPI (Write only) MPU = ”H”: 4 pin SPI (Write only)
11, 12	MPU	I	
14~16	CS1B	I	Chip select input pin. When CS1B is “L” and CS2 is ”H”, the data / command I/O is enabled. When chip select is non-active, D0 to D15 are high impedance
17~19	CS2	I	
25~27	D/I	I	Data / Command select input pin. D/I = “H”: Indicates that D0 to D15 are display data D/I = “L”: Indicates that D0 to D15 are control data
29~31	WRB (R/W)	I	When 6800 series MPU is selected, this is the read / write control input pin. R/W = “H”: read R/W = “L”: write When 8080 MPU is selected, this is the write enable clock input pin. The data on D0 to D15 are latched at the rising edge of the WRB signal.
32~34	RDB (E)	I	When 6800 series MPU is selected, this is the enable control input pin. R/W = “H”: D0 to D15 are in output status when E is “H”. R/W = “L”: The data on D0 to D15 are latched at the falling edge of WRB signal When 8080 MPU is selected, this is the read enable clock input pin. The data on D0 to D15 are in output status when RDB is “L”.
36~83	D15 ~ D8 D7 (SDI) D6 (SCL) D5 ~ D0	I/O	When parallel interface is selected, D15 to D0 (D7 to D0) are serves as the 16-bit (8-bit) bi-directional data bus. When the serial interface is selected, D7 (SDI): serial data input pin. The data is latched at the rising edge of SCL signal. D6 (SCL): serial clock input pin.

Timing Signal for Monitor

Pad No.	Designation	I/O	Description
21, 22	MON	O	Monitor signal output pin. (CL, FR, PM, SYNC)

Oscillator and Internal Regulator

Pad No.	Designation	I/O	Description
123, 124	OSCIN	I	External clock input pin when external clcok is used When the internal RC oscillator is used, fixed this pin to VDDIO or VSS
118, 119	REG_ENB	I	Internal regulator enable pin REG_ENB = "L": Enable internal regulator REG_ENB = "H": Disable internal regulator
131~133	REG_OUT	O	Internal regulator output pin This output voltage is used as a power supply for the internal digital and DDRAM block via VDD pin

Test Pads

Pad No.	Designation	I/O	Description
84~86	TEST0	O	Test pads. No connection
87~98	TEST1 ~ 4	I	Test pads. Must be connected to VSS

No Connected Pads

Pad No.	Designation	I/O	Description
1, 191, 263, 264, 289, 332, 729, 772, 797	DUMMY0 ~ DUMMY8	-	Dummy pads. No connection

Functional Descriptions

Microprocessor Interface

The NT7573 can transfer data via 16-bit bi-directional data bus (D15 to D0) or via serial data input (SDI). When high or low is selected for the parity of P/S, MPU pads and command bit 16B, either 8-bit/16-bit parallel data input or serial data input can be selected as shown in Table 1. When serial data input is selected, the RAM data cannot be read out.

Table 1. Data Bus Interface Selection Mode

P/S	MPU	16B	Type	CS1B	CS2	D/I	RDB (E)	WRB (R/W)	D15 to D8	D7	D6	D5 to D0
L	L	-	3-wire SPI	CS1B	CS2	-	-	-	-	SDI	SCL	-
	H	-	4-wire SPI	CS1B	CS2	D/I	-	-	-	SDI	SCL	-
H	L	L	8080 series 8-bit	CS1B	CS2	D/I	RDB	WRB	-	D7	D6	D5 to D0
	L	H	8080 series 16-bit	CS1B	CS2	D/I	RDB	WRB	D15 to D8	D7	D6	D5 to D0
	H	L	6800 series 8-bit	CS1B	CS2	D/I	E	R/W	-	D7	D6	D5 to D0
	H	H	6800 series 16-bit	CS1B	CS2	D/I	E	R/W	D15 to D8	D7	D6	D5 to D0

"-" Must always be VDDIO or VSS

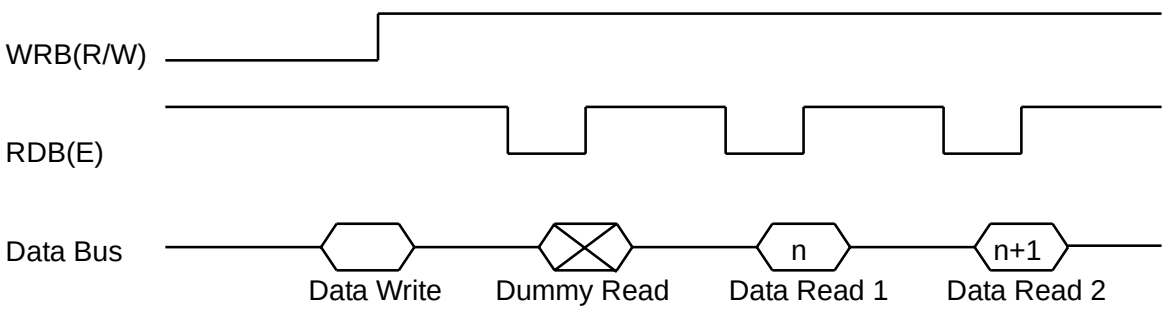
Parallel Interface

When the NT7573 selects parallel interface (P/S is high), the type of MPU interface is determined by MPU pad as shown in Table 1. The NT7573 identifies the data bus signal according to D/I, RDB (E), WRB (R/W) signals as shown in Table 2.

Table 2. Parallel Interface Read/Write Status

Control	6800 processor		8080 processor		Function
D/I	E	R/W	RDB	WRB	
0	1	1	0	1	Reads status
0	1	0	1	0	Writes instruction data
1	1	1	0	1	Reads display data
1	1	0	1	0	Writes display data

A dummy read is required before the first actual display data read for parallel interface.



Serial Interface

When the serial interface has been selected (P/S is low), the 3-wire or 4-wire SPI can be selected by causing the MPU pad to go high or low.

In the 4-wire SPI, the serial data is read from the serial data input pin on the rising edge of the serial clocks in the order of D7, D6, D5, ……, D0. This data is converted to 8-bit parallel data on the rising edge of the eighth serial clock for processing. The D/I input is read on every 8th rising edge of the serial clock and used to determine whether the serial data input is specified as command or display data.

In the 3-wire SPI, the D/I pin is not used. The serial data is read from the serial data input pin on the rising edge of the serial clocks in the order of D/I, D7, D6, D5, ……, D0. This data is converted to 8-bit parallel data on the rising edge of the ninth serial clock for processing as command or display data that is determined by the first bit D/I.

Figure 1. 4-wire SPI

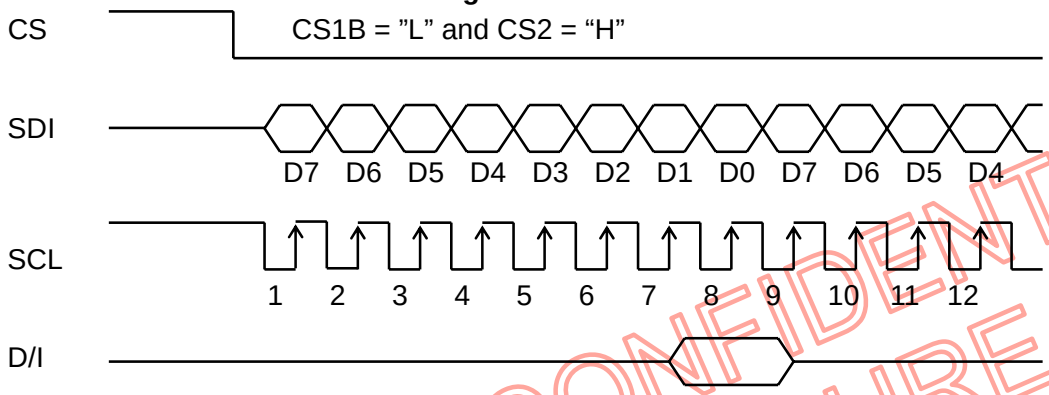
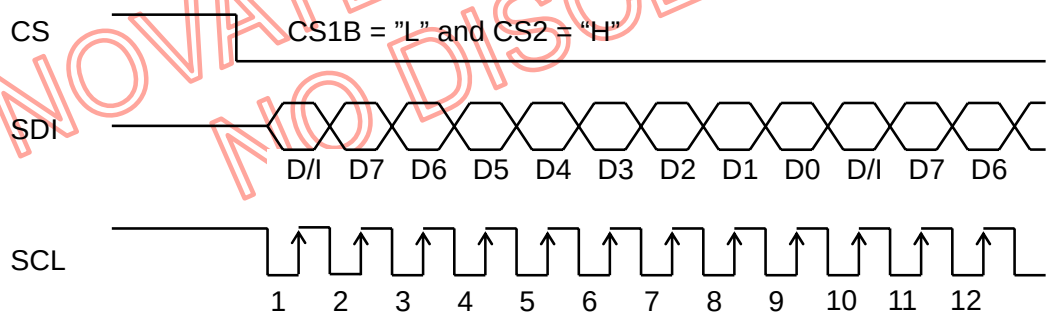


Figure 2. 3-wire SPI



Note:
1. When the chip is not active, the shift registers and the counter is reset to their initial states.
2. Reading is not possible while in serial interface mode.
3. Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend the operation be rechecked on the actual equipment.

Display Data RAM

The display data RAM (DDRAM) is RAM that stores the dot data for the display. It has a 132 x 132 x 16 bit structure. The 16 bits of data are stored into the DDRAM to display one dot (Red: 5 bits, Green: 6 bits, Blue: 5 bits) for 65,536 colors. It is controlled by row and column addresses. RAM area selection and automatic address count modes are achieved by Row/Column Address Set and Entry Mode Set commands. Figure 3 shows the DDRAM addressing maps for the 8-bit parallel mode and 16-bit parallel mode.

Moreover, reading from and writing to the DDRAM from the MPU side is performed through the I/O buffer, which is an independent operation from signal reading for the liquid crystal driver.

Access to DDRAM and Internal Registers

The NT7573 can perform a series of pipeline processes between LSI's using the bus holder of the internal data bus in order to match the operating frequency of DDRAM and internal registers with the MPU. Also, the MPU temporarily stores display data in the bus holder, and stores it in DDRAM until the next data write cycle starts.

When viewed from the MPU, the NT7573 access speed greatly depends on the cycle time rather than access time to the DDRAM (t_{ACC}). This view shows that the data transfer speed to/ from the MPU can increase. If the cycle time is inappropriate, the MPU can insert the NOP instruction that is equivalent to the wait cycle setup.

However, when an address is set, the specified address data is not output immediately following the read instruction. The address data is output during the second data read. A single dummy read must be inserted after address setup and after the write cycle (refer to the Parallel Interface description).

The Oscillator Circuit

The internal oscillator can produce the system clock. The oscillator circuit is only enabled when EXT=0. When EXT=1, the oscillation stops and the system clock is input through the OSCIN terminal.

Display Timing Generator Circuit

The display timing generator circuit generates the timing signal to the row address circuit and the display data decoder circuit using the system clock. Reading to the display data liquid crystal driver circuits is completely independent of access to the DDRAM by the MPU.

Moreover, the display timing generator circuit generates 4 type monitor signals from the system clock by setting Monitor Signal Control command. The 4 type monitor signals are common timing (CL), liquid crystal alternating current signal (FR), Field delimiter signal (PM), and Frame delimiter signal (SYNC).

Figure 3. Relationship Between DDRAM and Address

16-bit Data Bus Mode	D15 D14 D13 D12 D11	D10 D9 D8 D7 D6 D5	D4 D3 D2 D1 D0	D15 D14 D13 D12 D11	D10 D9 D8 D7 D6 D5	D4 D3 D2 D1 D0	.....	D15 D14 D13 D12 D11	D10 D9 D8 D7 D6 D5	D4 D3 D2 D1 D0	D15 D14 D13 D12 D11	D10 D9 D8 D7 D6 D5	D4 D3 D2 D1 D0	SWP = 0
8-bit Data Bus Mode	D7 D6 D5 D4 D3	D2 D1 D0 D7 D6 D5	D4 D3 D2 D1 D0	D7 D6 D5 D4 D3	D2 D1 D0 D7 D6 D5	D4 D3 D2 D1 D0	.....	D7 D6 D5 D4 D3	D2 D1 D0 D7 D6 D5	D4 D3 D2 D1 D0	D7 D6 D5 D4 D3	D2 D1 D0 D7 D6 D5	D4 D3 D2 D1 D0	
16-bit Data Bus Mode	D4 D3 D2 D1 D0	D10 D9 D8 D7 D6 D5	D15 D14 D13 D12 D11	D4 D3 D2 D1 D0	D10 D9 D8 D7 D6 D5	D15 D14 D13 D12 D11	.....	D4 D3 D2 D1 D0	D10 D9 D8 D7 D6 D5	D15 D14 D13 D12 D11	D4 D3 D2 D1 D0	D10 D9 D8 D7 D6 D5	D15 D14 D13 D12 D11	SWP = 1
8-bit Data Bus Mode	D4 D3 D2 D1 D0	D2 D1 D0 D7 D6 D5	D7 D6 D5 D4 D3	D4 D3 D2 D1 D0	D2 D1 D0 D7 D6 D5	D7 D6 D5 D4 D3	.....	D4 D3 D2 D1 D0	D2 D1 D0 D7 D6 D5	D7 D6 D5 D4 D3	D4 D3 D2 D1 D0	D2 D1 D0 D7 D6 D5	D7 D6 D5 D4 D3	

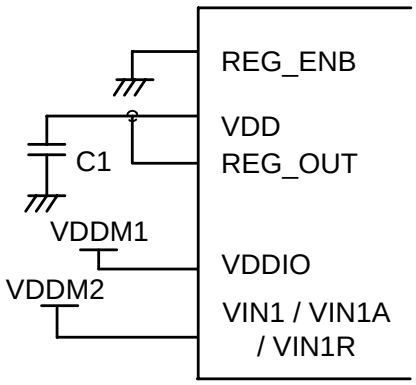
COM Output (CDR = 1)				Row Address MY = 1	R	G	B	R	G	B	.....	R	G	B	R	G	B	Row Address MY = 0	COM Output (CDR = 0)			
DL[1,0] = 11	DL[1,0] = 10	DL[1,0] = 01	DL[1,0] = 00																DL[1,0] = 00	DL[1,0] = 01	DL[1,0] = 10	DL[1,0] = 11
COM131	COM125	COM119	COM113	131														0	COM0	COM0	COM0	COM0
COM130	COM124	COM118	COM112	130														1	COM1	COM1	COM1	COM1
:	:	:	:	:														:	:	:	:	:
COM84	COM78	COM72	COM66	84														47	COM47	COM47	COM47	COM47
COM83	COM77	COM71	COM47	83														48	COM66	COM48	COM48	COM48
:	:	:	:	:														:	:	:	:	:
COM78	COM72	COM66	COM42	78														53	COM71	COM53	COM53	COM53
COM77	COM71	COM53	COM41	77														54	COM72	COM66	COM54	COM54
:	:	:	:	:														:	:	:	:	:
COM72	COM66	COM48	COM36	72														59	COM77	COM71	COM59	COM59
COM71	COM59	COM47	COM35	71														60	COM78	COM72	COM66	COM60
:	:	:	:	:														:	:	:	:	:
COM66	COM54	COM42	COM30	66														65	COM83	COM77	COM71	COM65
COM65	COM53	COM41	COM29	65														66	COM84	COM78	COM72	COM66
:	:	:	:	:														:	:	:	:	:
COM37	COM25	COM13	COM1	37							.....							94	COM112	COM106	COM100	COM94
COM36	COM24	COM12	COM0	36														95	COM113	COM107	COM101	COM95
:	:	:		:														:		:	:	:
COM31	COM19	COM7		31														100		COM112	COM106	COM100
COM30	COM18	COM6		30														101		COM113	COM107	COM101
:	:	:		:														:		:	:	:
COM25	COM13	COM1		25														106		COM118	COM112	COM106
COM24	COM12	COM0		24														107		COM119	COM113	COM107
:	:			:														:			:	:
COM19	COM7			19														112			COM118	COM112
COM18	COM6			18														113			COM119	COM113
:	:			:														:			:	:
COM13	COM1			13														118			COM124	COM118
COM12	COM0			12														119			COM125	COM119
:				:														:				:
COM7				7														124				COM124
COM6				6														125				COM125
:				:																		:
COM1				1														130				COM130
COM0				0														131				COM131

Column Address	MX = 0	0			1			.....	130			131							
	MX = 1	131			130			.....	1			0							
SEG Output		SEGA0	SEGB0	SEGC0	SEGA1	SEGB1	SEGC1	.....	SEGA130	SEGB130	SEGC130	SEGA131	SEGB131	SEGC131					

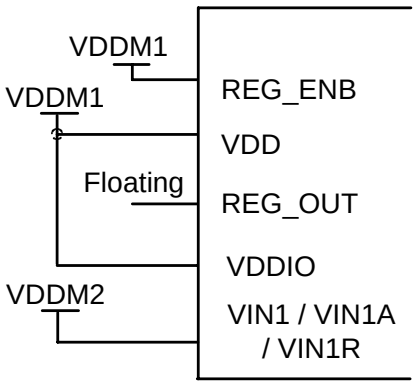
The Power Regulator Circuit

The NT7573 has a regulator circuit for VDD supply. The on-chip regulator configuration is shown as follows:

VDDM1 = 1.2 ~ 3.6V
VDDM2 = 2.4 ~ 3.6V



VDDM1 = 1.65 ~ 1.95V
VDDM2 = 2.4 ~ 3.6V



The Voltage Regulator Circuit for V1

The NT7573 has an internal high-accuracy fixed voltage power supply with 256 steps electronic volume function for V1 OP-Amp. Through the use of V1 electronic volume function, the LCD driving voltage V1 can be controlled by Contrast Control (1) or (2) command to adjust the V1 voltage from 2.0V to 3.3V by 5.098mV per step which then makes it possible to adjust LCD brightness. The 1st booster circuit generates V45 used for power supply of internal OP-Amps.

C1[7:0] or C2[7:0]	Value	V1
00000000	0	2.0
00000001	1	2.005098
00000010	2	2.010196
:	:	:
11111101	253	3.289804
11111110	254	3.294902
11111111	255	3.3

The Power Supply Circuit for VM, VRN and VRP

The common non-selected voltage VM is generated from V1 to keep V1 = 2 x VM. And through the DC2 OP-Amp and 2nd booster circuit, VRP can be controlled by Bias Set command and this keeps the relation VRP - VM = B x VM (bias ratio is 1/B). Finally, the 3rd booster circuit inverts the VRP that refers to VM to generate VRN. The VRN and VRP are both common selected voltages.

Multi-Time Programming (MTP) for V1 voltage

The NT7573 has a MTP function for V1 voltage calibration. Because the variation of LCD module in term of contrast level, the MTP (Multi-Time Program) can be used to achieve the best visual contrast of every LCD module by adjusting V1 voltage. The NT7573 provides only two times for V1 voltage programming. Refer to the Multi-Time Calibration Set and Multi-Time Programming Set command section.

The Discharge Circuit

When executing the command Standby Mode ON (STB is high), the driving voltage levels will be discharged. The relation between driving voltage levels and discharge time is as follows:

Driving Voltage	Condition	T	ΔV+, ΔV-
VCC, V1, VM, VEE	VCC = 11.55 V, V1 = 3.3V VEE = -8.25 V, VM= 1.65 V at t = 0	100 ms	< 50 mV
		300 ms	< 20 mV

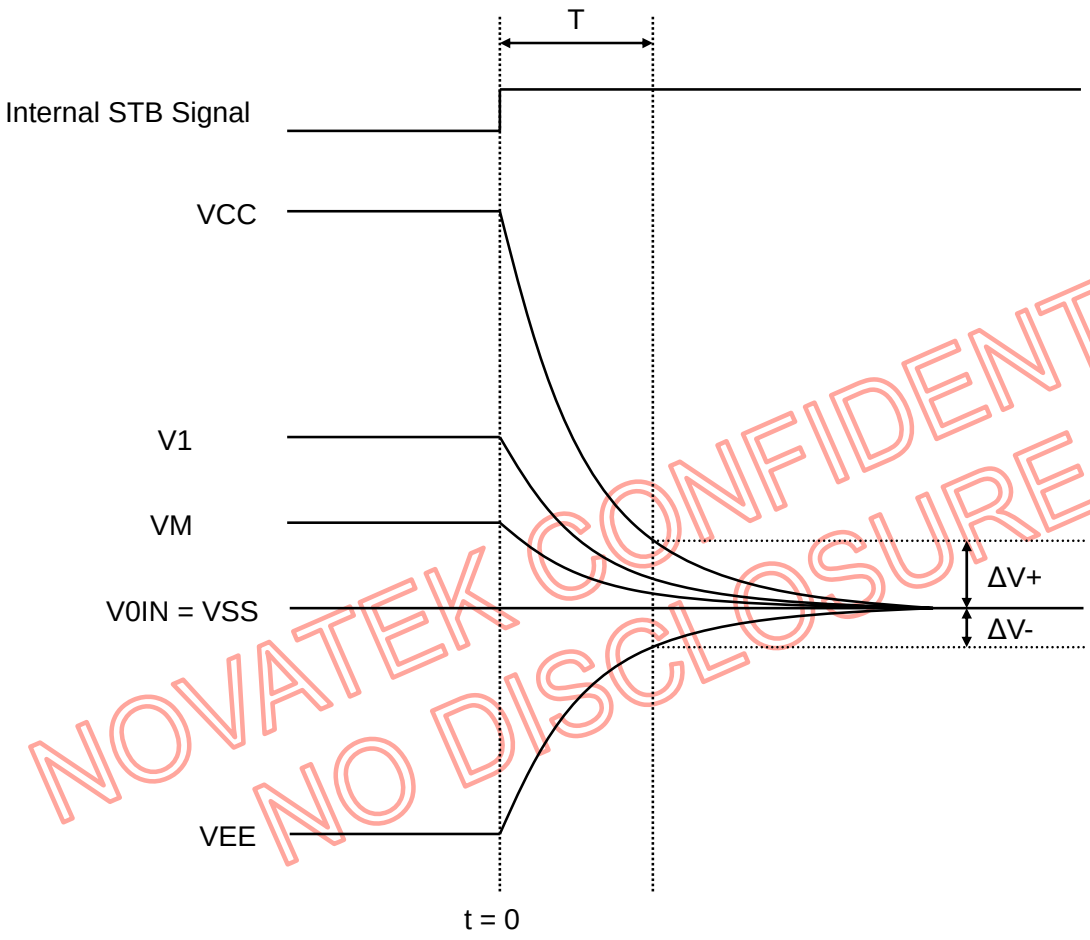


Figure 4. Internal Power Mode

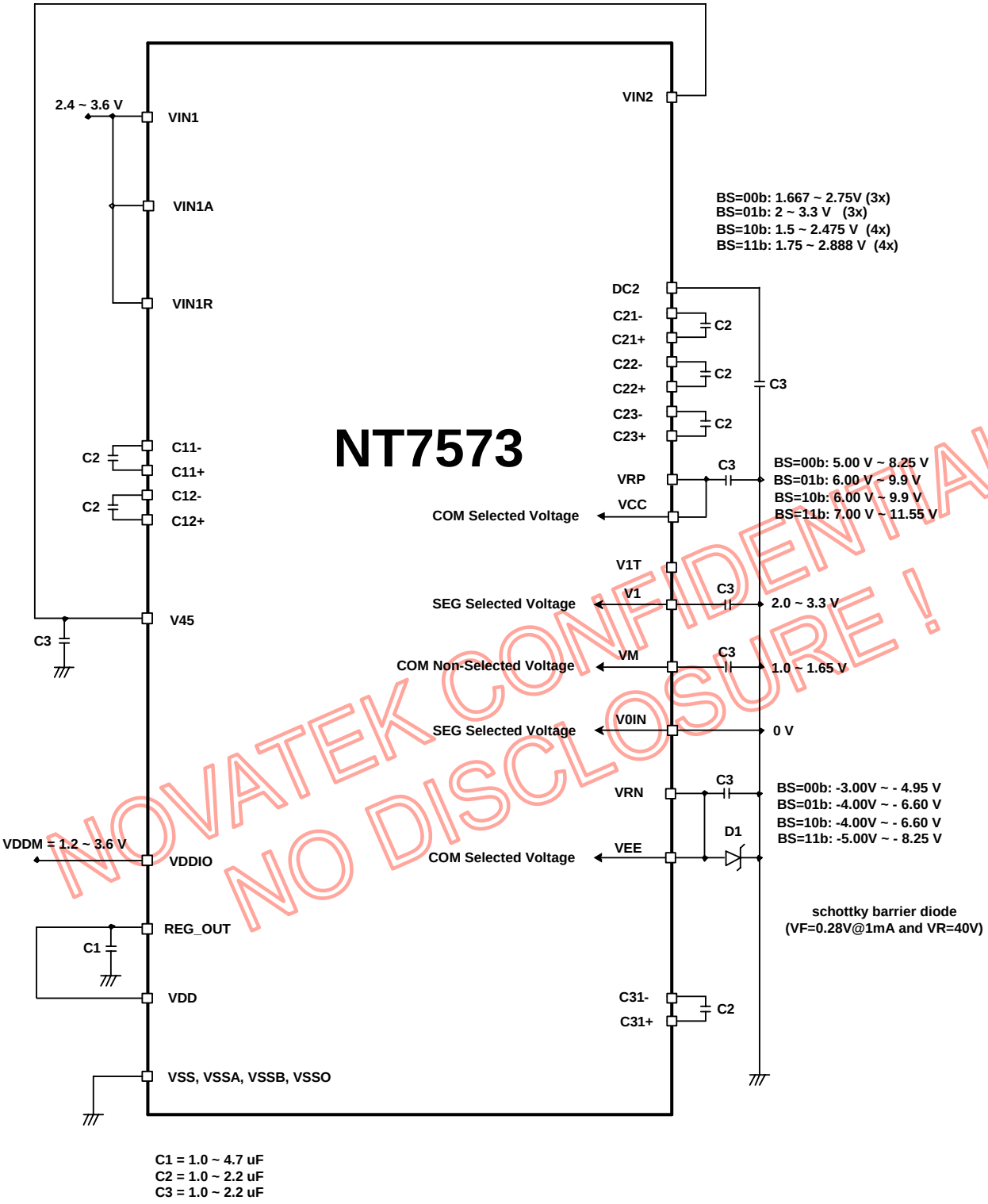
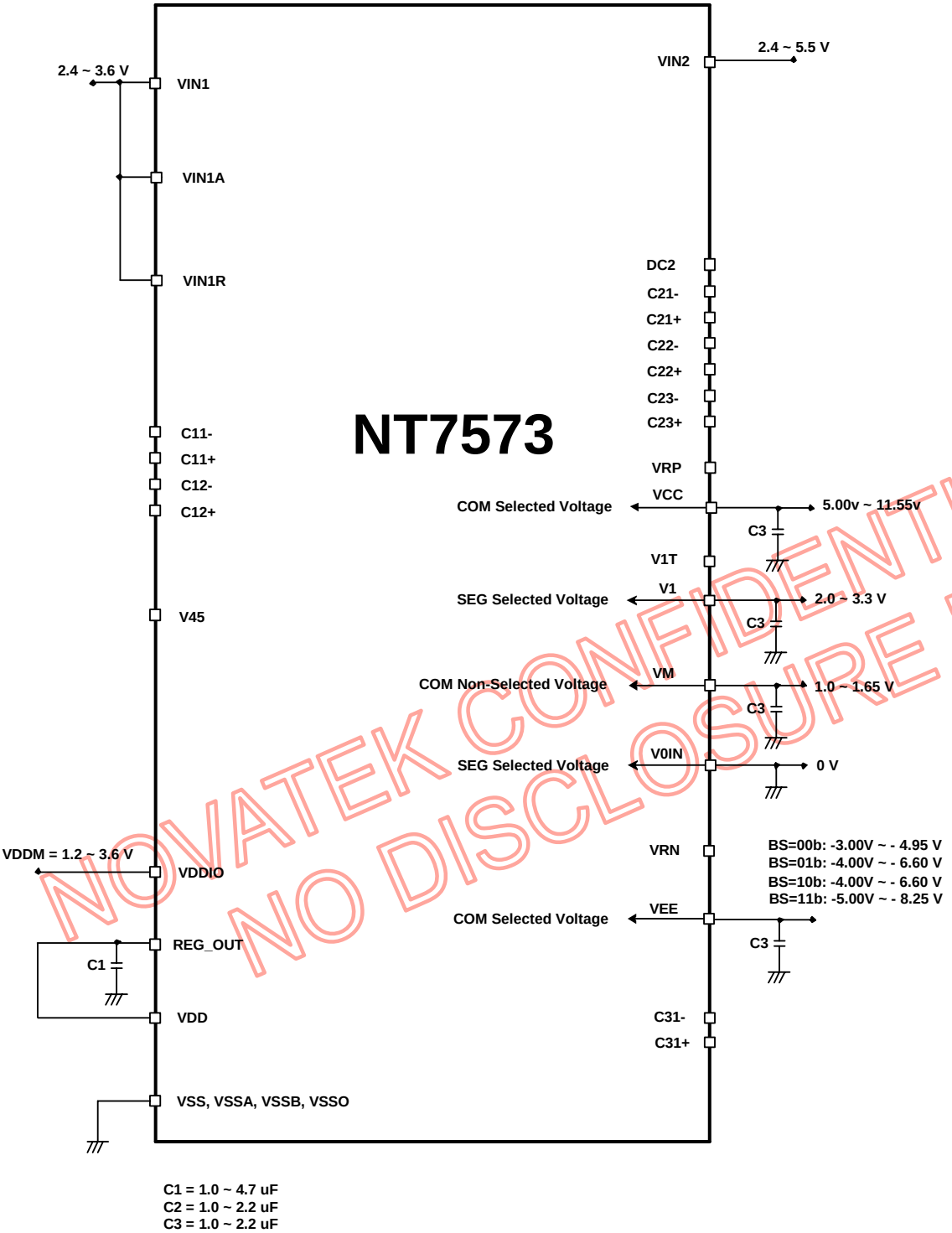


Figure 5. External Power Mode



Reset Circuit

When the RSTB input falls to LOW, the NT7573 enter their default state shown as below:

1. Internal clock mode and internal oscillator OFF, EXT=0, OSCEN=1
2. Driving Output Mode
   - Display duty ratio 1/132, DL[1:0]=(1,1)
   - No swap for segment driver and normal common scan direction, SWP=CDR=0
3. Monitor Signal Control
   SYNC, PM, CL and FR output VSS level, SYN=PM=CL=FR=0
   SYNC output at the head of the 1st subframe, SY[1:0]=(0,0)
4. x1.5 time boost for 1st booster circuit, DC[3:0]=(0,1,0,1)

1/4 bias ratio and x(3) time 2nd boost for Partial mode 1 and 1/6 bias ratio and x(4) time 2nd boost for Normal, Partial mode 0. BS[3:0]=(0,0,1,1)

5. DC/DC Clock Division
   - Clock division fOSC/8 for normal and partial display mode 0, DV[2:0] = (0,0,0)
   - Clock division fOSC/8 (1/66duty) or fOSC/32 (1/33duty) for partial display mode 1, DV[5:3] = (0,0,0)
6. All booster circuits and AMP circuit OFF, AMP=BT3=BT2=BT1=0
7. Temperature coefficient is -0.05%/°C, TC[1:0]=(0,1)
8. Contrast Control C1[7:0]=C2[7:0]=(0,0,0,0,0,0,0,0)
9. Standby Mode ON, STB=1
10. Addressing Mode
    - One extra dummy subgroup is none, DSG=1
    - Subgroup frame inversion ON, SGF=1
    - Subgroup is different phase by one pixel unit, SGP=1
11. Row vector increase by every subframe, INC=1
12. Frame inversion for AC driving, FIM=1 and NB[4:0]=(0,1,1,0,1)
13. Normal Frame Rate, LFS=0
14. Frame Frequency (1/132, 1/66, 1/33duty)=100Hz, FR[3:0]=(0,1,1,1)
15. Entry Mode
    - 8-bit parallel data bus mode, 16B=0
    - Memory data inversion OFF, MDI=0
    - Column/Row address count increment, MX=MY=0
    - Column address count first, Y/X=0
    - Read modify write mode OFF, RMW=0
16. Start row address YS[7:0]=(0,0,0,0,0,0,0,0), End row address YE[7:0]=(1,0,0,0,0,0,1,1)
17. Start column address XS[7:0]=(0,0,0,0,0,0,0,0), End column address XE[7:0]=(1,0,0,0,0,0,1,1)
18. LCD display OFF, DOF=0
19. Normal display pattern, DP[1:0]=(0,0)
20. Partial Display
    - Partial display mode OFF (Normal mode), PT=PDM=PDY=0
    - Partial display start line PS[7:0]=(0,0,0,0,0,0,0,0)
    - Partial display end line PE[7:0]=(0,0,0,0,0,0,0,0)
21. Area Scroll
    - Entire display scroll mode, SM[1:0]=(0,0)
    - Area scroll start line SS[7:0]=(0,0,0,0,0,0,0,0)
    - Area scroll end line SE[7:0]=(1,0,0,0,0,0,1,1)
    - Low fixed line number LF[7:0]=(0,0,0,0,0,0,0,0)
    - Start scroll line SL[7:0]=(0,0,0,0,0,0,0,0)
22. Internal status register is selected for Status Read command, SR[1:0]=(0,0)
23. MTP calibration function is turned ON, MOF=1

Commands

1. Non Operation

This command is non-operation.

D/I	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	0	0	0	0	0	0	0	0	00h

2. Oscillation Mode Set

This command is used to select the internal or external clock. When external clock is selected, the internal system clock is halted and the external system clock can be input from OSCIN pin. The internal oscillator circuit can be enabled or disabled by setting bit OSC. This command is only for internal or external system clock selection used. Do not use this command for LCD display control.

D/I	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	0	0	0	0	0	0	1	0	02h
0	1	0	0	0	0	0	0	0	EXT	OSC	XX

The setting status is as follows:

EXT	OSC	Status	OSC pins
0	0	Internal oscillator OFF	Connect resisters between OSC1, OSC2 and OSC3, OSC4
0	1	Internal oscillator ON	
1	*	External clock mode	System clock input to OSCIN

3. Driver Output Mode Set

This command is for setting the scan direction of COM output allowing flexible ITO layout in LCD module assembly. The display will have an immediate effect once this command is executed, except the SWP function.

D/I	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	0	0	0	1	0	0	0	0	10h
0	1	0	SEQ	0	DL1	DL0	0	0	SWP	CDR	XX

The non-used common outputs are no scanning field and set to VM level.

SEQ	DL[1:0]	Duty Ratio	Scan Line	Common Output Pads	
				CDR = 0	CDR = 1
0	00	1/96	Line 0 ~ 95	COM[0-47], COM[66-113]	COM[113-66], COM[47-0]
	01	1/108	Line 0 ~ 107	COM[0-53], COM[66-119]	COM[119-66], COM[53-0]
	10	1/120	Line 0 ~ 119	COM[0-59], COM[66-125]	COM[125-66], COM[59-0]
	11	1/132	Line 0 ~ 131	COM[0-65], COM[66-131]	COM[131-66], COM[65-0]

SEQ	DL[1:0]	Duty Ratio	Scan Line	Common Output Pads	
				CDR = 0	CDR = 1
1	00	1/96	Line 0~47	COM[0-2], COM[66-68], COM[3-5],COM[69-71], ……., COM[21-23], COM[87-89]	COM[122-120],COM[56-54], COM[119-117],COM[53-51], ……., COM[101-99],COM[35-33]
			Line 48~95	COM[33-35], COM[99-101], COM[36-38],COM[102-104], ……., COM[54-56],COM[120-122]	COM[89-87], COM[23-21], COM[86-84],COM[20-18], ……., COM[68-66], COM[2-0]
	01	1/108	Line 0~53	COM[0-2], COM[66-68], COM[3-5],COM[69-71], ……., COM[24-26], COM[90-92],	COM[125-123],COM[59-57], COM[122-120],COM[56-54], ……., COM[101-99],COM[35-33]
			Line 54~107	COM[33-35],COM[99-101], COM[36-38],COM[102-104], ……., COM[57-59], COM[123-125]	COM[92-90], COM[26-24], COM[89-87],COM[23-21], ……., COM[68-66], COM[2-0],
	10	1/120	Line 0~59	COM[0-2], COM[66-68], COM[3-5],COM[69-71], ……., COM[27-29], COM[93-95]	COM[128-126],COM[62-60], COM[125-124],COM[59-58], ……., COM[101-99],COM[35-33]
			Line 60~119	COM[33-35],COM[99-101], COM[36-38],COM[102-104], ……., COM[60-62], COM[126-128]	COM[95-93], COM[29-27], COM[92-90],COM[26-24], ……., COM[68-66], COM[2-0],
	11	1/132	Line 0~131	COM[0-2], COM[66-68], COM[3-5],COM[69-71], ……., COM[63-65], COM[129-131]	COM[131-129],COM[65-63], COM[128-126],COM[62-60], ……., COM[68-66], COM[2-0]

The SEG output can be swapped as follows:
SWP=0: Normal (SEGAi is D15~D11, SEGBi is D10~D5 and SEGCi is D4~D0)
SWP=1: Reverse (SEGAi is D4~D0, SEGBi is D10~D5 and SEGCi is D15~D11)

4. Monitor Signal Control

This command is used to control the MON output signal for SYNC, PM, CL or FR.

D/I	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	0	0	0	1	1	0	0	0	18h
0	1	0	0	0	SY1	SY0	SYN	PM	CL	FR	XX

The output status is shown as below:

Bit		Monitor Signal Status	Bit		Monitor Signal Status
SYNC	0	SYNC is output VSS level	CL	0	CL is output VSS level
	1	SYNC is operating		1	CL is operating
PM	0	PM is output VSS level	FR	0	FR is output VSS level
	1	PM is operating		1	FR is operating

When SYN=1, the output timing of SYNC is set by SY[1:0] as follows.

SY[1:0]	SYNC signal output timing
00	Head of 1st subframe
01	Head of 2nd subframe
10	Head of 3rd subframe
11	Head of 4th subframe

FR: Polarity indicator signal.

CL: Shift clock signal.

PM: Field delimiter signal.

SYNC: Frame delimiter signal.

Note: The priority of the monitor signal is: FR > CL > PM > SYNC.

5. DC/DC Select

To select the boost times of the 1st booster circuit in normal display mode, partial display mode 0 and partial display mode 1.

D/I	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	0	0	1	0	0	0	0	0	20h
0	1	0	0	0	DC3	DC2	0	0	DC1	DC0	XX

The boost times of 1st internal DC/DC converter circuit are set as follows:

In Partial Display Mode 1		In Normal, Partial Display Mode 0	
DC[3:2]	1st Booster Circuit Set Up	DC[1:0]	1st Booster Circuit Set Up
00	x 1.0	00	x 1.0
01	x 1.5	01	x 1.5
10	x 2.0	10	x 2.0
11	x 2.0	11	x 2.0

6. Bias Set

This command is the LCD driving bias ratio selection in normal display mode, partial display mode 0 and partial display mode 1.

D/I	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	0	0	1	0	0	0	1	0	22h
0	1	0	0	0	BS3	BS2	0	0	BS1	BS0	XX

The boost times of the 2nd booster circuit and output voltage of DC2 are decided when the bias ratio is set.

In Partial Display Mode 1			In Normal, Partial Display Mode 0		
BS[3:2]	Bias	2nd Booster Circuit Set Up	BS[1:0]	Bias	2nd Booster Circuit Set Up
00	1/4	x (3.0)	00	1/4	x (3.0)
01	1/5	x (3.0)	01	1/5	x (3.0)
10	1/5	x (4.0)	10	1/5	x (4.0)
11	1/6	x (4.0)	11	1/6	x (4.0)

7. DC/DC Clock Division Set

To set the internal booster clock frequency to normal display mode, partial display mode 0 and partial display mode 1.

D/I	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	0	0	1	0	0	1	0	0	24h
0	1	0	0	DV5	DV4	DV3	0	DV2	DV1	DV0	XX

The booster clock frequency is set as follows:

In Partial Display Mode 1		In Normal, Partial Display Mode 0	
DV[5:3]	Booster Clock Frequency	DV[2:0]	Booster Clock Frequency
	1/66, 1/33duty		1/132, 1/120, 1/108, 1/96duty
000	fOSC/8	000	fOSC/8
001	fOSC/16	001	fOSC/16
010	fOSC/32	010	fOSC/32
011	fOSC/64	011	fOSC/64
100	fOSC	100	fOSC
101	fOSC/2	101	fOSC/2
110	fOSC/4	110	fOSC/4
111	fOSC/8	111	fOSC/8

Note: 1. fOSC = (Duty/3 + Dummy) x 4 x 8 x frame frequency.
2. The suitable frequency of the boost clock is in a range from 5kHz to 16kHz.

8. DC/DC and AMP ON/OFF Set

This command is to turn ON or OFF the internal OP-AMP and booster circuits.

D/I	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	0	0	1	0	0	1	1	0	26h
0	1	0	0	0	0	0	AMP	BT3	BT2	BT1	XX

The setting status is shown as below:

Bit		Internal Power Circuit Status	Bit		Internal Power Circuit Status
AMP	0	Internal OP-AMP OFF	BT2	0	2nd booster circuit OFF
	1	Internal OP-AMP ON		1	2nd booster circuit ON
BT1	0	1st booster circuit OFF	BT3	0	3rd booster circuit OFF
	1	1st booster circuit ON		1	3rd booster circuit ON

9. Temperature Compensation Set

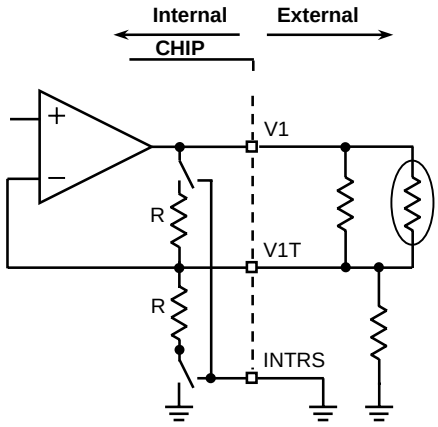
This command can select the average temperature compensation coefficients.

D/I	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	0	0	1	0	1	0	0	0	28h
0	1	0	0	0	0	0	0	0	TCS1	TCS0	XX

The four sets of temperature compensation coefficients can be selected as follows:

TCS[1:0]	Temperature Compensation Coefficient (at 25°C)
00	-0.00%/°C
01	-0.05%/°C
10	-0.10%/°C
11	-0.15%/°C

If external temperature compensation is needed, two resistors and one thermistor are connected as in the following circuit:



10. Contrast Control (1) and Contrast Control (2)

The command Contrast Control (1) is to set the contrast value C1[7:0] in normal display mode and partial display mode 0.

D/I	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	0	0	1	0	1	0	1	0	2Ah
0	1	0	C17	C16	C15	C14	C13	C12	C11	C10	XX

The command Contrast Control (2) is to set the contrast value C2[7:0] in partial display mode 1.

D/I	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	0	0	1	0	1	0	1	1	2Bh
0	1	0	C27	C26	C25	C24	C23	C22	C21	C20	XX

Both commands adjust V1 voltage from 2.0V to 3.3V, so the contrast resolution is 5.098mV in one step value.

11. Standby Mode ON/OFF Set

This command is used to set the IC to enter or exit the standby mode. When STB is high, the IC enters the standby mode to save the power consumption as in the following status:

(1) All LCD driver outputs (common and segment): VSS level
(2) Internal LCD driving power outputs (VRP, V1, VM and VRN): VSS level
(3) Internal booster circuits (1^{st}, 2^{nd} and 3^{rd} booster): OFF
(4) Oscillator circuit: OFF
(5) The content of DDRAM is not cleared and the data can be written through the MPU interface.

Set standby mode off and display on commands for returning to the normal operation status.

D/I	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	0	0	1	0	1	1	0	STB	2Ch 2Dh

12. Addressing Mode Set

This command is for setting the duty adjusts DSG, subgroup frame inversion mode SGF and subgroup phase mode SGP.

D/I	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	0	0	1	1	0	0	0	0	30h
0	1	0	0	0	0	DSG	SGF	0	SGP	0	XX

The setting function is shown as below:

Bit		Subgroup Function Status
DSG	0	Dummy subgroup is one subgroup
	1	Dummy subgroup is none
SGF	0	Subgroup frame inversion OFF
	1	Subgroup frame inversion ON

Bit		Subgroup Function Status
SGP	0	Same phase in all pixel
	1	Different phase by 1 pixel unit

13. Row Vector Mode Set

This command is to set the row vector update method.

D/I	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	0	0	1	1	0	0	1	0	32h
0	1	0	0	0	0	0	0	0	INC	0	XX

The row vector sequence is R1→R2→R3→R4→R1→… and updated as follows by setting INC.

Bit		Row Vector Update
INC	0	Every subgroup
	1	Every subframe

14. N-block Inversion Set

This command is for setting the N-block inversion for liquid crystal polarity alternation.

D/I	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	0	0	1	1	0	1	0	0	34h
0	1	0	FIM	0	0	NB4	NB3	NB2	NB1	NB0	XX

All the driver outputs will have polarity inversion as in the following setting:

FIM	NB[4:0]	Polarity Inversion Period	FIM	NB[4:0]	Polarity Inversion Period
0	00000	Frame Inversion	1	00000	Frame Inversion
0	00001	Every 1 block	1	00001	Every 1 block and every frame
0	:	:	1	:	:
0	11111	Every 31 block	1	11111	Every 31 block and every frame

15. Frame Frequency Set

This command can be set to low frame frequency for low power consumption. When the low frame rate is on (LFS is high), the frame frequency is set to 1/2x(normal frame frequency).

D/I	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	0	0	1	1	0	1	1	0	36h
0	1	0	FR[3:0]				0	0	0	LFS	XX

Note: fFR @(LFS=1) = fFR @(LFS=0) / 2

FR3	FR2	FR1	FR0	Oscillator (KHz)	Frame Rate (Hz)			
					1/132 duty	1/120 duty	1/108 duty	1/96 duty
0	0	0	0	91.52	65	71.5	79.444	89.375
0	0	0	1	98.56	70	77	85.556	96.25
0	0	1	0	105.6	75	82.5	91.667	103.125
0	0	1	1	112.64	80	88	97.778	110
0	1	0	0	119.68	85	93.5	103.889	116.875
0	1	0	1	126.72	90	99	110	123.75
0	1	1	0	133.76	95	104.5	116.111	130.625
0	1	1	1	140.8	100	110	122.222	137.5
1	0	0	0	147.84	105	115.5	128.333	144.375
1	0	0	1	154.88	110	121	134.444	151.25
1	0	1	0	161.92	115	126.5	140.556	158.125
1	0	1	1	168.96	120	132	146.667	165
1	1	0	0	176	125	137.5	152.778	171.875
1	1	0	1	183.04	130	143	158.889	178.75
1	1	1	0	190.08	135	148.5	165	185.625
1	1	1	1	197.12	140	154	171.111	192.5

16. Entry Mode Set

Setting the internal function mode.

D/I	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	0	1	0	0	0	0	0	0	40h
0	1	0	16B	0	0	MDI	MX	MY	Y/X	RMW	XX

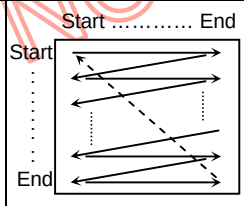
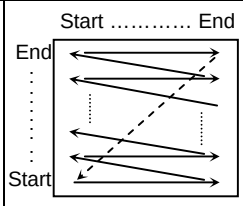
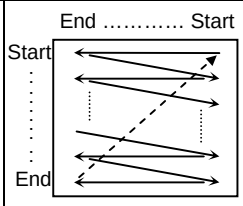
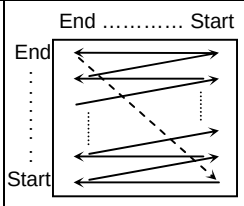
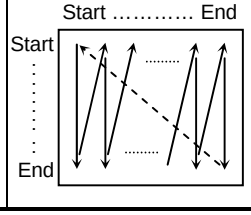
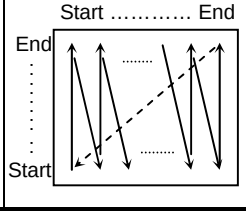
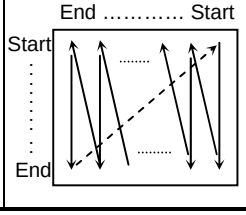
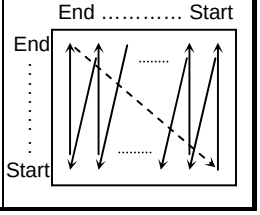
The MDI is the memory data inversion setting for low power consumption.

	MDI = 0		MDI = 1	
	Display Data Write	Display Data Read	Display Data Write	Display Data Read
Data Bus	00h	00h	00h	FFh
	↓	↑	↓	↑
Memory	00h	00h	FFh	00h

When entering the read modify write mode (RMW is high), the row/column address of DDRAM is not incremented in reading display data but is in writing display data.

Bit		Function Status	Bit		Function Status
16B	0	8-bit parallel data bus	MX	0	Column address increment
	1	16-bit parallel data bus		1	Column address decrement
MDI	0	Memory data inversion OFF	MY	0	Row address increment
	1	Memory data inversion ON		1	Row address decrement
RMW	0	Read modify write OFF	Y/X	0	Column address count first
	1	Read modify write ON		1	Row address count first

The directions of display data stored into DDRAM are shown as follows:

Display Data Direction	MX = 0, MY = 0 (Normal)	MX = 0, MY = 1 (Y-Mirror)	MX = 1, MY = 0 (X-Mirror)	MX = 1, MY = 1 (X-Mirror, Y-Mirror)
Y/X = 0 (Normal)				
Y/X = 1 (X-Y Exchange)				

17. Row Address Area Set

This command specifies the row address of DDRAM used to set a read/write area. In row address count mode (Y/X is high), the row address is incremented from the start address YS[7:0] to end address YE[7:0]. When the row address is equal to YE[7:0], the column address is automatically increased by 1 and the row address returns to the start address. Set the start address and the end address at the same time and the start address must be smaller than the end address.

D/I	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	0	1	0	0	0	0	1	0	42h
0	1	0	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	XX
0	1	0	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	XX

18. Column Address Area Set

This command specifies the column address of DDRAM used to set a read/write area. In column address count mode (Y/X is low), the column address is incremented from the start address XS[7:0] to end address XE[7:0]. When the column address is equal to XE[7:0], the row address is automatically increased by 1 and the column address returns to the start address. Set the start address and the end address at the same time and the start address must be smaller than the end address.

D/I	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	0	1	0	0	0	0	1	1	43h
0	1	0	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	XX
0	1	0	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	XX

19. Display ON/OFF Control

This command is for turning the LCD display ON or OFF. When the display is off (DOF is low), all the common and segment outputs are set to VSS level and the internal booster circuits still operate.

D/I	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	0	1	0	1	0	0	0	DOF	50h 51h

20. Specified Display Pattern Set

This command sets the specified display patterns regardless of DDRAM data.

D/I	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	0	1	0	1	0	0	1	1	53h
0	1	0	0	0	0	0	0	0	DP1	DP0	XX

DP[1:0]	Display Pattern	DP[1:0]	Display Pattern
00	Normal Display	10	All Display OFF
01	Reverse Display	11	All Display ON

21. Partial Display Mode Set

This command enables to select the display mode. The IC enters into partial display when PT is high, then PDM and PDY decide the different partial display mode and different display duty shown as follows. This command does not change the contents of DDRAM.

D/I	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	0	1	0	1	0	1	0	1	55h
0	1	0	0	0	0	0	0	PDY	PDM	PT	XX

PT	PDM	PDY	Display Mode	Display Duty Ratio	Oscillator
0	*	*	Normal Mode	Depend on DL[1:0] (refer to “Driver Output Mode Set”)	OSC
1	0	*	Partial Mode 0		
1	1	0	Partial Mode 1	1/66	OSC/2
1	1	1		1/33	OSC/4

22. Partial Display Start Line Set and Partial Display End Line Set

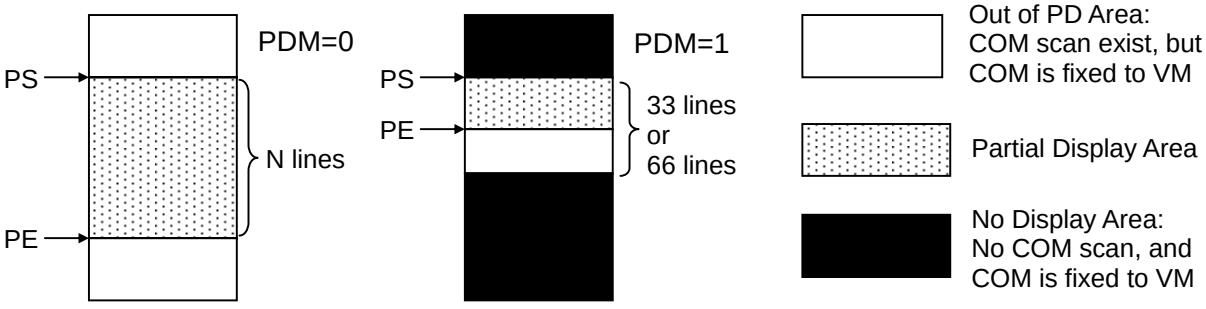
These two commands set the display area from the start common line PS[7:0] to the end common line PE[7:0] at the time of partial display. Set the start line and the end line at the same time so that the common start must be smaller than the common end. The PS[7:0] and PE[7:0] are specified as the scan line number of common output, not DDRAM row address.

D/I	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	0	1	0	1	0	1	1	0	56h
0	1	0	PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0	XX

D/I	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	0	1	0	1	0	1	1	1	57h
0	1	0	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0	XX

Note:

1. Partial Display Start Line PS[7:0] ≤ Partial Display End Line PE[7:0] ≤ Duty Ratio - 1.
2. Partial Display End Line PE[7:0] - Partial Display Start Line PS[7:0] ≤ Duty Ratio - 1.
3. When PDM=1, PS[7:0] should be 3n. If you don’t set PS[7:0]=3n and PE[7:0] - PS[7:0] > 33 or 66 (depend on PDY), you will get less than 33 or 66 display lines.



Partial Display Mode 0 (PDM=0)
On scanning except partial display area
- SEG output V0 or V1 levels depend on FR value and all of COM output is fixed to VM level.

On scanning partial display area
- It is equal to the normal mode

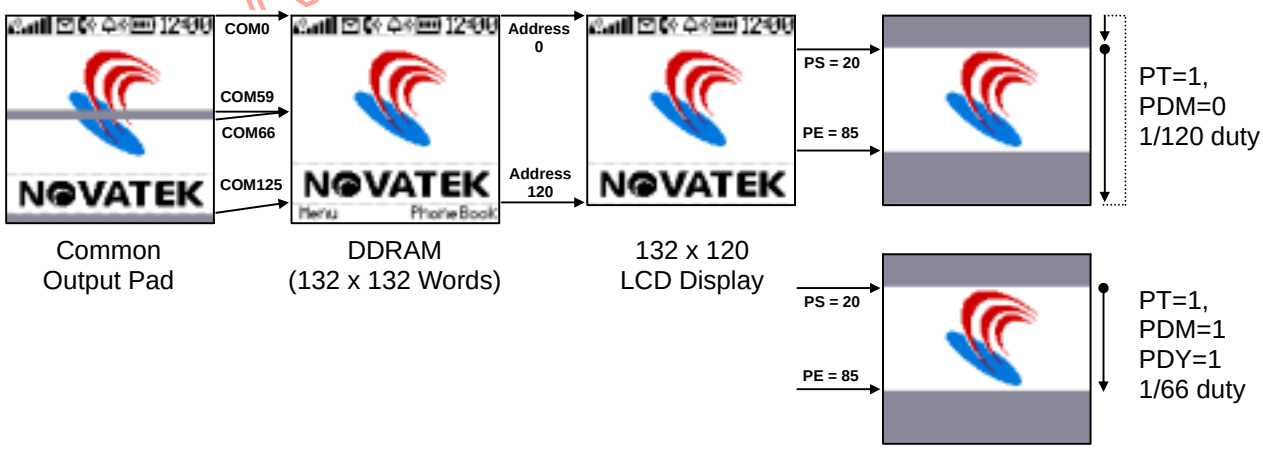
Item	Partial Display Area	Out of Partial Display Area
COM Output level	VCC, VEE or VM	VM
SEG Output level	Normal Display	V1 or V0 depends on FR
Duty Ratio	Depends on Driver Output Mode Set DL[1:0] (1/96, 1/108, 1/120 or 1/132)	
Contrast Control	Contrast Control (1)	
Bias	Depends on Bias Set BS[1:0]	
Oscillator	OSC1 and OSC2 for internal oscillator, OSCIN for external oscillator	

Partial Display Mode 1 (PDM=1)
Display area is from partial start line (PS) to partial end line (PE) and only max. 66-line (PDY=0) or 33-lines (PDY=1) output COM signal.
On scanning except partial display area
- SEG output V0 or V1 levels depend on FR value and all of COM output is fixed VM level.

On scanning partial display area
- It is equal to 33-line or 66-line output.

Item	Partial Display Area	Out of Partial Display Area	Out of Display Area
COM Output level	VCC, VEE or VM	VM (with scan field)	VM (without scan field)
SEG Output level	Normal Display	V1 or V0 depends on FR	-
Duty Ratio	Depends on Partial Display Mode Set PDY (1/66, 1/33)		
Contrast Control	Contrast Control (2)		
Bias	Depends on Bias Set BS[3:2]		
Oscillator	OSC3 and OSC4 for internal oscillator, OSCIN for external oscillator		

Example: 132x120 LCD display (DL[1:0]=10, 1/120 duty), PS[7:0]=14h, PE[7:0]=55h



23. Area Scroll Set

This command specifies the portion of the screen for scrolling. The command sets the scroll area start line SS[7:0], scroll area end line SE[7:0], specific lower fixed number LF[7:0] and the area scroll mode SM[1:0] of the area scrolling.

D/I	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	0	1	0	1	1	0	0	1	59h
0	1	0	0	0	0	0	0	0	SM1	SM0	XX
0	1	0	SS7	SS6	SS5	SS4	SS3	SS2	SS1	SS0	XX
0	1	0	SE7	SE6	SE5	SE4	SE3	SE2	SE1	SE0	XX
0	1	0	LF7	LF6	LF5	LF4	LF3	LF2	LF1	LF0	XX

The set area scroll function is divided into four parts.

Part I – Specify the number of top fixed area lines = scroll area start line SS[7:0]. If in the upper screen scroll or the entire screen scroll mode, specify the 0_{th} line for the top fixed area address.

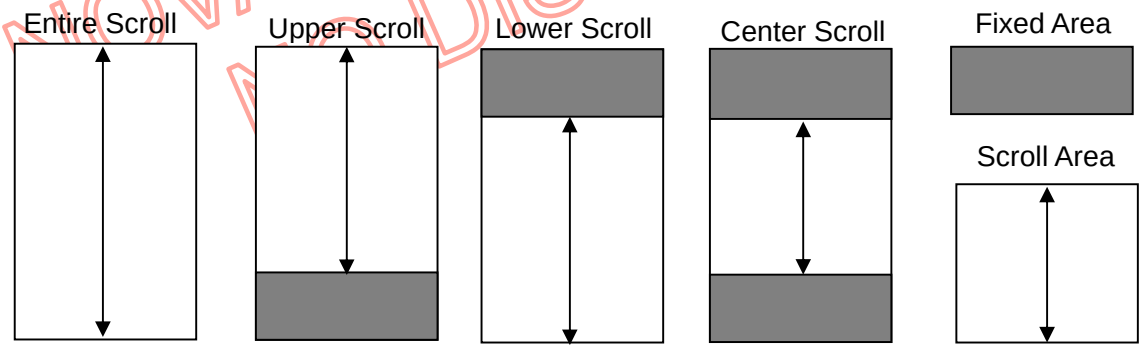
Part II – Specify number of scroll display area lines = scroll area end line SE[7:0].

Part III – Specify the number of bottom fixed area lines = display line number DL[1:0] – lower fixed number LF[7:0] - 1. If in the lower screen scroll or the entire screen scroll mode, specify the 0 line for the lower fixed number. When the lower scroll or entire screen scroll is chosen, the resulted value is identical to the value = 0.

Part IV – Specify the area scroll mode. There are four types of area scroll modes.

The area scroll function is executed by the prompt in the set area scroll command followed by changing the scroll start line address by the "Scroll Start Line Set" command.

SM[1:0]	Area Scroll Mode	SM[1:0]	Area Scroll Mode
0,0	Entire Scroll Mode	1,0	Lower Scroll Mode
0,1	Upper Scroll Mode	1,1	Center Scroll Mode



Note:

1. The scroll area start line SS[7:0] must be smaller than the scroll area end address SE[7:0].
2. In lower and center scroll mode, scroll area end line SE[7:0) must be smaller than duty ratio subtract low fixed number LF[7:0].

Example: In the Center screen scroll with the partial display mode 0.

(1) Area Scroll Set command: 59h.

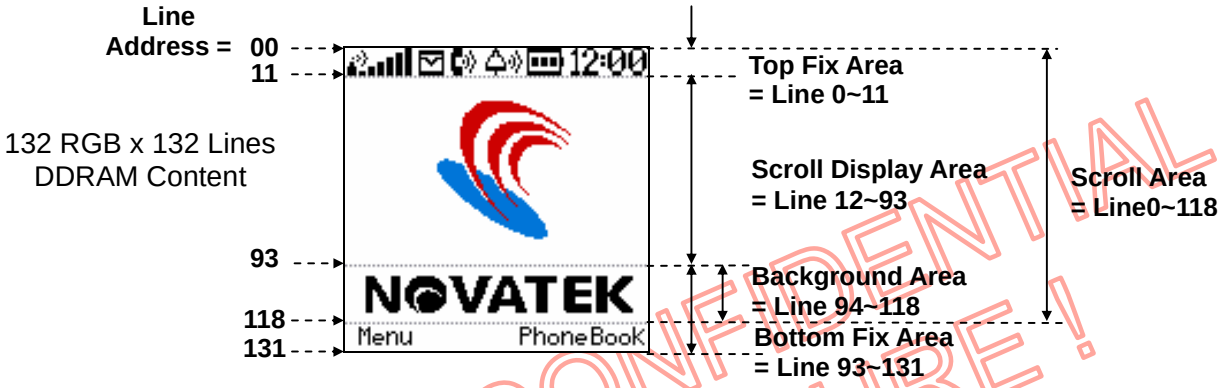
(2) Set Area Scroll Mode is center screen scroll mode, SM[1:0] = 03h.

(3) 0^{th} ~ 11^{th} line (12 lines) are specified for the number of top fixed area line.
Scroll area start line SS[7:0] = 0Ch.

(4) 0^{th} ~ 118^{th} line (119 lines) are specified the number of scroll area line.
Scroll area end line SE[7:0] = 76h (118).

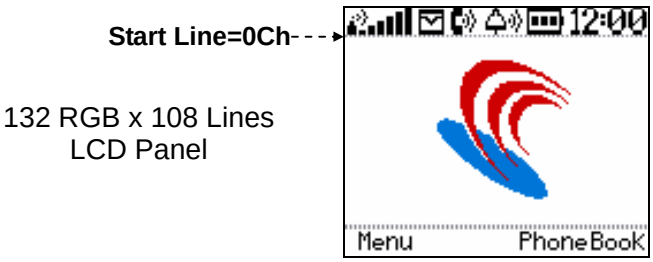
(5) 93^{rd} ~ 131^{st} line (38 lines) are specified for the number of bottom fixed area line.
LF[7:0] = 25h (131 - 93 – 1 = 37).

(6) 94^{th} ~ 118^{th} line (25 lines) are specified the background areas.



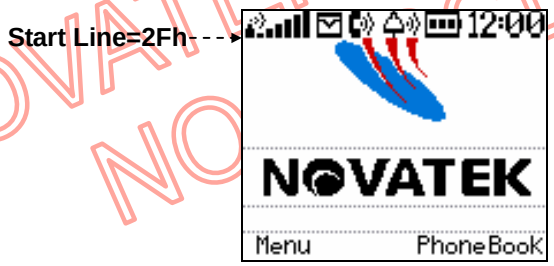
(7) Start Scroll Line Set command: 5Ah.
- Set Start Scroll Line Address, SL[7:0] data = 0Ch.

(8) Partial Display Mode Set command: 55h and 01h.
Partial Display Start Line Set command: 56h.
- Set Partial Display Start Line PS[7:0] = 00h.
Partial Display End Line Set command: 57h.
- Set Partial Display End Line PE[7:0] = 6Bh (107).

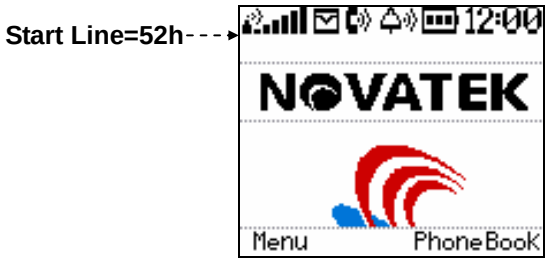


(9) Start Scroll Line Set command: 5Ah.
- Set Start Scroll Line Address, SL[7:0] data = 16h.

(10) Start Scroll Line Set command: 5Ah.
- Set Start Scroll Line Address, SL[7:0] data = 2Fh.

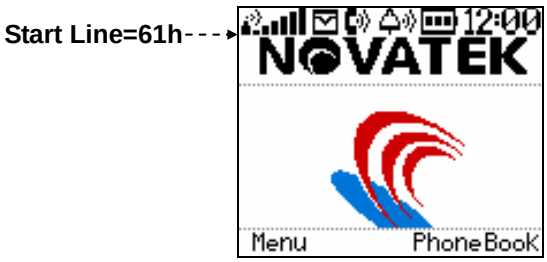


(11) Start Scroll Line Set command: 5Ah.
- Set Start Scroll Line Address, SL[7:0] data = 52h.



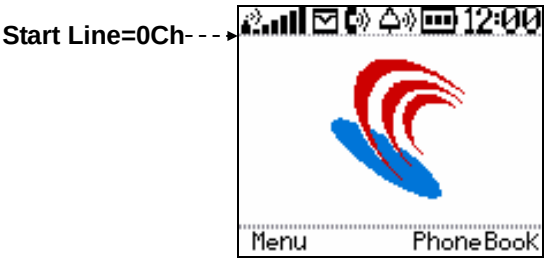
(12) Start Scroll Line Set command: 5Ah.

- Set Start Scroll Line Address, SL[7:0] data = 61h.



(13) Start Scroll Line Set command: 5Ah.

- Set Start Scroll Line Address, SL[7:0] data = 0Ch.



24. Scroll Start Line Set

This command specifies the scroll starting line address SL[7:0] of the area scrolling then executes the area scroll by changing the start line address dynamically after the Scroll Start Line Set command is executed.

D/I	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	0	1	0	1	1	0	1	0	5Ah
0	1	0	SL7	SL6	SL5	SL4	SL3	SL2	SL1	SL0	XX

Note:

1. Scroll Area Start Line SS[7:0] ≤ Start Scroll Address SL[7:0] ≤ Scroll Area End Line SE[7:0].
2. DLN - LFN < SS[7:0]
3. DLN = 132, 120, 108, 96, 66, or 33.

25. CR Volume Up/Down

This command to count the register value of contrast control (1) or (2) up/down.
CUD = 0, contrast control (1) or (2) depending on display mode at present is increased by 1.
If register value is FFh, then register value becomes 00h after issuing this command.
CUD = 1, contrast control (1) or (2) depending on display mode at present is decreased by 1
If the register value is 00h, then the register value becomes FFh after issuing this command.

D/I	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	0	1	1	1	0	0	0	CUD	70h 71h

26. Status Read Mode Set and Status Read

The Status Read Mode Set command is used to select status content for reading.

D/I	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	0	1	1	1	1	1	1	1	7Fh
0	1	0	0	0	0	0	0	0	SR1	SR0	XX

SR[1:0]	Status Read
00	Status
01	Contrast Control (1), C1[7:0]
10	Contrast Control (2), C2[7:0]
11	Reversed

The Status Read command read out the following status on D7 to D0 according to SR[1:0].

D/I	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	0	1	PM2	PM1	Y/X	PDM	PT	STB	REV	DOF	XX
0	0	1	C17	C16	C15	C14	C13	C12	C11	C10	XX
0	0	1	C27	C26	C25	C24	C23	C22	C21	C20	XX

Bit		Internal Status	Bit		Internal Status
PM2	0	MTP 2 is not programmed	PT	0	Partial display mode OFF status
	1	MTP 2 is programmed		1	Partial display mode ON status
PM1	0	MTP 1 is not programmed	STB	0	Standby mode OFF status
	1	MTP 1 is programmed		1	Standby mode ON status
Y/X	0	Column address count mode	REV	0	Display image non-reversing
	1	Row address count mode		1	Display image reversing
PDM	0	In Partial display mode 0	DOF	0	Display OFF status
	1	In Partial display mode 1		1	Display ON status

27. Display Data Write

This command is for writing display data in display data RAM. When this command is executed, the row address and column address turn into the start address. After the display data byte WD[15:0] is written to DDRAM, the row address or column address is increased by 1 depending on Y/X bit is high or low that set by Entry Mode command. Input any other command to get out of the status set by this command.

D/I	RDB	WRB	D15	D14	D13	……	D2	D1	D0	Hex
1	1	0	WD15	WD14	WD13	……	WD2	WD1	WD0	XX
1	1	0	:	:	:	……	:	:	:	:

28. Read Display Data

This command is for reading display data from display data RAM. When this command is executed, the read status becomes available and the row address and column address are set to the start address. After the content of DDRAM is read to register RD[15:0], the row address or column address is increased by 1 depending on Y/X bit is high or low that is set by Entry Model command. Input any other command to get out of status set by this command.

D/I	RDB	WRB	D15	D14	D13	……	D2	D1	D0	Hex
1	0	1	RD15	RD14	RD13	……	RD2	RD1	RD0	XX
1	0	1	:	:	:	……	:	:	:	:

Note: In 8-bit mode, you should read or write twice (two bytes) and address counter will be increased by 1.

29. MTP Calibration ON/OFF Control

This command is for turning the MTP Calibration ON or OFF. When MTP Calibration is OFF (MOF is low), the function will be disabled. After reset operation, MTP Calibration is ON (MOF is high).

D/I	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	1	1	0	1	0	1	MOF	EAh EBh

30. Multi-Time Calibration Set

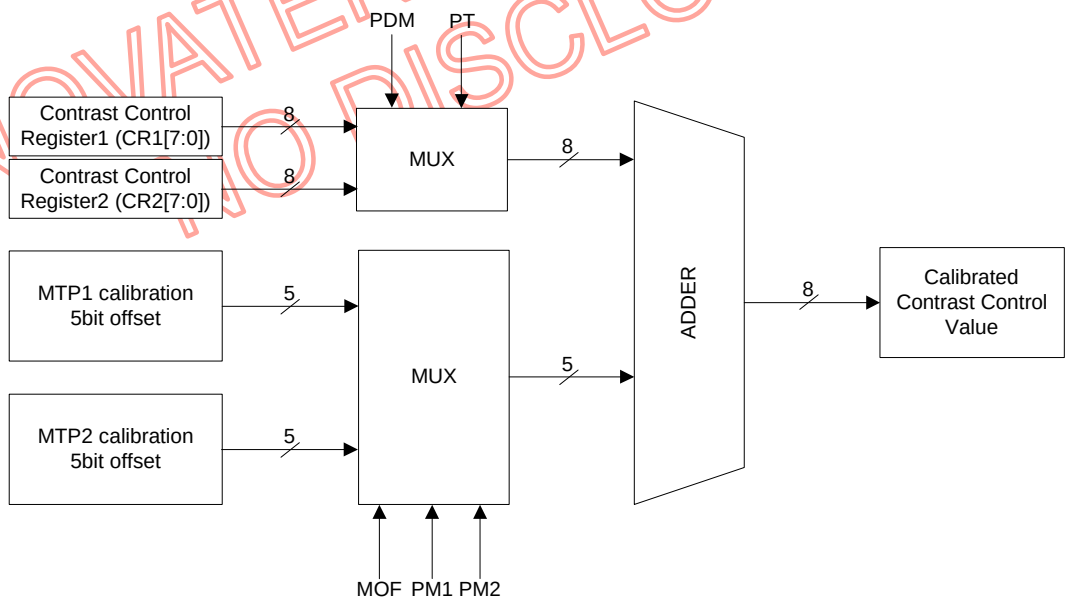
D/I	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	0	1	1	1	1	0	1	1	0	1	EDh
0	0	1	0	0	0	MT4	MT3	MT2	MT1	MT0	XX

The Setting of the offset value of contrast

MT[4:0]	Offset Value	MT[4:0]	Offset Value	MT[4:0]	Offset Value	MT[4:0]	Offset Value
00000	Original	01000	+16 step	10000	Original	11000	-16 step
00001	+2 step	01001	+18 step	10001	-2 step	11001	-18 step
00010	+4 step	01010	+20 step	10010	-4 step	11010	-20 step
00011	+6 step	01011	+22 step	10011	-6 step	11011	-22 step
00100	+8 step	01100	+24 step	10100	-8 step	11100	-24 step
00101	+10 step	01101	+26 step	10101	-10 step	11101	-26 step
00110	+12 step	01110	+28 step	10110	-12 step	11110	-28 step
00111	+14 step	01111	+30 step	10111	-14 step	11111	-30 step

31. Multi-Time Programming Set

D/I	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	0	1	1	1	1	0	1	1	1	1	EFh



This contrast adjustment function should include the following two steps:

(1) Find the offset value

1) Set hardware reset and send the original initialization settings to display properly (fix a specified electronic volume)
2) Read Status bit PM1 and PM2 (refer to Status Read Mode Set and Status Read command), and check had MTP1 and MTP2 programmed. If PM1 and PM2 = 1, it means that you can't do the MTP procedure anymore.
3) Set golden test patterns to judge the contrast is best or not by vision
4) Adjust the electronic volume value by Multi-Time Calibration Set command (MT[4:0]), until there is the best visual contrast.

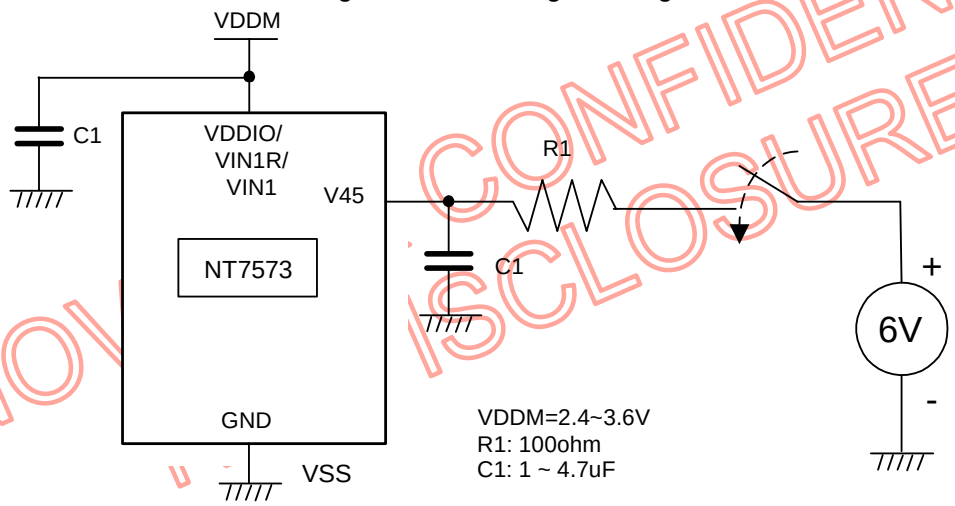
(2) Programming the offset value

5) Set Display OFF (0x50) and Set DC/DC and AMP ON/OFF Set command (0x26) to 01h (1st Pump ON only)
6) Connect an external voltage about 6V to V45 pin.
7) Execute the Multi-Time Program command.
8) Wait at lease 2 seconds and remove the high voltage from V45 pin

(3) Check the display contrast

9) Set DC/DC and AMP ON/OFF Set command to FFh and Set Display ON
10) Check the contrast is the same with golden LCM sample by vision immediately.

Figure 6. MTP Programming Circuit



Note:

1. R1 is current limitation resister.

32. Test Mode

These commands (F9h to FBh and FDh to FFh) are for IC tests only. If executed, it has to be reset.

D/I	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	1	1	1	*	*	*	*	XX

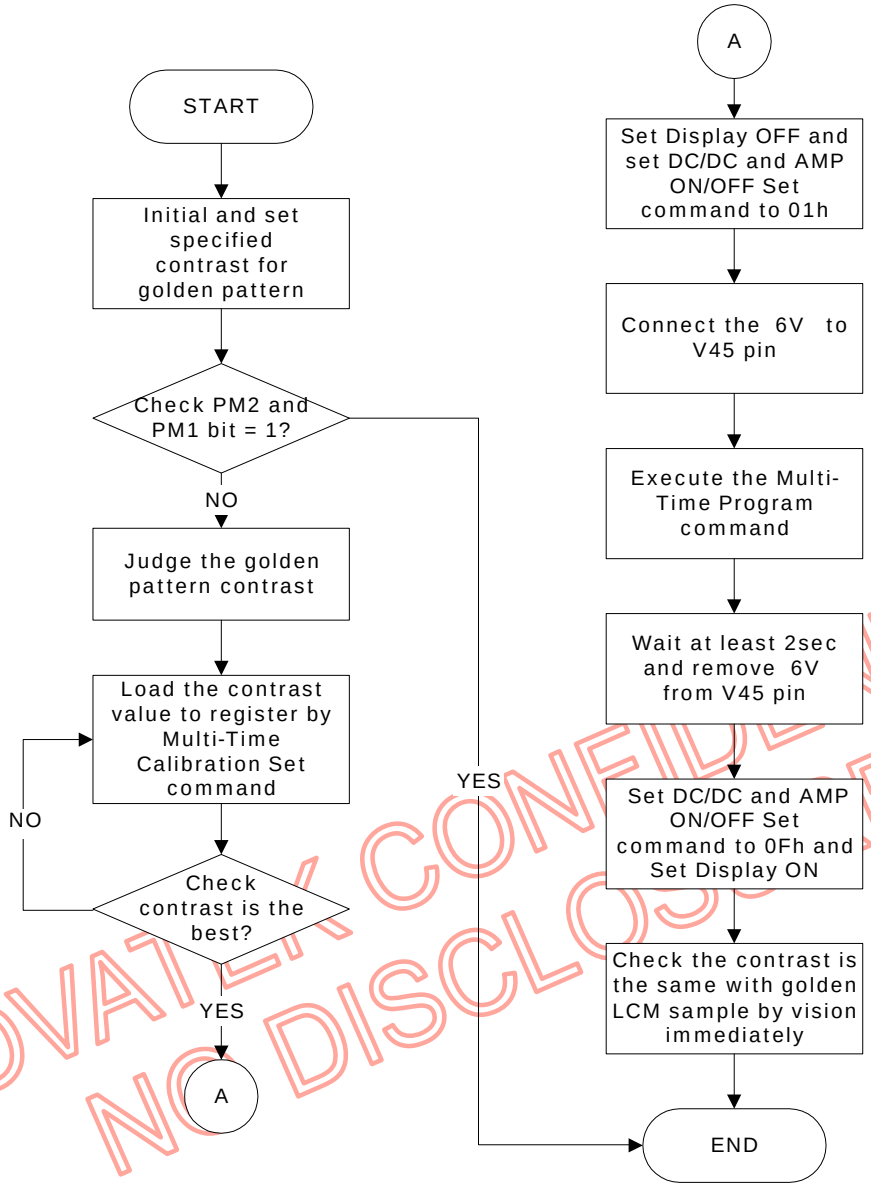


Table 3. Command Table

Command	D/I	RDB	WRB	Code										Function
				D15 ~ D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	
(1) Non Operation	0	1	0	*	0	0	0	0	0	0	0	0	00h	Non operation
(2) Oscillation Mode Set	0	1	0	*	0	0	0	0	0	0	1	0	02h	Set oscillator mode
	0	1	0	*	0	0	0	0	0	0	EXT	OSC	-	
(3) Driver Output Mode Set	0	1	0	*	0	0	0	1	0	0	0	0	10h	Set the display direction
	0	1	0	*	SEQ	0	DL1	DL0	0	0	SWP	CDR	-	
(4) Monitor Signal Control	0	1	0	*	0	0	0	1	1	0	0	0	18h	Timing signal monitor control
	0	1	0	*	0	0	SY1	SY0	SYNC	PM	CL	FR	-	
(5) DC/DC Select	0	1	0	*	0	0	1	0	0	0	0	0	20h	Select boosting times of 1st booster circuit
	0	1	0	*	0	0	DC3	DC2	0	0	DC1	DC0	-	
(6) Bias Set	0	1	0	*	0	0	1	0	0	0	1	0	22h	Set LCD bias ratio
	0	1	0	*	0	0	BS3	BS2	0	0	BS1	BS0	-	
(7) DC/DC Clock Division Set	0	1	0	*	0	0	1	0	0	1	0	0	24h	Set internal booster clock frequency
	0	1	0	*	0	DV5	DV4	DV3	0	DV2	DV1	DV0	-	
(8) DC/DC and AMP ON/OFF Set	0	1	0	*	0	0	1	0	0	1	1	0	26h	DC/DC converter and AMP ON/OFF set up
	0	1	0	*	0	0	0	0	AMP	BT3	BT2	BT1	-	
(9) Temperature Compensation Set	0	1	0	*	0	0	1	0	1	0	0	0	28h	Set driving voltage slope for temperature compensation
	0	1	0	*	0	0	0	0	0	0	TC1	TC0	-	
(10)Contrast Control(1)	0	1	0	*	0	0	1	0	1	0	1	0	2Ah	Set V1 output voltage for normal and partial display mode 0
	0	1	0	*	C17	C16	C15	C14	C13	C12	C11	C10	-	
(11)Contrast Control(2)	0	1	0	*	0	0	1	0	1	0	1	1	2Bh	Set V1 output voltage for partial display mode 1
	0	1	0	*	C27	C26	C25	C24	C23	C22	C21	C20	-	
(12)Standby Mode ON/OFF Set	0	1	0	*	0	0	1	0	1	1	0	STB	2Ch 2Dh	Release/Enter the standby mode
(13)Addressing Mode Set	0	1	0	*	0	0	1	1	0	0	0	0	30h	Set the DDRAM addressing mode
	0	1	0	*	0	0	0	DSG	SGF	0	SGP	0	-	
(14)Row Vector Mode Set	0	1	0	*	0	0	1	1	0	0	1	0	32h	Set row vector function
	0	1	0	*	0	0	0	0	0	0	INC	0	-	
(15)N-block Inversion Set	0	1	0	*	0	0	1	1	0	1	0	0	34h	Set N-block inversion for LCD AC driving
	0	1	0	*	FIM	0	0	NB4	NB3	NB2	NB1	NB0	-	
(16)Frame Frequency Set	0	1	0	*	0	0	1	1	0	1	1	0	36h	Set frame frequency
	0	1	0	*	FR3	FR2	FR1	FR0	0	0	0	LFS	-	
(17)Entry Mode Set	0	1	0	*	0	1	0	0	0	0	0	0	40h	Set internal function
	0	1	0	*	16B	0	0	MDI	MX	MY	Y/X	RMW	-	
(18)Row Address Area Set	0	1	0	*	0	1	0	0	0	0	1	0	42h	Set row address area of DDRAM
	0	1	0	*	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	-	
	0	1	0	*	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	-	
(19)Column Address Area Set	0	1	0	*	0	1	0	0	0	0	1	1	43h	Set column address area of DDRAM
	0	1	0	*	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	-	
	0	1	0	*	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	-	
(20)Display ON/OFF Control	0	1	0	*	0	1	0	1	0	0	0	DOF	50h 51h	Turn the display off/on
(21)Specified Display Pattern Set	0	1	0	*	0	1	0	1	0	0	1	1	53h	Set the display pattern status
	0	1	0	*	0	0	0	0	0	0	DP1	DP0	-	

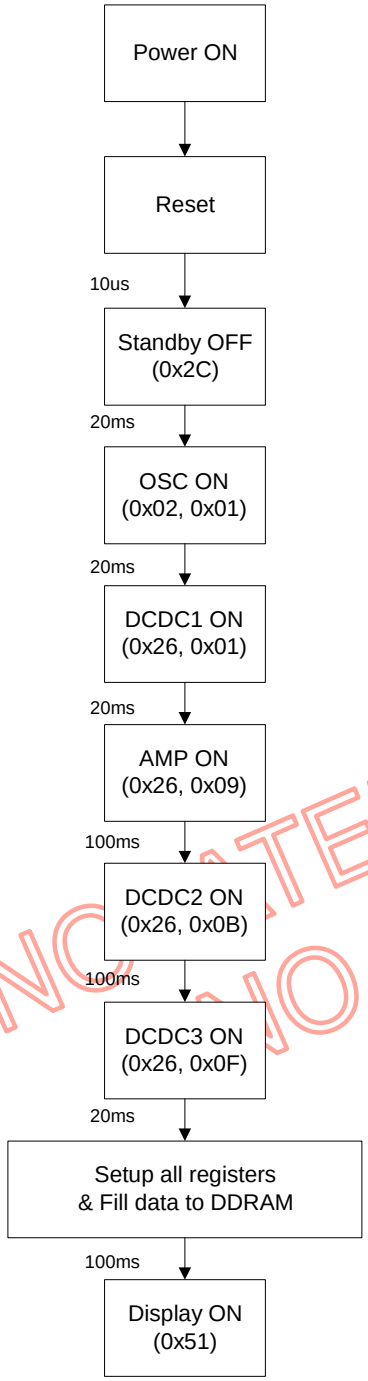
Table 4. Command Table (continued)

Command	D/I	RDB	WRB	Code										Function
				D15 ~ D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	
(22)Partial Display Mode Set	0	1	0	*	0	1	0	1	0	1	0	1	55h	Set partial display mode
	0	1	0	*	0	0	0	0	0	PDY	PDM	PT	-	
(23)Partial Display Start Line Set	0	1	0	*	0	1	0	1	0	1	1	0	56h	Set start line for partial display area
	0	1	0	*	PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0	-	
(24)Partial Display End Line Set	0	1	0	*	0	1	0	1	0	1	1	1	57h	Set end line for partial display area
	0	1	0	*	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0	-	
(25)Area Scroll Set	0	1	0	*	0	1	0	1	1	0	0	1	59h	Set area scroll field
	0	1	0	*	0	0	0	0	0	0	SM1	SM0	-	
	0	1	0	*	SS7	SS6	SS5	SS4	SS3	SS2	SS1	SS0	-	
	0	1	0	*	SE7	SE6	SE5	SE4	SE3	SE2	SE1	SE0	-	
	0	1	0	*	LF7	LF6	LF5	LF4	LF3	LF2	LF1	LF0	-	
(26)Scroll Start Line Set	0	1	0	*	0	1	0	1	1	0	1	0	5Ah	Set the start scroll line
	0	1	0	*	SL7	SL6	SL5	SL4	SL3	SL2	SL1	SL0	-	
(27)CR Volume Up/Down	0	1	0	*	0	1	1	1	0	0	0	CUD	70h 71h	Count up/down the value of contrast control (1) or (2)
(28)Status Read Mode Set	0	1	0	*	0	1	1	1	1	1	1	1	7Fh	Select the content that read by command "Read Status
	0	1	0	*	0	0	0	0	0	0	SR1	SR0	-	
(29)Status Read	0	0	1	0	PM2	PM1	Y/X	PDM	PT	STB	REV	DP	-	Indicate the internal status of register
	0	0	1	0	C17	C16	C15	C14	C13	C12	C11	C10	-	
	0	0	1	0	C27	C26	C25	C24	C23	C22	C21	C20		
(30)Display Data Write	1	1	0	WD[15:0]									-	Write display data to DDRAM
(31)Display Data Read	1	0	1	RD[15:0]									-	Read display data from DDRAM
(32)MTP Calibration ON/OFF Control	0	1	0	*	1	1	1	0	1	0	1	MOF	EAh EBh	Turn MTP Calibration function OFF/ON
(33)Multi-Time Calibration Set	0	1	0	*	1	1	1	0	1	1	0	1	EDh	Use for V1 voltage calibration
	0	1	0	*	0	0	0	MT4	MT3	MT2	MT1	MT0	-	
(34) Multi-Time Programming Set	0	1	0	*	1	1	1	0	1	1	1	1	EFh	Use for V1 voltage programming
(35)Test Mode	0	1	0	*	1	1	1	1	1	*	*	*	-	Use for IC test (F9h~FBh, FDh~FFh)

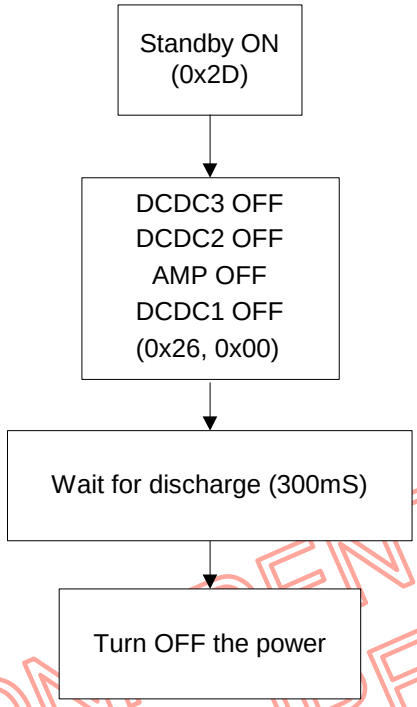
Note: "*" is don't care.

Power ON/OFF Sequence

Power ON Sequence

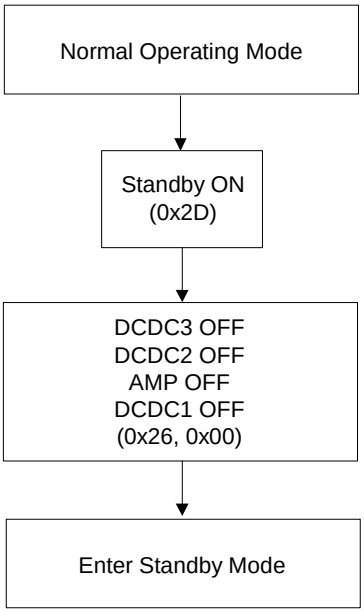


Power OFF Sequence

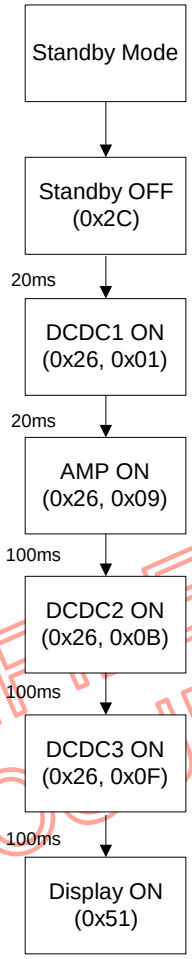


Enter/Exit Standby Mode Sequence

Enter Standby Mode Sequence



Exit Standby Mode Sequence



Absolute Maximum Rating

DC Supply Voltage (VDDIO) ..... -0.3V to +3.6V
DC Supply Voltage (VIN1, VIN1A, VIN1R) ..... -0.3V to +3.6V
DC Supply Voltage (VDD) ..... -0.3V to +1.95V
DC Supply Voltage (VCC-VEE) ..... -0.3V to +19.8V
Input Voltage (Vin) ..... -0.3V to VDDIO
Operating Ambient Temperature ..... -40°C to +85°C
Storage Temperature ..... -55°C to +125°C

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

DC Characteristics (1) (VSS = 0V, VDDIO = 1.2 ~ 3.6V, VIN1 = 2.4 ~ 3.6V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
VDDIO	Operating Voltage	1.2	-	3.6	V	
VDD	Operating Voltage	1.65	1.8	1.95	V	
VIN1	Operating Voltage	2.4	-	3.6	V	The booster times of 1st booster set to 1x, 1.5x (VIN1=VIN1A=VIN1R)
		2.4	-	2.75	V	The booster times of 1st booster set to 2x (VIN1=VIN1A=VIN1R)
DC2	Operating Voltage	1.66	-	2.75	V	1/4 bias, 2nd booster X(3)
		2.0	-	3.3	V	1/5 bias, 2nd booster X(3)
		1.5	-	2.475	V	1/5 bias, 2nd booster X(4)
		1.75	-	2.88	V	1/6 bias, 2nd booster X(4)
VIN2	Operating Voltage	2.4	-	5.5	V	
V45	Operating Voltage	2.4	-	5.5	V	
2VR	Operating Voltage	4.0	-	19.8	V	2VR=VCC-VEE
VREG	Voltage Regulator Out Voltage	1.65	1.8	1.95	V	REG_OUT, Ta = 25°C
VCC	Driving Voltage Input Range	6.0	-	11.55	V	External power supply mode
V1		2.0	-	3.3	V	
VM		1.0	-	1.65	V	
VEE		-8.25	-	-4.0	V	
VIHC	High-level Input Voltage	0.8 x VDDIO	-	VDDIO	V	D/I, RDB(E), WRB(R/W), CS1B, CS2, RSTB, D0~D15, OSCIN, P/S, MPU
VILC	Low-level Input Voltage	VSS	-	0.2 x VDDIO	V	
VOHC	High-level Output Voltage	0.8 x VDDIO	-	VDDIO	V	IOH=-0.5mA / VDDIO=1.65~3.6V IOH=-0.1mA / VDDIO=1.2~1.65V (D0~D15, CL, PM, SYNC, FR)
VOLC	Low-level Output Voltage	VSS	-	0.2 x VDDIO	V	IOL=0.5mA / VDDIO=1.65~3.6V IOL=0.1mA / VDDIO=1.2~1.65V (D0~D15, CL, PM, SYNC, FR)
ILI	Input Leakage Current	-1.0	-	1.0	µA	Vin=VDDIO or VSS (P/S, MPU, D/I, RDB(E), WRB(R/W), CS1B, CS2, RSTB)
IHZ	HZ Leakage Current	-3.0	-	3.0	µA	When the D0~D15 are in high impedance
fOSC	Oscillator Frequency Range (note 1)	97.52	-	197.12	kHz	In normal and partial display mode 0 and mode 1
ΔfOSC	Oscillator Frequency Tolerance (note 2)	126.72	140.8	154.88	kHz	In normal and partial display mode 0 and mode 1

Note: The condition of values for oscillator is based on 1/132 duty, 1/66duty, 1/33duty, no dummy subgroup (DSG =1) and the following is specified:

1. Minimum value of fOSC is defined at frame frequency = 65Hz
   Maximum value of fOSC is defined at frame frequency = 140Hz
2. Typical value of ΔfOSC is defined at frame frequency = 100Hz

DC Characteristics (2) (VSS = 0V, VDDIO = 1.2 ~ 3.6V, VIN1 = 2.4 ~ 3.6V, Ta = -40 ~ +85°C)

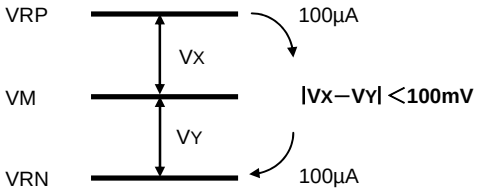
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
RONC	LCD Driver ON Resistance for COM	-	1.0	1.5	KΩ	VCC=11.55V, VM=1.65V, VEE=-8.25V, Iload=100µA, Ta=25°C
RONS	LCD Driver ON Resistance for SEG	-	1.5	3.0	KΩ	V1=3.3V, VM=1.65V, V0IN=0V, Iload=100µA, Ta=25°C
IDD	Current Consumption (without Regulator)	-	TBD	TBD	uA	VDDIO=VDD=1.8V, VIN1=2.4V, 1/6 bias, 1st booster is x1.5, 132 display lines, fOSC=140.8 kHz, no load, no access, all white display pattern, CR=0xFF, Ta=25°C
	Current Consumption (with Regulator)	-	TBD	TBD		VDDIO=VIN1=3.0V, VDD=REG_OUT, 1/6 bias, 1st booster is x1.5, 132 display lines, fOSC=140.8 kHz, no load, no access, all white display pattern, CR=0xFF, Ta=25°C
ISB	Standby Current	-	15	TBD	uA	VDD=REG_OUT, VDDIO=VIN1=VIN1A= VIN1R=3.0V, Ta=25°C, REG_ENB=L
		-	1.5	TBD		VDD=1.8V, VDDIO=VIN1=VIN1A= VIN1R=3.0V, Ta=25°C, REG_ENB=H

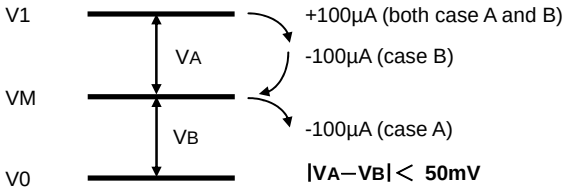
DC Characteristics (3) (VSS = 0V, VDDIO = 1.2 ~ 3.6V, VIN1 = 2.4 ~ 3.6V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
Δ(VRP)	Voltage Shift Range (note 1)	-	-	150	mV	Isource=80µA
Δ(VRN)		-	-	150	mV	Isink=80µA
Δ(VM)		-	-	20	mV	Isource,sink=250µA
Δ(V1)		-	-	20	mV	Isource=250µA
ΔVRP0 ΔVRN0	Tolerance of Bias Ratio (no load)	-100	-	100	mV	ΔVRP0=(VRP-VM)-VMxBias
						ΔVRN0=(VM-VRN)-VMxBias
ΔVofs1	Offset Voltage (note2)	-	-	100	mV	Iload=100µA (VRP) Iload=-100µA (VRN)
ΔVosf2		-	-	50	mV	A. Iload=100µA (V1, VM) B. Iload=100µA (V1) Iload=-100µA (VM)
ΔV1	Voltage Range	1.95	2.00	2.05	V	Contrast control=00h, Ta = 25°C
		3.25	3.30	3.35	V	Contrast control=FFh, Ta = 25°C
ΔVM		0.95	1.00	1.05	V	Contrast control=00h, Ta = 25°C
		1.60	1.65	1.70	V	Contrast control=FFh, Ta = 25°C
ΔVstep	Tolerance of Contrast Step of V1	2.549	5.098	7.647	mV	V1=3.3V
ΔVt	Temperature Compensation Tolerance	-0.02	-	+0.02	%/°C	VIN1=VIN1A=VIN1R=3.0V, Ta=-20 ~ +70°C
V1	Output Voltage Level (note 3)	2.0	-	3.3	V	1st booster is x1.5
VM		1.0	-	1.65	V	
DC2		1.67	-	2.75	V	

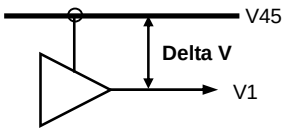
Notes:

1. Voltage Shift Range means output voltage difference between output current in loading and unloading.
2. ΔVofs1 = ||VRP - VM| - |VM - VRN||, ΔVofs2 = ||V1 - VM| - |VM – V0||



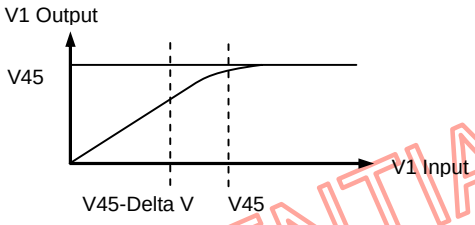


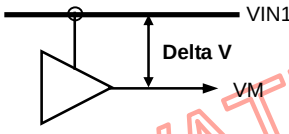
3. The definition of these three output voltage levels are shown as below.



Delta V＞0.3V (External V45)
Delta V＞0.5V (Internal V45)

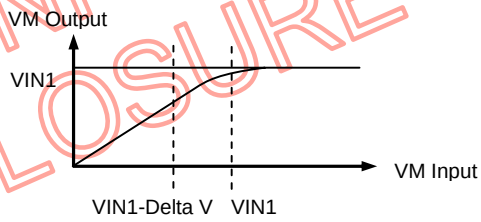
If V1 input voltage is set over V45, V1 output voltage must be clipped near V45. In this case, V1 output level must not be unstable.

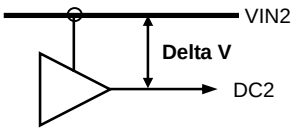




Delta V＞0.3V

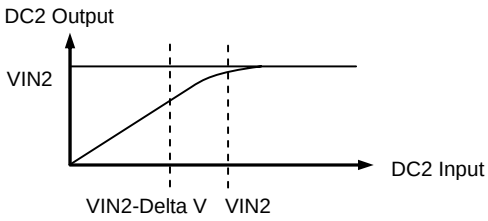
If VM input voltage is set over VIN1, VM output voltage must be clipped near VIN1. In this case, VM output level must not be unstable.





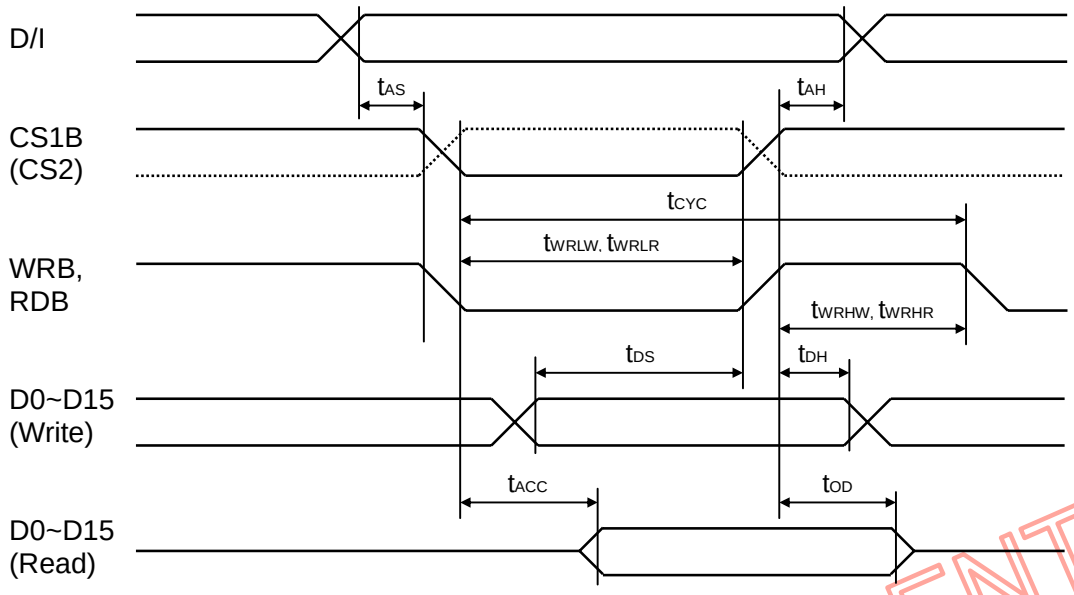
Delta V＞0.3V (External VIN2)
Delta V＞0.5V (VIN2=VOUT)

If DC2 input voltage is set over VIN2, DC2 output voltage must be clipped near VIN2. In this case, DC2 output level must not be unstable.



AC Characteristics

1. System Buses Read/Write Characteristics (for 8080 Series MPU)



(VDDIO=1.65~3.6V, VDD = 1.65~1.95V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{AH}	Address hold time	0	-	-	ns	D/I
t_{AS}	Address setup time	0	-	-	ns	
t_{CYC}	System cycle time	50	-	-	ns	
$t_{CYC(READ)}$	System cycle time(READ)	100	-	-	ns	
t_{WRLW}	Low pulse width for write	20	-	-	ns	WRB
t_{WRLR}	Low pulse width for read	60	-	-	ns	RDB
t_{WRHW}	High pulse width for write	20	-	-	ns	WRB
t_{WRHR}	High pulse width for read	20	-	-	ns	RDB
t_{DS}	Data setup time	5	-	-	ns	D0~D15
t_{DH}	Data hold time	5	-	-	ns	
t_{ACC}	Access time	-	-	80	ns	D0~D15, C_L = 100pF
t_{OD}	Output disable time	20	-		ns	

*1. The input signal rise time and fall time (t_r, t_f) is specified at 10ns or less.
($t_r + t_f$) < ($t_{CYC} - t_{CSLW} - t_{CSHW}$) for write, ($t_r + t_f$) < ($t_{CYC} - t_{CSLR} - t_{CSHR}$) for read.

*2. All timing is specified using 20% and 80% of VDDIO as the reference.

*3. t_{WRLW} and t_{WRLR} are specified as the overlap interval when CS1B is low (CS2 is high) and WRB or RDB is low.

(VDDIO=1.2~1.65V, VDD = 1.65~1.95V, Ta = -40 ~ +85°C)

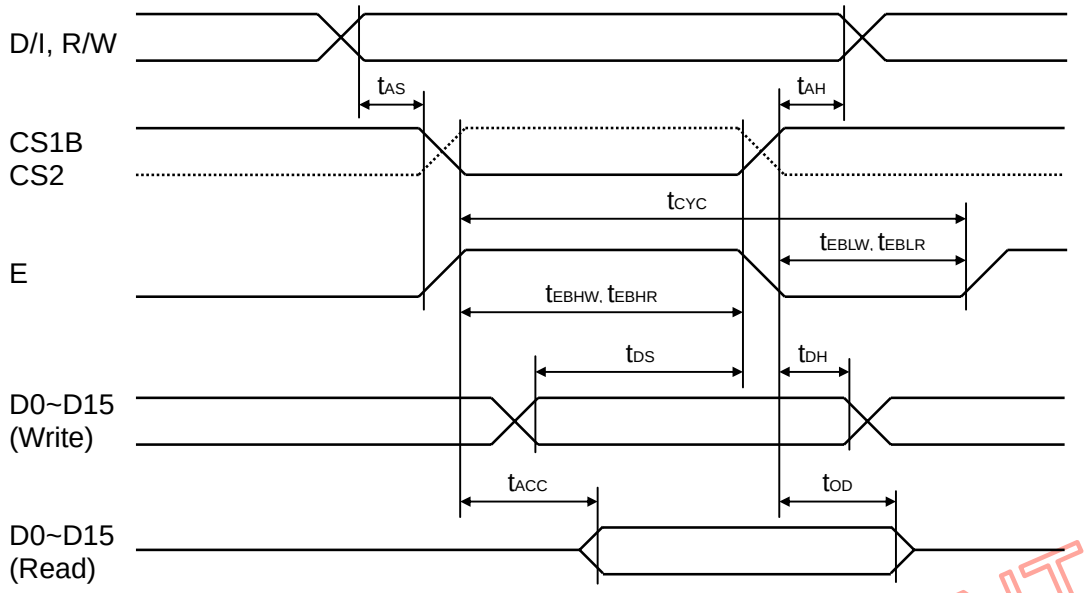
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{AH}	Address hold time	TBD	-	-	ns	D/I
t_{AS}	Address setup time	TBD	-	-	ns	
t_{CYC}	System cycle time	TBD	-	-	ns	
$t_{CYC(READ)}$	System cycle time(READ)	TBD	-	-	ns	
t_{WRLW}	Low pulse width for write	TBD	-	-	ns	WRB
t_{WRLR}	Low pulse width for read	TBD	-	-	ns	RDB
t_{WRHW}	High pulse width for write	TBD	-	-	ns	WRB
t_{WRHR}	High pulse width for read	TBD	-	-	ns	RDB
t_{DS}	Data setup time	TBD	-	-	ns	D0~D15
t_{DH}	Data hold time	TBD	-	-	ns	
t_{ACC}	Access time	-	-	TBD	ns	D0~D15, C_L = 100pF
t_{OD}	Output disable time	TBD	-	-	ns	

*1. The input signal rise time and fall time (t_r, t_f) is specified at 10ns or less.
($t_r + t_f$) < ($t_{CYC} - t_{CSLW} - t_{CSHW}$) for write, ($t_r + t_f$) < ($t_{CYC} - t_{CSLR} - t_{CSHR}$) for read.

*2. All timing is specified using 20% and 80% of VDDIO as the reference.

*3. t_{WRLW} and t_{WRLR} are specified as the overlap interval when CS1B is low (CS2 is high) and WRB or RDB is low.

2. System Buses Read/Write Characteristics (for 6800 Series MPU)



(VDDIO=1.65~3.6V, VDD = 1.65~1.95V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{AH}	Address hold time	0	-	-	ns	D/I
t_{AS}	Address setup time	0	-	-	ns	
t_{CYC}	System cycle time	50	-	-	ns	
$t_{cyc(READ)}$	System cycle time (READ)	100	-	-	ns	
t_{EBHW}	High pulse width for write	20	-	-	ns	E
t_{EBHR}	High pulse width for read	60	-	-	ns	E
t_{EBLW}	Low pulse width for write	20	-	-	ns	E
t_{EBLR}	Low pulse width for read	20	-	-	ns	E
t_{DS}	Data setup time	5	-	-	ns	D0~D15
t_{DH}	Data hold time	5	-	-	ns	
t_{ACC}	Access time	-	-	80	ns	D0~D15, C_L = 100pF
t_{OD}	Output disable time	20	-		ns	

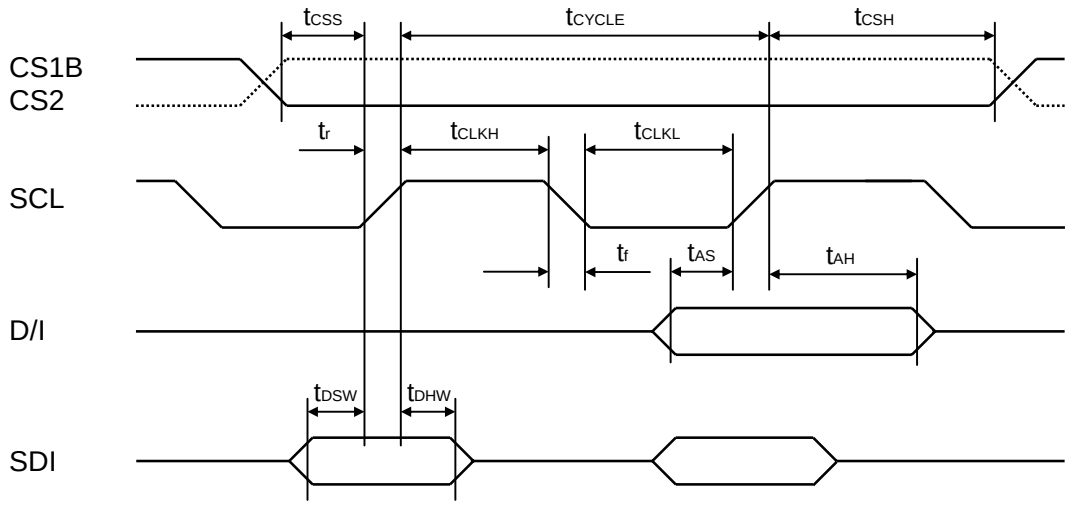
*1. The input signal rise time and fall time (t_r, t_f) is specified at 10ns or less.
($t_r + t_f$) < ($t_{CYC} - t_{CSLW} - t_{CSHW}$) for write, ($t_r + t_f$) < ($t_{CYC} - t_{CSLR} - t_{CSHR}$) for read.
*2. All timing is specified using 20% and 80% of VDDIO as the reference.
*3. t_{EBHW} and t_{EBHR} are specified as the overlap interval when CS1B is low (CS2 is high) and E is high.

(VDDIO=1.2~1.65V, VDD = 1.65~1.95V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{AH}	Address hold time	TBD	-	-	ns	D/I
t_{AS}	Address setup time	TBD	-	-	ns	
t_{CYC}	System cycle time	TBD	-	-	ns	
$t_{cyc(READ)}$	System cycle time (READ)	TBD	-	-	ns	
t_{EBHW}	High pulse width for write	TBD	-	-	ns	E
t_{EBHR}	High pulse width for read	TBD	-	-	ns	E
t_{EBLW}	Low pulse width for write	TBD	-	-	ns	E
t_{EBLR}	Low pulse width for read	TBD	-	-	ns	E
t_{DS}	Data setup time	TBD	-	-	ns	D0~D15
t_{DH}	Data hold time	TBD	-	-	ns	
t_{ACC}	Access time	-	-	TBD	ns	D0~D15, C_L = 100pF
t_{OD}	Output disable time	TBD	-	-	ns	

*1. The input signal rise time and fall time (t_r, t_f) is specified at 10ns or less.
($t_r + t_f$) < ($t_{CYC} - t_{CSLW} - t_{CSHW}$) for write, ($t_r + t_f$) < ($t_{CYC} - t_{CSLR} - t_{CSHR}$) for read.
*2. All timing is specified using 20% and 80% of VDDIO as the reference.
*3. t_{EBHW} and t_{EBHR} are specified as the overlap interval when CS1B is low (CS2 is high) and E is high.

3. Serial Interface Timing



(VDDIO=1.65~3.6V, VDD = 1.65~1.95V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYCLE}	Serial clock cycle	50	-	-	ns	SCL
t_{CLKH}	Serial clock H pulse width	5	-	-	ns	SCL
t_{CLKL}	Serial clock L pulse width	10	-	-	ns	SCL
t_{AS}	Address setup time	25	-	-	ns	D/I
t_{AH}	Address hold time	5	-	-	ns	D/I
t_{DSW}	Data setup time	5	-	-	ns	SDI
t_{DHW}	Data hold time	5	-	-	ns	SDI
t_{CSS}	Chip select setup time	10	-	-	ns	CS1B, CS2
t_{CSH}	Chip select hold time	0	-	-	ns	CS1B, CS2

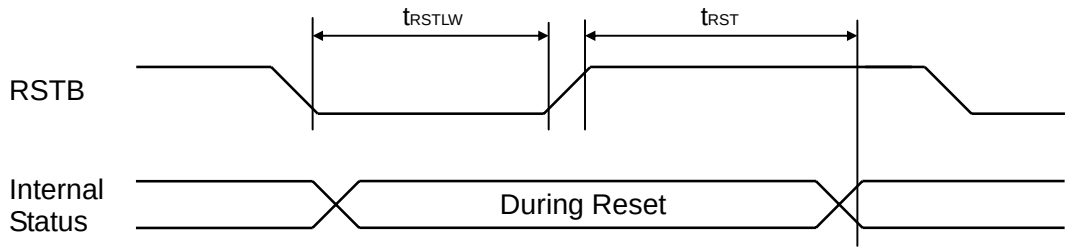
*1. The input signal rise time and fall time (t_r, t_f) is specified at 10ns or less.
*2. All timing is specified using 20% and 80% of VDDIO as the standard.

(VDDIO=1.2~1.65V, VDD = 1.65~1.95V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYCLE}	Serial clock cycle	TBD	-	-	ns	SCL
t_{CLKH}	Serial clock H pulse width	TBD	-	-	ns	SCL
t_{CLKL}	Serial clock L pulse width	TBD	-	-	ns	SCL
t_{AS}	Address setup time	TBD	-	-	ns	D/I
t_{AH}	Address hold time	TBD	-	-	ns	D/I
t_{DSW}	Data setup time	TBD	-	-	ns	SDI
t_{DHW}	Data hold time	TBD	-	-	ns	SDI
t_{CSS}	Chip select setup time	TBD	-	-	ns	CS1B, CS2
t_{CSH}	Chip select hold time	TBD	-	-	ns	CS1B, CS2

*1. The input signal rise time and fall time (t_r, t_f) is specified at 10ns or less.
*2. All timing is specified using 20% and 80% of VDDIO as the standard.

4. Reset Timing



(VDDIO=1.65~3.6V, VDD = 1.65~1.95V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{RSTLW}	Reset low pulse width	10	-	-	µs	RSTB
t_{RST}	Reset Time	-	-	1	µs	
tr_{RST}	Reset Rise Time	-	-	1	ms	

(VDDIO=1.2~1.65V, VDD = 1.65~1.95V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{RSTLW}	Reset low pulse width	TBD	-	-	µs	RSTB
t_{RST}	Reset Time	-	-	TBD	µs	
tr_{RST}	Reset Rise Time	-	-	TBD	ms	

Microprocessor Interface (for reference only)

8080-series microprocessors

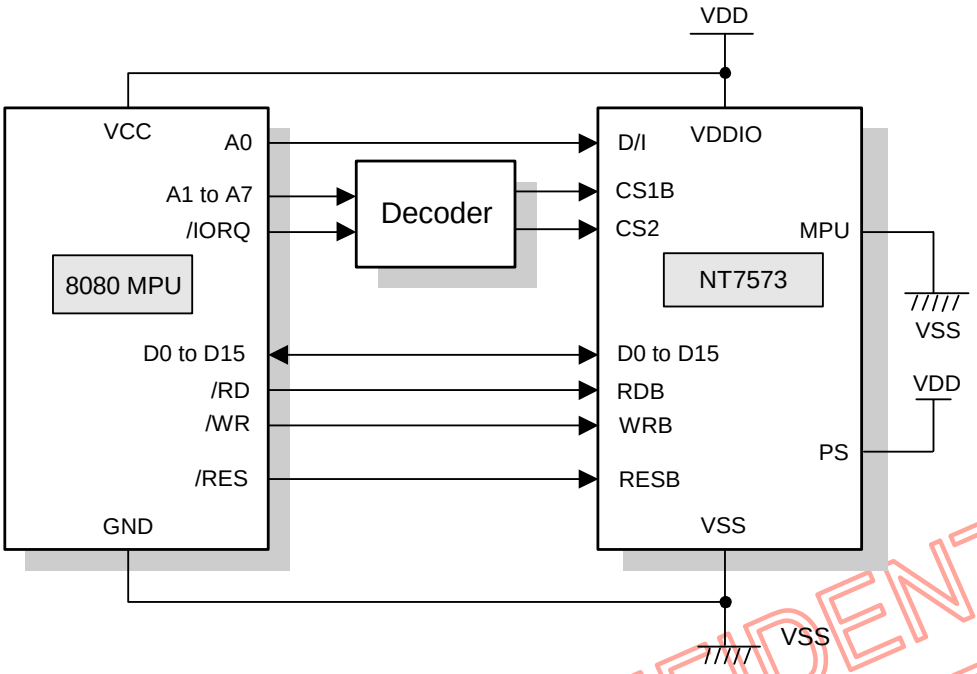


Figure 7

6800-series microprocessors

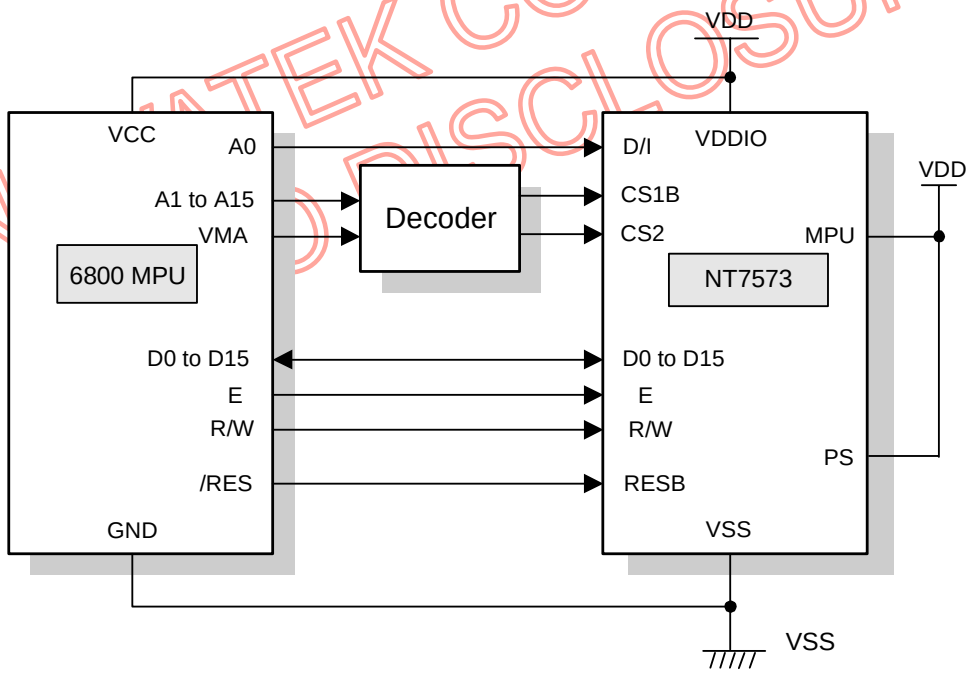
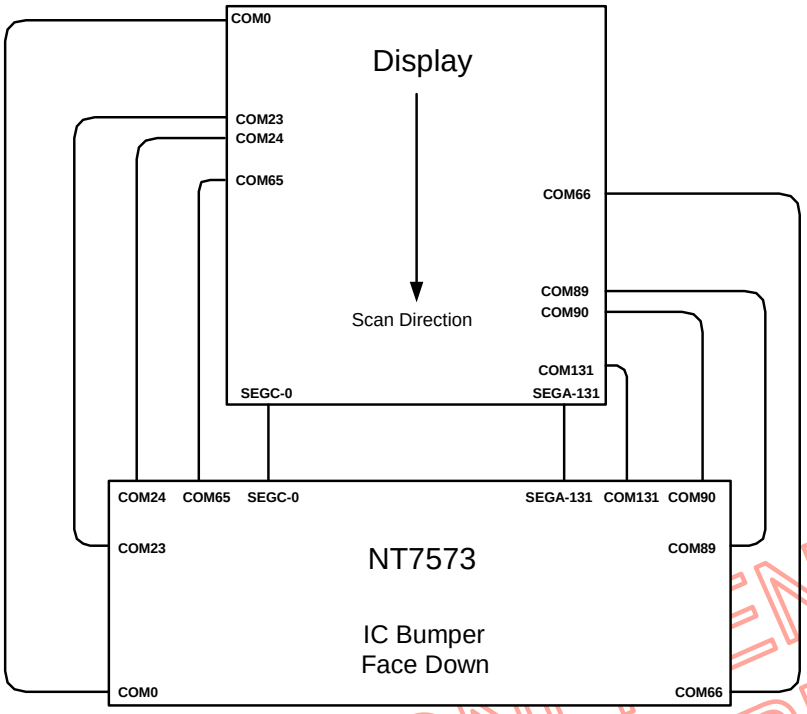


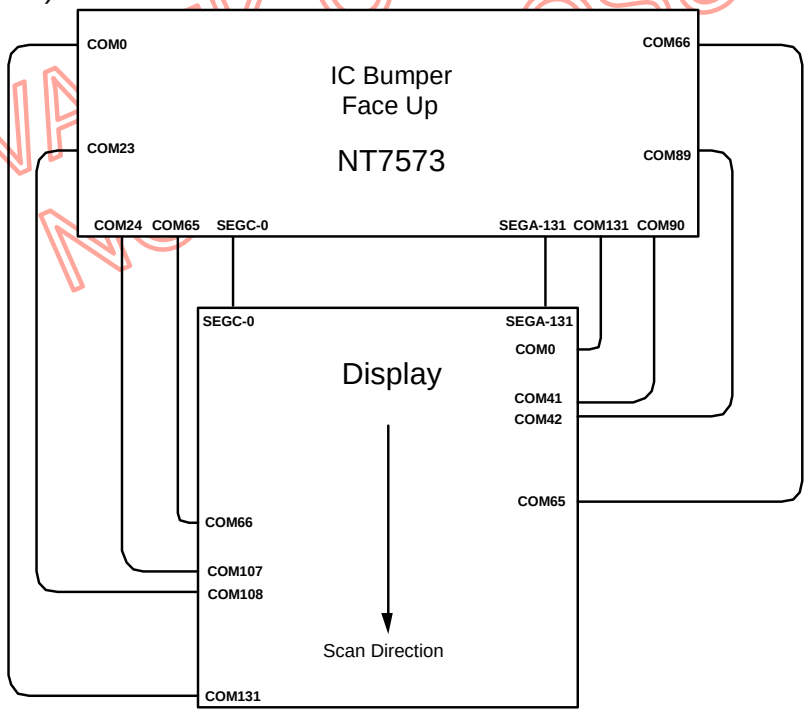
Figure 8

Application information for LCD panel (for reference only)

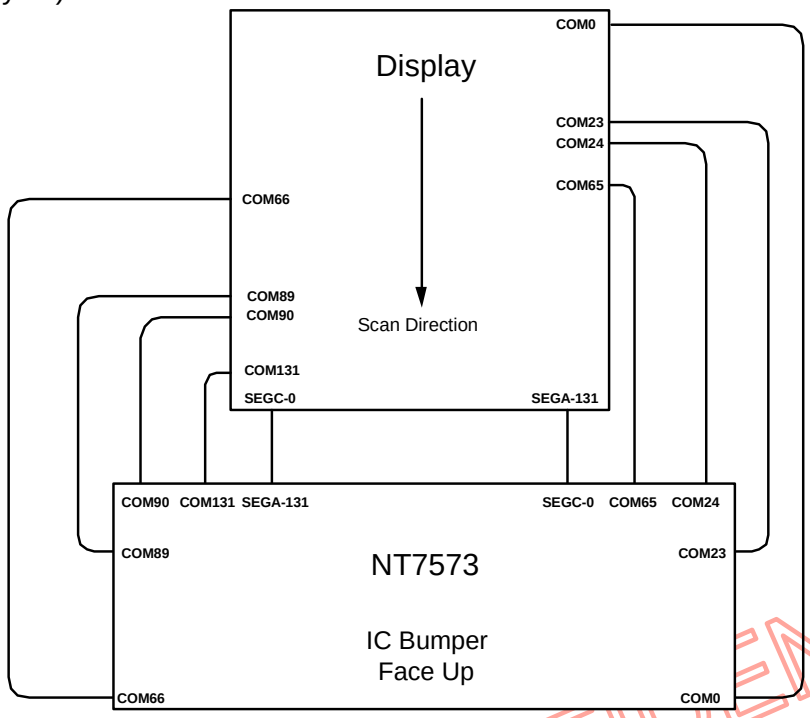
1. Type I (CDR = 0, COM Scan direction from COM0 to COM131, MX = 0, No Mirror X, SEQ = 0, Progressive Layout)



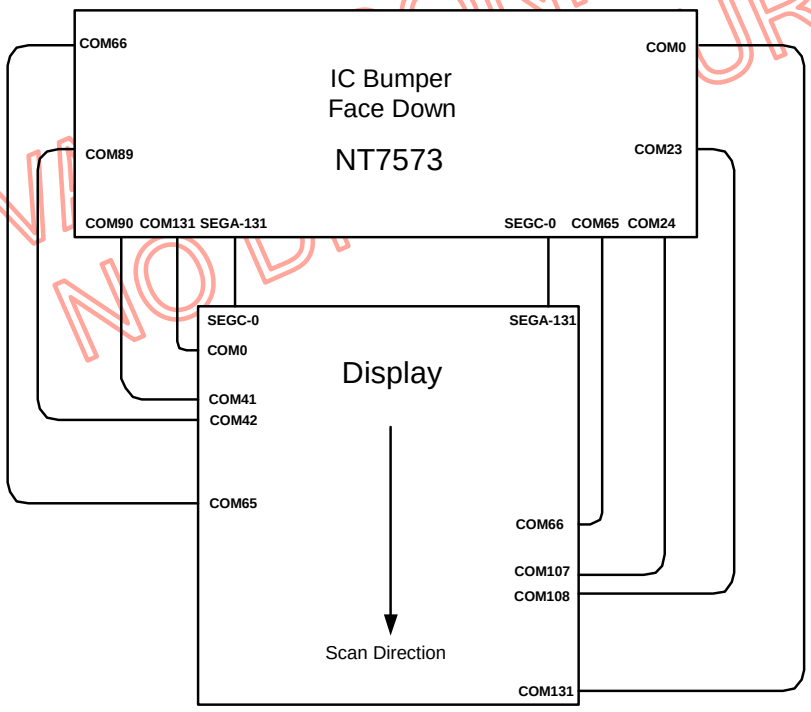
2. Type II (CDR = 1, COM Scan direction from COM131 to COM0, MX = 0, No Mirror X, SEQ = 0, Progressive Layout)



3. Type III (CDR = 0, COM Scan direction from COM0 to COM131, MX = 1, Mirror X, SEQ = 0, Progressive Layout)

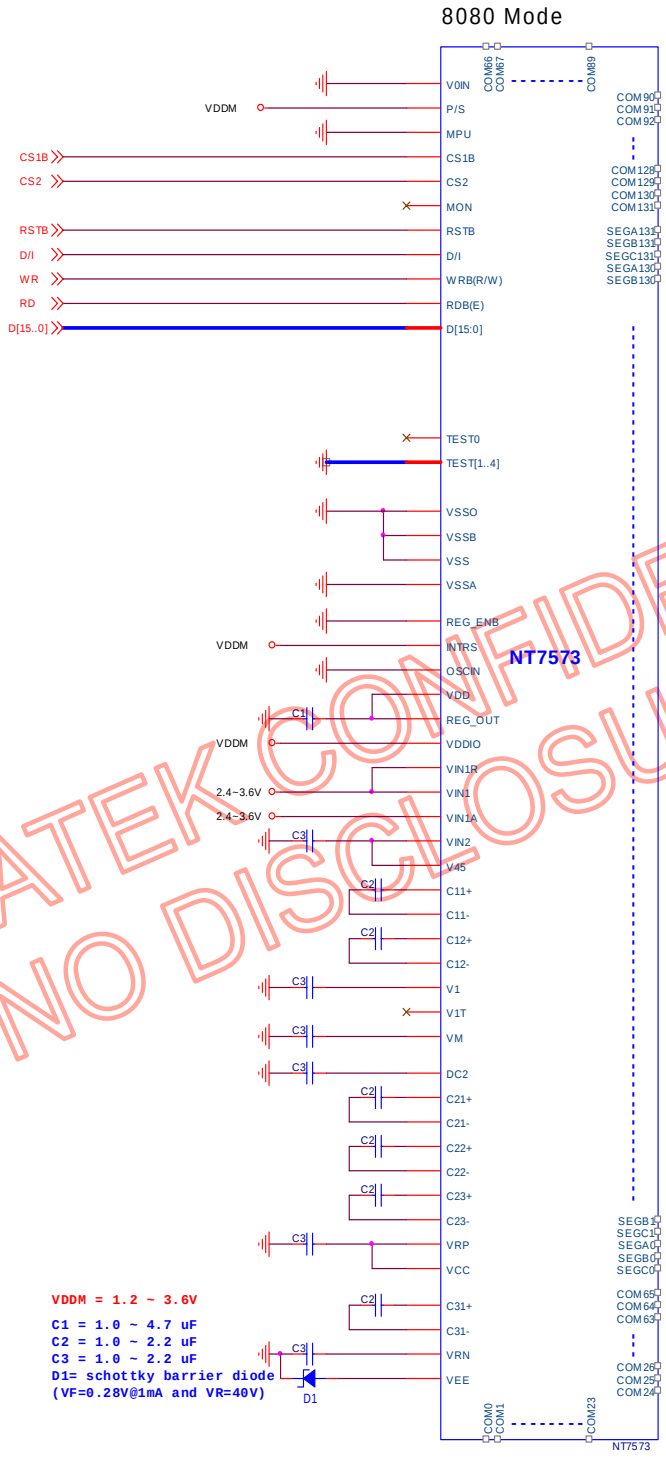


4. Type IV (CDR = 1, COM Scan direction from COM131 to COM0, MX = 1, Mirror X, SEQ = 0, Progressive Layout)

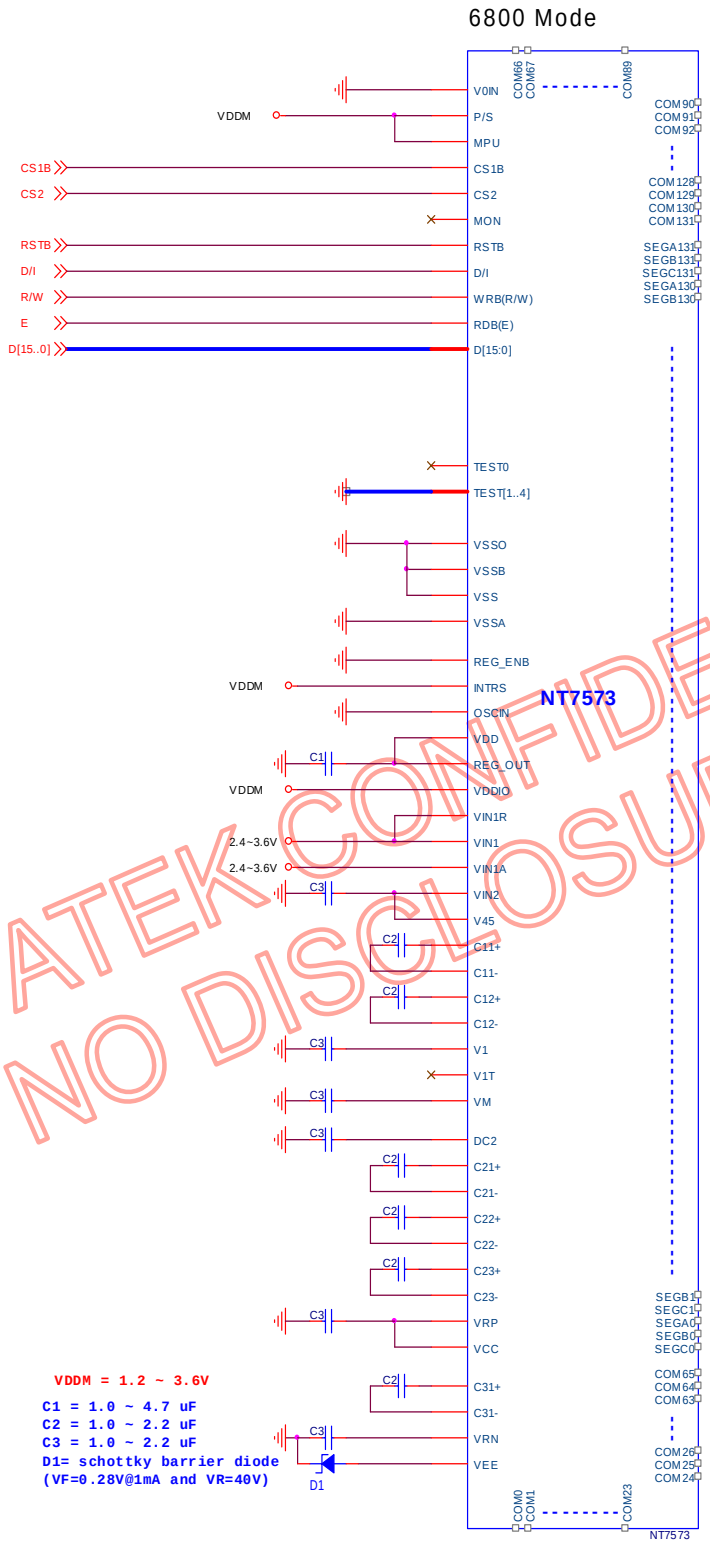


Application information for pin connection to MPU (for reference only)

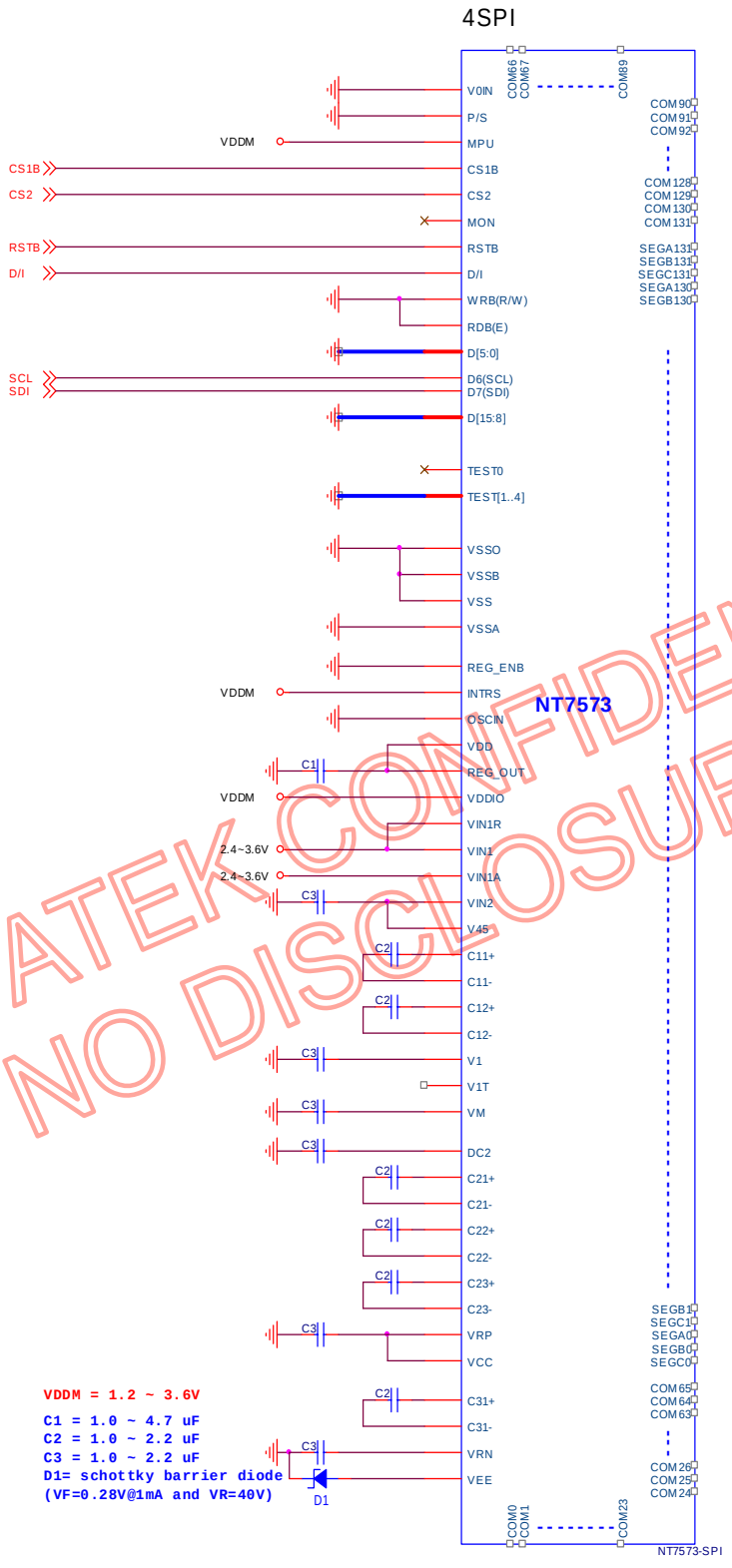
1. 8080 MPU Mode: (P/S=H, MPU=L, REG_ENB=L, INTRS=H)



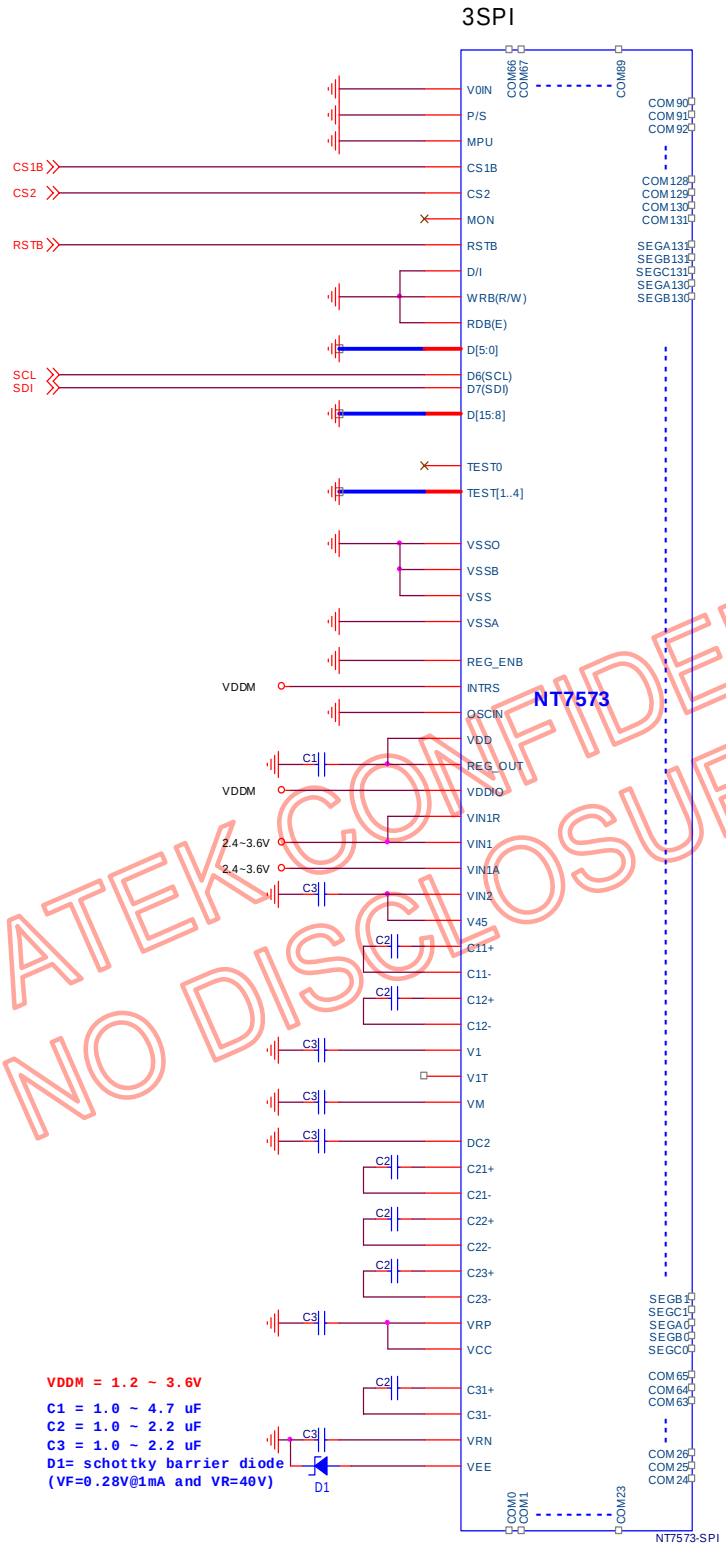
2. 6800 MPU Mode: (P/S=H, MPU=H, REG_ENB=L, INTRS=H)



3. 4-wire Serial Mode: (P/S=L, MPU=H, REG_ENB=L, INTRS=H)



4. 3-wire Serial Mode: (P/S=L, MPU=L, REG_ENB=L, INTRS=H)



Ordering Information

Part No.	Packages
NT7573H-BDT	Gold Bump on Chip Tray

Cautions

1. The contents of this document will be subjected to change without notice.
2. Precautions against light projection:
   Light has the effect of causing the electrons of semiconductor to move; so light projection may change the characteristics of semiconductor devices. For this reason, it is necessary to take account of effective protection measures for the packages (such as COB, COG, TCP and COF, etc.) causing chip to be exposed to a light environment in order to isolate the projection of light on any part of the chip, including top, bottom and the area around the chip.
   Observe the following instructions in using this product:
   a. During the design stage, it is necessary to notice and confirm the light sensitivity and preventive measures for using IC on substrate (PCB, Glass or Film) or product.
   b. Test and inspect the product under an environment free of light source penetration.
   c. Confirm that all surfaces around the IC will not be exposed to light source.