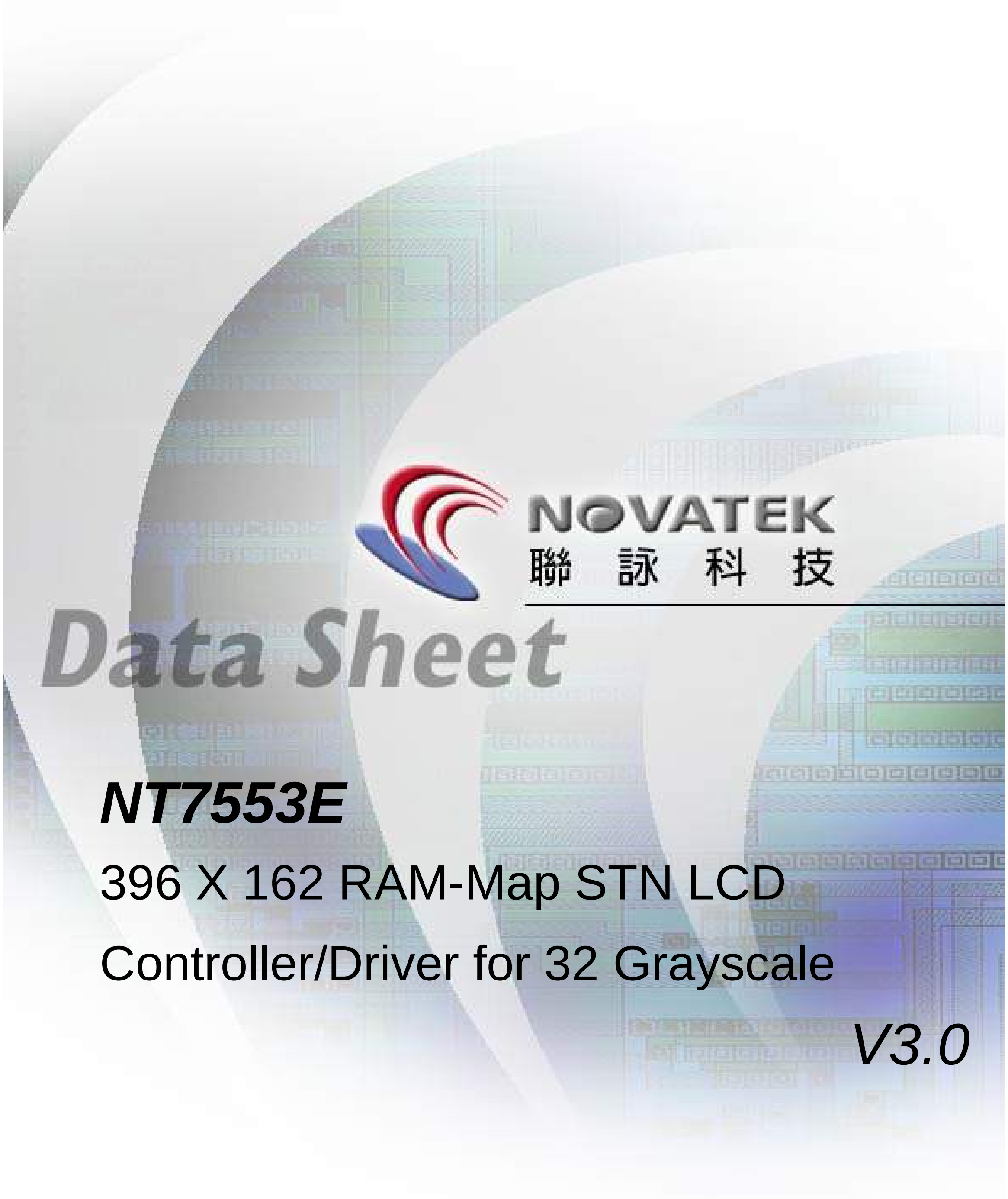

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Data Sheet

NT7553E

396 X 162 RAM-Map STN LCD
Controller/Driver for 32 Grayscale

V3.0

Revision History

NT7553E Specification Revision History					
Version	**Content**	**Prepared by**	**Checked by**	**Approved by**	**Date**
1.0	Released	-	-	-	Sep. 2007
2.0	1. Correct the stabilization time between instruction (1) to (3) on figure 21.(Page 39) 2. Add ITO Layout Notice for Segment outputs. (Page 57) 3. Add Application Notice for Large Panel Design section. (Page 58) 4. Add Absolute Maximum Rating of VOUT condition. (Page 81)	Mike Chen	Edwards Tseng	Dennis Kuo	Sep. 2008
3.0	1. Add 100ms delay time between “display on sequence” and “display on” (Page 39) 2. Add specification of Schottky Barrier Didoe.(Page 45) 3. Correct recommend resistance of VDD and VSS from 100Ω to 50Ω.(Page 55) 4. Add recommend external VOUT voltage on/off sequence.(Page 59, 60) 5. Add MTPT description in table32. (Page 74) 6. Add specification of Sleep Mode Current Consumption. (Page 83) 7. Add specification of Reset Timing. (Page 91) 8. Add specification of Chip Thickness. (Page 102)	Mike Chen	Edwards Tseng	Dennis Kuo	Nov. 2008

Features

- 396 x 162-dot graphics display LCD controller/driver for 32 level grayscale.
- RAM capacity: 396x 162 x 5 = 320,760 bits
- 8-bit and 16-bit parallel bus interface for both 8080 and 6800 series, and 4-wire Serial Peripheral Interface (SPI)
- Various grayscale-display control functions
  - 32 grayscale out of 52 possible grayscale can be displayed at the same time (grayscale palette incorporated)
  - Vertical scroll display function in raster-row units
  - Partial LCD drive of two screens in any position
- Shift change of segment and common drivers
- Power supply voltage:
  - VDD = 2.4 ~ 3.6 V (REGENB=L)
  - VDD = 1.6 ~ 2.3 V (REGENB=H)
  - VDD2 = 2.4 ~ 3.6 V
  - VDD3 = 2.4 ~ 3.6 V
  - VCC = 1.6 ~2.3V
  - Common driving voltage = 8 ~ 36 V (power for DC-DC converter)
  - Segment driving voltage = 2 ~ 4 V
  - VOUT = 4.5 ~ 5.5 V
  - VCI2 Maximum 4-times step-up circuit for liquid crystal drives voltage and voltage inverting circuit
  - VCI1 Maximum 3-times step-up circuit for VOUT
- Power save functions such as standby and sleep mode
- On chip LCD driving voltage generator or external power supply selectable
- 128-step contrast adjuster and on chip voltage follower to decrease direct current flow in the LCD drive bleeder-resisters
- Programmable drive duty ratios (1/8~1/162) and bias values (1/2~1/13) displayed on LCD
- Programmable partial display function
- Bit-operation functions for graphics processing:
  - Write-data mask function in bit units
  - Logical operation in pixel unit and conditional write function
- N-line inversion AC liquid-crystal drive (C-pattern waveform drive)
- On chip oscillation and hardware reset
- Multi-Time Programming (2 times) for VSH voltage
- Programmable LCD Driving Voltage Temperature Compensation Coefficients (selected by software command)
- COM positioned on both sides in one chip for COG form
- CMOS process

General Description

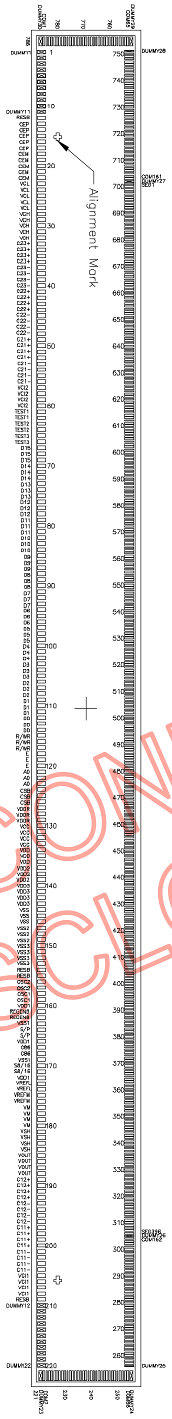
The NT7553E is a single-chip LCD controller/driver LSI for grayscale-graphics, which displays 396 x 162-dot graphics for 32 levels STN grayscale. It accepts display data through 8-bit or 16-bit parallel (8080 or 6800 series) or serial interface directly sent from a microcomputer and stores it in an on-chip display RAM. It generates an LCD drive signal independent of microprocessor clock.

The set of the on-chip display RAM of 396 x 162 x 5 bits and every 5 bits correspondence between LCD panel dots and on-chip RAM bits permits implementation of displays with a high degree of freedom.

The NT7553E contains 162 common output circuits and 396 segment output circuits. It can make 8 to 162 x 396-dot displays with instructions.

The NT7553E has various functions for reducing the power consumption, such as low operation voltage of 2.4/Min., a DC-DC converter to generate a maximum of 12-times the LCD drive voltage from the supplied voltage, voltage follower to decrease the direct current flow in the LCD drive bleeder-resisters, and no external operation clock is required for RAM read/write operations. Accordingly, this driver can be operated with minimum current consumption and its on-board low-current-consumption liquid crystal power supply can implement a high-performance handy display system with minimum current consumption and the smallest LSI configuration.

Pad Configuration



Block Diagram

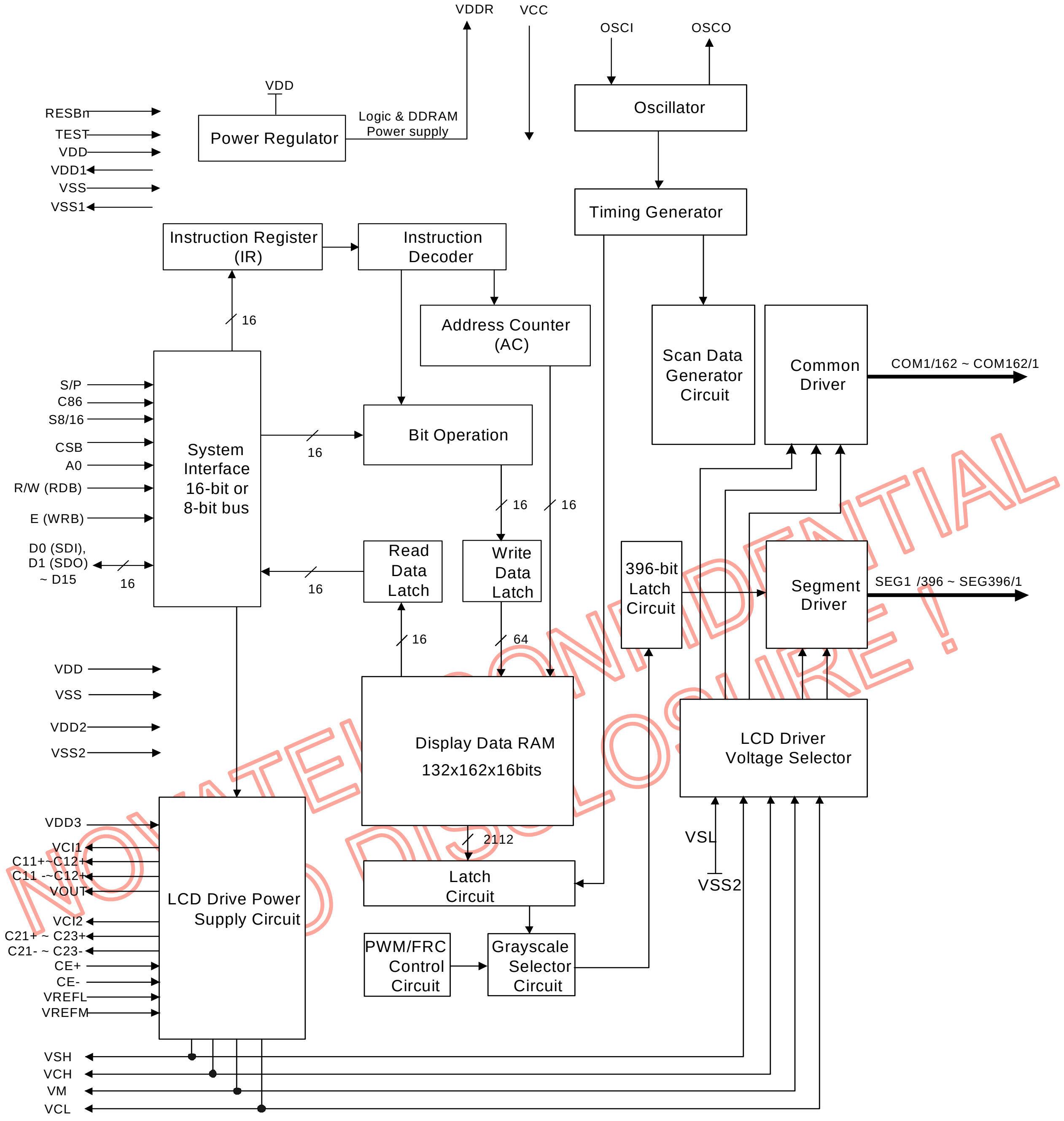


Figure 1. NT7553E Block Diagram Description

Pad Descriptions

Power Supply

Pad No.	Designation	I/O	Description
134~136	VDD	Supply	Power supply for logic
160,166,172	VDD1	O	Power supply output for pad option
137~139	VDD2	Supply	Power supply for analog, input the same level of voltage as VDD
140~143	VDD3	Supply	Voltage-input pin for step-up circuit 1.
144~146	VSS	Supply	Ground for logic
163,169	VSS1	O	Ground output for pad option
147~149	VSS2	Supply	Ground for analog
150~153	VSS3	Supply	Ground for VDD3
173~174	VREFL	Supply	Inputs reference voltage for LCD drives power supply. Inputs a lower level than VDD. Since input current does not run, level input, which is divided by resistors, is also possible.
205~208	VCI1	Supply	Voltage-input pin for step-up circuit 1. When the VCI adjuster is used, input the power supply from VCIOUT. When not used, input the external power supply.
57~60	VCI2	Supply	Capacitor for stabilization or open, connect capacitor for stabilization. When the internal power supply circuit is not used, leave this pin open.
185~188	VOUT	Supply	A voltage that doubles or triples the voltage between VCI1 and VSS is output here. The step-up factor can be set in an internal register. When internal operational amplifier is not used, supply external voltage.
181~184	VSH	Supply	The selection level for the segment signal. When internal operational amplifier is used, it is output from the internal operational amplifier and connects the capacitors for stabilization. When internal operational amplifier is not used, supply external voltage.
28~32	VCH	Supply	Selection level for the common signal. When internal power supply is used, connect the capacitors for stabilization to VCH, When internal power supply is not used, supply external voltage.
23~27	VCL	Supply	Selection level for the common signal. When internal power supply is used, connect the capacitors for stabilization to VCL, and shot key barrier diode to VCL. When internal power supply is not used, supply external voltage.

Power Supply (CONTINUTE)

177~180	VM	Supply	Non-selection level for the common signal. When internal operational amplifier is used, it is output from the internal operational amplifier and connects the capacitors for stabilization. When internal operational amplifier is not used, supply external voltage.
175~176	VREFM	Supply	Capacitor for stabilization or external power supply. Connect capacitor for stabilization for internal power supply. When internal operational amplifier is not used, supply external voltage.
130~133	VCC	Supply	Capacitor for stabilization or open Connect capacitor for stabilization for internal power supply.
127~129	VDDR	O	Capacitor for stabilization or open Connect capacitor for stabilization for internal power supply.

STEP-UP Capacitor Pad

Pad No.	Designation	I/O	Description
13~17	CEP	O	Connect a step-up capacitor to generate VCL level by VCH and VM. When step-up circuit is not used, leave this pin open.
18~22	CEM	O	
33~36	C23+	O	When step-up circuit is used, connect a step-up capacitor.
37~40	C23-	O	When step-up circuit is used, connect a step-up capacitor.
41~44	C22+	O	When step-up circuit is used, connect a step-up capacitor.
45~48	C22-	O	When step-up circuit is used, connect a step-up capacitor.
49~52	C21+	O	When step-up circuit is used, connect a step-up capacitor.
53~56	C21-	O	When step-up circuit is used, connect a step-up capacitor.
189~192	C12+	O	When step-up circuit is used, connect a step-up capacitor.
193~196	C12-	O	When step-up circuit is used, connect a step-up capacitor.
197~200	C11+	O	When step-up circuit is used, connect a step-up capacitor.
201~204	C11-	O	When step-up circuit is used, connect a step-up capacitor.

Liquid Crystal Drive Pad

Pad No.	Designation	I/O	Description
306~701	SEG1 ~ SEG396	O	Output signals for segment drive. In the display-off period (D1–0 = 00, 01) or standby mode (STB = 1), all pins output VSS level. The SGS bit can change the shift direction of the segment signal. For example, if SGS = 0, RAM address 0000 is output from SEG1 to SEG396. If SGS = 1, it is output from SEG396 to SEG1.
222~254, 257~304, 703~750, 753~785	COM1 ~ COM162	O	Output signals for common drive. In the display-off period (D1–0 = 00, 01) sleep mode (SLP = 1) or standby mode (STB = 1), all pins output VSS level. The CMS bit can change the shift direction of the common signal. For example, if CMS = 0, driver outputs from COM1 to COM162. If CMS = 1, driver outputs COM162 to COM1. Note that the start position of the common driver output is changed by screen diving position function.

System Bus Connection Pads

Pad No.	Designation	I/O	Description
164~165	S/P	I	Serial/Parallel selection pad: S/P = ”L”: parallel interface S/P = ”H”: serial interface
167~168	C86	I	Select MPU parallel interface mode: When S/P = “L”: C86 = ”L”: 6800 series MPU interface C86 = ”H”: 8080 series MPU interface When S/P = “H”: C86 should be connected to VSS.
170~171	S8/16 (SID)	I	8/16-bit parallel interface selection pad: When S/P = “L”: S8/16 = ”L”: 16-bit parallel interface S8/16 = ”H”: 8-bit parallel interface When S/P = “H”: This pad is used as the serial ID (SID) setting for a device code.
124~126	CSB	I	This is the chip select signal. When CSB = “L”, then the chip select becomes active, and data/command I/O is enabled. It must be fixed to VSS when not in use.
121~123	A0	I	A0 = “L”: Indicates that D0 to D7 are Index or Status data A0 = “H”: Indicates that D0 to D7 are Control data When a register or serial interface is selected, fix this pad to VDD or VSS level.
12 154~155 209	RESB1 RESB2 RESB3	I	Reset pin. Initializes the LSI when low. Must be reset after power-on. Since NT7553E has three RESET pins, use one pin and open two unused pins.
115~117	R/W (RDB)	I	When connected to a 6800 Series MPU, this is the read/write control signal input terminal. Low: Write, High: Read When connected to an 8080 MPU, this is active LOW. This terminal connects to the 8080 MPU RDB signal and the NT7553E data bus is in an output status when this signal is LOW. When the serial interface is selected, fix this pad to VDD or VSS level.
118~120	E (WRB) (SCL)	I	When connected to a 6800 Series MPU, this is active HIGH. This is used as an enable clock input of the 6800 series MPU. When connected to an 8080 MPU, it is active LOW. This pad is connected to the WRB signal of the 8080 MPU, and writes data at the low level. When the serial interface is selected, it serves as the serial clock input pin (SCL).

System Bus Connection Pads (continued)

112~114	D0 (SDI)	I/O	When 16-bit parallel interface is selected, it serves as the bi-directional data bus. When 8-bit parallel interface is selected, data transfer uses D8 ~ D15; fix the unsed pads: D0 ~ D7 to the VDD or VSS level. When the serial interface is selected, it serves as the serial data input terminal (SDI). The input level is read on the rising edge of SCL signal.
109~111	D1 (SDO)	I/O	When 16-bit parallel interface is selected, it serves as the bi-directional data bus. When 8-bit parallel interface is selected, data transfer uses D8 ~ D15; fix the unsed pads: D0 ~ D7 to the VDD or VSS level. When the serial interface is selected, it serves as the serial data output terminal (SDO).
67~108	D2 ~ D15	I/O	When 16-bit parallel interface is selected, it serves as the bi-directional data bus. When 8-bit parallel interface is selected, data transfer uses D8 ~ D15; fix the unsed pads: D0 ~ D7 to the VDD or VSS level. When the serial interface is selected, fix these pads to VDD or VSS level.
161~162	REGENB	I	Input pin for VDDR supply control, REGENB = “L”: VDDR regulator enable REGENB = “H”: VDDR regulator disable

Oscillation Pads

Pad No.	Designation	I/O	Description
158~159 156~157	OSCI OSCO	I/O	For external clock supply, input clock pulses to OSCI. For internal clock mode, OSCI must connect to OSCO.

Dummy Pads

Pad No.	Designation	I/O	Description
1~11, 210~221, 255~256, 305,702, 751~752, 786	Dummy	-	Dummy pads. No connection for user.

Test Pads

Pad No.	Designation	I/O	Description
61~62	Test1	-	Test pad. Must disconnect this pad.
63~64	Test2	-	Test pad. Must disconnect this pad.
65~66	Test3	-	Test pad. Must disconnect this pad.

Functional Descriptions

Microprocessor Interface

The NT7553E can transfer data via 8-bit (D8 ~D15)/16-bit (D0~D15) bi-directional data bus or via serial data input (SDI). When high or low is selected for the S/P, C86, and S8/16 pads, either 8-bit/16-bit parallel data input or serial data input can be selected as shown in Table 1. When serial data input is selected, the RAM data can also be read out via serial data output (SDO).

Table 1. Data Bus Interface Selection Mode

S/P	C86	S8/16 (SID)	Type	CSB	A0	E (WRB) (SCL)	R/W (RDB)	D0	D1	D2~D7	D8~D15
H	L	L	Serial interface bus SID = 0	CSB	A0	SCL	-	SDI	SDO	-	-
	L	H	Serial interface bus SID = 1	CSB	A0	SCL	-	SDI	SDO	-	-
L	L	L	6800 series 16-bit parallel bus	CSB	A0	E	R/W	D0	D1	D2~D7	D8~D15
	L	H	6800 series 8-bit parallel bus	CSB	A0	E	R/W	-	-	-	D8~D15
	H	L	8080 series 16-bit parallel bus	CSB	A0	WRB	RDB	D0	D1	D2~D7	D8~D15
	H	H	8080 series 8-bit parallel bus	CSB	A0	WRB	RDB	-	-	-	D8~D15

"-" Must always be high or low

Parallel Interface

When the NT7553E selects parallel input (S/P = Low), the 8080 series microprocessor or 6800 series microprocessor can be selected by the C86 pad to be connected high or low. The NT7553E identifies the data bus signal according to A0, E (WRB), R/W (RDB) signals as shown in Table 2.

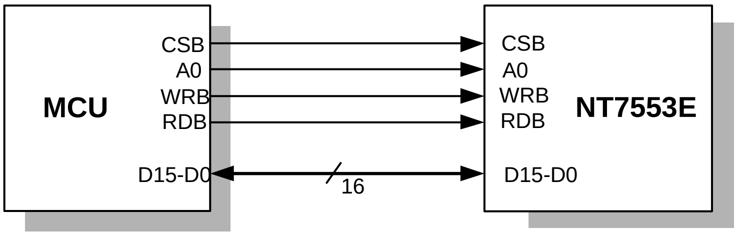
Table 2.Parallel Interface Read/Write Status

Common	6800 processor		8080 processor		Function
A0	E	R/W	RDB	WRB	
0	1	1	0	1	Reads internal status
0	1	0	1	0	Writes indexes into IR (index register)
1	1	1	0	1	Read from RAM data through RDR
1	1	0	1	0	Write control registers or RAM data through WDR

A dummy read is required before the first actual display data is read for parallel interface.

16-bit Bus Interface

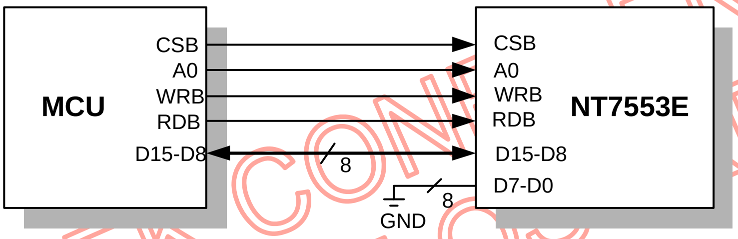
Setting the C86 and S8/16 (interface mode) to the VSS/VSS level allows 68-system E-clock-synchronized 16-bit parallel data transfer. Setting the C86 and S8/16 to the VDD/VSS level allows 80-system 16-bit parallel data transfer. When the number of buses or the mounting area is limited, use an 8-bit bus interface.



. Interface to 16-bit Microcomputer

8-bit Bus Interface

Setting the C86 and S8/16 (interface mode) to the VSS/VDD level allows 68-system E-clock-synchronized 8-bit parallel data transfer using pins D15 to D8. Setting the C86 and S8/16 to the VDD/VDD level allows 80-system 8-bit parallel data transfer. The 16-bit instructions and RAM data are divided into eight upper/lower bits and the transfer starts from the upper eight bits. Fix unused pins D7 to D0 to the VDD or VSS level. Note that the upper bytes must also be written when the index register is written.



Interface to 8-bit Microcomputer

Note:

Transfer synchronization function for an 8-bit bus interface

The NT7553E supports the transfer synchronization function, which resets the upper/lower counter to count upper/lower 8-bit data transfer in the 8-bit bus interface. Noise causing transfer mismatch between the eight upper and lower bits can be corrected by a reset triggered by consecutively writing a 00H instruction four times. The next transfer starts from the upper eight bits. Executing synchronization function periodically can recover any runaway in the display system.

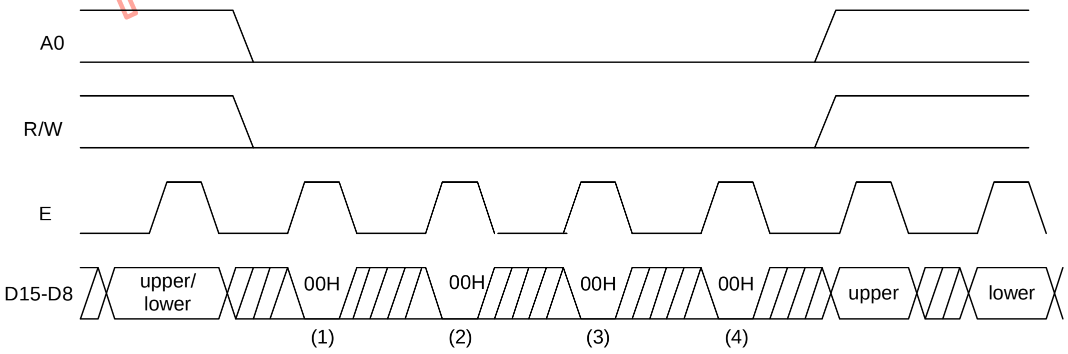


Figure 2. 8-bit Transfer Synchronization

Serial Interface

When the serial interface has been selected (S/P = High, C86 = Low), the SID (serial device ID) can be selected by the S8/16 pad to be connected high or low. The unused pads (D2~15) should be connected to VDD or VSS. When the chip is in serial interface, using the chip select input (CSB), serial clock input (SCL), serial data input (SDI) and serial data output (SDO) pins. The NT7553E initiates serial data transfer by transferring the start byte at the falling edge of CSB input. It ends serial data transfer at the rising edge of CSB input.
The NT7553E is selected when the 6-bit chip address in the start byte transferred from the transmitting device matches the 6-bit device identification code assigned to the NT7553E. The NT7553E, when selected, receives the subsequent data string. The ID (S8/16) pin can determine the LSB of the identification code. The five upper bits must be “01110”. Two different chip addresses must be assigned to a single NT7553E because the seventh bit of the start byte is used as a register select bit (A0): that is, when A0 = “0”, data can be written to the index register or status can be read, and when A0 = “1”, an instruction can be issued or data can be written to or read from RAM. Read or write is selected according to the eighth bit of the start byte (R/W bit). The data is received when the R/W bit is “0”, and is transmitted when the R/W bit is “1”.

After receiving the start byte, the NT7553E receives or transmits the subsequent data byte-by-byte. The data is transferred with the MSB first. All NT7553E instructions are 16 bits. Two bytes are received with the MSB first (D15 to 0), and then the instructions are internally executed. After the start byte has been received, the first byte is fetched internally as the upper eight bits of the instruction and the second byte is fetched internally as the lower eight bits of the instruction. Five bytes of RAM read data after the start byte are invalid. The NT7553E starts to read correct RAM data from the sixth byte.

Table 3.Serial Interface Read/Write Status

A0	R/W	Function
0	1	Reads internal status
0	0	Writes indexes into IR (index register)
1	1	Read from RAM data through RDR
1	0	Writes control registers and RAM data through WDR

Note:
1. When the chip is not active, the shift registers and the counter is reset to their initial states.
2. Caution is required on the SCL signal when it comes to line-end reflections and external noise.
   We recommend the operation be rechecked on the actual equipment.

Serial Data Transfer

Setting the S/P pin to the "VDD" level and the C86 pin to the "VSS" level allows standard clock-synchronized serial data transfer, using the chip select line (CSB), serial transfer clock line (SCL), serial input data line (SDI), and serial output data line (SDO). For a serial interface, the S8/16/ID pin function uses an ID pin. If the chip is set up for serial interface, the D15-2 pins, which are not used, must be fixed at "VDD" or "VSS".

The NT7553E initiates serial data transfer by transferring the start byte at the falling edge of CSB input. It ends serial data transfer at the rising edge of CSB input.

The NT7553E is selected when the 6-bit chip address in the start byte transferred from the transmitting device matches the 6-bit device identification code assigned to the NT7553E. The NT7553E, when selected, receives the subsequent data string. The LSB of the identification code can be determined by the ID pin. The five upper bits must be "01110". Two different chip addresses must be assigned to a single NT7553E because the seventh bit of the start byte is used as a register select bit (A0): that is, when A0 = "0", data can be written to the index register or status can be read, and when A0 = "1", an instruction can be issued or data can be written to or read from RAM. Read or write is selected according to the eighth bit of the start byte (R/W bit). The data is received when the R/W bit is "0", and is transmitted when the R/W bit is "1". After receiving the start byte, the NT7553E receives or transmits the subsequent data byte-by-byte. The data is transferred with the MSB first. All NT7553E instructions are 16 bits. Two bytes are received with the MSB first (D15 to 0), and then the instructions are internally executed. After the start byte has been received, the first byte is fetched internally as the upper eight bits of the instruction and the second byte is fetched internally as the lower eight bits of the instruction. Five bytes of RAM read data after the start byte are invalid. The NT7553E starts to read correct RAM data from the sixth byte.

Table 4. Start Byte Format

Transfer Bit	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						A0	R/W
		0	1	1	1	0	ID		

Note: The S8/16/ID pin selects ID bit.

a) Timing of basic data-transfer through clock synchronized serial interface

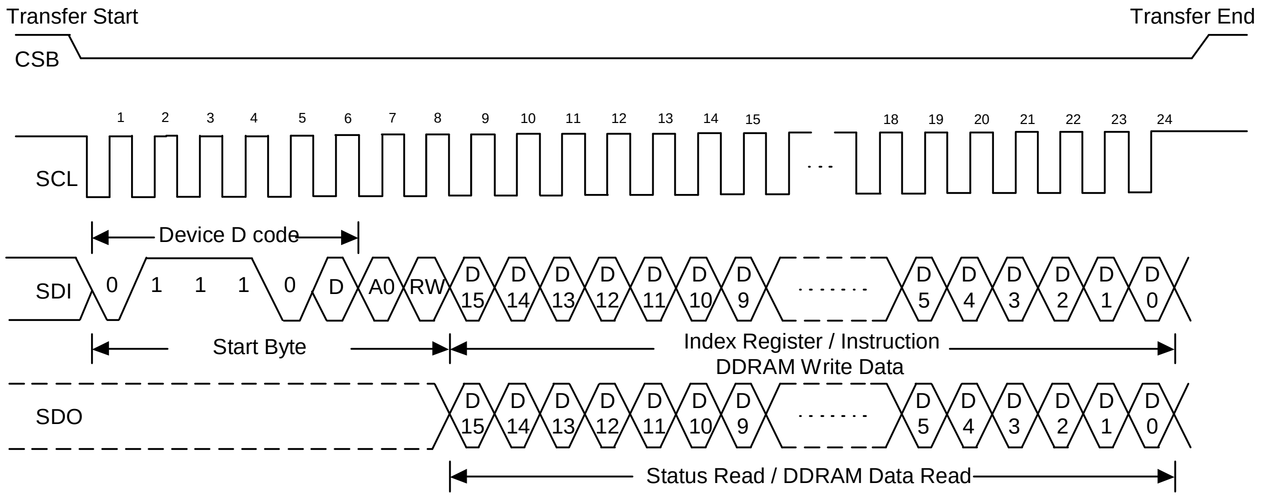


Figure 3. Procedure for transfer through the clock synchronized serial interface (a)

b) Timing of consecutive data transfer through clock synchronized serial interface

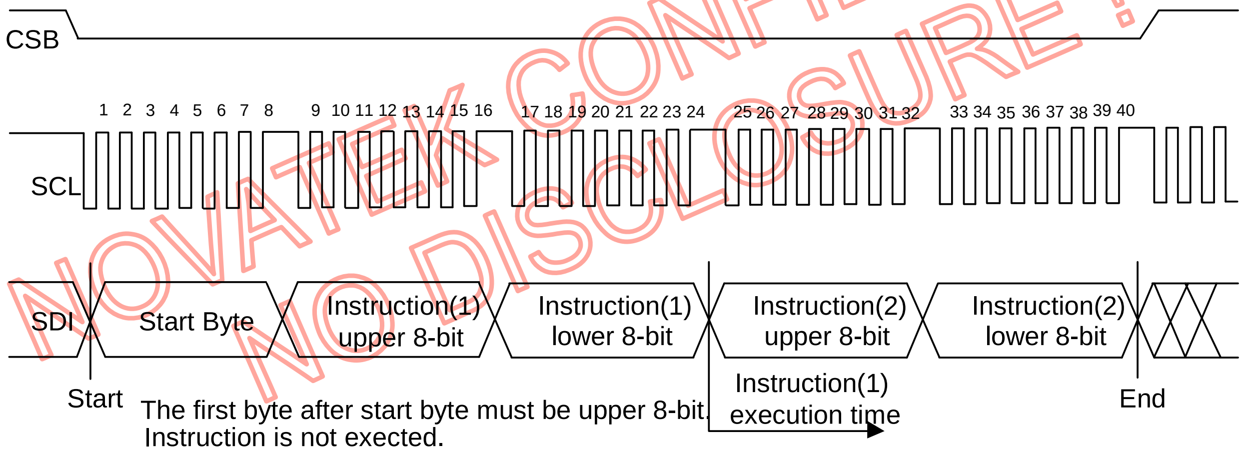
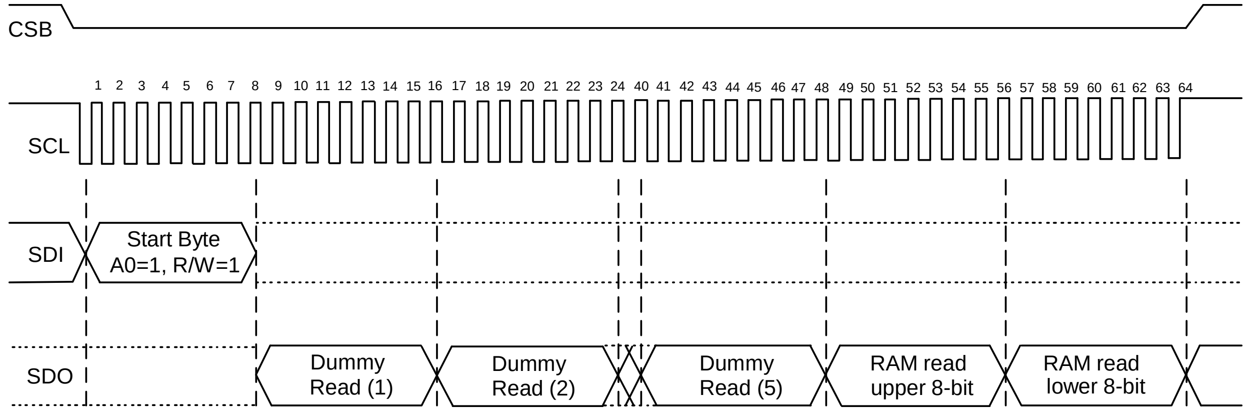


Figure 4. Procedure for transfer through the clock synchronized serial interface (b)

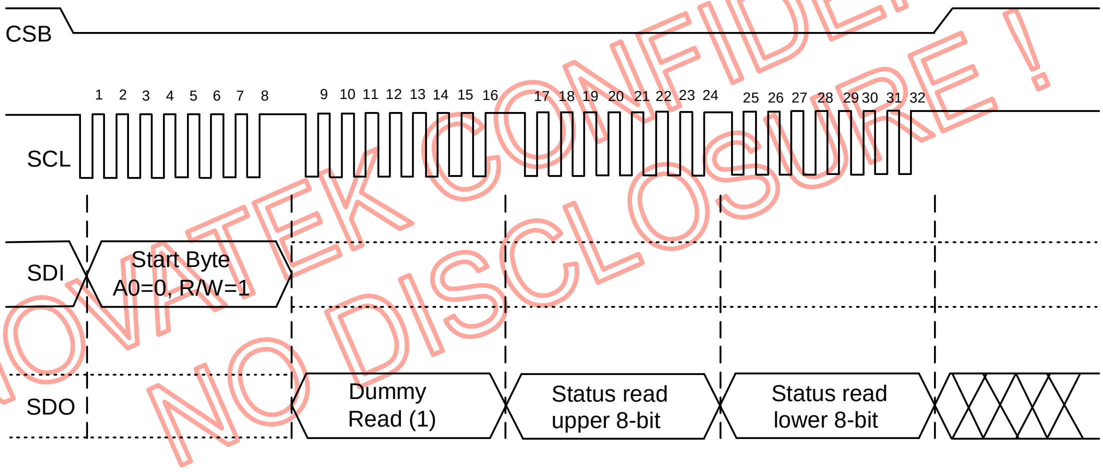
c) Transfer data read from DDRAM



Five bytes invalid dummy data are read after start byte.
6th data is valid from DDRAM.

Figure 5. Procedure for transfer through the clock synchronized serial interface (c)

d) Status Read / Instruction Read



One byte invalid dummy data is read after start byte.
2nd data is valid from DDRAM.

Figure 6. Procedure for transfer through the clock synchronized serial interface (d)

High-Speed Burst RAM Write Function

The NT7553E has a high-speed burst RAM-write function that can be used to write data to RAM in one-fourth the access time required for an equivalent standard RAM-write operation. This function is especially suitable for applications which require the high-speed rewriting of the display data, for example, display of gray animations, etc.

When the high-speed RAM-write mode (HWM) is selected, data for writing to RAM is stored once to the NT7553E internal register. When data is selected four times per word, all data is written to the on-chip RAM. While this is taking place, the next data can be written to an internal register so that high-speed and consecutive RAM writing can be executed for animated displays, etc.

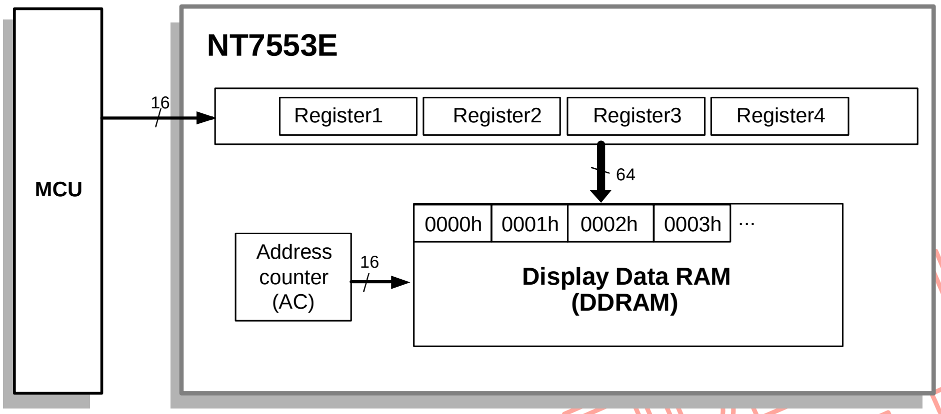


Figure 7. High-Speed Burst RAM Write Function

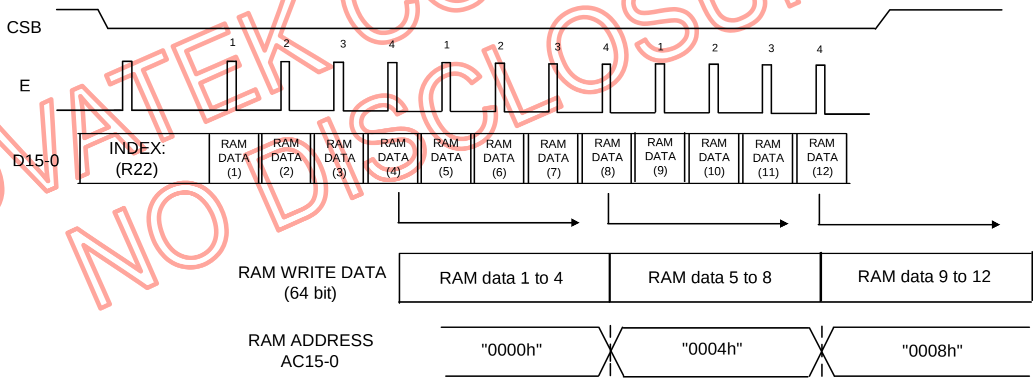


Figure 8. High-Speed Burst RAM Write timing

Note the following when using high-speed RAM write mode.

1. The lower two bits of the address must be set in the following way in high-speed write mode. When D0 becomes 0, the lower two bits of the address must be set to "11". When D1 becomes 1, the lower two bits of the address must be set to "00".
2. When a high-speed RAM write is canceled, the next instruction must only be executed after the RAM write execution time has elapsed.
3. The logical and compare operation cannot be used.

4. Data is written to RAM for each four words. When an address is set, the lower two bits in the address must be set to the following values.
   *When I/D0=0, the lower two bits in the address must be set to “11” and be written to RAM.
   *When I/D0=1, the lower two bits in the address must be set to “00” and be written to RAM.
5. Data is written to RAM for each four words. If less than four words of data are written to RAM, the last data will not be written to RAM.
6. When the index register and RAM data write (“22”h) have been selected, the data is always written first. RAM cannot be written to and read from at the same time. HWM must be set to “0” while RAM is being read.
7. High-speed and normal RAM write operations cannot be executed at the same time. The mode must be switched and the address must then be set.
8. When high-speed RAM write is used with a window address-range specified, dummy write operation may be required to suit the window address range-specification. Refer to the High-Speed RAM Write in the Window Address section.

Table 5. Comparisons between Normal and High-Speed RAM Write Operations

	Normal RAM Write (HWM=0)	**High-Speed RAM Write (HWM=1)**
Logical operation function	Can be used	Can’t be used
Compare operation function	Can be used	Can’t be used
Write mask function	Can be used	Can be used
RAM address set	Can be specified by word	ID0 bit=0: Set the lower two bits to 11 ID0 bit=1: Set the lower two bits to 00
RAM read	Can be read by word	Cannot be used
RAM write	Can be written by word	Dummy write operations may have to be inserted according to a window address range specification
Window address	Can be set by word	Can be set by four words

High-Speed RAM Write in the Window Address

When a window address range is specified, RAM data which is in an optional window area can be rewritten consecutively and quickly by inserting dummy write operations so that RAM access counts become 4N as shown in the tables below.

Dummy write operations may have to be inserted as the first or last operations for a row of data, depending on the horizontal window-address range specification bits (HSA1 to 0, HEA1 to 0). The number of dummy write operations of a row must be 4N.

Table 6. Number of Dummy Write Operations in High-Speed RAM Write (HSA Bits)

HSA1	HSA0	Number of Dummy Write Operations to be Inserted at the Start of a Row
0	0	0
0	1	1
1	0	2
1	1	3

Table 7. Number of Dummy Write Operations in High-Speed RAM Write (HEA Bits)

HEA1	HEA0	Number of Dummy Write Operations to be Inserted at the End of a Row
0	0	3
0	1	2
1	0	1
1	1	0

Each row of access must consist of 4 x N operations, including the dummy writes.
Horizontal access count = first dummy write count + write data count + last dummy write count = 4 x N

An example of high-speed RAM write with a window address-range specified is shown below.
The window address-range can be rewritten consecutively and quickly by inserting two dummy writes at the start of a row and three dummy writes at the end of a row, as determined by using the window address-range specification bits (HSA1 to 0 = “10”, HEA1 to 0 =“00”).

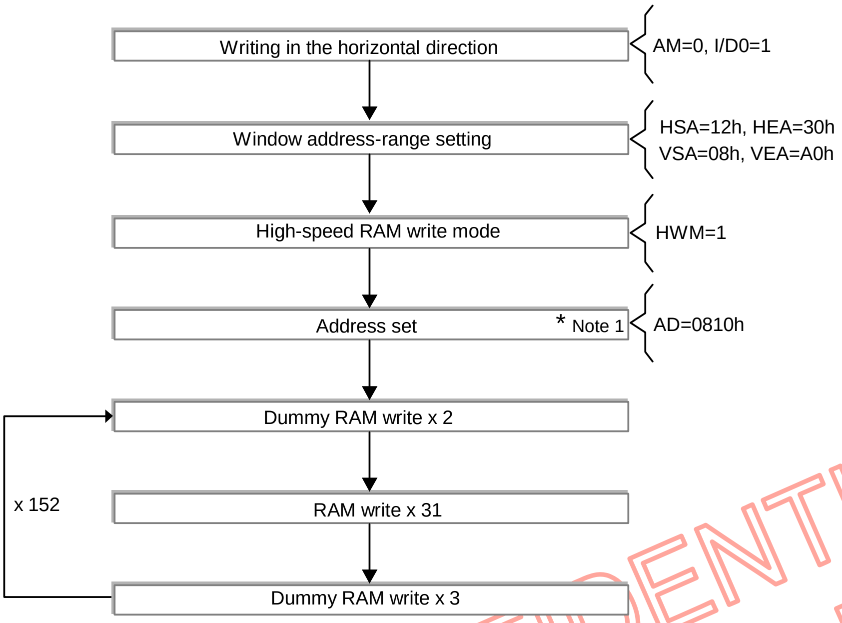
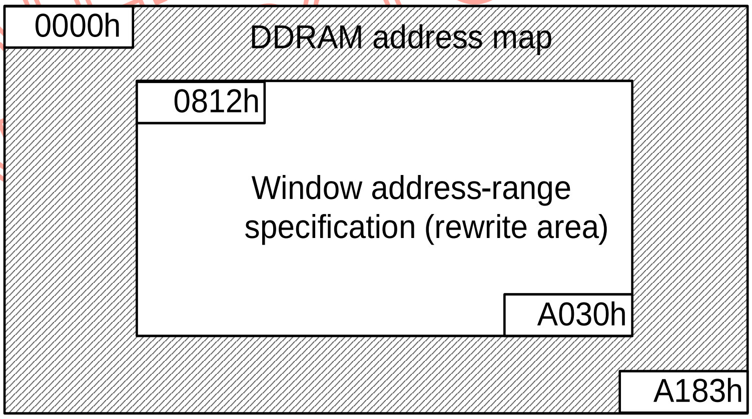


Figure 9. High-Speed Burst RAM with a window mask write

*Note1The address set for the high-speed RAM write must be 00 or 11 according to the value of I/D0 bit. Only RAM in the specified window address-range will be overwritten.



Window address-range setting
HSA=12h, HEA=30h
VSA=08h, VEA=A0h

Figure 10. Example of the High-Speed RAM write with a window address-range specification

Window Address Function

When data is written to the on-chip DDRAM, a window address-range that is specified by the horizontal address register (start: HSA[7:0], end: HEA[7:0]) or the vertical address register (start: VSA[7:0], end: VEA[7:0]) can be written consecutively.

Data is written to addresses in the direction specified by the AM bit (increment/decrement). When image data, etc. is being written, data can be written consecutively without thinking a data wrap by doing this. The window must be specified to be within the DDRAM address area described below. Addresses must be set within the window address.

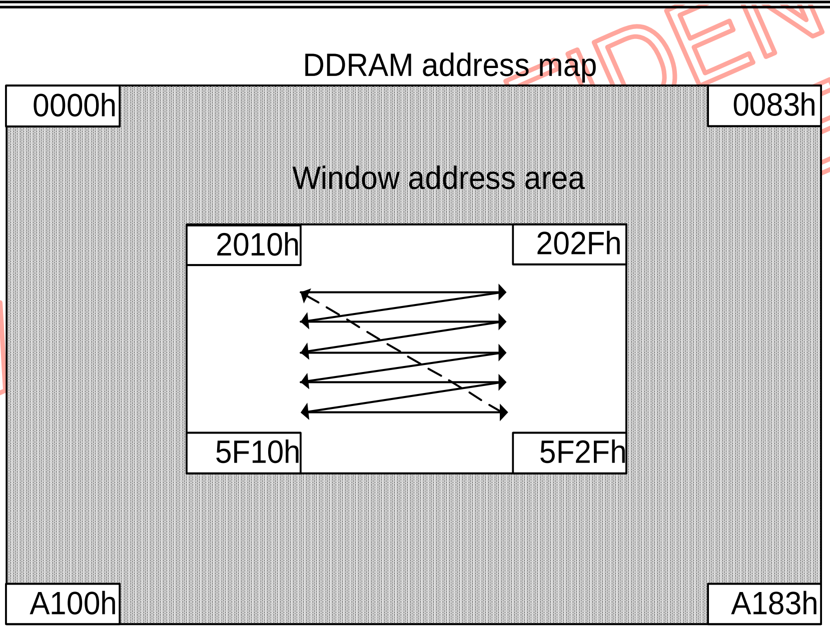
[Restriction on window address-range settings]

(Horizontal direction) 00h ≤ HSA[7:0] ≤ HEA[7:0] ≤ 83h
(Vertical direction) 00h ≤VSA[7:0] ≤ VEA[7:0] ≤ A1h

[Restriction on address settings during the window address]

(RAM address) HSA[7:0] ≤ AD[7:0] ≤ HEA[7:0]
VSA[7:0] ≤ AD[15:8] ≤ VEA[7:0]

Note: In high-speed RAM-write mode, the lower two bits of the address must be set as shown below according to the value of the ID0 bit.
ID0 = 0: The lower two bits of the address must be set to “11”.
ID0 = 1: The lower two bits of the address must be set to “00”.



I/D0=1 (increment)
AM=0 (horizontal writing)
Window address-range specification area
HSA5-0=10h, HSE5-0=2Fh
VSA7-0=20h, VEA7-0=5Fh

Figure 11. Example of Address Operation in the Window Address Specification

Display Data RAM (DDRAM)

The display data RAM stores the segment data for the display. It has 162 x 396 x 5 bit structure for 32 gray scale levels.

DDRAM Address Map

Table 8. Relationship between Display Position and DDRAM Address

		Horizontal Address	00h	01h	02h	03h	...	80h	81h	82h	83h
		SGS=0	SEG1 SEG2 SEG3	SEG4 SEG5 SEG6	SEG7 SEG8 SEG9	SEG10 SEG11 SEG12	...	SEG385 SEG386 SEG387	SEG388 SEG389 SEG390	SEG391 SEG392 SEG393	SEG394 SEG395 SEG396
		SGS=1	SEG396 SEG395 SEG394	SEG393 SEG392 SEG391	SEG390 SEG389 SEG387	SEG386 SEG385 SEG384	...	SEG12 SEG11 SEG10	SEG9 SEG8 SEG7	SEG6 SEG5 SEG4	SEG3 SEG2 SEG1
CMS=0	CMS=1	Vertical Address	D15 ~ D0	D15 ~ D0	D15 ~ D0	D15 ~ D0	...	D15 ~ D0	D15 ~ D0	D15 ~ D0	D15 ~ D0
COM1	COM162	00h	0000h	0001h	0002h	0003h	...	0080h	0081h	0082h	0083h
COM2	COM161	01h	0100h	0101h	0102h	0103h	...	0180h	0181h	0182h	0183h
COM3	COM160	02h	0200h	0201h	0202h	0203h	...	0280h	0281h	0282h	0283h
COM4	COM159	03h	0300h	0301h	0302h	0303h	...	0380h	0381h	0382h	0383h
COM5	COM158	04h	0400h	0401h	0402h	0403h	...	0480h	0481h	0482h	0483h
COM6	COM157	05h	0500h	0501h	0502h	0503h	...	0580h	0581h	0582h	0583h
COM7	COM156	06h	0600h	0601h	0602h	0603h	...	0680h	0681h	0682h	0683h
COM8	COM155	07h	0700h	0701h	0702h	0703h	...	0780h	0781h	0782h	0783h
COM9	COM154	08h	0800h	0801h	0802h	0803h	...	0880h	0881h	0882h	0883h
COM10	COM153	09h	0900h	0901h	0902h	0903h	...	0980h	0981h	0982h	0983h
⋮	⋮	⋮	⋮	⋮	⋮	⋮	...	⋮	⋮	⋮	⋮
COM159	COM4	9Eh	9E00h	9E01h	9E02h	9E03h	...	9E80h	9E81h	9E82h	9E83h
COM160	COM3	9Fh	9F00h	9F01h	9F02h	9F03h	...	9F80h	9F81h	9F82h	9F83h
COM161	COM2	A0h	A000h	A001h	A002h	A003h	...	A080h	A081h	A082h	A083h
COM162	COM1	A1h	A100h	A101h	A102h	A103h	...	A180h	A181h	A182h	A183h

Table 9. Relationship between DDRAM data and Segment output pin

DDRAM Data	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Selected Palette	PK palette					PK palette					0	PK palette				
Output Pin	SEG (3n+1)					SEG (3n+2)					0	SEG (3n+3)				
Output Pin	SEG (396-3n)					SEG (395-3n)					0	SEG (394-3n)				

Note: 1. n=Lower 8 bits address (00h ~83h)

2. **D5** is dummy bit must fixed this bit to **"0"**.

Bit Operation

The NT7553E supports the following functions. A write data mask function that selects data into the display data RAM in bit units, and a logic operation function that performs logic operations or conditional determination on the display data set in the RAM and writes into the RAM. With the 16-bit bus interface, these functions can greatly reduce the processing load of the MPU graphics software for the display data in the RAM at high speed. For details, see the Graphics Operation Function section.

Graphic Operation Function

The NT7553E can greatly reduce the load of the microcomputer graphics software processing through the 16-bit bus architecture and internal graphics-bit operation function. This function supports the following:

1. A write data mask function that selectively rewrites some of the bits in the 16-bit write data.
2. A conditional write function that compares the write data and compares-bit data and writes the data sent from the microcomputer only when the conditions match. Even if the display size is large, the display data in the display data RAM (DDRAM) can be quickly rewritten. The graphics bit operation can be controlled by combining the entry mode register. The bit set value of the RAM-write-data mask register, and the write from the microcomputer.

Table 10. Graphics Operation

Operation Mode	Bit Setting			Operation and Usage
	I/D	AM	LG[2:0]	
Write mode 1	0/1	0	000	Horizontal data replacement, horizontal-border drawing
Write mode 2	0/1	1	000	Vertical data replacement, vertical-border drawing
Write mode 3	0/1	0	110,111	Conditional horizontal data replacement, horizontal-border drawing
Write mode 4	0/1	1	110,111	Conditional vertical data replacement, vertical-border drawing

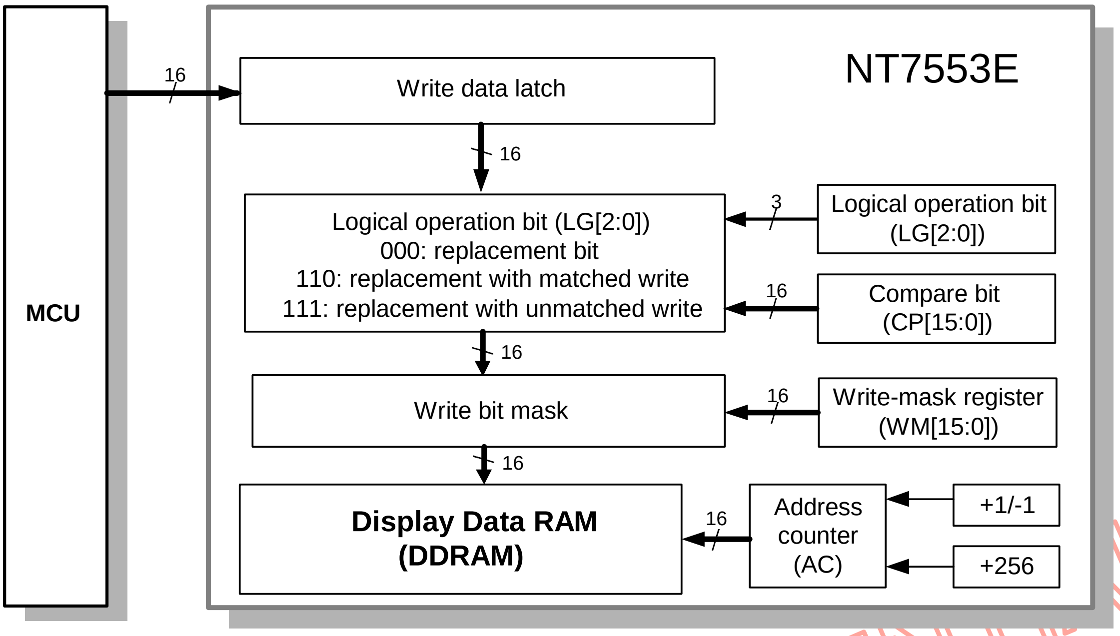


Figure 12. Graphics Operation Flow

Write-data Mask Function

The NT7553E has a bit-wise write-data mask function that controls writing the 16-bit data from the microcomputer to the DDRAM. Bits that are "0" in the write-data mask register (WM [15:0]) cause the corresponding D bit to be written to the DDRAM. Bits that are "1" prevent writing to the corresponding DDRAM bit to the DDRAM; the data in the DDRAM is retained. This function can be used when only one dot data is rewritten or the particular display gray level is selectively rewritten.

Table 11. Write-data Mask Function Operation

Interface data bus	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	P04	P03	P02	P01	P00	P14	P13	P12	P11	P10	0	P24	P23	P22	P21	P20
Write mask register	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	1	1	1	1	1	0	0	0	0	0	0	1	1	0	0	0
DDRAM data	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	*	*	*	*	*	P14	P13	P12	P11	P10	0	*	*	P22	P21	P20

*** D5** is dummy bit must fixed this bit to **"0"**.

Graphics Operation Processing

1. Write mode 1: AM = 0, LG [2:0] = “000”

This mode is used when the data is horizontally written at high speed. It can also be used to initialize the graphics RAM (DDRAM) or to draw borders. The write-data mask function (WM [15:0]) is also enabled in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster below after it has reached the left or right edge of the DDRAM.

Operation Examples:

1) I/D =1, AM=0, LG[2:0]=000
2) WM[15:0]=07FFH
3) AC=0000H

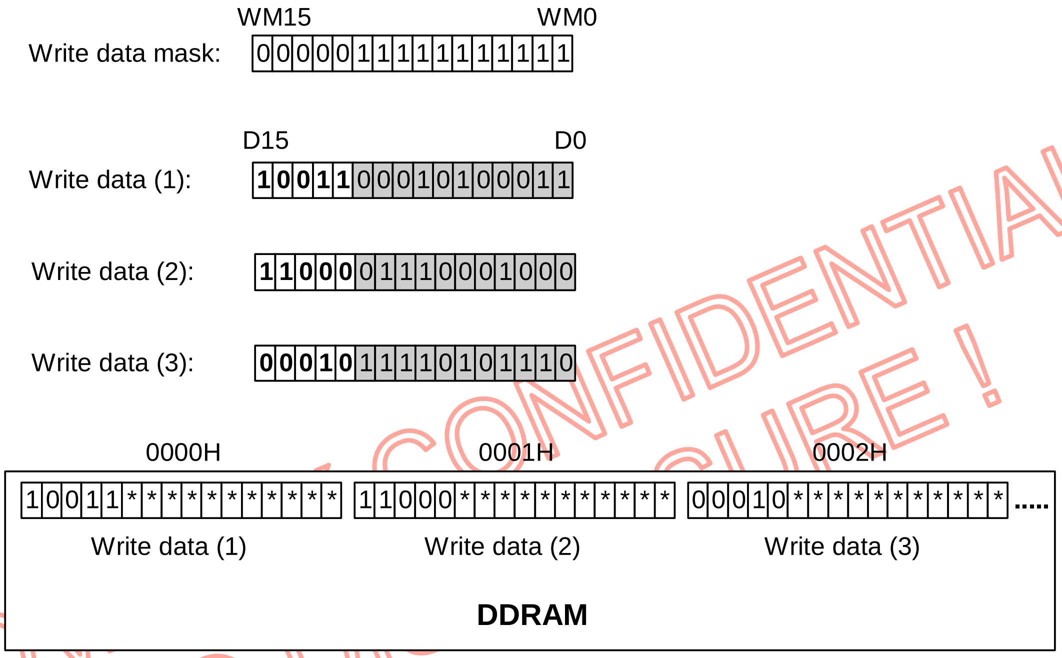


Figure 13. Writing Operation of Write Mode 1

2. Write mode 2: AM = 1, LG [2:0] = “000”

This mode is used when the data is vertically written at high speed. It can also be used to initialize the DDRAM, develop the font pattern in the vertical direction, or draw borders. The write-data mask function (WM [15:0]) is also enabled in these operations. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D =1) or upper left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the DDRAM.

Operation Examples:

1) I/D =1, AM=0, LG[2:0]=000
2) WM[15:0]=07FFH
3) AC=0000H

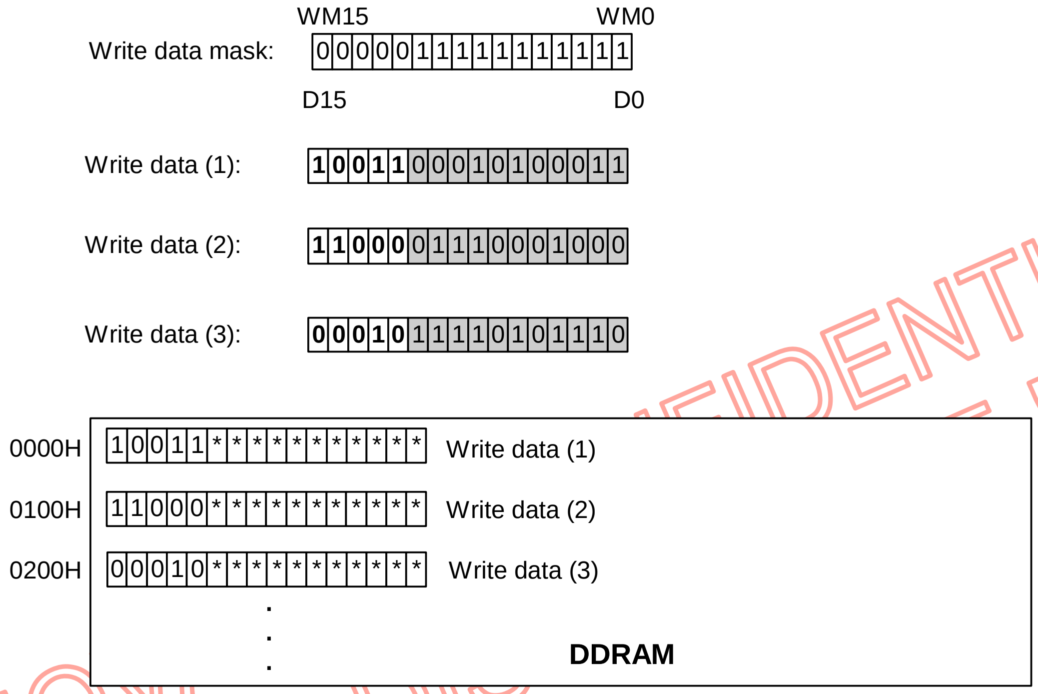


Figure 14. Operation of Write Mode 2

3. Write mode 3: AM = 0, LG [2:0] = 110/111

This mode is used when the data is horizontally written by comparing the write data and the set value of the compare register (CP [7:0]). When the result of the comparison in a byte unit satisfies the condition write-data mask function (WM [15:0]) is also enabled. After writing, the address counter (AC) automatically increments by 1 (I/D =1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-raw below after it has reached the left or right edge of the DDRAM.

Operation Examples:

1) I/D =1, AM=0, LG[2:0]=110 (Matched Write)
2) CP[15:0]=2860H
3) WM[15:0]=0000H
3) AC=0000H

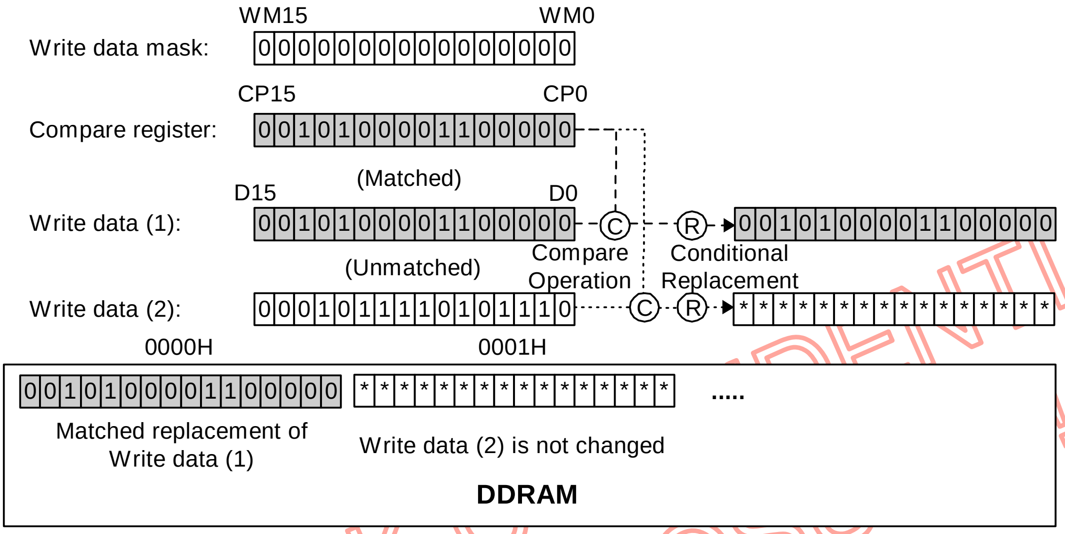


Figure 15. Operation of Write Mode 3

4. Write mode 4: AM = 1, LG [2:0] = 110/111

This mode is used when a vertical comparison is performed between the write data and the set value of the compare register (CP [15:0]) to write the data. When the result by the comparison in a byte unit satisfies the condition, the write data sent from the microcomputer is written to the DDRAM. In this operation, write data mask function (WM [15:0]) is also enabled. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the DDRAM.

Operation Examples:
1) I/D =1, AM=1, LG[2:0]=111 (Unmatched Write)
2) CP[15:0]=2860H
3) WM[15:0]=0000H
3) AC=0000H

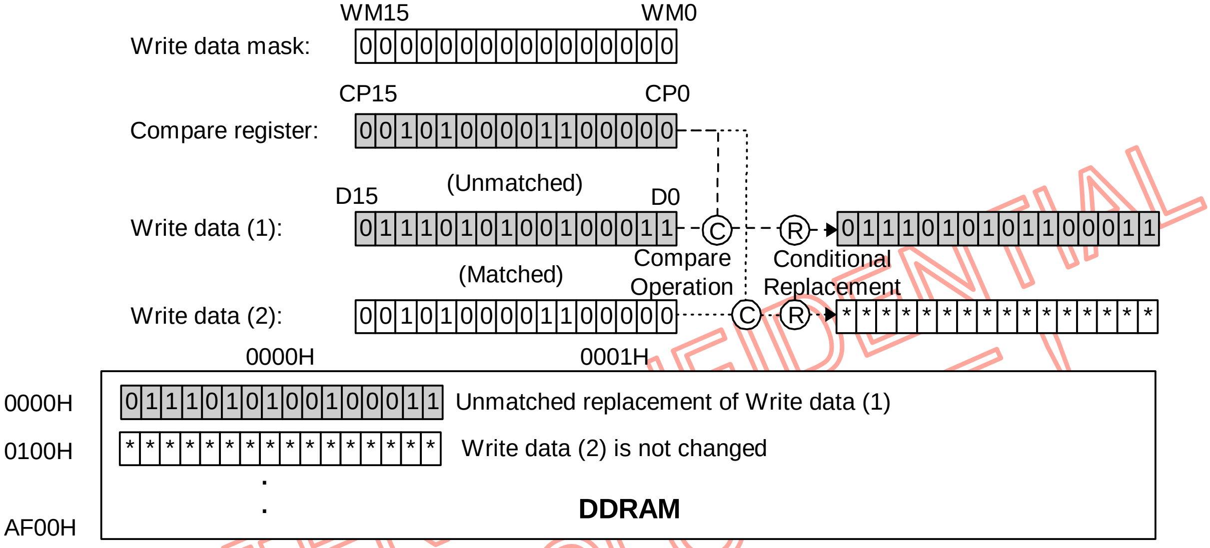


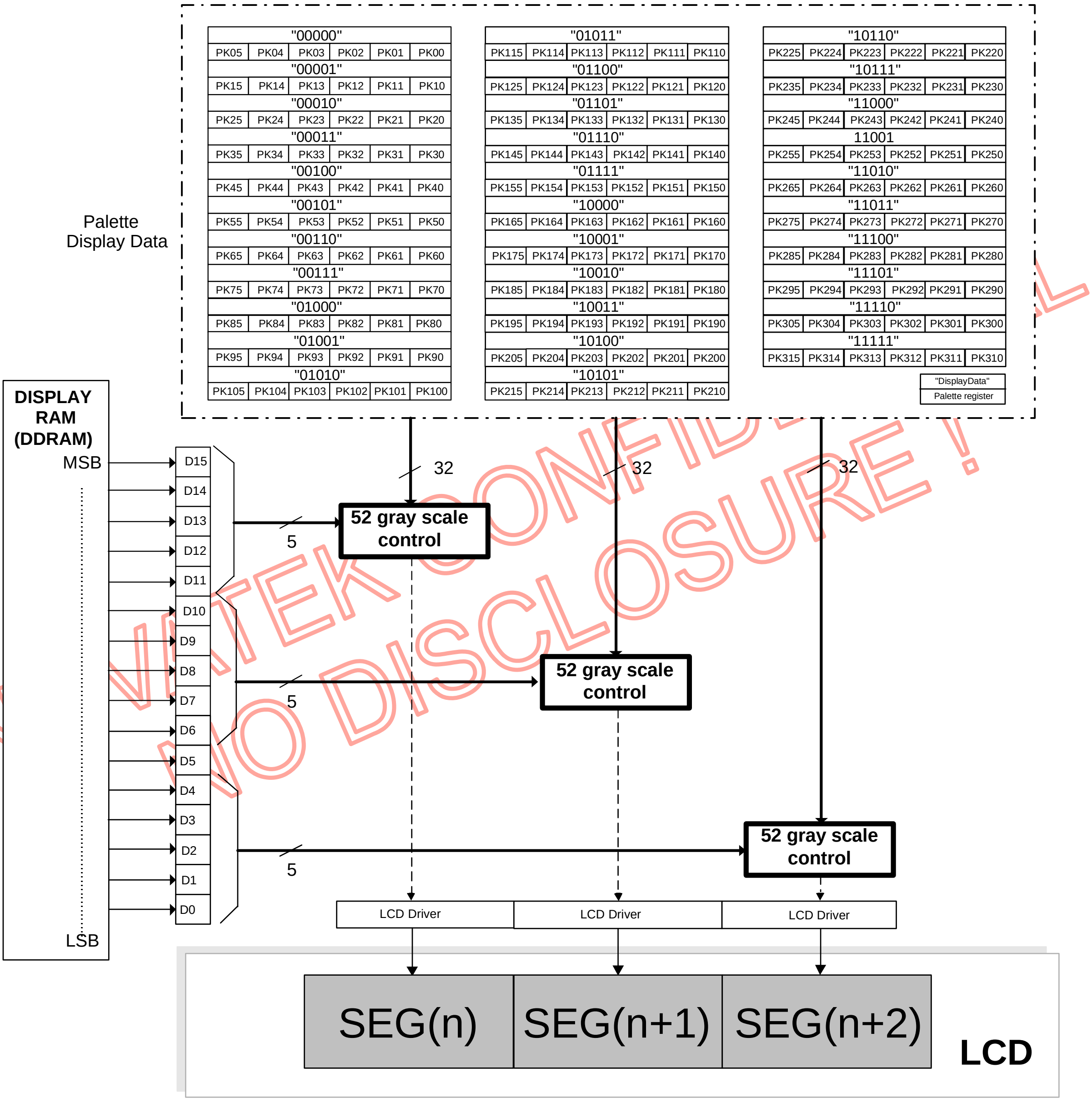
Figure 16. Writing Operation of Write Mode 4

Grayscale Palette

The NT7553E incorporates a grayscale palette to simultaneously display 32-grayscale of the 52-grayscale possible levels. The grayscales consist of 32 6-bit palettes. The 52-stage grayscale levels can be selected from the 6-bit palette data.

For the display data, the four-bit data in the DDRAM written from the microcomputer is used.

In this palette, a pulse-width control system (PWM) is used to eliminate flickers in the LCD display. The time over which the LCD is switched on is adjusted according to the level and grayscales are displayed so that flicker is reduced and grayscales are clearly displayed.



"00000"	PK05	PK04	PK03	PK02	PK01	PK00
"00001"	PK15	PK14	PK13	PK12	PK11	PK10
"00010"	PK25	PK24	PK23	PK22	PK21	PK20
"00011"	PK35	PK34	PK33	PK32	PK31	PK30
"00100"	PK45	PK44	PK43	PK42	PK41	PK40
"00101"	PK55	PK54	PK53	PK52	PK51	PK50
"00110"	PK65	PK64	PK63	PK62	PK61	PK60
"00111"	PK75	PK74	PK73	PK72	PK71	PK70
"01000"	PK85	PK84	PK83	PK82	PK81	PK80
"01001"	PK95	PK94	PK93	PK92	PK91	PK90
"01010"	PK105	PK104	PK103	PK102	PK101	PK100
"01011"	PK115	PK114	PK113	PK112	PK111	PK110
"01100"	PK125	PK124	PK123	PK122	PK121	PK120
"01101"	PK135	PK134	PK133	PK132	PK131	PK130
"01110"	PK145	PK144	PK143	PK142	PK141	PK140
"01111"	PK155	PK154	PK153	PK152	PK151	PK150
"10000"	PK165	PK164	PK163	PK162	PK161	PK160
"10001"	PK175	PK174	PK173	PK172	PK171	PK170
"10010"	PK185	PK184	PK183	PK182	PK181	PK180
"10011"	PK195	PK194	PK193	PK192	PK191	PK190
"10100"	PK205	PK204	PK203	PK202	PK201	PK200
"10101"	PK215	PK214	PK213	PK212	PK211	PK210
"10110"	PK225	PK224	PK223	PK222	PK221	PK220
"10111"	PK235	PK234	PK233	PK232	PK231	PK230
"11000"	PK245	PK244	PK243	PK242	PK241	PK240
11001	PK255	PK254	PK253	PK252	PK251	PK250
"11010"	PK265	PK264	PK263	PK262	PK261	PK260
"11011"	PK275	PK274	PK273	PK272	PK271	PK270
"11100"	PK285	PK284	PK283	PK282	PK281	PK280
"11101"	PK295	PK294	PK293	PK292	PK291	PK290
"11110"	PK305	PK304	PK303	PK302	PK301	PK300
"11111"	PK315	PK314	PK313	PK312	PK311	PK310

Figure 17. Grayscale Palette Control

Grayscale Palette Table

The grayscale register that is set for each palette register (PK) can be set to any level. 52-grayscale lighting levels can be set according to palette values (“000000” to “110100”).

Table 12. Grayscale Control Level

Palette Register Value (PK)						Value	Grayscale Control Level
0	0	0	0	0	0	00h	All off level
0	0	0	0	0	1	01h	1/52 level
0	0	0	0	1	0	02h	2/52 level
0	0	0	0	1	1	03h	3/52 level
0	0	0	1	0	0	04h	4/52 level
0	0	0	1	0	1	05h	5/52 level
0	0	0	1	1	0	06h	6/52 level
0	0	0	1	1	1	07h	7/52 level
0	0	1	0	0	0	08h	8/52 level
0	0	1	0	0	1	09h	9/52 level
0	0	1	0	1	0	0Ah	10/52 level
0	0	1	0	1	1	0Bh	11/52 level
0	0	1	1	0	0	0Ch	12/52 level
0	0	1	1	0	1	0Dh	13/52 level
0	0	1	1	1	0	0Eh	14/52 level
0	0	1	1	1	1	0Fh	15/52 level
0	1	0	0	0	0	10h	16/52 level
0	1	0	0	0	1	11h	17/52 level
0	1	0	0	1	0	12h	18/52 level
0	1	0	0	1	1	13h	19/52 level
0	1	0	1	0	0	14h	20/52 level
0	1	0	1	0	1	15h	21/52 level
0	1	0	1	1	0	16h	22/52 level
0	1	0	1	1	1	17h	23/52 level
0	1	1	0	0	0	18h	24/52 level
0	1	1	0	0	1	19h	25/52 level
0	1	1	0	1	0	1Ah	26/52 level
0	1	1	0	1	1	1Bh	27/52 level
0	1	1	1	0	0	1Ch	28/52 level
0	1	1	1	0	1	1Dh	29/52 level
0	1	1	1	1	0	1Eh	30/52 level
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	0	1	1	1	0	2Eh	46/52 level
1	0	1	1	1	1	2Fh	47/52 level
1	1	0	0	0	0	30h	48/52 level
1	1	0	0	0	1	31h	49/52 level
1	1	0	0	1	0	32h	50/52 level
1	1	0	0	1	1	33h	51/52 level
1	1	0	1	0	0	34h	All on level

Display data and Grayscale level

Table 13. Display data and output level

Display data	Output level
00000	PK0
00001	PK1
00010	PK2
00011	PK3
00100	PK4
00101	PK5
00110	PK6
00111	PK7
01000	PK8
01001	PK9
01010	PK10
01011	PK11
01100	PK12
01101	PK13
01110	PK14
01111	PK15
10000	PK16
10001	PK17
10010	PK18
10011	PK19
10100	PK20
10101	PK21
10110	PK22
10111	PK23
11000	PK24
11001	PK25
11010	PK26
11011	PK27
11100	PK28
11101	PK29
11110	PK30
11111	PK31

Address Counter (AC)

The address counter (AC) assigns an address to the data display RAM. When an address set instruction is written into the IR, the address information is sent from the IR to the AC. After writing into the RAM, the AC is automatically incremented by 1 (or decremented by 1). After reading from the RAM, the AC is not updated.

PWM Control Circuit

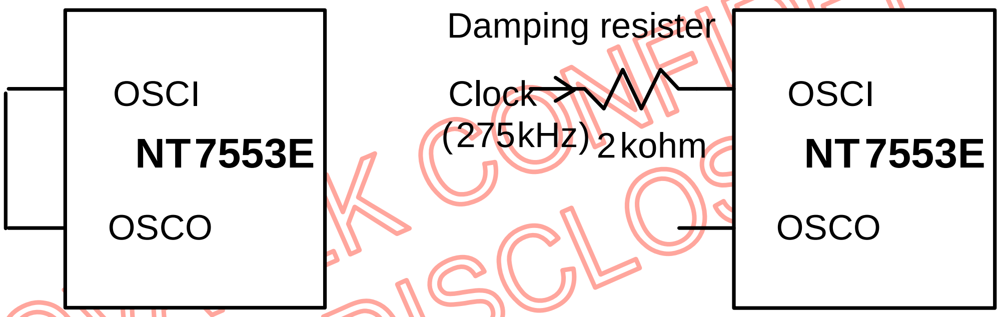
The grayscale palette generates a PWM signal for segment pins, which corresponds to the specified grayscale level. Any 32-grayscale out of the 52-grayscale possible levels can be displayed simultaneously.

Display Data Latch

The display data latch circuit is a latch that temporarily stores the display data that is output to the liquid crystal driver circuit from the display data RAM.

Oscillation Circuit

The NT7553E can set internal oscillate mode and external clock mode, when use internal oscillate mode, OSCI must connect to OSCO to set R-C start oscillation and select oscillation frequency by R0B command .



1) Internal oscillator mode

2) External clock mode

Figure 18. Oscillation Circuits

The relationship between the SEG and COM output levels is as shown in the following figure. While the display is off, SEG and COM outputs go to VSS level.

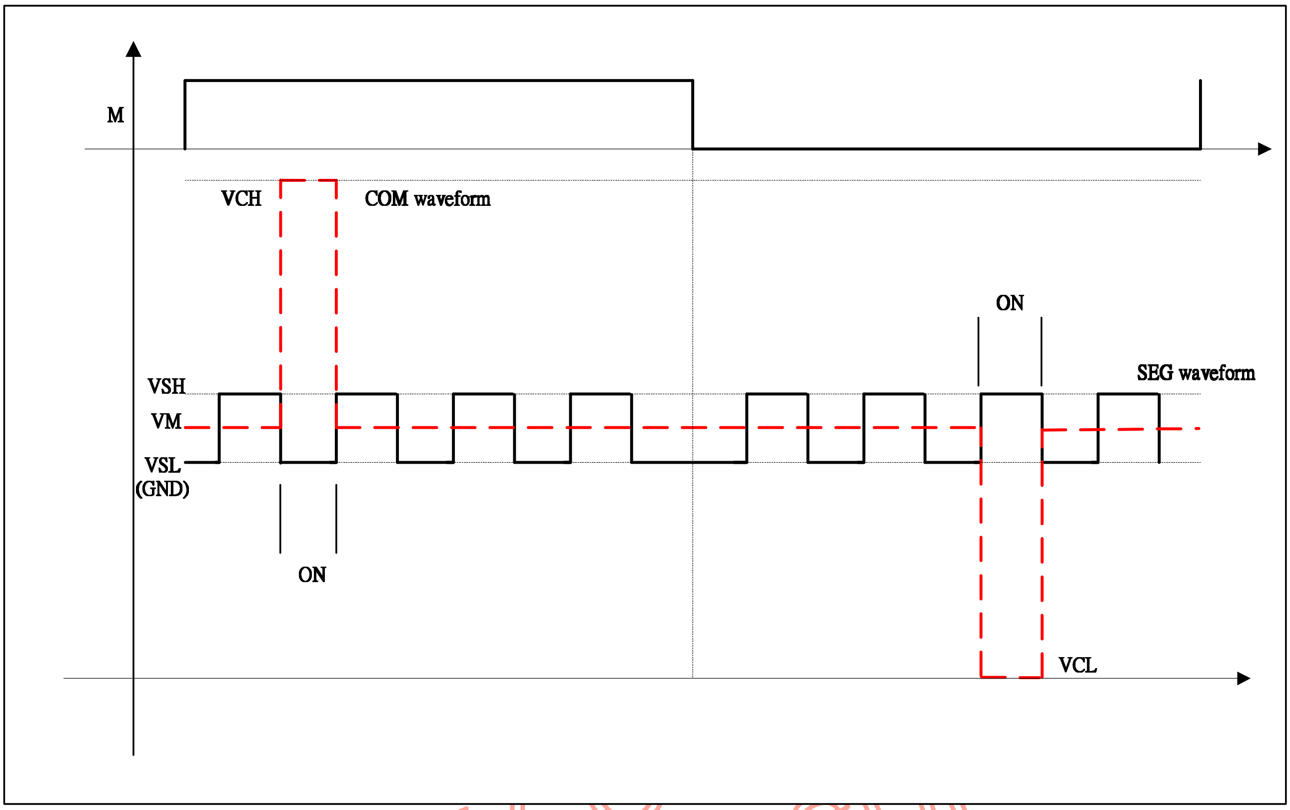


Figure 19. Relationship with SEG/COM output level

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 162 common signal drivers (COM1 to COM162) and 396 segment signal drivers (SEG1 to SEG396). Display pattern data from display data RAM is latched to the 396-bit latch circuit. The latched data then enables the segment signal drivers to generate drive waveform outputs. The common driver outputs one of the VCH, VM or VCL voltage level. The SGS bit can change the shift direction of 396-bit data for the segment. The CMS bit can also change the shift direction for the common by selecting an appropriate direction for the device-mounting configuration. When display is off, or during the standby or sleep mode, all the above common and segment signal drivers output the VSS level, halting the display.

LCD drive power supply circuit

LCD drive power supply circuit generates VCH, VSH, VM and VCL voltage level to drive the LCD panel.

Display Timing Generator Circuit

The display timing generator circuit generates the timing signal to the display data latch circuit using the system clock. The display data is latched into the display data latch circuit synchronized with the display clock, and is output to the data driver output terminal. Reading to the display data liquid crystal driver circuits is completely independent of access to the display data RAM by the MPU.
Moreover, the display timing generator circuit generates a drive waveform using an alternating current drive method that is determined by N -Line Inversion command for the liquid crystal drive circuit.

Common Output Control Circuit

This circuit controls the relationship between the number of common output and specified duty ratio.
Common output mode select instruction specifies the scanning direction of the common output pads.

Sleep Mode

Setting the sleep mode bit (SLP) to “1” puts the NT7553E in the sleep mode, where the device stops all internal display operations, thus reducing current consumption. Specifically, LCD operation is completely halted. Here, all the SEG (SEG1 to SEG396) and COM (COM1 to COM162) pins output the “VSS” level, resulting in no display. If the AP [1:0] bits in the power control register are set to “00” in the sleep mode, the LCD drive power supply can be turned off, reducing the total current consumption of the LCD module.

Table 14. Comparisons of Sleep Mode and Standby Mode

Function	Sleep Mode (SLP = 1)	Standby Mode (STB = 1)
LCD control	Turned off	Turned off
Oscillation circuit	Operates normally	Operation stopped

Standby Mode

Setting the standby mode bit (STB) to “1” puts the NT7553E in the standby mode, where the device stops completely, halting all internal operations including the Oscillation circuit, thus further reducing current consumption compared to that in the sleep mode. Specifically, all the SEG (SEG1 to SEG396) and COM (COM1 to COM162) pins for the time-sharing drive output the VSS level, resulting in no display. If the AP [1:0] bits are set to “00” in the standby mode, the LCD drive power supply can bet turned off. During the standby mode, no instructions can be accepted other than the start-oscillation instruction. To cancel the standby mode, issue the start-oscillation instruction to stabilize oscillation before setting the STB bit to “0”.

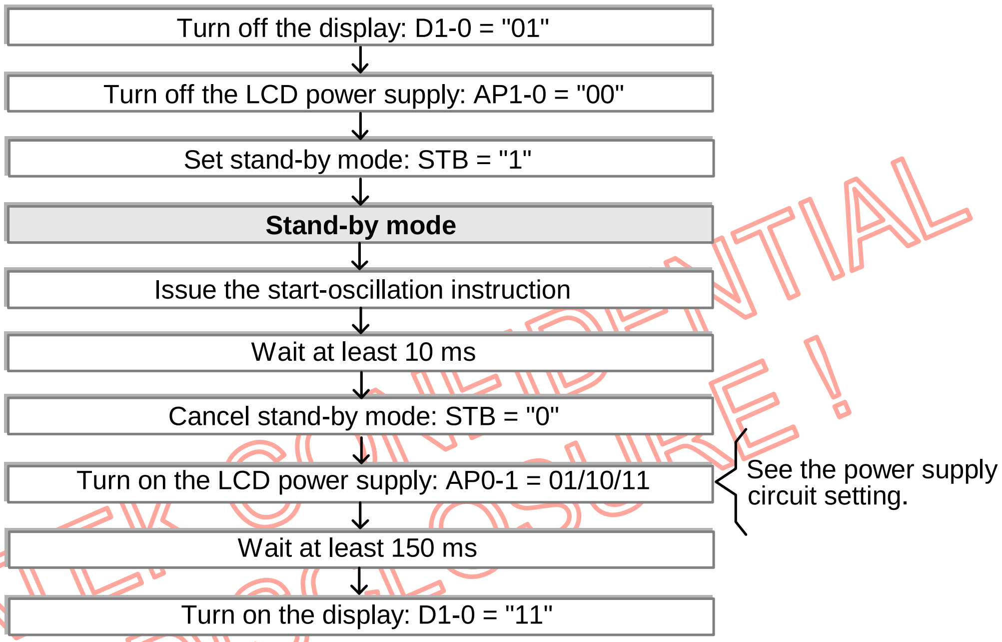


Figure 20. Procedure for Setting and Canceling Standby Mode

Setting Flows for Power Supply and Display Instruction

Power-on / off Sequence

To prevent pulse lighting of LCD screens at power-on/off, the power-on/off sequence is activated as shown below. However, since the sequence depends on LCD materials to be used, confirm the conditions by using your own system.

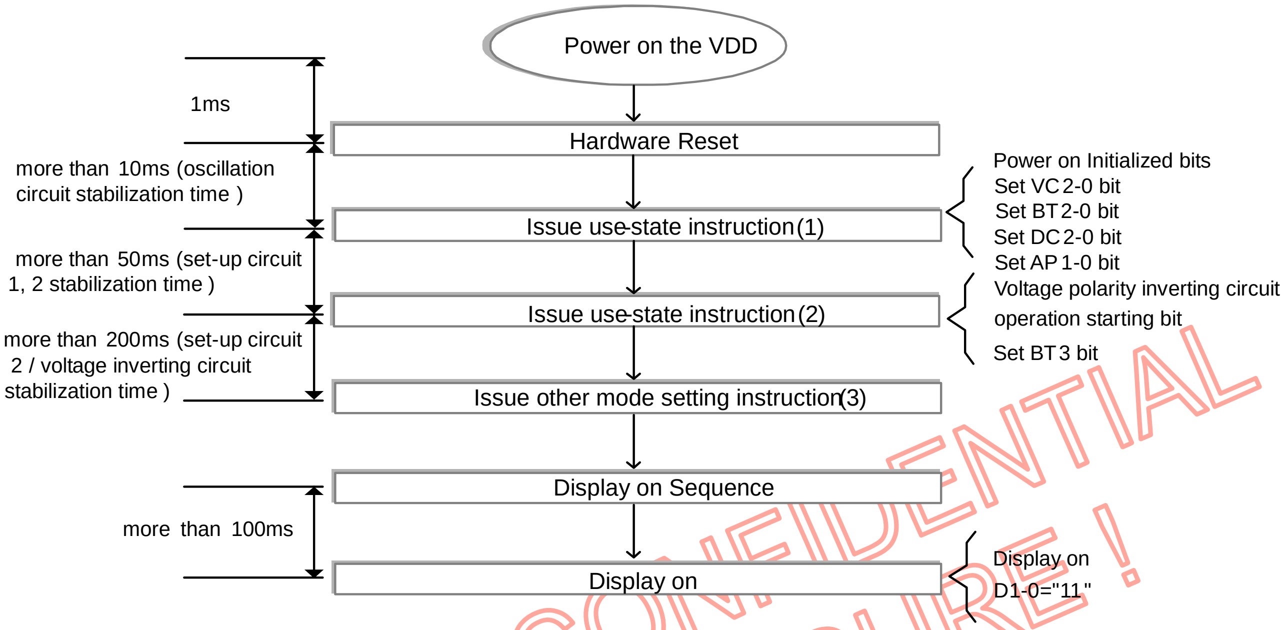


Figure 21. Power On sequence

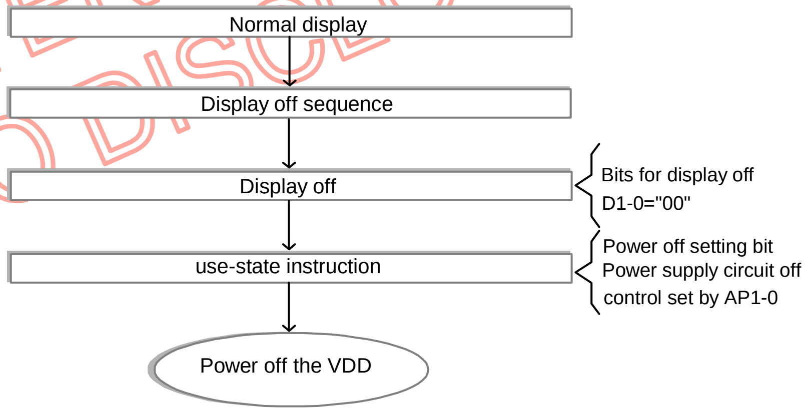


Figure 22. Power Off sequence

Power-off Sequence

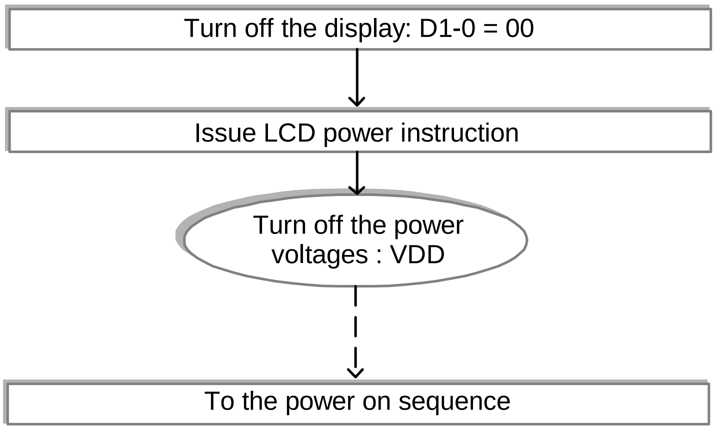


Figure 23. Normal case

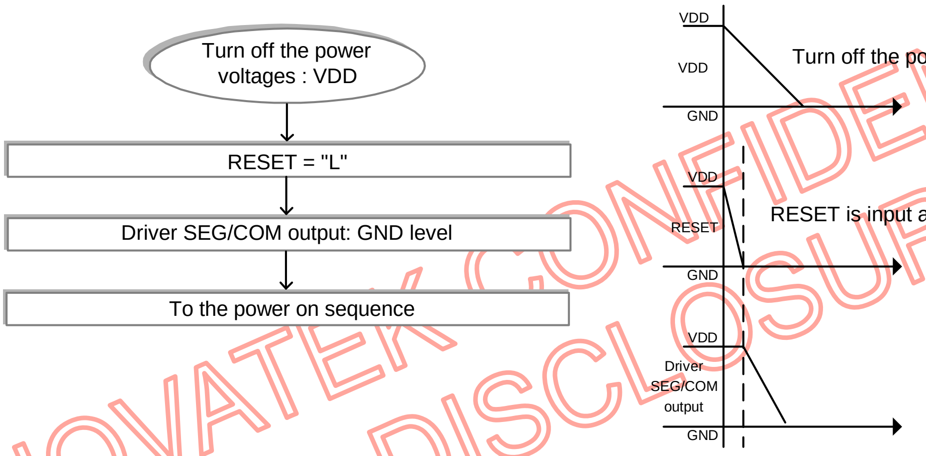


Figure 24. Emergency case

Note: When hardware reset is input during the power-off period, the D1-0 bits are cleared to "00" and SEG/COM output is forcibly lowered to the VSS levels.

Partial Sequence Setting Flow

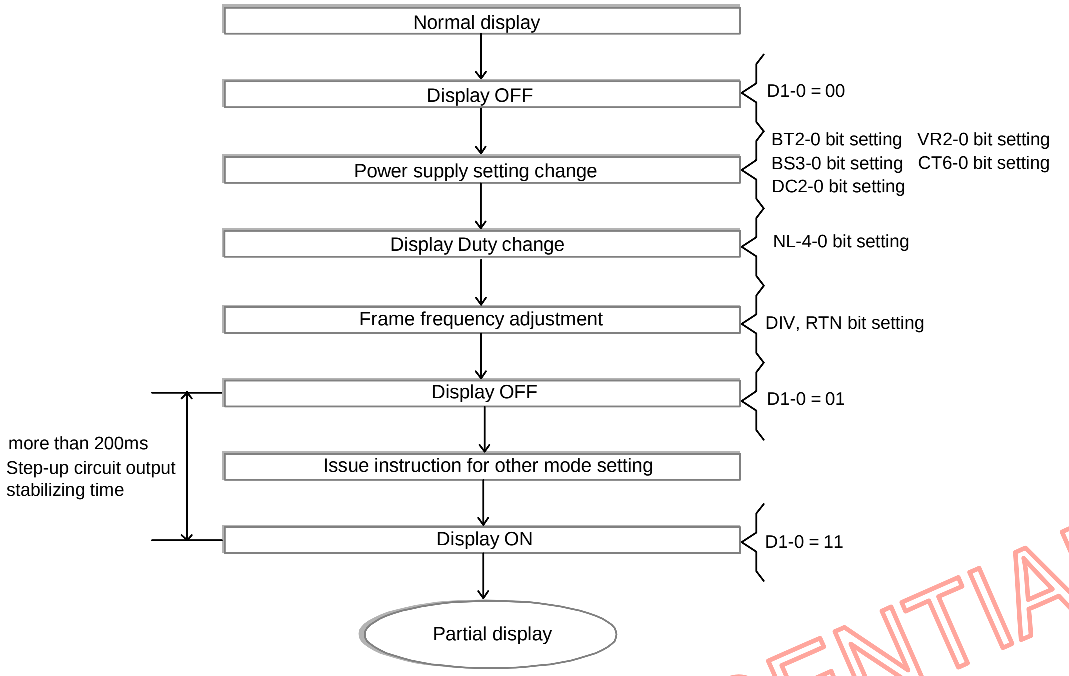


Figure 25. Normal to partial case

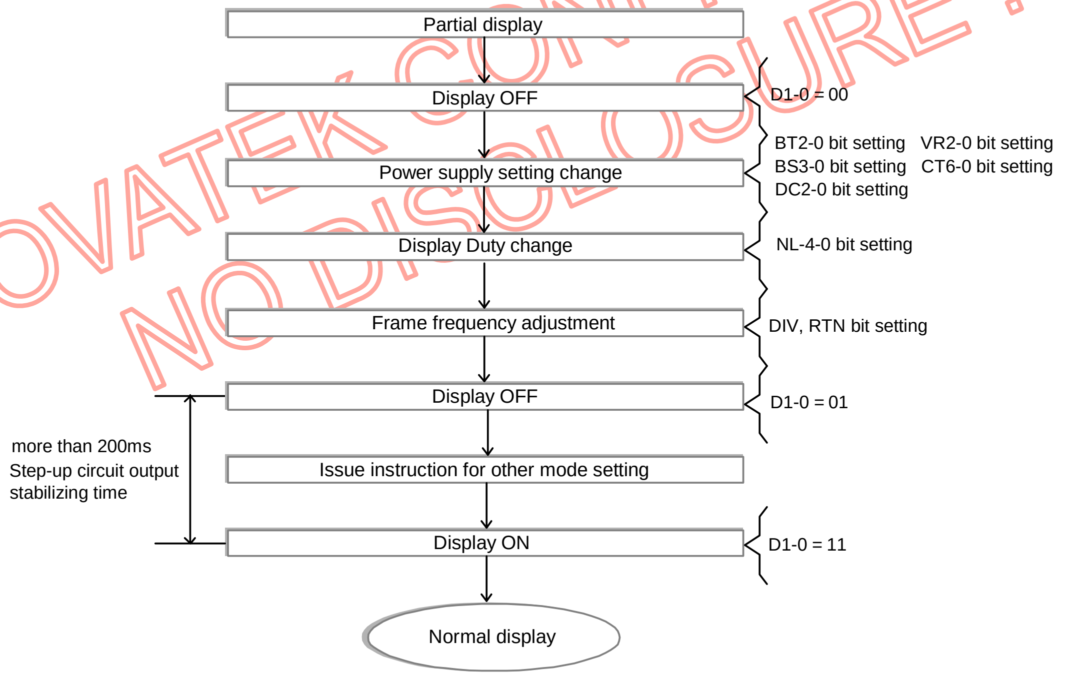


Figure 26. Partial to normal case

Frame-Frequency Adjustment Function

The NT7553E has an on-chip frame-frequency adjustment function. The frame frequency can be adjusted by the instruction setting (DIV, RTN) during the LCD drive, as the oscillation frequency is always the same. When the display duty is changed, the frame frequency can be adjusted to be the same.

If the oscillation frequency is set to high, an animation or a static image can be displayed in suitable ways by changing the frame frequency. When a static image is displayed, the frame frequency can be set low and the low-power consumption mode can be entered. When high-speed screen switching, for an animated display, etc. is required, the frame frequency can be set high.

Relationship between LCD Drive Duty and Frame Frequency

The relationship between the LCD driver duty and the frame frequency is calculated by the following expression. The frame frequency can be adjusted in the retrace-line period bit (RTN) and in the operation clock division bit (DIV) by the instructions.

(Formula for the frame frequency)
Frame frequency = fosc / (Clock cycles per raster-row × division ratio × duty cycle) [Hz]
fosc: Oscillation frequency
Duty: drive duty (NL bit)
Clock cycles per raster-row: (RTN + 26) clock cycles
Division ratio: DIV bit

n-raster-row Reversed AC Drive

The NT7553E supports not only the LCD reversed AC drive in a one-frame unit (B-pattern waveform) but also the n-raster-row reversed AC drive which alternates in an n-raster-row unit from one to 64 raster rows (C-pattern waveform). When a problem affecting display quality occurs, such as cross talk at high-duty driving of more than 1/64 duty, the n-raster-row reversed AC drive (C-pattern waveform) can improve the quality.

Determine the number of raster-rows n (NW bit set value + 1) for alternating after confirmation of the display quality with the actual LCD panel. However, if the number of AC raster-rows is reduced, the LCD alternating frequency becomes high. Because of this, the charge or discharge current is increased in the LCD cells.

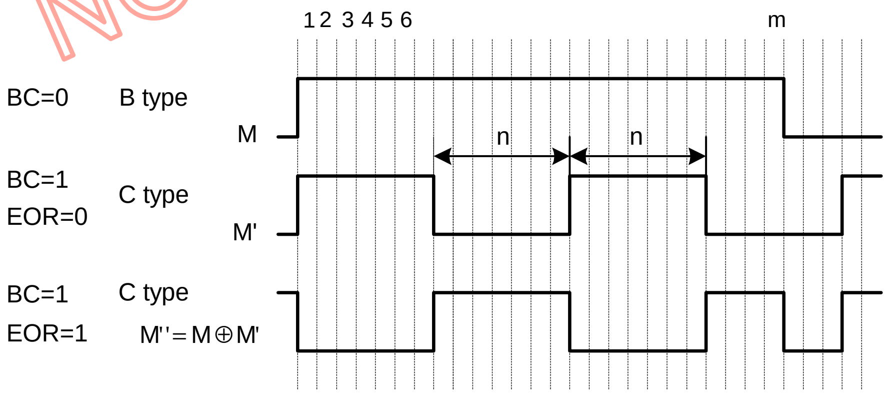
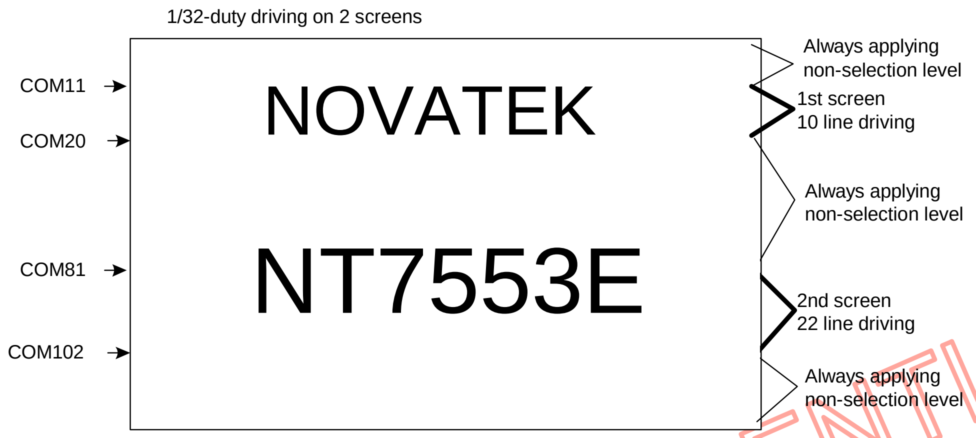


Figure 27. Example of an AC Signal under n-raster-row Reversed AC Drive

Screen-division Driving Function

The NT7553E can select and drive two screens at any position with the screen-driving position registers (R14h and R15h). Any two screens required for display are selectively driven and a duty ratio is lowered by LCD-driving duty setting (NL [4:0]), thus reducing LCD-driving voltage and power consumption. For the 1st division screen, start line (SS1[7:0]) and end line (SE1[7:0]) are specified by the 1st screen-driving position register (R14h). For the 2nd division screen, start line (SS2 [7:0]) and end line (SE2 [7:0]) are specified by the 2nd screen-driving position register (R15h). The 2nd screen control is effective when the SPT bit is “1”. The total count of selection-driving lines for the 1st and 2nd screens must correspond to the LCD-driving duty set value.



- Driving Duty: NL[4:0]= ”00011” (1/32 duty) , SPT=1
- 1st Screen setting: SS1[7:0]=”0A”H, SE1[7:0]= ”13”H
- 2nd Screen setting: SS2[7:0]=”50”H, SE2[7:0]= ”65”H
- SPT=1

Figure 28. Display examples in 2-screen division driving

Restrictions on the 1st / 2nd Screen Driving Position Register Settings

The following restrictions must be satisfied when setting the start line (SS1[7:0]) and end line (SE1[7:0]) of the 1st screen driving position register (R14h) and the start line (SS2[7:0]) and end line (SE2[7:0]) of the 2nd screen driving position register (R15h) for the NT7553E. Note that incorrect display may occur if the restrictions are not satisfied.

Table 15. Restrictions on the 1st/2nd Screen Driving Position Register Settings

	1st Screen Driving (SPT = 0)	2nd Screen Driving (SPT = 1)
Register setting	SS1 [7:0] ≤ SE1 [7:0] ≤ DUTY SET ≤ A1h	SS1 [7:0] ≤SE1 [7:0] < SS2 [7:0] ≤ SE2 [7:0] ≤ DUTY SET ≤ A1h
Display operation	■ Time-sharing driving for COM pins (SS1+1) to (SE1+1) ■ Non-selection level driving for others	■ Time-sharing driving for COM pins (SS1+1) to (SE1+1) and (SS2+1) to (SE2+1) ■ Non-selection level driving for others

Notes:1. When the total line count in screen division driving settings is less than the duty setting, non-selection level driving is performed without the screen division driving setting range.

2. When the total line count in screen division driving settings is larger than the duty setting, the start line, the duty setting line and the lines between them are displayed and no selection level driving is performed for other lines.

3. For the 1st screen driving, the SS2[7:0] and SE2[7:0] settings are ignored.

LCD Voltage Supply Circuit

Figure 29 shows NT7553E LCD controller circuit of the single power supply mode.

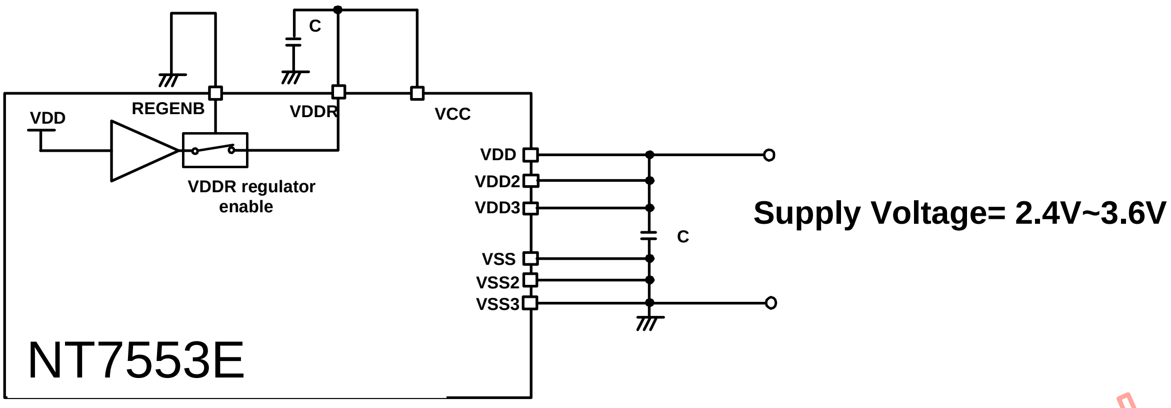
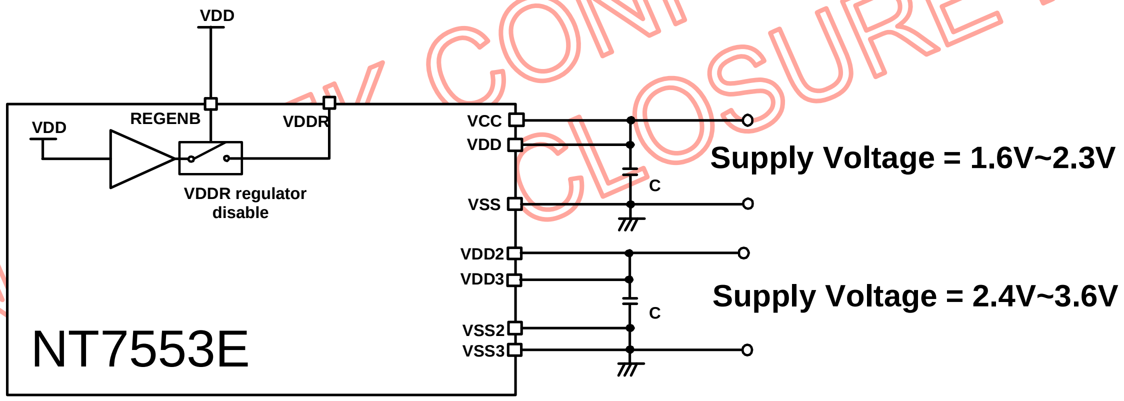


Figure 30 shows NT7553E LCD controller circuit of the dual power supply mode.



LCD Voltage Generation Circuit

Figure 31 shows a configuration of the NT7553E LCD drive voltage generation circuit. It consists of step-up circuit 1 that doubles or triples the voltage that is applied to VCI1, step-up circuit 2 that multiplies the voltage from step-up circuit 1 by two to five times, and a polarity circuit that generates a VCL level by inverting the VCH level centered around the VM level. These circuits generate VCH and VCL that are the power supply for COM outputs. The LCD driving level for SEG outputs (VSH and VM) are generated by dividing resistance at the VREF level.

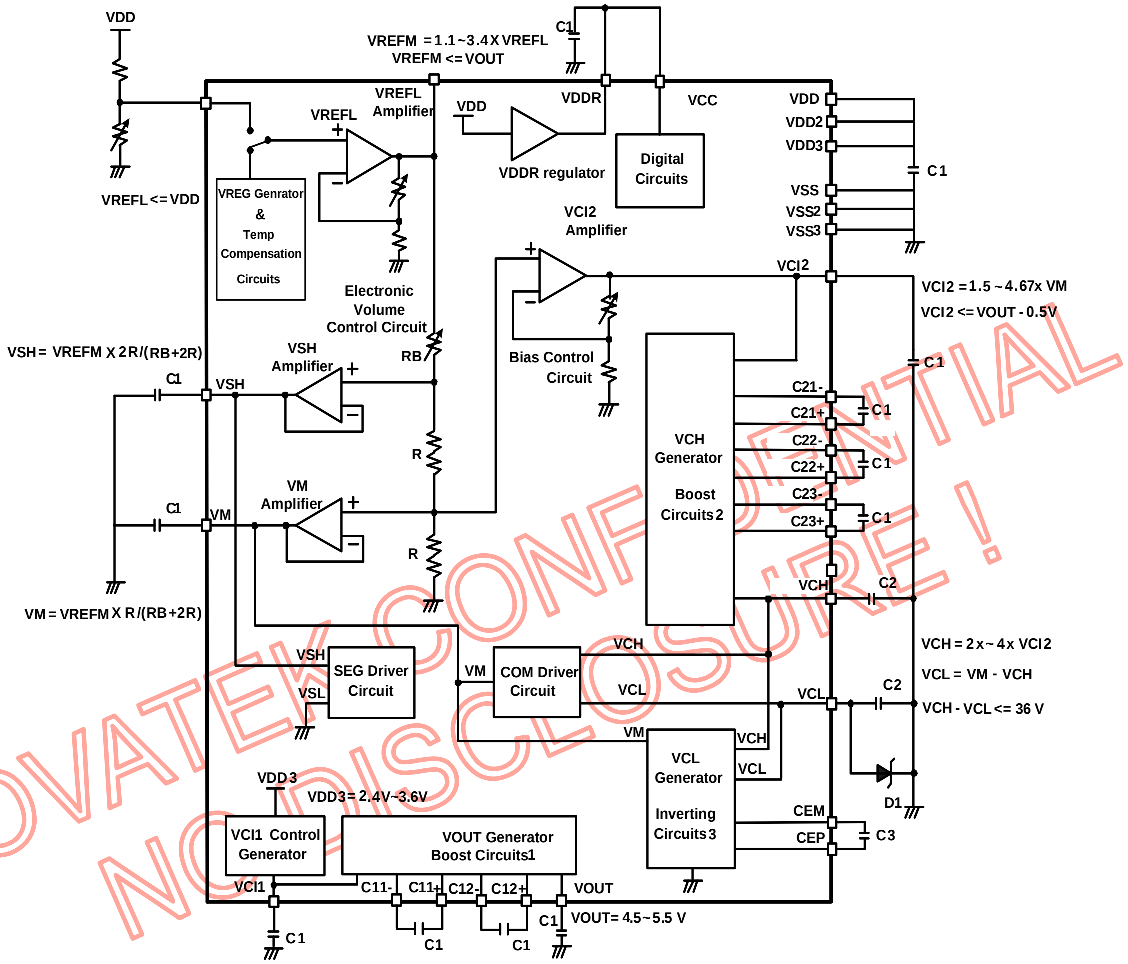


Figure 31. Configuration of internal power circuit

Notes:
1. Generate an output voltage (VOUT) from step-up circuit 1 within the range from 4.5 to 5.5V.
2. Do not allow the output voltage (VCH-VCL) from step-up circuit 2 and step-up circuit 3 to exceed 36 V.
3. Do not allow the output from VCI2 to exceed VOUT-0.5v voltage.
4. When capacitor with polarity is used, be sure that an inverted voltage is not applied to it in any state of the system.
5. VCI1 is used as both the reference voltage input and power supply in the step-up circuit. Keep sufficient LCD drive current.
6. Rated voltage of capacitors possible to be used are as described below. Required voltage depends on used panels. When actual voltage is less than 16V, capacitors with 16V rated voltage can be used.
7. The VCL must be connected one schottky barrier diode. The specification of SBD are VF=Max. 0.3V@1mA and VR=Min. 20V. The recommended SBD is Toshiba 1SS388 (VF=0.28V@1mA and VR=40V)

LCD Drive Voltage

The required voltage can be calculated by applying the following expressions. Drive voltages are standard; generate a voltage to suit the panel to be used.

LCD Drive Bias

An optimal bias can be calculated by applying the following expression. The value that has been calculated is theoretically optimal. If a lower bias value than the optimal value is used to drive the LCD, contrast may be reduced depending on lighting conditions. However, lowering the drive voltage can reduce the power consumption. Adjust the value according to the system to be used.
Bias value =1/Root (N)

How to determine the VCH voltage

$VCH = 2 \times VM \times N_B \times N_{D2}$
N_B: Bias ratio
N_{D2}: Step-up factor of the step-up circuit 2

Contrast adjustment

Rb: Contrast resistance (0.000R to 1.016R)
VSH = VREFM x 2R / (Rb + 2R)

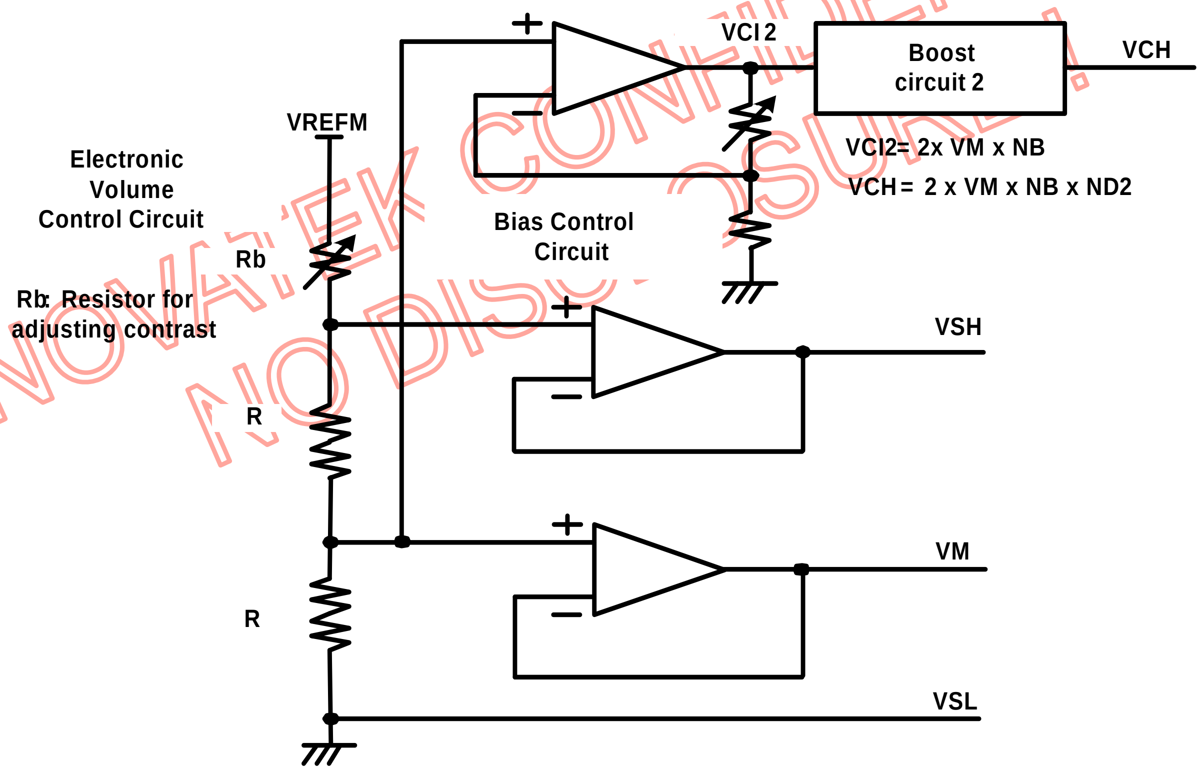


Figure 32. Contrast control circuit

Multi-time Calibration Function

The multi-time calibration function can be modifies and offset the contrast value. Because the variation of LCD module in term of contrast level, the multi-time calibration function can be used to achieve the best visual contrast of every LCD module by adjusting VSH voltage.

Multi-time calibration for contrast flow

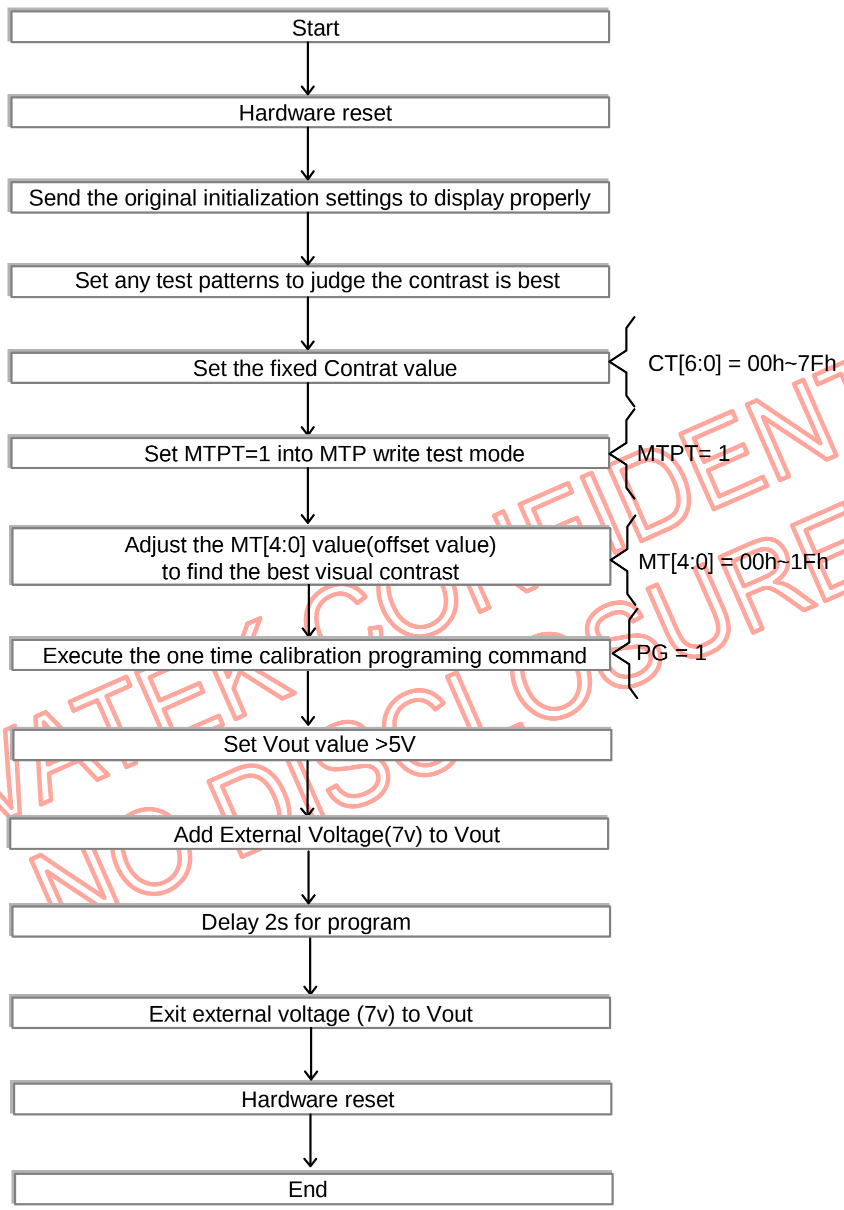
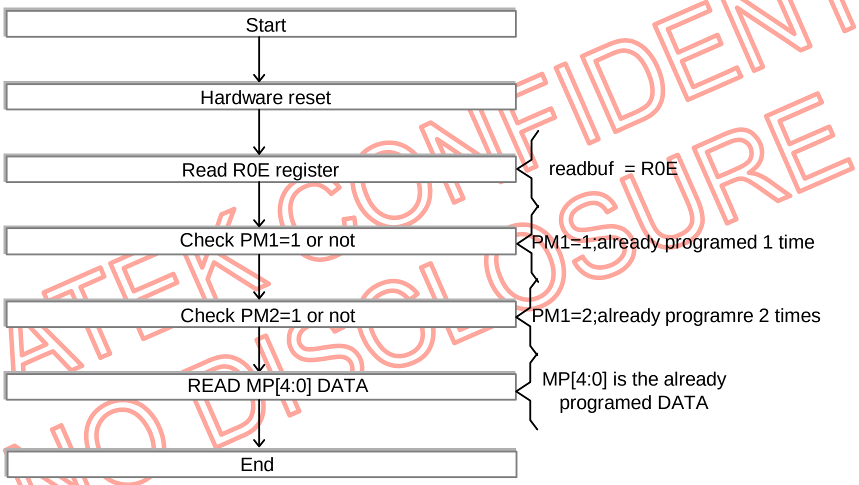


Figure 33. Contrast control circuit

Example source C code for MTP Flow

```
LCD_RES=0；                          //hardware reset
Delay (1)；
LCD_RES=1；
Init7553 ()；                        //Call initialization function
Command (0x0004, 0x013F)；           //Set the default value for the contrast
Command (0x000D, 0x0100 )；          //set MTPT INTO MTP test mode
Command (0x000D, 0x0112 )；          //Adjust the contrast value to the best visual
Command (0x000C,0x0001)；            //Execute the MTP programming command
Command (0x0003,0x017C)；            //Set pump on and set Vout > 5V
Extenal_7v_ON()；                    //External 7v to Vout on
Delay (2000)；                       //Delay 2 sec
Extenal_7v_OFF()；                   //External 7v to vout off
LCD_RES=0；                          //hardware reset
```

Read MTP function Flow



Example source C code for read MTP function Flow

```
LCD_RES=0；                               //hardware reset
Delay (1)；
LCD_RES=1；
write_i (0x000E);
readbuf = read_ i();
if ((readbuf & 0x0020) != 0){ PM1=1}   //CHECK PM1
if ((readbuf & 0x0040) != 0){ PM2=1}   //CHECK PM2
MP_DATA = readbuf & 0x001F ;           //Load already programmed DATA to
```

Application information for LCD panel (for reference only)

Type I (CMS = 0, SGS = 0)

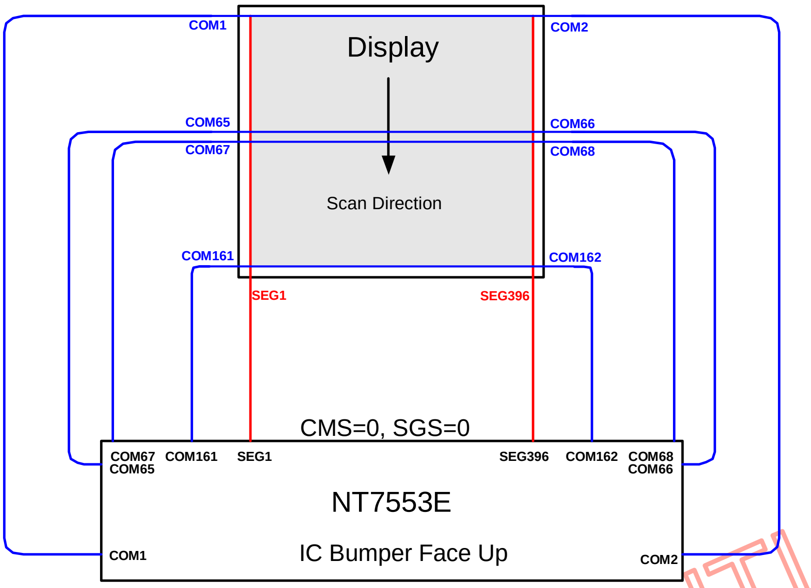


Figure 34. Application information for LCD panel type1

Type II (CMS = 0, SGS = 1)

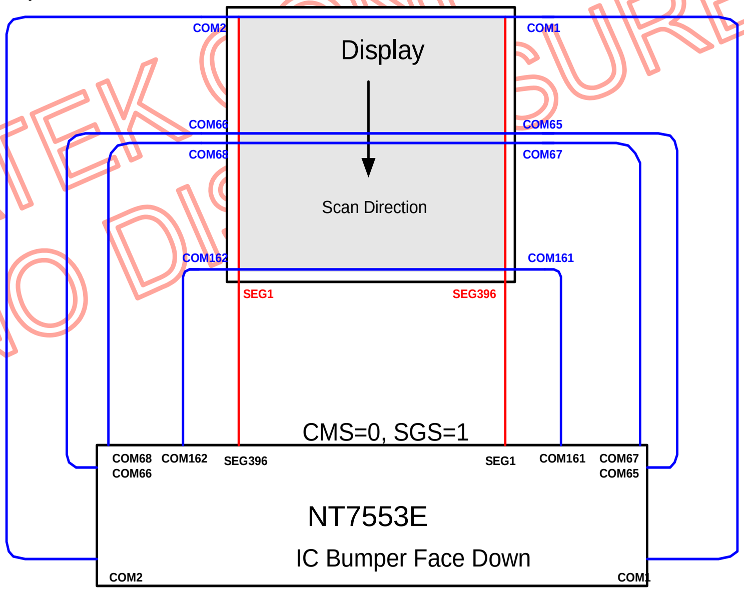


Figure 35. Application information for LCD panel type2

Type III (CMS = 1, SGS = 0)

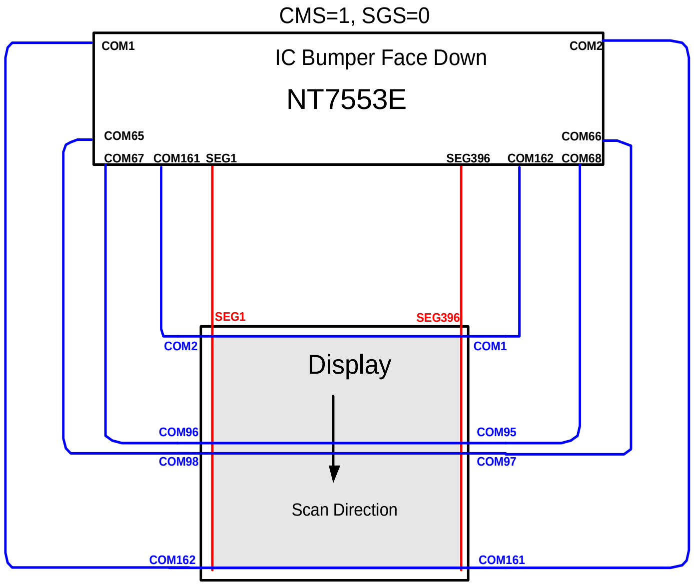


Figure 36. Application information for LCD panel type3

Type IV (CMS = 1, SGS = 1)

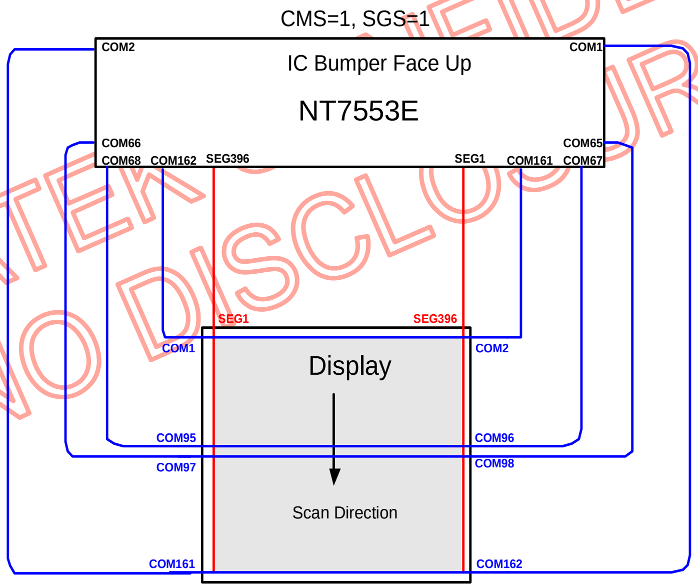
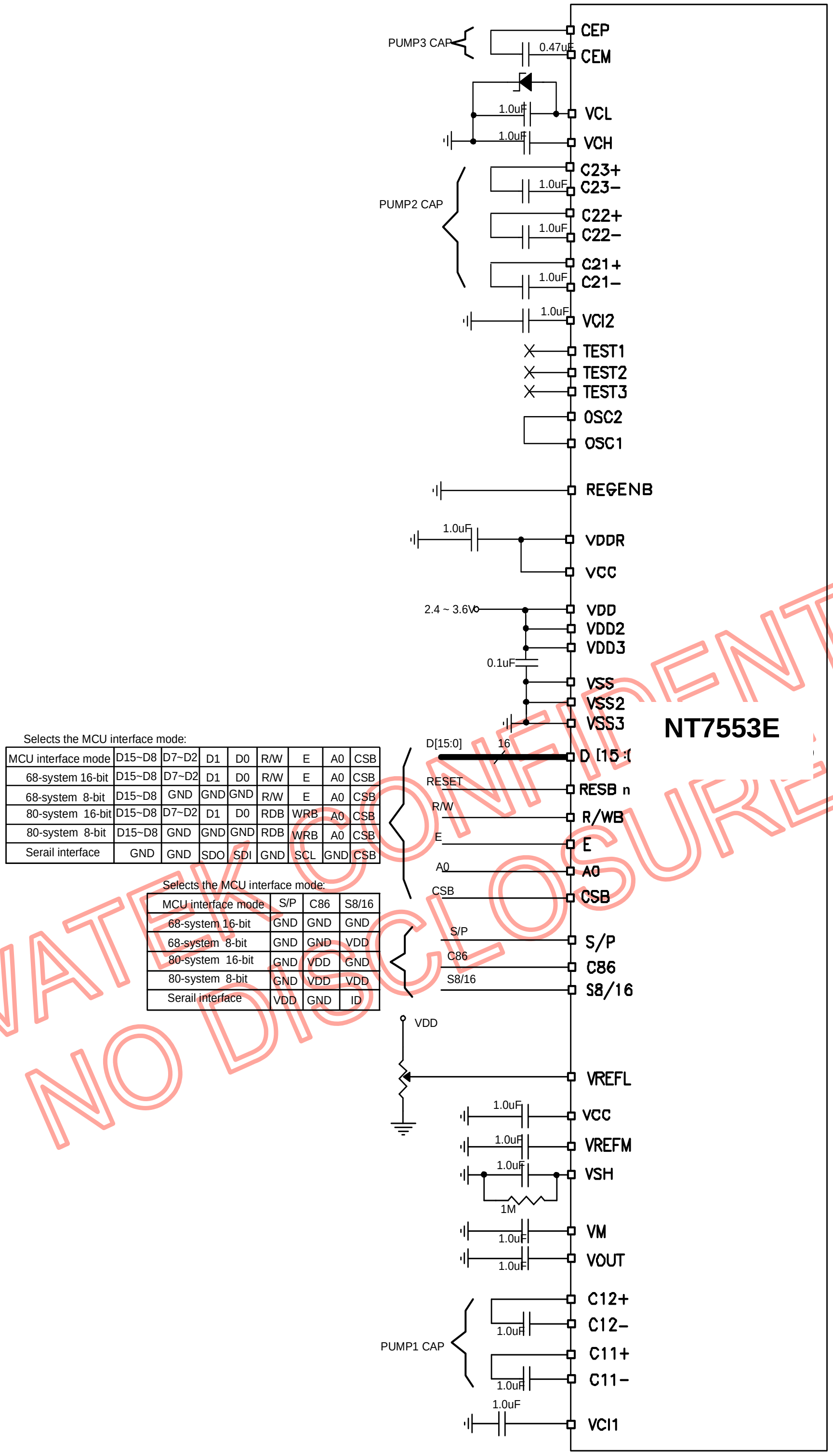


Figure 37. Application information for LCD panel type4

Note: If segment of the display panel is less than 396 outputs , we would recommend connecting most central segment pins to display panel. For example, in terms of 320 outputs application, connecting SEG 39~SEG359 to display panel is recommended.

Application information for Pin Connection to MPU (for reference only)



Selects the MCU interface mode:

MCU interface mode	D15~D8	D7~D2	D1	D0	R/W	E	A0	CSB
68-system 16-bit	D15~D8	D7~D2	D1	D0	R/W	E	A0	CSB
68-system 8-bit	D15~D8	GND	GND	GND	R/W	E	A0	CSB
80-system 16-bit	D15~D8	D7~D2	D1	D0	RDB	WRB	A0	CSB
80-system 8-bit	D15~D8	GND	GND	GND	RDB	WRB	A0	CSB
Serail interface	GND	GND	SDO	SDI	GND	SCL	GND	CSB

Selects the MCU interface mode:

MCU interface mode	S/P	C86	S8/16
68-system 16-bit	GND	GND	GND
68-system 8-bit	GND	GND	VDD
80-system 16-bit	GND	VDD	GND
80-system 8-bit	GND	VDD	VDD
Serail interface	VDD	GND	ID

Figure 38. Application information for Pin Connection to MPU

Application information for Pin Connection to of step up circuit (for reference only)

1. 2 times step-up circuit1 (2 x VCI1)

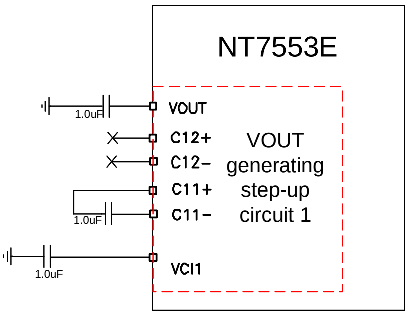


Figure 39.

2. 3 times step-up circuit1 (3 x VCI1)

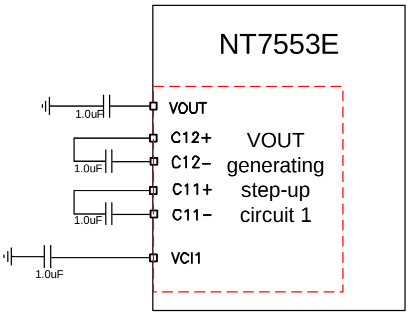


Figure 40.

3. 2 times step-up circuit2 (2 x VCI2)

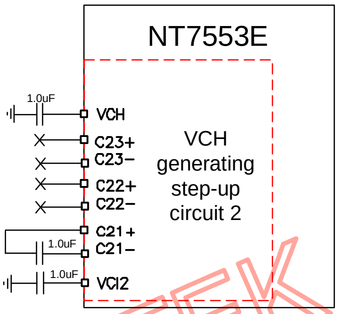


Figure 41.

4. 3 times step-up circuit2 (3 x VCI2)

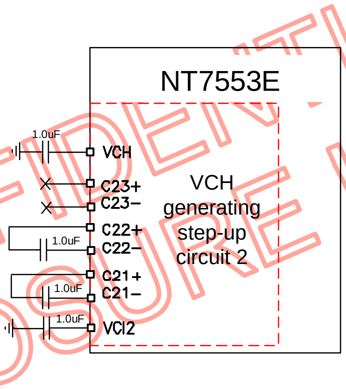


Figure 42.

5. 4 times step-up circuit2 (4 x VCI2)

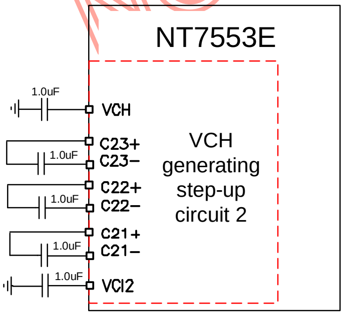


Figure 43.

Application information for LCD panel (for reference only)

External supply voltage for driver application circuit (for reference only)

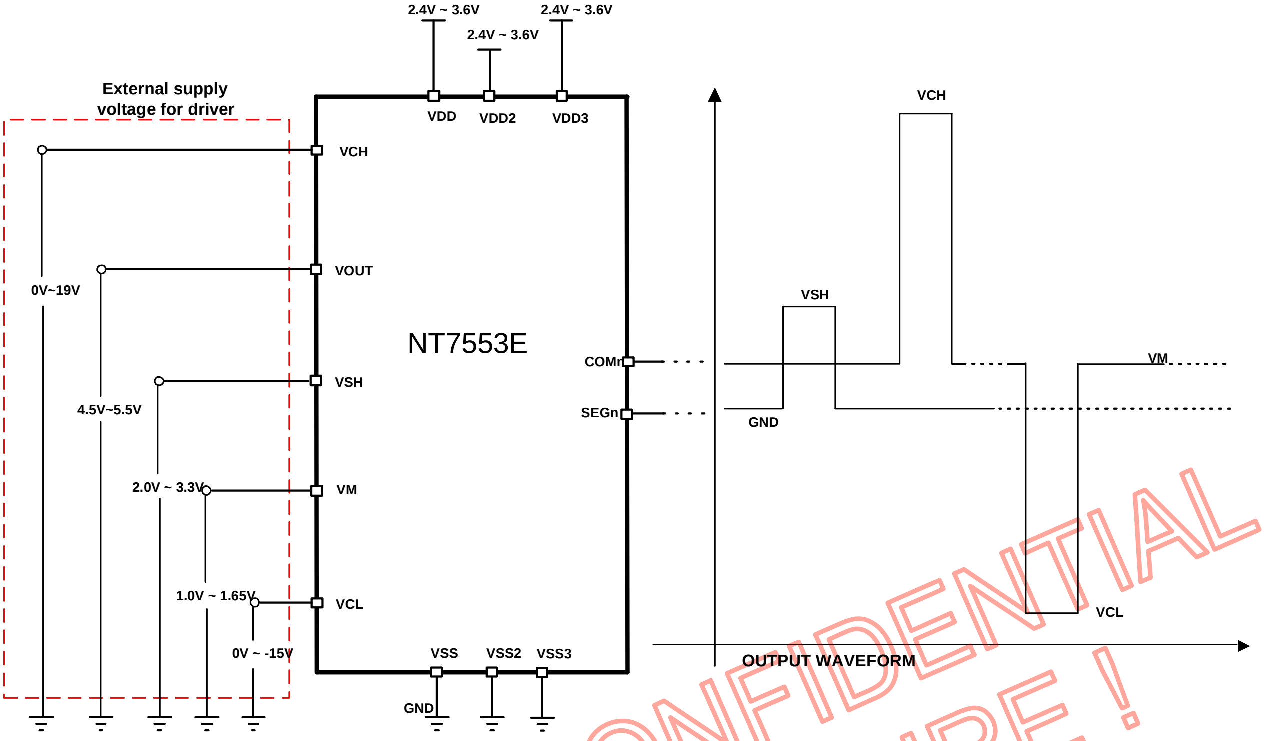
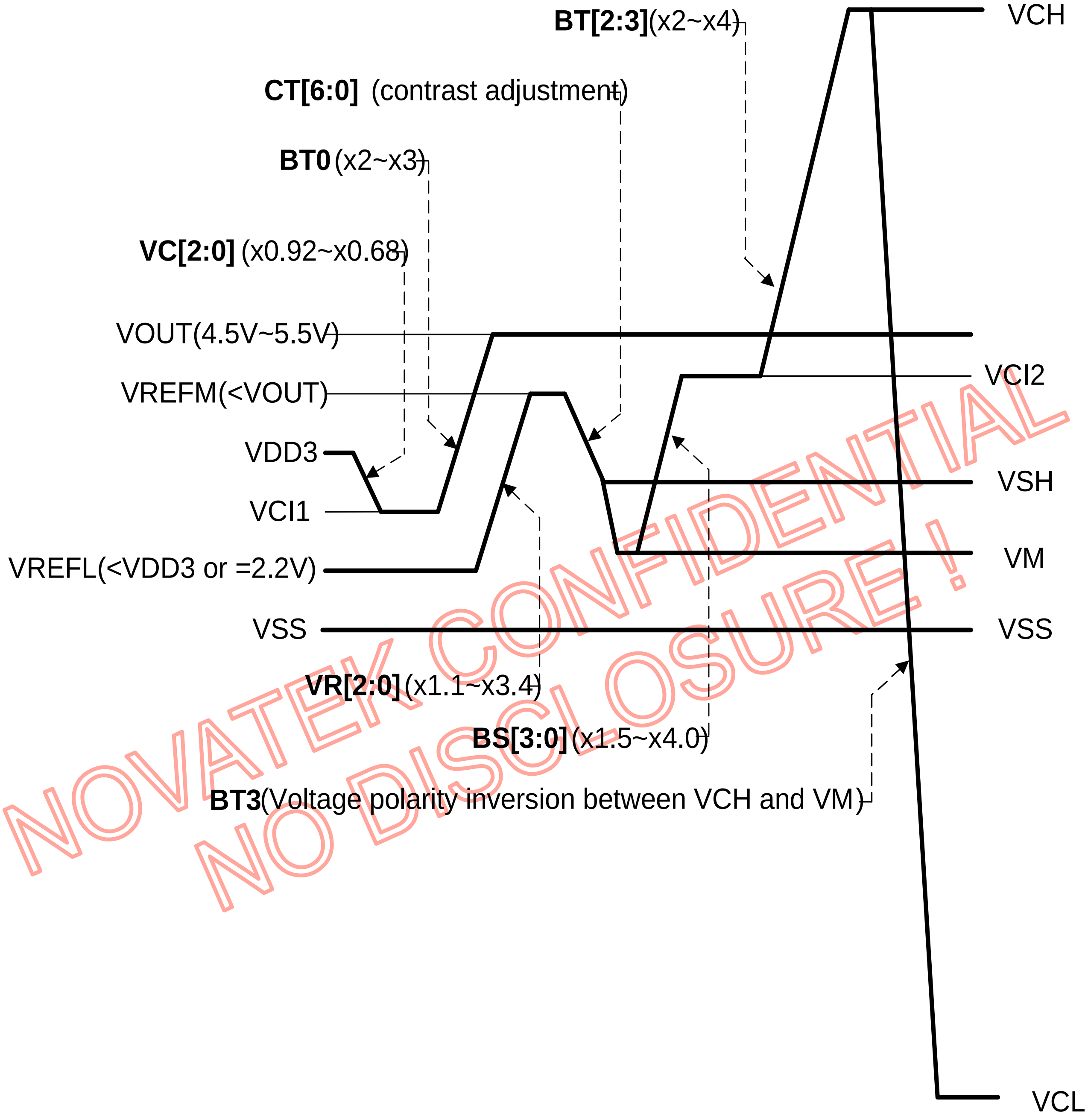


Figure 44. External supply voltage for driver application circuit

Notes: 1. When use external supply voltages, the internal operational amplifier must be off (AP[1:0]=00).
2. When use external supply voltages, the VOUT must supply 4.5V~5.5V.
3. The external supply voltages, must always keep the relationship of VCH ≥ VSH ≥ VM ≥ VSS2 ≥ VCL.
4. The external supply voltages, must always keep the relationship of VCH – VCL< 36V

Power supply level correlation



ITO Layout Notice

1. Specifically with COG application, it is important to reduce the resistance of the ITO path. To make the overall display performance of the LCM better, there are some suggestions for ITO layout described as below:
   a) Please keep the resistance of VDD & VSS path between PCB and corresponding pads of IC ≤ 50Ω. This value includes the ITO resistors' values, the FPC/Heat seal resistor; the ACF contact resistors between IC and Glass, Glass and FPC/Heat seal, FPC/Heat seal and PCB.
   b) Large resistance will reduce the efficiency of the voltage booster; the user should make the ITO resistance of charge pump pads as small as possible. The resistance of C11+, C11-, C12+, C12-, C21+, C21-, C22+, C22-, C23+, C23-,CEM and CEP ≤ 100Ω; the resistance of VOUT, VM, VSH,VCH,VCL,VCI2 and VCI1 ≤ 300Ω.
   c) The value of the other pins of the interface ≤ 500Ω (except the RSTB pin).
   d) Make a long thin ITO line with an impedance of 5KΩ ~ 10KΩ between the RESET of interface and IC's RSTB pads to work as a low-pass filter. With experience, it can filter some EMI and prevent the errors caused by ESD.

ITO Path	Max. Resistance
VDD, VSS, VDD2, VSS2, VDD3, VSS3, VDDR, VCC	50Ω
C11+, C11-, C12+, C12-, C21+, C21-, C22+, C22-, C23+, C23-, CEM, CEP	100Ω
VOUT, VM, VSH, VCH, VCL, VCI2, VCI1	300Ω
RSTB	5KΩ~10KΩ
A0, CSB, E, R/W, D0 ~ D15	500Ω

2. To meet the value demanded above while laying out ITO, users may accept the rules below:
   a) In order to keep the ITO resistance to a minimum, the vary pitch and position of the module connection to the outside should be selected to make the power lines go as straight as possible.
   b) The distance between NT7553E and FPC is the shorter the better. Then the length of ITO will be the shortest and you can get a smaller resistor value.
   c) The ITO interface may fill the blank area on the LCD panel to reduce the ITO resistance.

3. Reference the figures for ITO Layout:
   a) Figure 45 is ITO Layout for All-interface mode.

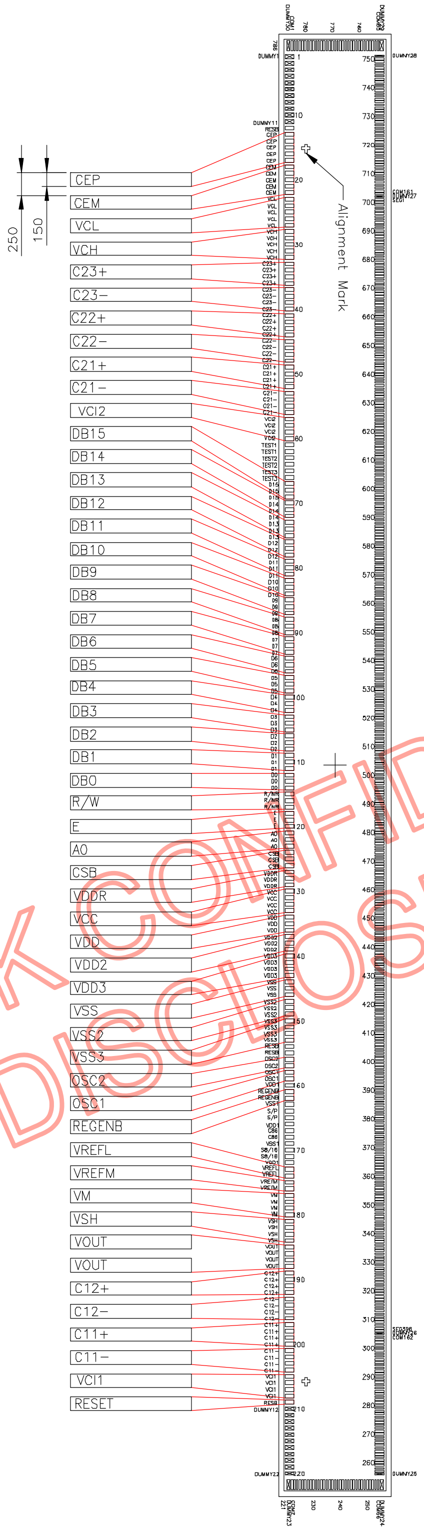
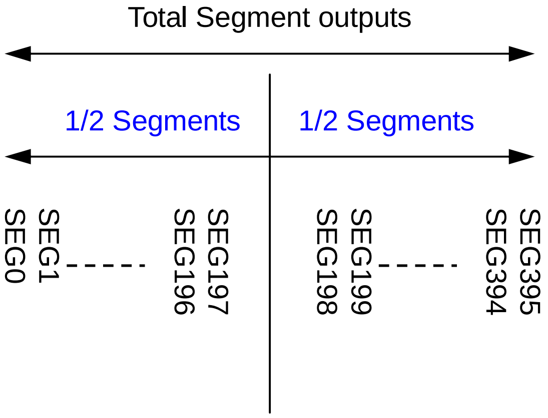


Figure 45. ITO Layout for all-interface mode.

4. If not all segment be used, we suggest the selection of segments should according to below figure.



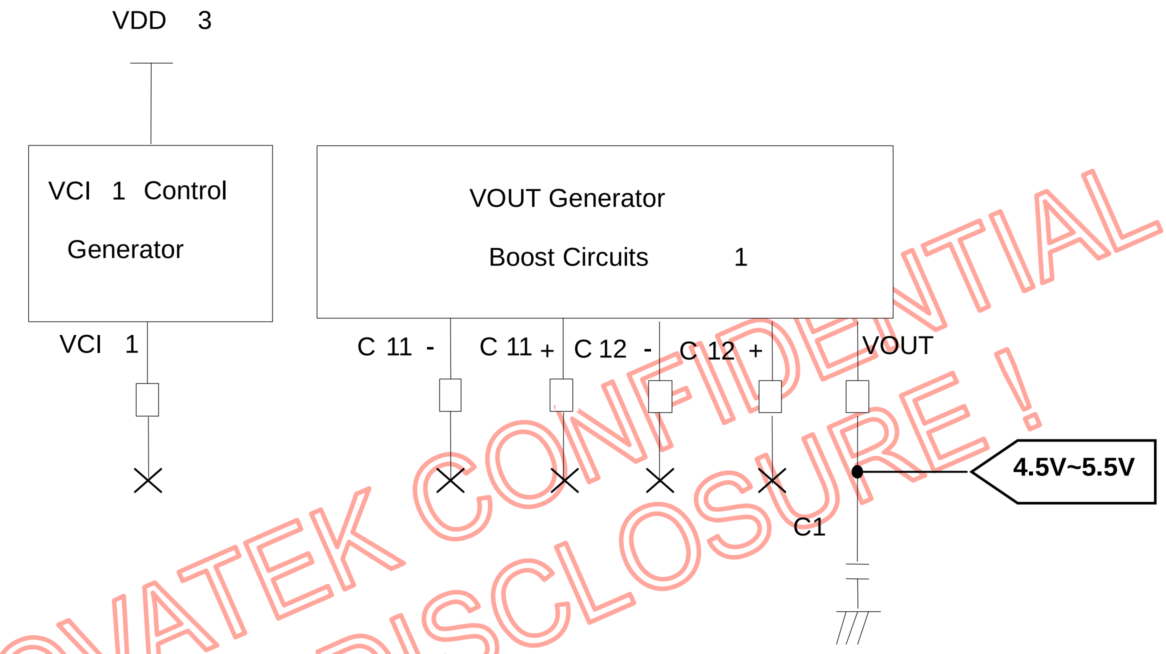
Application Notice of Large Panel Design

1. If active display areas of LCD larger than 4”, we recommend below items could be apply.

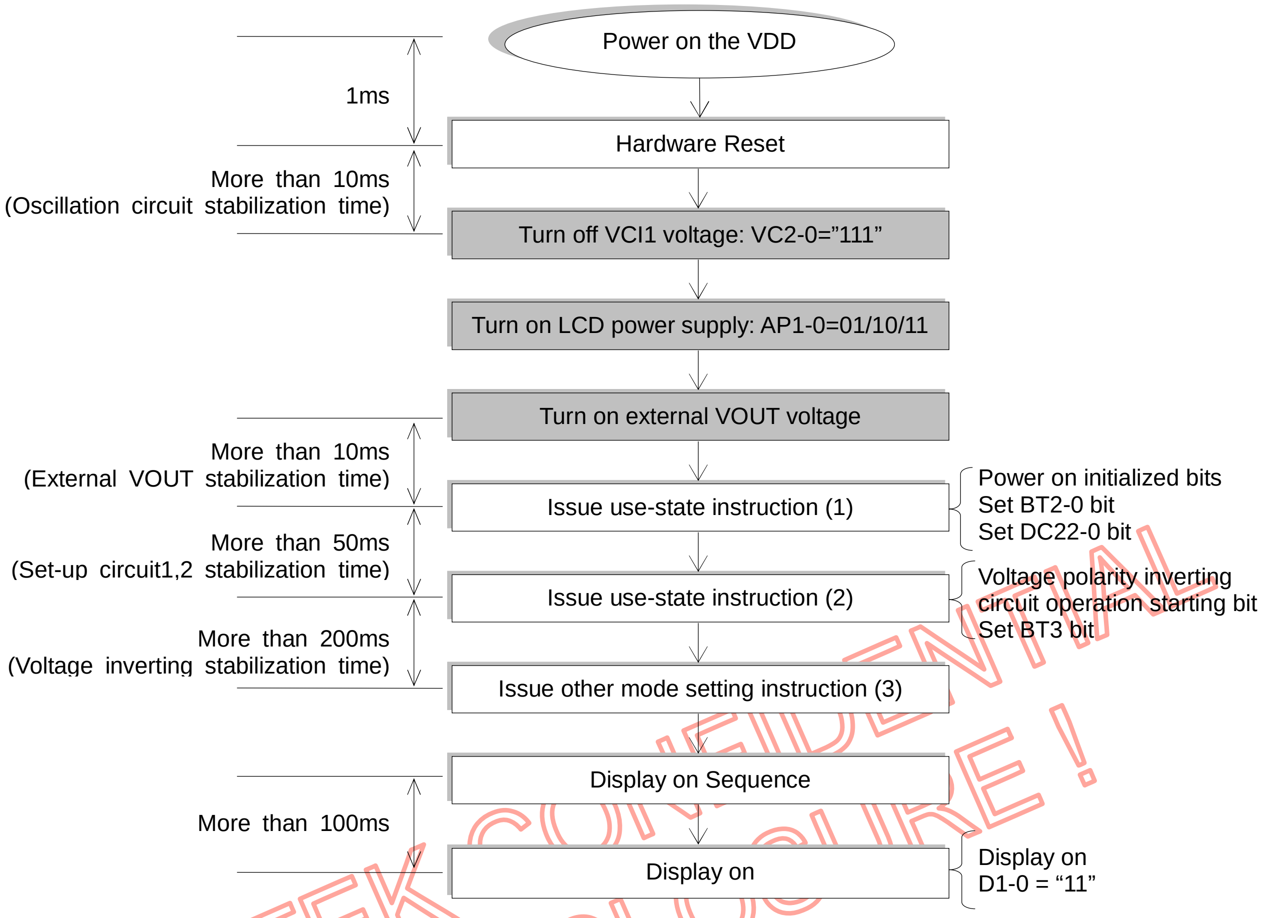
   a) Set register of VC[2:0] = 111B to turn off VCI1 generator circuit.

R0C	W	1	0	0	0	0	0	0	TC1	TC0	0	0	0	RV0	0	VC2	VC1	VC0
R0C	W	1	0	0	0	0	0	0	1/0	1/0	0	0	0	1/0	0	**1**	**1**	**1**

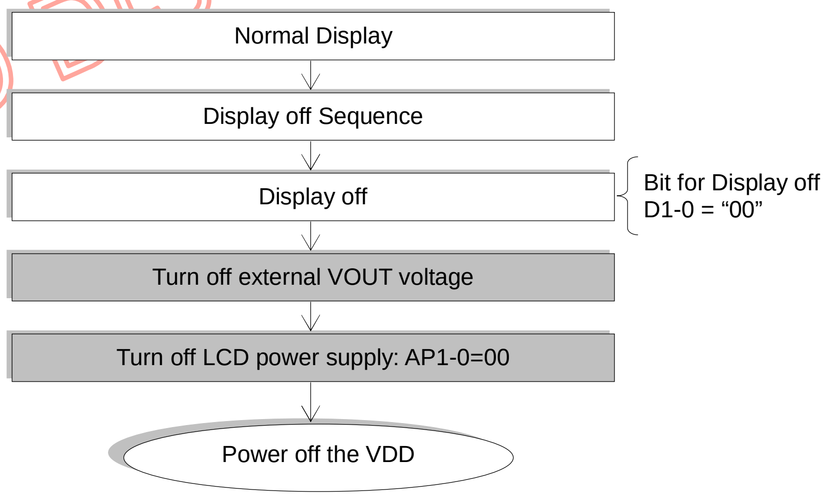
   b) Supply a voltage on VOUT pad by external power supply in order to enhance the display quality and steady LCD driving voltages. The application circuit showed as below.



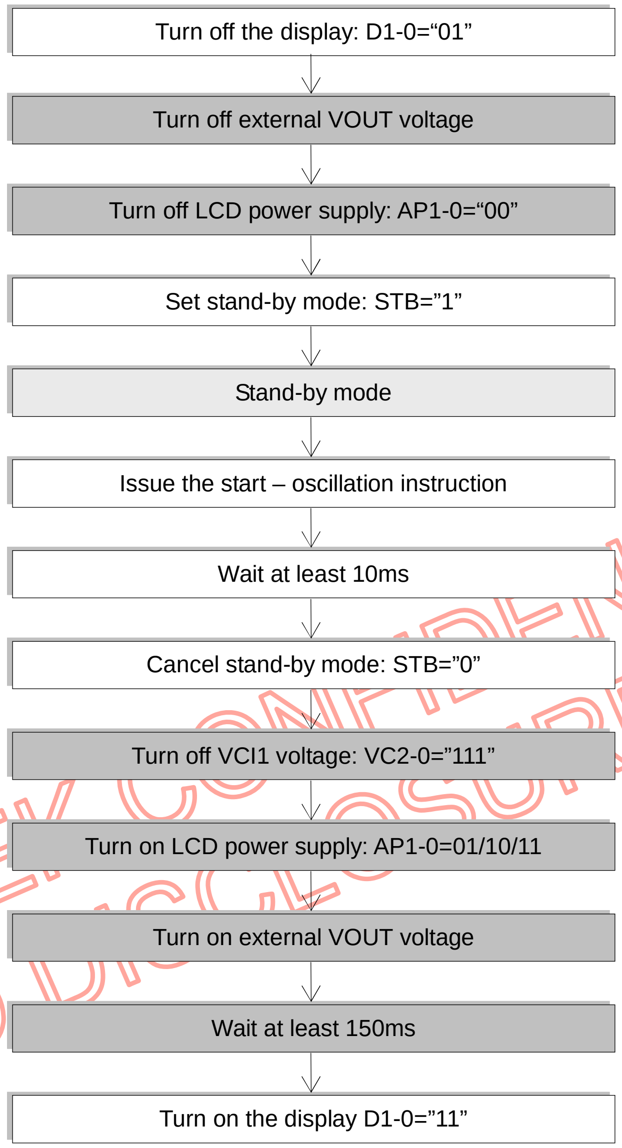
c) Recommend external VOUT voltage on/off sequence.



Power on sequence for external VOUT



Power off sequence for external VOUT



Stand-by on/off sequence for external VOUT

Reset Function

The NT7553E is internally initialized by RESB input pin. Reset the gate driver/Power supply IC, as its settings are not automatically reinitialized when the NT7553E is reset. The reset input must be held to Low for at least 10 ms. Don’t access the DDRAM or initially set the instructions until the oscillation frequency is stable after power has been supplied (10 ms).

Instruction Set Initialization

After resetting the NT7553E, the default settings are shown below:

1. Start oscillation executed
2. Driver output control: NL [4:0] = (1,0,0,1,1), SGS = 0, CMS = 0
3. B-pattern waveform AC drive: RST=0,B/C = 0, EOR = 0, NW [5:0] = (0,0,0,0,0,0)
4. Power control 1: DC [2:0] = (0,0,0), AP [1:0] = (0,0): LCD power off, STB = 0: Standby mode off, SLP = 0, BS [3:0] = (0,0,0,0), BT[3:0] = (0,0,0,0)
5. Contrast control (Weak contrast): VR [2:0] = (0,0,0), CT [6:0] = (0,0,0,0,0,0,0)
6. Entry mode set: SPR= 0, HWM = 0, I/D [1:0] = (1,1): Increment by 1, AM = 0: Horizontal move, LG [2:0]=(0,0,0): Replace mode
7. Compare register: CP [15:0] = (0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0)
8. Display control: VLE [2:1] = (0,0): No vertical scroll, SPT = 0,B/W = 0,REV = 0,DIP[1:0]= (0,0)
   D[1:0] = (0,0): Display off , DIP[1:0] =(0,0).
9. Frame cycle control: CLK [2:0] =(0,0,0), DIV [1:0] = (0,0): 1-divided clock, RTN [3:0]: No line retrace period
10. Power control 2: VC [2:0] = (0,0,0),RV0 = 0,TC[1:0]=(0,0)
11. MTPT = 0, MT[4:0]= (0,0,0,0,0), PG = 0
12. Vertical scroll: VL2 [7:0] = (0,0,0,0,0,0,0,0), VL1 [7:0] = (0,0,0,0,0,0,0,0)
13. 1st screen division: SE1 [7:0] = (1,1,1,1,1,1,1,1), SS1 [7:0] = (0,0,0,0,0,0,0,0)
14. 2nd screen division: SE2 [7:0] = (1,1,1,1,1,1,1,1), SS2 [7:0] = (0,0,0,0,0,0,0,0)
15. Horizontal RAM address position: HEA [7:0] = (1,0,0,0,0,0,1,1), HSA [7:0] = (0,0,0,0,0,0,0,0)
16. Vertical RAM address position: VEA [7:0] = (1,0,1,0,0,0,0,1), VSA [7:0] = (0,0,0,0,0,0,0,0)
17. RAM write data mask: WM [15:0] = (0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0): No mask
18. RAM address set: AD [15:0] = (0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0)
19. Grayscale palette:
   PK0 = (0,0,0,0,0,0), RK1= (0,0,0,0,1,1), PK2= (0,0,0,1,1,0), PK3= (0,0,1,0,0,0),
   PK4= (0,0,1,0,1,0), PK5= (0,0,1,1,0,0), PK6= (0,0,1,1,1,0), PK7= (0,0,1,1,1,1),
   PK8= (0,1,0,0,0,0), PK9= (0,1,0,0,0,1), PK10= (0,1,0,0,1,0), PK11= (0,1,0,0,1,1),
   PK12= (0,1,0,1,0,0), PK13= (0,1,0,1,0,1), PK14= (0,1,0,1,1,0), PK15= (0,1,0,1,1,1),
   PK16 = (0,1,1,0,0,0), PK17= (0,1,1,0,0,1), PK18= (0,1,1,0,1,0), PK19= (0,1,1,0,1,1),
   PK20= (0,1,1,1,0,0), PK21= (0,1,1,1,0,1)”, PK22= (0,1,1,1,1,0), PK23= (1,0,0,0,0,0),
   PK24= (1,0,0,0,1,0), PK25= (1,0,0,1,0,0), PK26= (1,0,0,1,1,0), PK27= (1,0,1,0,0,0),
   PK28 = (1,0,1,0,1,1), PK29= (1,0,1,1,1,0), PK30= (1,1,0,0,0,1), PK31= (1,1,0,1,0,0)

DDRAM Data Initialization

This is not automatically initialized by reset input but must be initialized by software while display is off (D [1:0] = (0,0)).

Output Pin Initialization

1. LCD driver output pins (SEG/COM): Output VSS level
2. Oscillator output pin (OSCO): Output oscillation signal

General Commands Description

Outline

The NT7553E uses the 16-bit bus architecture. Before the internal operation of the NT7553E starts, control information is temporarily stored in the registers described below to allow high-speed interfacing with a high-performance microcomputer. The internal operation of the NT7553E is determined by signals sent from the microcomputer. These signals, which include the register selection signal (A0), the read/write signal (R/W), and the data bus signals (D15 to D0), make up the NT7553E instructions.

- There are eight categories of instructions that:
- Specify the index
- Read the status
- Control the display
- Control power management
- Process the graphics data
- Set internal DDRAM addresses
- Transfer data to and from the internal DDRAM
- Set the grayscale level for the internal grayscale palette table

Normally, instructions that write data are used the most. However, an auto-update of internal DDRAM addresses after each data write can lighten the microcomputer program load. Because instructions are executed in 0 cycles, they can be written in succession.

Instruction Descriptions

1. Index (IR):

The index instructions specify the RAM control indexes (R00h to R3Fh). It sets the register number in the range of 000000 to 111001 in binary form. However, R40 to R44 are disabled since they are test registers.

NO.	RW	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
IR	W	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Index Instruction

2. Status Read (SR):

The status read instruction reads the internal status of the NT7553E.

No.	RW	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SR	R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	C6	C5	C4	C3	C2	C1	C0

Status Read Instruction

L [7:0]: Indicates the driving raster-row position where the liquid crystal display is being driven.
C [6:0]: Reads the contrast setting values (CT[6:0])

3. Start Oscillation (R00h):

The start oscillation instruction restarts the oscillator from the halt state in the standby mode. After issuing these instruction, wait at least 10 ms for oscillation to stabilize before issuing the next instruction. (See the Standby Mode section.)
If this register is read forcibly, “7553”H is read.

No.	RW	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R00	W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
	R	1	0	1	1	1	0	1	0	1	0	0	1	0	0	0	1	1

Start Oscillation Instruction

4. Driver Output Control (R01h):

No.	RW	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R01	W	1	*	*	*	*	*	*	CMS	SGS	*	*	*	NL4	NL3	NL2	NL1	NL0

Driver Output Control Instruction

CMS: Selects the output shift direction of a common driver. When CMS = 0, COM1 shifts to COM162. When CMS = 1, COM162 shifts to COM1.

SGS: Selects the output shift direction of the segment driver. When SGS = 0, data are output SEG1 to SEG396. When SGS = 1, data are output SEG396 to SEG1. Re-write to the RAM when intending to change the SGS bit.

NL[4:0]: Specify the LCD drive duty ratio. The duty ratio can be adjusted for every eight raster-rows. DDRAM address mapping does not depend on the setting value of the drive duty ratio.

Table16. NL Bits and Drive Duty

NL4	NL3	NL2	NL1	NL0	Display Size (Dots)	LCD Drive Duty	Common Driver Used	
							CMS=”0”	CMS=”1”
0	0	0	0	0	396 x 8	1/8	COM1 – COM8	COM162 – COM155
0	0	0	0	1	396 x 16	1/16	COM1 - COM16	COM162 – COM147
0	0	0	1	0	396 x 24	1/24	COM1 - COM24	COM162 – COM139
0	0	0	1	1	396 x 32	1/32	COM1 - COM32	COM162 – COM101
0	0	1	0	0	396 x 40	1/40	COM1 – COM40	COM162 – COM123
0	0	1	0	1	396 x 48	1/48	COM1 - COM48	COM162 – COM115
0	0	1	1	0	396 x 56	1/56	COM1 – COM56	COM162 – COM107
0	0	1	1	1	396 x 64	1/64	COM1 – COM64	COM162 – COM99
0	1	0	0	0	396 x 72	1/72	COM1 - COM72	COM162 – COM91
0	1	0	0	1	396 x 80	1/80	COM1 – COM80	COM162 – COM83
0	1	0	1	0	396 x 88	1/88	COM1 - COM88	COM162 – COM75
0	1	0	1	1	396 x 96	1/96	COM1 – COM96	COM162 – COM67
0	1	1	0	0	396 x 104	1/104	COM1- COM104	COM162 – COM59
0	1	1	0	1	396 x 112	1/112	COM1 - COM112	COM162 – COM51
0	1	1	1	0	396 x 120	1/120	COM1 - COM120	COM162 – COM43
0	1	1	1	1	396 x 128	1/128	COM1 - COM128	COM162 – COM35
1	0	0	0	0	396 x 136	1/136	COM1 - COM136	COM162 – COM27
1	0	0	0	1	396 x 144	1/144	COM1 - COM144	COM162 – COM19
1	0	0	1	0	396 x 152	1/152	COM1 - COM152	COM162 – COM11
1	0	0	1	1	396 x 160	1/160	COM1 - COM160	COM162 – COM3
1	0	1	0	0	396 x 162	1/162	COM1 - COM162	COM162 – COM1

5. LCD Driving Waveform Control (R02h):

No.	RW	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R02	W	1	0	0	0	0	0	RST	B/C	EOR	0	0	NW5	NW4	NW3	NW2	NW1	NW0

LCD Drive Waveform Control Instruction

B/C: When B/C = 0, a B-pattern waveform is generated and alternates in every frame for the LCD drive.When B/C = 1, a C-pattern waveform is generated and alternates in each raster-row specified by bits EOR and NW[4:0] in the LCD-driving-waveform control register. For details, see the n-raster-row Reversed AC Drive section.

EOR: When the C-pattern waveform is set (B/C = 1) and EOR = 1, the odd/even frame-select signals and the n-raster-row reversed signals are EORed for alternating drive. EOR is used when combining the set values of the number of the LCD drive duty ratio and the n raster-row does not alternate the LCD. For details, see the n-raster-row Reversed AC Drive section.

RST: When RST = 1, software reset function is started. This function is the same as the hardware RESET pin. It takes a 10-clock cycle period. This bit is automatically cleared after reset function is completed. Therefore, before the 10-clock cycle other instructions cannot be issued. Do not set the RST bit during stand-by mode.

NW[5:0]: Specify the number of raster-rows n that will alternate at the C-pattern waveform setting (B/C =1). NW [5:0] alternate for every set value + 1 raster-row, and the first to the 64th raster-rows can be selected.

6. Power Control 1 (R03h) & Power Control 2 (R0Ch)

No.	RW	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R03	W	1	BS3	BS2	BS1	BS0	BT3	BT2	BT1	BT0	0	DC2	DC1	DC0	AP1	AP0	SLP	STB
R0C	W	1	0	0	0	0	0	0	TC1	TC0	0	0	0	RV0	0	VC2	VC1	VC0

Power Control Instructions

STB: When STB = 1, the NT7553E enters the standby mode, where display operation completely stops, the COM driver signal and SEG driver signal are at the VSS level, halting all the internal operations including the internal oscillator and no external clock pulses are supplied.

During the stand by mode the DDRAM data is not cleared, but the DDRAM data can’t be read and written through the MPU interface. Only the following instructions can be executed during the standby mode.

a. Standby mode cancel (STB = “0”)
b. Start oscillation

SLP: When SLP = 1, the NT7553E enters the sleep mode, where the internal display operations are halted except for the oscillator, thus reducing current consumption. Only the following instructions can be executed during sleep mode. Power control (BS [2:0], BT [3:0], DC [2:0], AP [1:0], SLP, STB). During sleep mode, the other DDRAM data and instructions cannot be updated although they are retained.

BS[3:0]: The LCD drive bias value is set. The LCD drive bias value can be selected according to its drive duty ratio and voltage.
Determine the LCD drive bias according to its display duty, and select combination of boosting ratio of the step-up circuit 2 and bias amplifier ratio so as not to exceed voltage control of VCI2 and VCH. See the LCD Voltage Generation Circuit regarding how to determine the LCD drive bias, VCH voltage and contrast adjustment for the following settings.

Table 17-1. Display bias setting

LCD bias	Booster ratio of the set-up circuit2 (ND2)	BS3	BS2	BS1	BS0	Bias ratio (NB)	VCI2 ≤ (Vout-0.5)	Recommended value of the (VCH-VCL ≤ 36V)	Total booster ratio (VCH =N x VM)
1/2	x 2	0	0	0	0	0.75	1.50 x VM	VCI2 x 2	3 x VM
1/4	x 2	0	1	0	0	1.25	2.50 x VM	VCI2 x 2	5 x VM
	x 3	0	0	0	1	0.875	1.75 x VM	VCI2 x 3	5.25 x VM
1/6	x 2	1	0	1	1	1.75	3.50 x VM	VCI2 x 2	7 x VM
	x 3	0	0	1	1	1.165	2.33 x VM	VCI2 x 3	6.99 x VM
	x 4	0	0	0	1	0.875	1.75 x VM	VCI2 x 4	7 x VM
1/8	x 3	1	0	0	0	1.50	3.00 x VM	VCI2 x 3	9 x VM
	x 4	0	0	1	0	1.125	2.25 x VM	VCI2 x 4	9 x VM
1/9	x 3	1	0	1	0	1.675	3.35 x VM	VCI2 x 3	10.05 x VM
	x 4	0	1	0	0	1.25	2.50 x VM	VCI2 x 4	10 x VM
1/10	x 3	1	1	0	0	1.825	3.65 x VM	VCI2 x 3	10.95 x VM
	x 4	0	1	1	0	1.375	2.75 x VM	VCI2 x 4	11 x VM
1/11	x 3	1	1	0	1	2.00	4.00 x VM	VCI2 x 3	12 x VM
	x 4	1	0	0	0	1.50	3.00 x VM	VCI2 x 4	12 x VM
1/12	x 3	1	1	1	0	2.165	4.33 x VM	VCI2 x 3	12.99 x VM
	x 4	1	0	0	1	1.625	3.25 x VM	VCI2 x 4	13 x VM
1/13	x 3	1	1	1	1	2.335	4.67 x VM	VCI2 x 3	14.01 x VM
	x 4	1	0	1	1	1.75	3.50 x VM	VCI2 x 4	14 x VM

Table 17-2. Display bias setting

BS3	BS2	BS1	BS0	VCI2 ≤ (Vout-0.5)
0	0	0	0	1.50 x VM
0	0	0	1	1.75 x VM
0	0	1	0	2.25 x VM
0	0	1	1	2.33 x VM
0	1	0	0	2.50 x VM
0	1	0	1	2.60 x VM
0	1	1	0	2.75 x VM
0	1	1	1	2.80 x VM
1	0	0	0	3.00 x VM
1	0	0	1	3.25 x VM
1	0	1	0	3.35 x VM
1	0	1	1	3.50 x VM
1	1	0	0	3.65 x VM
1	1	0	1	4.00 x VM
1	1	1	0	4.33 x VM
1	1	1	1	4.67 x VM

AP [1:0]: The amount of fixed current from the fixed current source in the operational amplifier for the LCD is adjusted. When the amount of fixed current is large, the LCD driving ability and the display quality becomes high, but the current consumption is increased. Adjust the fixed current considering the display quality and the current consumption. During no display, when AP [1:0] = “00”, the current consumption can be reduced by ending the operational amplifier and step-up circuit operation.

Table 18. AP Bits and Amount of Fixed Current

AP1	AP0	Amount of Fixed Current in the Operational Amplifier
0	0	Operational amplifier does not operate.
0	1	Small
1	0	Middle
1	1	Large

DC [2:0]: The operating frequency in the step-up circuit is selected. When the step-up operating frequency is high, the driving ability of the step-up circuit becomes high, but the current consumption is increased. Adjust the frequency considering the step-up ability and the current consumption.

Table 19. DC Bits and Operating Clock Frequency

DC2	DC1	DC0	Operating clock frequency in the booster 1	Operating clock frequency in the voltage inverting circuit and the booster 2
0	0	0	32-divided clock	32-divided clock
0	0	1	64-divided clock	32-divided clock
0	1	0	32-divided clock	64-divided clock
0	1	1	64-divided clock	64-divided clock
1	0	0	32-divided clock	96-divided clock
1	0	1	64-divided clock	96-divided clock
1	1	0	32-divided clock	128-divided clock
1	1	1	64-divided clock	128-divided clock

BT [2:0]: The output factor of step-up circuit is switched. The LCD drive voltage level can be selected according to its drive duty ratio and bias. Lower amplification of the step-up circuit consumes less current.

Table 20. BT[2:0] Bits and Output Level

BT2	BT1	BT0	VOUT output of the booster 1 (Use VOUT within the range of 4.5 to 5.5V.)	VCH output of the booster 2 (Set VCH-VCL lower than 36v)
0	0	0	2 x VCI1	2 x VCI2
0	0	1	3 x VCI1	2 x VCI2
0	1	0	2 x VCI1	3 x VCI2
0	1	1	3 x VCI1	3 x VCI2
1	0	0	2 x VCI1	4 x VCI2
1	0	1	3 x VCI1	4 x VCI2

Notes: Set the factor of the booster 2 according to voltage of VCI2 and VCH.
When the factor is set low, current consumption can be lowered.

VC [2:0]: Set an adjustment factor for the VCI1 voltage (VC [2:0]).

Table 21. Display bias setting table

VC2	VC1	VC0	VCI1 control range
0	0	0	0.92 x VDD
0	0	1	0.87 x VDD
0	1	0	0.83 x VDD
0	1	1	0.80 x VDD
1	0	0	0.76 x VDD
1	0	1	0.73 x VDD
1	1	0	0.68 x VDD
1	1	1	VCI1 control amplifier suspends. (VCI1 can be supplied externally.)

The VSH voltage should be controlled to be less than supply voltage or device proof voltage level since VCH voltage level is generated by bias amplifier ratio corresponding to LCD driving bias value and boosting the ratio of the step-up circuit 2.

BT3: Operation/halt of voltage inverting circuit is set. BT3=”0”: voltage-inverting circuit is halted. BT3=”1”: voltage-inverting circuit is operated. See the Power-on/off Sequence section to be activated.

Table 22. BT3 Bit and Operation of Voltage Inverting Circuit

BT3	**VCL output of the voltage inverting circuit (Set VCH-VCL lower than 36v)**
0	Halt boosting
1	Output voltage between VCH and VM by inverting

The VSH voltage should be controlled to be less than supply voltage or device proof voltage level since VCH voltage level is generated by bias amplifier ratio corresponding to LCD driving bias value and boosting ratio of the step-up circuit 2.

RV0: This bit set the reference voltage generation circuit. .

Table 23. RV0 Bits and reference Voltage

RV0	**VREFL voltage**
0	VREFL can be supplied externally.
1	2.2V (Fuse adjust)

TC [1:0]: These bits can select the average temperature compensation coefficients.

The four sets of temperature compensation coefficients can be selected as follows:

Table 24. Temperature compensation table

TC[1:0]	Temperature Compensation Coefficient (at 25℃)
00	-0.05%/℃
01	-0.10%/℃
10	-0.15%/℃
11	-0.20%/℃

7. Contrast Control (R04h)

No.	RW	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R04	W	1	0	0	0	0	0	VR2	VR1	VR0	0	CT6	CT5	CT4	CT3	CT2	CT1	CT0

Contrast Control Instruction

CT [6:0]: These bits control the LCD drive voltage to adjust 128-step contrast.

Table 25. CT Bits and Contrast Control

CT6	CT5	CT4	CT3	CT2	CT1	CT0	Contrast
0	0	0	0	0	0	0	1.016R (Minimum)
0	0	0	0	0	0	1	1.008R
0	0	0	0	0	1	0	1.000R
0	0	0	0	0	1	1	0.992R
0	0	0	0	1	0	0	0.984R
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	0	0.008R
1	1	1	1	1	1	1	0.000R (Maximum)

VR [2:0]: These bits amplify 1.1 to 3.4 times the VREFL as output voltage VREFM of LCD drive reference voltage generation circuit. The VREFM should be smaller than VOUT level.

Table 26. VR Bits and VREFM Voltage

VR2	VR1	VR0	VREFM voltage
0	0	0	1.1 x VREFL
0	0	1	1.3 x VREFL
0	1	0	1.4 x VREFL
0	1	1	1.5 x VREFL
1	0	0	1.7 x VREFL
1	0	1	1.8 x VREFL
1	1	0	3.4 x VREFL
1	1	1	2.6 x VREFL

8. Entry Mode (R05h) and Compare Register (R06h):

The write data sent from the microcomputer is modified in the NT7553E and written to the DDRAM. The display data in the DDRAM can be quickly rewritten to reduce the load of the microcomputer software processing. For details, see the Graphics Operation Function section.

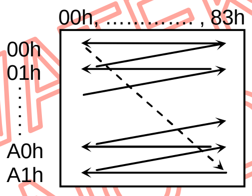
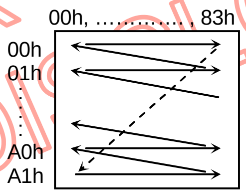
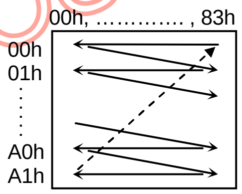
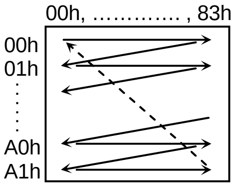
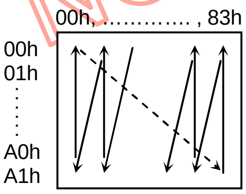
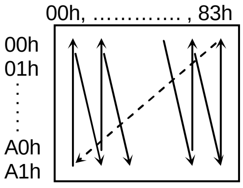
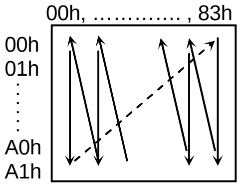
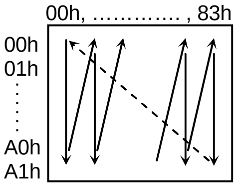
No.	RW	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R05	W	1	0	0	0	0	0	0	HWM	0	0	0	I/D1	I/D0	AM	LG2	LG1	LG0
R06	W	1	CP15	CP14	CP13	CP12	CP11	CP10	CP9	CP8	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0

Compare Register Instruction

HWM: When HWM=1, data can be written to the DDRAM at high speed. In high-speed write mode, Write to RAM four times, otherwise the four words cannot be written to the DDRAM. Thus, set the lower 2 bits to 0 when setting the RAM address. For details, see the High-Speed RAM Write Mode section.

I/D [1:0]: When I/D[1:0] = “1”, the address counter (AC) is automatically incremented by 1 after the data is written to the DDRAM. When I/D [1:0] = “0”, the AC is automatically decremented by 1 after the data is written to the DDRAM. The increment/decrement setting of the address counter by I/D[1:0] is done independently for the upper (AD[15:8]) and lower (AD[7:0]) addresses. The AM bit sets the direction of moving through the addresses when the DDRAM is written.

AM: Set the automatic update method of the AC after the data is written to the DDRAM. When AM= “0”, the data is continuously written in horizontally. When AM = “1”, the data is continuously written vertically. When window address range is specified, the DDRAM in the window address range can be written according to the I/D [1:0] and AM settings.

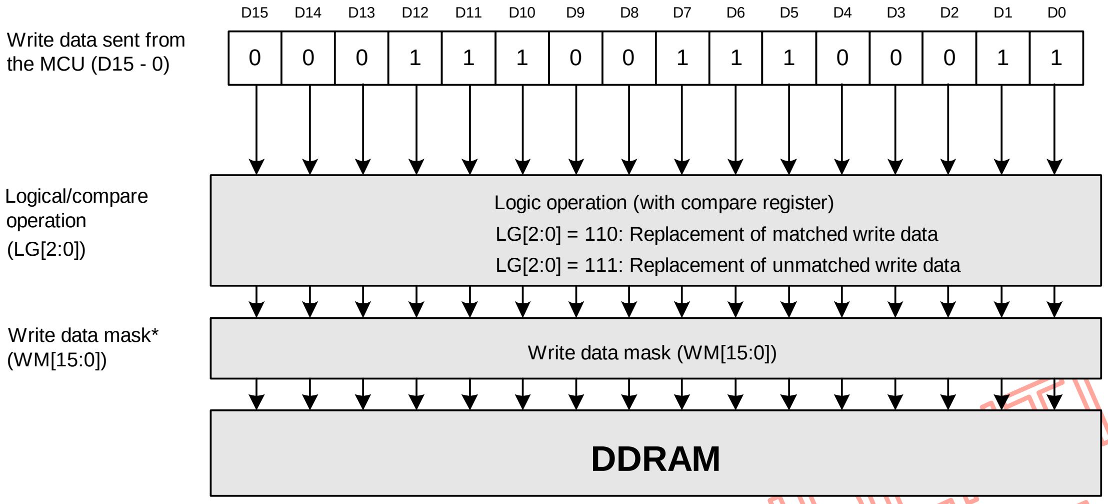
	I/D[1:0]="00" Horizontal: decrement Vertical: decrement	I/D[1:0]="01" Horizontal: increment Vertical: decrement	I/D[1:0]="10" Horizontal: decrement Vertical: increment	I/D[1:0]="11" Horizontal: increment Vertical: increment
AM = 0 Horizontal				
AM = 1 Vertical				

Note: When a window address range has been set, the DDRAM can only be written to within that range.

Figure 46. Address Direction Settings

LG [2:0]: Compare the data read from the DDRAM by the microcomputer with the compare registers (CP [15:0]) by a compare/logical operation and writes the results to DDRAM. For details, see the Logical/Compare Operation Function in page 28 for details.

CP [15:0]: Set the compare register for the compare operation with the data read from the DDRAM or written by the microcomputer**.**



Note: The write data mask (WM[15:0]) is set by the register in the RAM Write Data Mask section.

Figure 47. Logical/Compare Operations for the DDRAM

9. Display Control (R07h):

No.	RW	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R07	W	1	DIP1	DIP0	0	0	0	VLE2	VLE1	SPT	0	0	0	0	B/W	REV	D1	D0

Display Control Instruction

VLE [2:1]: When VLE1 = 1, a vertical scroll is performed in the 1st screen. When VLE2 = “1”, a vertical scroll is performed in the 2nd screen. Vertical scrolling on the two screens can be independently controlled.

SPT: When SPT = 1, the 2-division LCD drive is performed. For details, see the Screen-division Driving Function section.

B/W: When B/W = “1”, displayed data can be “all on” or “all off” regardless DDRAM contents. (B/W = “1”, REV = “0”: all dot on, B/W = “1”, REV = “1”: all dot off) When B/W = “1”, grayscale palette has to be default value.

REV: Displays all character and graphics display sections with reversal when REV = 1.Since the grayscale level can be reversed, display of the same data is enabled on normally white and normally black panels.

D [1:0]: Display is on when D1 = “1” and off when D1 = 0. When off, the display data remains in the DDRAM, and can be displayed instantly by setting D1 = “1”. When D1 is “0”, the display is off with all of the SEG/COM pin outputs set to the VSS level. Because of this, the NT7553E can control the charging current for the LCD with AC driving.
When D [1:0] = “01”, the internal display of the NT7553E is performed although the display is off. When D [1:0] = “00”, the internal display operation halts and the display is off.

Table 27. D Bits and Operation

D1	D0	SEG/COM Output	Internal Display Operation
0	0	VSS	Halt
0	1	VSS	Operate
1	0	All off display	Operate
1	1	Display	Operate

Notes: 1. Writing from the microcomputer to the DDRAM is independent from the state of D [1:0].
2. In the sleep and standby modes, D [1:0] = 00. However, the register contents of D [1:0] are not modified.

DIP [1:0]: Sets the DIP [1:0] = 11 to improve the display quality by controlling the rising time and falling time of the internal LCD output waveform. When DIP [1:0] = 00 disable this function.

10. Frame Cycle Control (R0Bh):

No.	RW	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0B	W	1	0	CLK 2	CLK 1	CLK 0	0	0	DIV 1	DIV 0	0	0	0	0	RTN 3	RTN 2	RTN 1	RTN 0

Frame Cycle Control Instruction

RTN[3:0]: Set the line retrace period (RTN[3:0]) to be added to raster-row cycles. The raster-row cycle becomes long according to the number of clocks set at RTN [3:0].

Table 28. RTN Bits and Clock Cycles

RTN3	RTN2	RTN1	RTN0	Line retrace period (Clock Cycles)	Clock Cycles per one raster-row
0	0	0	0	0 clock	26 clock
0	0	0	1	1 clock	27 clock
0	0	1	0	2 clock	28 clock
⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	0	14 clock	40 clock
1	1	1	1	15 clock	41 clock

DIV [1:0]: Set the division ratio of clocks for internal operation (DIV [1:0]). Internal operations are driven by clocks, which are frequency divided according to the DIV [1:0] setting. Frame frequency can be adjusted along with the line retrace period (RTN [3:0]). When changing the drive-duty, adjust the frame frequency. For details, see the Frame Frequency Adjustment Function section.

Table 29. DIV Bits and Clock Frequency

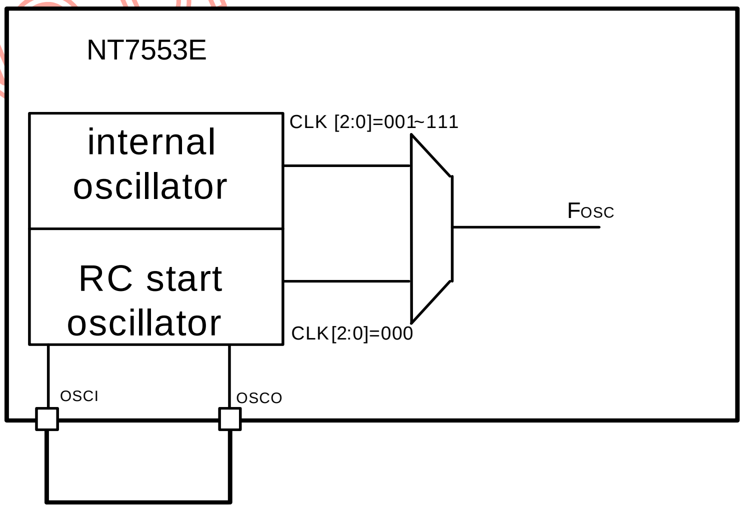
DIV1	DIV0	Division ratio	Internal Operation Clock Frequency
0	0	1	fosc/1
0	1	2	fosc/2
1	0	4	fosc/4
1	1	8	fosc/8

Formula for the frame frequency:
Frame frequency = fosc / (Clock cycles per raster-row x division ratio x 1/duty cycle) [Hz]
fosc: oscillation frequency
Duty: Drive duty (NL bit)
Division ratio: DI V bit
Clock cycles per raster-row: (RTN+26) clock

CLK [2:0]: Set the oscillation frequency clocks for operation (CLK [2:0]).

Table 30. CLK Bits and Clock oscillation Frequency

CLK2	CLK1	CLK0	Internal Operation Clock Frequency
0	0	0	R-C start oscillation
0	0	1	210kHz
0	1	0	250kHz
0	1	1	280kHz (Recommend)
1	0	0	310kHz
1	0	1	330kHz
1	1	0	360kHz
1	1	1	380kHz



11. Multi- Time Calibration Setting and Programming

No.	RW	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0D	W	1	0	0	0	0	0	0	0	MTPT	0	0	0	MT4	MT3	MT2	MT1	MT0
R0E	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PG
	R	1	0	0	0	0	0	0	0	0	PG	PM2	PM1	MP4	MP3	MP2	MP1	MP0

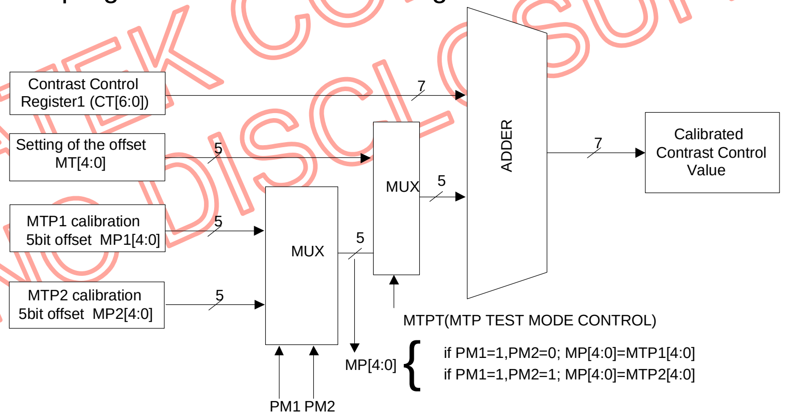
Multi- Time Calibration Setting and Programming Instruction

MT [4:0]: This command sets the offset value of contrast

Table 31. The Setting of the offset value of contrast

MT[4:0]	Offset Value	MT[4:0]	Offset Value	MT[4:0]	Offset Value	MT[4:0]	Offset Value
00000	Original	01000	+8 step	10000	Original	11000	-8 step
00001	+1 step	01001	+9 step	10001	-15 step	11001	-7 step
00010	+2 step	01010	+10 step	10010	-14 step	11010	-6 step
00011	+3 step	01011	+11step	10011	-13 step	11011	-5 step
00100	+4 step	01100	+12 step	10100	-12 step	11100	-4 step
00101	+5 step	01101	+13 step	10101	-11 step	11101	-3 step
00110	+6 step	01110	+14 step	10110	-10 step	11110	-2 step
00111	+7 step	01111	+15 step	10111	- 9 step	11111	-1 step

PG: When PG = 1, start to program LCD driver with MTP offset value.
MP [4:0]: It can read the programmed data with this register.



MTPT	PM bits		MP[4:0]	Calibrated Contrast Control Value [6:0]
0 (Default)	PM2	0	MTP 2 is not programmed	CT[6:0] (if PM1 = 0)
		1	MTP 2 is programmed	MP2[4:0] + CT[6:0]
	PM1	0	MTP 1 is not programmed	CT[6:0]
		1	MTP 1 is programmed	MP1[4:0] + CT[6:0]
1	PM2	0	Don't care; the programmed data of MTP will be bypass.	MT[4:0] + CT[6:0]
		1		
	PM1	0		
		1		

Table 32. The Setting of the PM1, PM2 and MTPT

12. Vertical Scroll Control (R11h):

No.	RW	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R11	W	1	VL27	VL26	VL25	VL24	VL23	VL22	VL21	VL20	VL17	VL16	VL15	VL14	VL13	VL12	VL11	VL10

Vertical Scroll Control Instruction

VL1 [7:0]: Specify the display-start raster-row at the 1st screen display for vertical smooth scrolling. Any raster-row from the first to 162th can be selected. After the 162th raster-row is displayed, the display restarts from the first raster-row. The display-start raster-row (VL1 [7:0]) is valid only when VLE1 = “1”. The raster-row display is fixed when VLE1 = “0”. (VLE1 is the 1st -screen vertical-scroll enable bit.) VL2 [7:0]: Specify the display-start raster-row at the 2nd screen display. The display-start raster-row (VL2 [7:0]) is valid only when VLE2 = “1”. The raster-row display is fixed when VLE2 = “0”. (VLE2 is the 1st -screen vertical-scroll enable bit.)

Table 33. VL Bits and Display Start Line Control

VL27 **VL17**	**VL26** **VL16**	**VL25** **VL15**	**VL24** **VL14**	**VL23** **VL13**	**VL22** **VL12**	**VL21** **VL11**	**VL20** **VL10**	**Display start line**
0	0	0	0	0	0	0	0	**1st raster - row**
0	0	0	0	0	0	0	1	**2nd raster - row**
0	0	0	0	0	0	1	0	**3rd raster - row**
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	0	1	0	0	0	0	0	**161th raster - row**
1	0	1	0	0	0	0	1	**162th raster - row**

Note: Do not set over the 162th ("A1"H) raster - row

13. 1st Screen Driving Position (R14h) and 2nd Screen Driving Position (R15h):

No.	RW	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R14	W	1	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
R15	W	1	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20

Screen Driving Position Instructions

SS1 [7:0]: Specify the driving start position for the first screen in a line unit. The LCD driving starts from the 'set value+1' common driver.

SE1 [7:0]: Specify the driving end position for the first screen in a line unit. The LCD driving is performed to the 'set value +1 ' common driver. For instance, when SS1 [7:0] = “07”h and SE1 [7:0] = “10”h are set, the LCD driving is performed from COM8 to COM17, and non-selection driving is performed from COM1 to COM7, COM18 and others. Ensure that SS1[7:0] ≦ SE1[7:0] ≦ “A1”h. For details, see the Screen-division Driving Function section.

SS2 [7:0]: Specify the driving start position for the second screen in a line unit. The LCD driving starts from the 'set value+1' common driver. The second screen is driven when SPT = “1”.

SE2 [7:0]: Specify the driving end position for the second screen in a line unit. The LCD driving is performed to the 'set value+1' common driver. For instance, when SPT = “1”, SS2 [7:0] = “20”H, and SE2 [7:0] = “4F”h are set, the LCD driving is performed from COM33 to COM80. Ensure that SS1 [7:0] ≤ SE1 [7:0] ≤ SS2 [7:0] ≤ SE2 [7:0] ≤ DUTYSET ≤ “A1”h. For details, see the Screen-division Driving Function section.

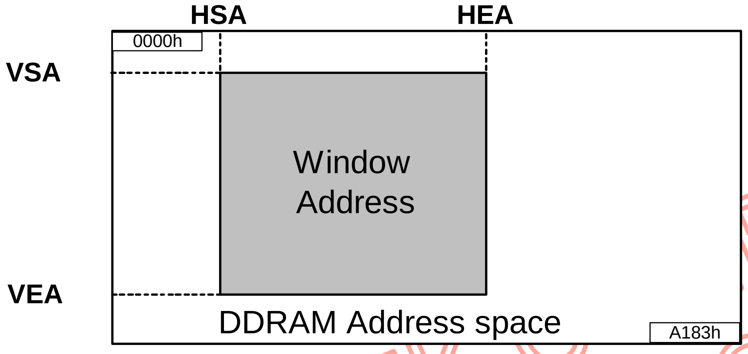
14. Horizontal RAM Address Position (R16h) and Vertical RAM Address Position (R17h):

No.	RW	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R16	W	1	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
R17	W	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0

Horizontal/Vertical RAM Address Position Instruction

HSA [7:0]/HEA [7:0]: Specify the horizontal start/end positions of a window for access in memory. Data can be written to the DDRAM from the address specified by HEA [7:0] from the address specified by HSA [7:0]. Note that an address must be set before RAM is written. Ensure “00”h ≤ HSA [7:0] ≤HEA [7:0] ≤ “83”h

VSA [7:0]/VEA [7:0]: Specify the vertical start/end positions of a window for access in memory. Data can be written to the DDRAM from the address specified by VEA [7:0] from the address specified by VSA [7:0]. Note that an address must be set before RAM is written to. Ensure “00”h ≤ VSA [7:0] ≤ VEA [7:0] ≤ “A1”h.



Window address setting range:
00h HSA7-0 HEA7-0 83h
00h VSA7-0 VEA7-0 A1h

Figure 48. Window Address Setting Range

Notes: 1. Ensure that the window address area is within the DDRAM address space.
2. In high-speed write mode, data are written to DDRAM in four-words. Thus, dummy write operations should be inserted depending on the window address area. For details, see the High-Speed Burst RAM Write Function section.

15. RAM Write Data Mask (R20h)

No.	RW	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R20	W	1	WM 15	WM 14	WM 13	WM 12	WM 11	WM 10	WM 9	WM 8	WM 7	WM 6	WM 5	WM 4	WM 3	WM 2	WM 1	WM 0

RAM Write Data Mask Instruction

WM [15:0]: In writing to the DDRAM, these bits mask writing in a bit unit. When WM15 = “1”, this bit masks the write data of D15 and does not write to the DDRAM. Similarly, the WM14 to 0 bits mask the write data of D14 to D0 in a bit unit.

16. RAM Address Set (R21h)

No.	RW	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R21	W	1	AD 15	AD 14	AD 13	AD 12	AD 11	AD 10	AD 9	AD 8	AD 7	AD 6	AD 5	AD 4	AD 3	AD 2	AD 1	AD 0

RAM Address Set Instruction

AD [15:0]: Initially set DDRAM addresses to the address counter (AC). Once the DDRAM data is written, the AC is automatically updated according to the AM and I/D bit settings. This allows consecutive access without resetting addresses. Once the DDRAM data is read, the AC is not automatically updated.

DDRAM address setting is not allowed in the standby mode. Ensure that the address is set within the specified window address.

Table 34. DDRAM Address Range

AD15 to AD0	DDRAM Setting
"0000"h to “0083"h	Bitmap data for COM1
"0100"h to "0183"h	Bitmap data for COM2
"0200"h to "0283"h	Bitmap data for COM3
"0300"h to "0383"h	Bitmap data for COM4
⋮	⋮
"9E00"h to "9E83"h	Bitmap data for COM159
"9F00"h to "9F83"h	Bitmap data for COM160
"A000"h to "A083"h	Bitmap data for COM161
"A100"h to "A183"h	Bitmap data for COM162

17. Write Data to DDRAM (R22h)

No.	RW	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R22	W	1	WD 15	WD 14	WD 13	WD 12	WD 11	WD 10	WD 9	WD 8	WD 7	WD 6	WD 5	WD 4	WD 3	WD 2	WD 1	WD 0

Write Data to DDRAM Instructions

WD [15:0]: Write 16-bit data to the DDRAM; this data calls each grayscale palette. After a write, the address is automatically updated according to the AM and I/D bit settings. During stand by mode, the DDRAM cannot be accessed.

DDRAM writes data during normal mode (16 bit mode)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
WD 15	WD 14	WD 13	WD 12	WD 11	WD 10	WD 9	WD 8	WD 7	WD 6	WD 5	WD 4	WD 3	WD 2	WD 1	WD 0
P04	P03	P02	P01	P00	P14	P13	P12	P11	P10	0	P24	P23	P22	P21	P20
SEG(n)					SEG(n+1)						SEG(n+2)				

* **WD5** is dummy bit must fixed this bit to **"0"**

DDRAM writes data during normal mode (8 bit mode)

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1st write	WD 15	WD 14	WD 13	WD 12	WD 11	WD 10	WD 9	WD 8	WD 7	WD 6	WD 5	WD 4	WD 3	WD 2	WD 1	WD 0
	SEG(n)					SEG(n+1)			Fixed these pins to VDD or VSS							
2nd write	WD 15	WD 14	WD 13	WD 12	WD 11	WD 10	WD 9	WD 8								
	SEG(n+1)		0	SEG(n+2)												

* **WD13** is dummy bit must fixed this bit to **"0"** while 2nd write cycle.

18. Read Data to DDRAM (R22h)

No.	RW	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R22	R	1	RD 15	RD 14	RD 13	RD 12	RD 11	RD 10	RD 9	RD 8	RD 7	RD 6	RD 5	RD 4	RD 3	RD 2	RD 1	RD 0

Read Data from DDRAM Instruction

RD [15:0]: Read 16-bit data from the DDRAM. When the data is read to the microcomputer, the first-word read immediately after the DDRAM address setting is latched from the DDRAM to the internal read-data latch. The data on the data bus (D[15:0]) becomes invalid and the second-word read is normal.

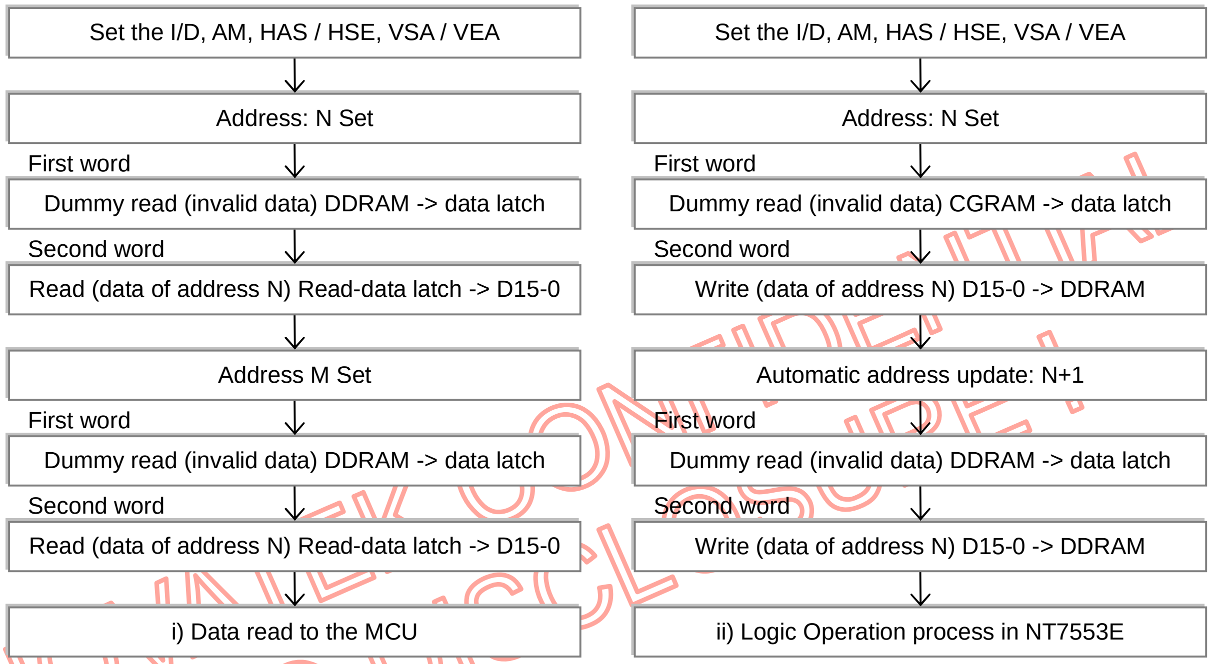


Figure 49. DDRAM Read Sequence

19. Grayscale Palette Control (R30h to R3Fh):

No.	RW	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R30	W	1	0	0	PK 15	PK 14	PK 13	PK 12	PK 11	PK 10	0	0	PK 5	PK 4	PK 3	PK 2	PK 1	PK 0
R31	W	1	0	0	PK 35	PK 34	PK 33	PK 32	PK 31	PK 30	0	0	PK 25	PK 24	PK 23	PK 22	PK 21	PK 20
R32	W	1	0	0	PK 55	PK 54	PK 53	PK 52	PK 51	PK 50	0	0	PK 45	PK 44	PK 43	PK 42	PK 41	PK 40
R33	W	1	0	0	PK 75	PK 74	PK 73	PK 72	PK 71	PK 70	0	0	PK 65	PK 64	PK 63	PK 62	PK 61	PK 60
R34	W	1	0	0	PK 95	PK 94	PK 93	PK 92	PK 91	PK 90	0	0	PK 85	PK 84	PK 83	PK 82	PK 81	PK 80
R35	W	1	0	0	PK 115	PK 114	PK 113	PK 112	PK 111	PK 110	0	0	PK 105	PK 104	PK 103	PK 102	PK 101	PK 100
R36	W	1	0	0	PK 135	PK 134	PK 133	PK 132	PK 131	PK 130	0	0	PK 125	PK 124	PK 123	PK 122	PK 121	PK 120
R37	W	1	0	0	PK 155	PK 154	PK 153	PK 152	PK 151	PK 150	0	0	PK 145	PK 144	PK 143	PK 142	PK 141	PK 140
R38	W	1	0	0	PK 175	PK 174	PK 173	PK 172	PK 171	PK 170	0	0	PK 165	PK 164	PK 165	PK 162	PK 161	PK 160
R39	W	1	0	0	PK 195	PK 194	PK 193	PK 192	PK 191	PK 190	0	0	PK 185	PK 184	PK 183	PK 182	PK 181	PK 180
R3A	W	1	0	0	PK 215	PK 214	PK 213	PK 212	PK 211	PK 210	0	0	PK 205	PK 204	PK 203	PK 202	PK 201	PK 200
R3B	W	1	0	0	PK 235	PK 234	PK 233	PK 232	PK 231	PK 230	0	0	PK 225	PK 224	PK 223	PK 222	PK 221	PK 220
R3C	W	1	0	0	PK 255	PK 254	PK 253	PK 252	PK 251	PK 250	0	0	PK 245	PK 244	PK 243	PK 242	PK 241	PK 240
R3D	W	1	0	0	PK 275	PK 274	PK 273	PK 272	PK 271	PK 270	0	0	PK 265	PK 264	PK 263	PK 262	PK 261	PK 260
R3E	W	1	0	0	PK 295	PK 294	PK 293	PK 292	PK 291	PK 290	0	0	PK 285	PK 284	PK 283	PK 282	PK 281	PK 280
R3F	W	1	0	0	PK 315	PK 314	PK 313	PK 312	PK 311	PK 310	0	0	PK 305	PK 304	PK 303	PK 302	PK 301	PK 300

Table 35. Grayscale Palette Control Instruction

PK [31:0]: Specify the grayscale level for thirty-two palettes from the 52-grayscale levels. For details, see the Grayscale Palette and the Grayscale Palette Table sections.

General Command Table

				Upper Code								Lower Code								
Reg. No.	**Register Name**	**R/W**	**A0**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Description**	**Exe-cution Cycle**
IR	Index	0	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0	Sets the index register value	0
SR	Status read	1	0	L7	L6	L5	L4	L3	L2	L1	L0	0	C6	C5	C4	C3	C2	C1	C0	Reads the setting of N-line inversion L[7:0] and contrast setting C[6:0]	0
R00	Start oscillation	0	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1	Starts the oscillation mode	10 ms
	Device code read	1	1	0	1	1	1	0	1	0	1	0	0	1	0	0	0	1	1	Reads 7553h	0
R01	Driver output control	0	1	0	0	0	0	0	0	CMS	SGS	0	0	0	NL4	NL3	NL2	NL1	NL0	Sets the common driver shift direction (CMS), segment driver shift direction (SGS), driving duty ratio (NL[4:0])	0
R02	LCD Drive-waveform control	0	1	0	0	0	0	0	RST	B/C	EOR	0	0	NW5	NW4	NW3	NW2	NW1	NW0	Sets the LCD drive AC waveform (B/C), EOR output (EOR), the number of N-line inversion (NW[4:0]) at C-type LCD driver, and software reset (RST).	0
R03	Power control 1	0	1	BS3	BS2	BS1	BS0	BT3	BT2	BT1	BT0	0	DC2	DC1	DC0	AP1	AP0	SLP	STB	Sets the sleep mode (SLP), standby mode (STB), LCD power on (AP[1:0]), boosting cycle (DC[3:0]), boosting output multiplying factor (BT[2:0]), operation of voltage inverting circuit (BT3), and LCD driver bias value (BS[3:0]).	0
R04	Contrast control	0	1	0	0	0	0	0	VR2	VR1	VR0	0	CT6	CT5	CT4	CT3	CT2	CT1	CT0	Sets the regulator adjustment (VR[2:0]) and contrast adjustment (CT[6:0])	0
R05	Entry mode	0	1	0	0	0	0	0	0	HWM	0	0	0	I/D1	I/D0	AM	LG2	LG1	LG0	Specifies the logical operation (LG[2:0]), AC counter mode (AM[1:0]), increment/ decrement mode (I/D[1:0]), high-speed write mode (HWM).	0
R06	Compare register	0	1	CP15	CP14	CP13	CP12	CP11	CP10	CP9	CP8	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0	Specifies the compare register (CP[15:0]).	0
R07	Display control	0	1	DIP1	DIP0	0	0	0	VLE2	VLE1	SPT	0	0	0	0	B/W	REV	D1	D0	Control Specifies display on (D[1:0]), black-and-white reversed display (REV), all on/off (B/W), screen division (SPT), and vertical scroll (VLE[2:1])	0
R0B	Frame frequency control	0	1	0	CLK2	CLK1	CLK0	0	0	DIV1	DIV0	0	0	0	0	RTN3	RTN2	RTN1	RTN0	Specifies the line retrace period (RTN[3:0]) and operating clock frequency division ratio (DIV[1:0])	0
R0C	Power control 2	0	1	0	0	0	0	0	0	TC1	TC0	0	0	0	RV0	0	VC2	VC1	VC0	Sets the adjustment factor for the VCI voltage (VC[2:0])	0
R0D	MTP setting	0	1	0	0	0	0	0	0	0	MTPT	0	0	0	MT4	MT3	MT2	MT1	MT0	This command set the offset value of contrast (MT[4:0])	0
R0E	MTP programming	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PG	This command starts to program LCD driver with OTC offset value (PG)	2s
R11	Vertical scroll control	0	1	VL27	VL26	VL25	VL24	VL23	VL22	VL21	VL20	VL17	VL16	VL15	VL14	VL3	VL12	VL11	VL10	Sets the 1st screen display start line (VL[17:10]) and 2nd screen display start line (VL[27:20]).	0
R14	1st screen driving position	0	1	SE 17	SE 16	SE 15	SE 14	SE 13	SE 12	SE 11	SE 10	SS 17	SS 16	SS 15	SS 14	SS 13	SS 12	SS 11	SS 10	Sets 1st screen start (SS1[7:0]) and end (SE1[7:0]).	0
R15	2nd screen driving position	0	1	SE 27	SE 26	SE 25	SE 24	SE 23	SE 22	SE 21	SE 20	SS 27	SS 26	SS 25	SS 24	SS 23	SS 22	SS 21	SS 20	Sets 2nd screen start (SS2[7:0]) and end (SE2[7:0]).	0

General Command Table (Continued)

Reg. No.	Register Name	R/W	A0	Upper Code								Lower Code								Description	Execution Cycle
				D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0		
R16	Horizontal RAM address position	0	1	HEA 7	HEA 6	HEA 5	HEA 4	HEA 3	HEA 2	HEA 1	HEA 0	HSA 7	HSA 6	HSA 5	HSA 4	HSA 3	HSA 2	HSA 1	HSA 0	Sets start (HSA[7:0]) and end (HEA[7:0]) of the horizontal RAM address range.	0
R17	Vertical RAM address position	0	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	Sets start (VSA[7:0]) and end (VEA[7:0]) of the vertical RAM address range.	0
R20	RAM write data mask	0	1	WM 15	WM 14	WM 13	WM 12	WM 11	WM 10	WM 9	WM 8	WM 7	WM 6	WM 5	WM 4	WM 3	WM 2	WM 1	WM 0	Specifies write data mask (WM[15:0]) at RAM write	0
R21	RAM address set	0	1	AD[15:8] (upper)								AD[7:0] (lower)								Initially set the RAM address to the counter (AC)	0
R22	RAM data write	0	1	Write data (upper)								Write data (lower)								Write data to the RAM	0
	RAM data read	1	1	Read data (upper)								Read data (lower)								Read data from the RAM	0
R30	Grayscale palette control 1	0	1	0	0	PK15	PK14	PK13	PK12	PK11	PK10	0	0	PK05	PK04	PK03	PK02	PK01	PK00	Specified the grayscale palette 1	0
R31	Grayscale palette control 2	0	1	0	0	PK35	PK34	PK33	PK32	PK31	PK30	0	0	PK25	PK24	PK23	PK22	PK21	PK20	Specified the grayscale palette 2	0
R32	Grayscale palette control 3	0	1	0	0	PK55	PK54	PK53	PK52	PK51	PK50	0	0	PK45	PK44	PK43	PK42	PK41	PK40	Specified the grayscale palette 3	0
R33	Grayscale palette control 4	0	1	0	0	PK75	PK74	PK73	PK72	PK71	PK70	0	0	PK65	PK64	PK63	PK62	PK61	PK60	Specified the grayscale palette 4	0
R34	Grayscale palette control 5	0	1	0	0	PK95	PK94	PK93	PK92	PK91	PK90	0	0	PK85	PK84	PK83	PK82	PK81	PK80	Specified the grayscale palette 5	0
R35	Grayscale palette control 6	0	1	0	0	PK 115	PK 114	PK 113	PK 112	PK 111	PK 110	0	0	PK 105	PK 104	PK 103	PK 102	PK 101	PK 100	Specified the grayscale palette 6	0
R36	Grayscale palette control 7	0	1	0	0	PK 135	PK 134	PK 133	PK 132	PK 131	PK 130	0	0	PK 125	PK 124	PK 123	PK 122	PK 121	PK 120	Specified the grayscale palette 7	0
R37	Grayscale palette control 8	0	1	0	0	PK 155	PK 154	PK 153	PK 152	PK 151	PK 150	0	0	PK 145	PK 144	PK 143	PK 142	PK 141	PK 140	Specified the grayscale palette 8	0
R38	Grayscale palette control 9	0	1	0	0	PK 175	PK 174	PK 173	PK 172	PK 171	PK 170	0	0	PK 165	PK 164	PK 163	PK 162	PK 161	PK 160	Specified the grayscale palette 9	0
R39	Grayscale palette control 10	0	1	0	0	PK 195	PK 194	PK 193	PK 192	PK 191	PK 190	0	0	PK 185	PK 184	PK 183	PK 182	PK 181	PK 180	Specified the grayscale palette 10	0
R3A	Grayscale palette control 11	0	1	0	0	PK 215	PK 214	PK 213	PK 212	PK 211	PK 210	0	0	PK 205	PK 204	PK 203	PK 202	PK 201	PK 200	Specified the grayscale palette 11	0
R3B	Grayscale palette control 12	0	1	0	0	PK 235	PK 234	PK 233	PK 232	PK 231	PK 230	0	0	PK 215	PK 214	PK 213	PK 212	PK 211	PK 210	Specified the grayscale palette 12	0
R3C	Grayscale palette control 13	0	1	0	0	PK 255	PK 254	PK 253	PK 252	PK 251	PK 250	0	0	PK 245	PK 244	PK 243	PK 242	PK 241	PK 240	Specified the grayscale palette 13	0
R3D	Grayscale palette control 14	0	1	0	0	PK 275	PK 274	PK 273	PK 272	PK 271	PK 270	0	0	PK 265	PK 264	PK 263	PK 262	PK 261	PK 260	Specified the grayscale palette 14	0
R3E	Grayscale palette control 15	0	1	0	0	PK 295	PK 294	PK 293	PK 292	PK 291	PK 290	0	0	PK 285	PK 284	PK 283	PK 282	PK 281	PK 280	Specified the grayscale palette 15	0
R3F	Grayscale palette control 16	0	1	0	0	PK 315	PK 314	PK 313	PK 312	PK 311	PK 310	0	0	PK 305	PK 304	PK 303	PK 302	PK 301	PK 300	Specified the grayscale palette 16	0

Absolute Maximum Rating

DC Supply Voltage1 (VDD, VDD2)…………………………………………………… -0.3V to +4.6V
DC Supply Voltage2 (VCI1) ……………………………………………………… -0.3V to +4.6V
DC Supply Voltage3 (VCH - VCL) ………………………………………………… -0.3V to +36.0V
DC Supply Voltage4 (VOUT) ……………………………………………………… -0.3V to +6.5V
Input Voltage ……………………………………………………………… -0.3V to VDD+0.3V
Operating Ambient Temperature ………………………………………………-40°C to +85°C
Storage Temperature ……………………………………………………………-55°C to +110°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

DC Characteristics

(VSS = 0V, VDD = 2.4 ~ 3.6V, VCH-VCL=8V to 36V, Ta = - 40 to 85°C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
VDD	Operating Voltage	2.4	2.8	3.6	V	
VDD2	Operating Voltage	VDD	-	3.6	V	
VCC	Operating Voltage	1.6	1.9	2.3	V	For dual power supply mode
VDDR	Operating Voltage	1.8	1.9	2.0	V	For single power supply to VCC
IDD	Dynamic Current Consumption 1	-	480	600	µA	VDD, VDD2 = 3.0V, VCH = 19.2V, VM = 1.6V, VCL = -16V, fosc = 280KHz (1/162duty), 1/11bias, CT = 0, AP = 01, display on, display data = all on and no MPU access, Ta = 25°C, Boost1 = 2X, Boost2 = 4X, VCI1 = 0.92 x VDD, with oscillation. Step up cycle of step up circuit 2: 128 divided cycle
ISB	Standby Mode Current Consumption	-	5	15	µA	During standby mode, Ta = 25°C
		-	-	50		During standby mode, Ta = 85°C
ISLP	Sleep Mode Current Consumption		70	100	µA	During standby mode, Ta = 25°C
				150		During standby mode, Ta = 85°C
ILI	Input Leakage Current	-1.0	-	1.0	µA	VIN = VDD or VSS (S/P, C86, S8/16, A0, R/W (RDB),E(WRB),CSB,RESB)
IHZ	HZ Leakage Current	-3.0	-	3.0	µA	When the D0 - D15, are in high impedance
VIH	High-level Input Voltage	0.80 x VDD	-	VDD	V	A0, R/W (RDB),E(WRB),CSB,RESB, D0 - D15, OSCI, C86, S/P, S8/16
VIL	Low-level Input Voltage	VSS	-	0.20 x VDD	V	
VOH	High-level Output Voltage	0.80 x VDD	-	VDD	V	VDD = 2.4 ~ 3.6V, IOH = -0.1mA (D0 - D15)
VOL	Low -level Output Voltage	VSS	-	0.20 x VDD	V	VDD = 2.4 ~ 3.6V, IOL = 0.1mA (D0 - D15)

DC Characteristics (Continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
fosc	Oscillation Clock	266	280	294	kHz	VDD = 3.0V, TA = 25°C
fEXT	External Oscillation Clock	151	275	640	kHz	VDD2 = 2.4 ~ 3.6V
fDUTY	External Oscillation Clock Duty	45	50	55	%	VDD2 = 2.4 ~ 3.6V
trosc	External Oscillation Rise Time	--	--	0.2	µs	VDD2= 2.4 ~ 3.6V
tfosc	External Oscillation Fall Time	--	--	0.2	µs	VDD2 = 2.4 ~ 3.6V
RSEG	LCD SEG Driver ON Resistance	-	0.35	3	KΩ	Id = +/- 0.05mA, VSH = 3V
RCOM	LCD COM Driver ON Resistance	-	0.9	3	KΩ	Id = +/-0.05mA, VCH - VCL = 36V
VREF	Internal Reference Voltage	2.15	2.2	2.25	V	Ta = 25°C
VCI2	Boost Circuit2 Output Voltage	-	-	VOUT	V	
VREFL	Input Voltage	-	-	VDD	V	
VREFM	Output Voltage	-	-	VOUT -0.5	V	
VOUT	Step up circuit 1	5.25	5.48	-	V	VDD = 3.0V，VCI factor=0.92，Step up factor: two times，Step up cycle: 32 divided cycle，Load current = 400uA
VCH	Step up circuit 2	19.55	19.75	19.95	V	VDD = 3.0V，VOUT=5.5V，VREFL = 2.2V，VREFM = 1.5 x VREFL，Constant current of operation amplifier: small Contrast adjustment value = 0.000R 1/11 bias，Step up cycle of step up circuit 2: 96 divided cycle，Step up factor: Four times VM=1.65V, display on, display data = all on
VCL	Step up circuit 3	-16.55	-16.45	-16.25	V	VDD = 3.0V，VOUT=5.5V，VREFL = 2.2V，VREFM= 1.5 x VREFL，Constant current of operation amplifier: small Contrast adjustment value = 0.000R 1/11 bias，Step up cycle of polarity inversion circuit: 96 divided cycle Step up factor: Four times VM=1.65V, display on, display data = all on

Note: Voltages VCH≥VSH≥VM≥VSS2≥VCL must always be satisfied.

AC Characteristics (TA = -40°C ~ +85°C, unless otherwise noted)

1. System Buses Read/Write Characteristics (for 8080 Series MPU)
(VDD = VCC = 1.6 ~ 2.3V, TA = -40 ~ 85°C) (Dual power supply mode)

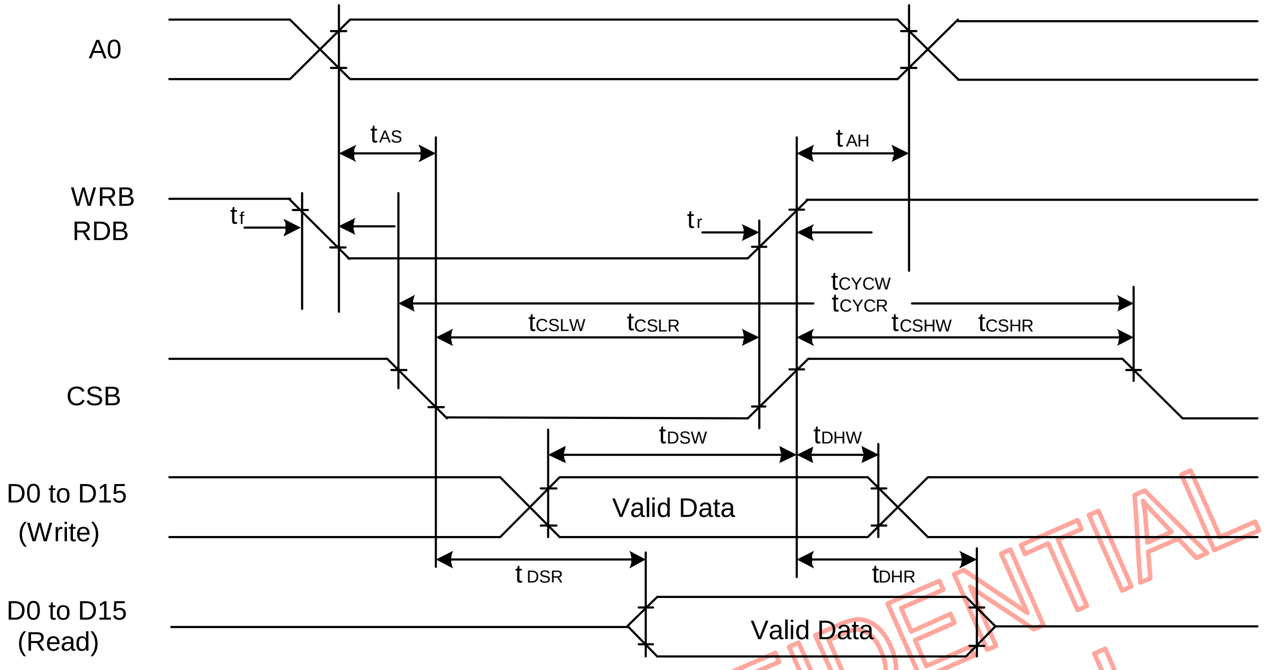


Figure 50. 80-system Bus Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{AS}	Address setup time	10	-	-	ns	
t_{AH}	Address hold time	5	-	-	ns	
t_{CYCW}	Write system cycle time	600 200	- -	- -	ns	Normal Mode (HWM = 0) High-Speed Write (HWM = 1)
t_{CYCR}	Read system cycle time	800			ns	
t_{CSLW}	Write control L pulse width	90	-	-	ns	
t_{CSHW}	Write control H pulse width	300 90	-	-	ns	Normal Mode (HWM = 0) High-Speed Write (HWM = 1)
t_{CSLR}	Read control L pulse width	350	-	-	ns	
t_{CSHR}	Read control H pulse width	400	-	-	ns	
t_r / t_f	Rise time / Fall time	-	-	25	ns	
t_{DSW}	Write data setup time	60	-	-	ns	
t_{DHW}	Write data hold time	15	-	-	ns	
t_{DSR}	Read data setup time	-	-	200	ns	C_L = 50pF
t_{DHR}	Read data hold time	5	-	-	ns	C_L = 50pF

2. System Buses Read/Write Characteristics (for 8080 Series MPU)
(VDD = 2.4 ~ 3.6V, VCC = VDDR =1.9±0.1V, TA = -40 ~ 85°C) (Single power supply mode)

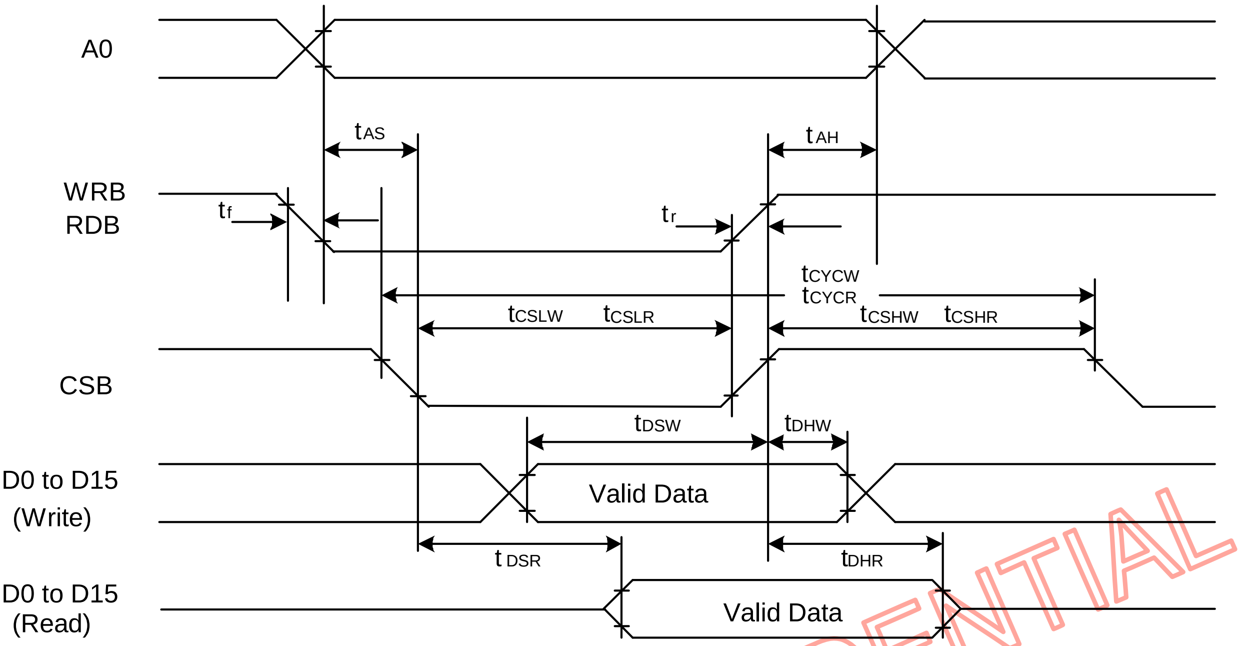


Figure 51. 80-system Bus Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{AS}	Address setup time	10			ns	
t_{AH}	Address hold time	2	-	-	ns	
t_{CYCW}	Write system cycle time	200	-	-	ns	Normal Mode (HWM = 0)
		100	-	-		High-Speed Write (HWM = 1)
t_{CYCR}	Read system cycle time	300			ns	
t_{CSLW}	Write control L pulse width	40	-	-	ns	
t_{CSHW}	Write control H pulse width	100	-	-	ns	Normal Mode (HWM = 0)
		40				High-Speed Write (HWM = 1)
t_{CSLR}	Read control L pulse width	150	-	-	ns	
t_{CSHR}	Read control H pulse width	100	-	-	ns	
t_r / t_f	Rise time / Fall time	-	-	25	ns	
t_{DSW}	Write data setup time	60	-	-	ns	
t_{DHW}	Write data hold time	2	-	-	ns	
t_{DSR}	Read data setup time	-	-	100	ns	C_L = 50pF
t_{DHR}	Read data hold time	5	-	-	ns	C_L = 50pF

3. System Buses Read/Write Characteristics (for 6800 Series MPU)
(VDD = VCC = 1.6 ~ 2.3V, TA = -40 ~ 85°C) (Dual power supply mode)

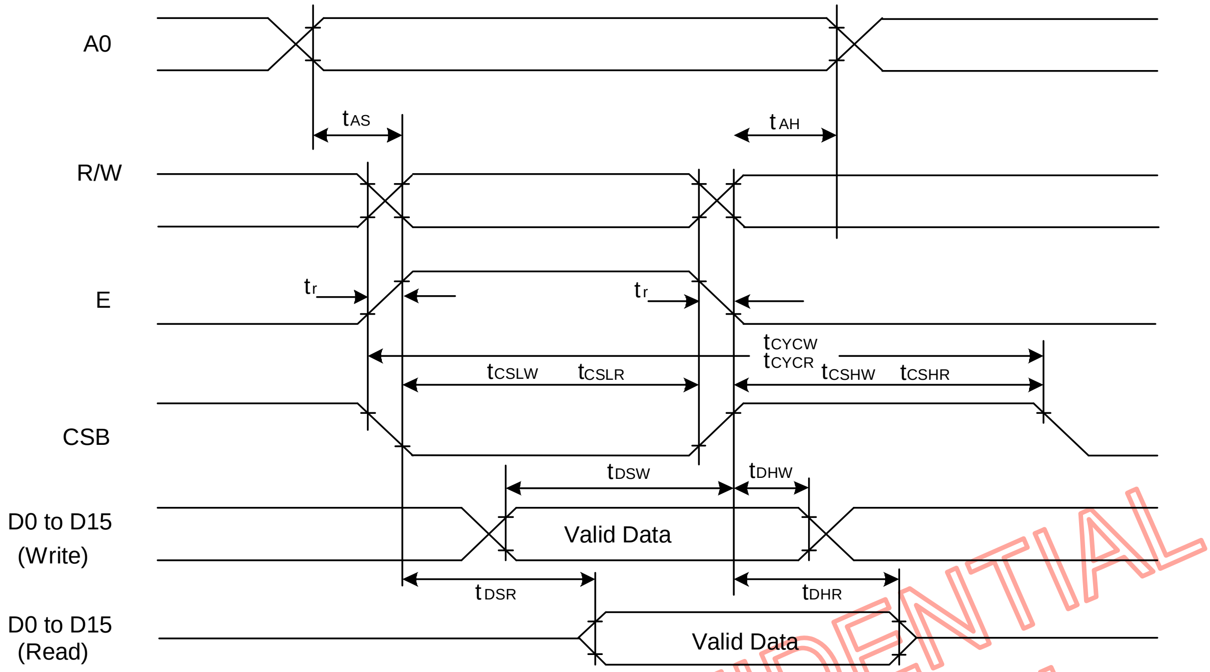


Figure 52. 68-system Bus Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{as}	Address setup time	10	-	-	ns	
t_{AH}	Address hold time	5	-	-	ns	
t_{CYCW}	Write system cycle time	600 200	- -	- -	ns	Normal Mode (HWM = 0) High-Speed Write (HWM = 1)
t_{CYCR}	Read system cycle time	800			ns	
t_{CSLW}	Write control L pulse width	90	-	-	ns	
t_{CSHW}	Write control H pulse width	300 90	-	-	ns	Normal Mode (HWM = 0) High-Speed Write (HWM = 1)
t_{CSLR}	Read control L pulse width	350	-	-	ns	
t_{CSHR}	Read control H pulse width	400	-	-	ns	
t_r / t_f	Rise time / Fall time	-	-	25	ns	
t_{DSW}	Write data setup time	60	-	-	ns	
t_{DHW}	Write data hold time	15	-	-	ns	
t_{DSR}	Read data setup time	-	-	200	ns	C_L = 50pF
t_{DHR}	Read data hold time	5	-	-	ns	C_L = 50pF

4. System Buses Read/Write Characteristics (for 6800 Series MPU)

(VDD = 2.4 ~ 3.6V, VCC = VDDR = 1.9±0.1V, TA = -40 ~ 85°C) (Single power supply mode)

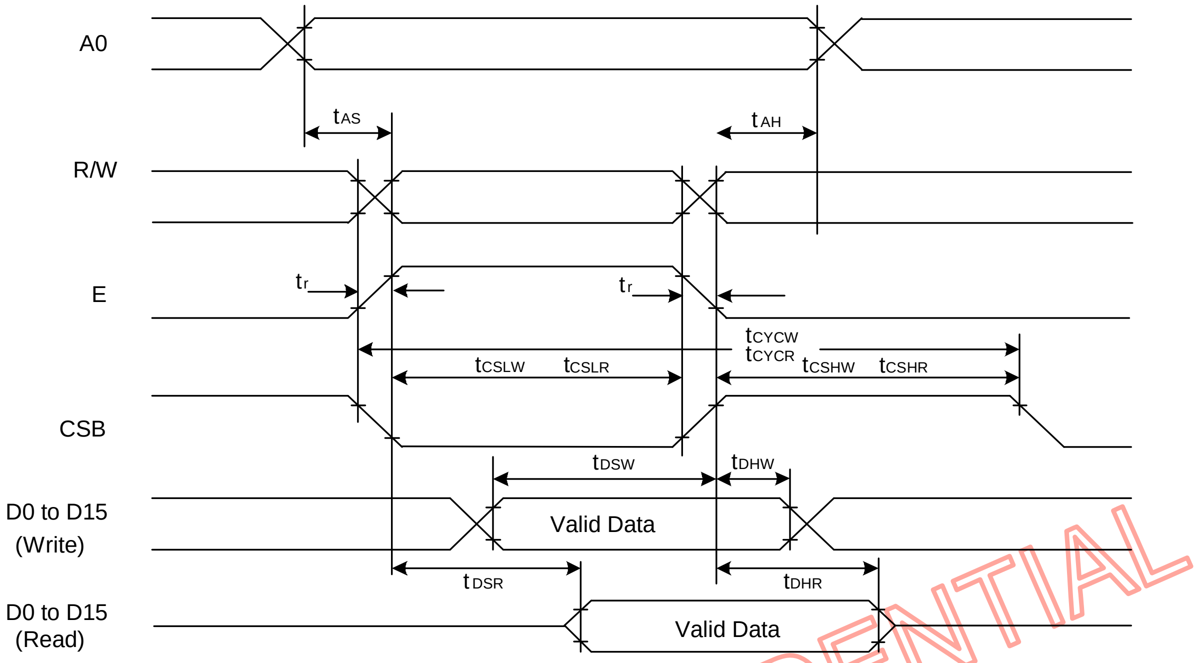


Figure 53. 68-system Bus Timing for

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{AS}	Address setup time	10			ns	
t_{AH}	Address hold time	2	-	-	ns	
t_{CYCW}	Write system cycle time	200 100	- -	- -	ns	Normal Mode (HWM = 0) High-Speed Write (HWM = 1)
t_{CYCR}	Read system cycle time	300			ns	
t_{CSLW}	Write control L pulse width	40	-	-	ns	
t_{CSHW}	Write control H pulse width	100 40	-	-	ns	Normal Mode (HWM = 0) High-Speed Write (HWM = 1)
t_{CSLR}	Read control L pulse width	150	-	-	ns	
t_{CSHR}	Read control H pulse width	100	-	-	ns	
t_r / t_f	Rise time / Fall time	-	-	25	ns	
t_{DSW}	Write data setup time	60	-	-	ns	
t_{DHW}	Write data hold time	2	-	-	ns	
t_{DSR}	Read data setup time	-	-	100	ns	C_L = 50pF
t_{DHR}	Read data hold time	5	-	-	ns	C_L = 50pF

5. Serial Interface

(VDD = VCC = 1.6 ~ 2.3V, TA = -40 ~ 85°C) (Dual power supply mode)

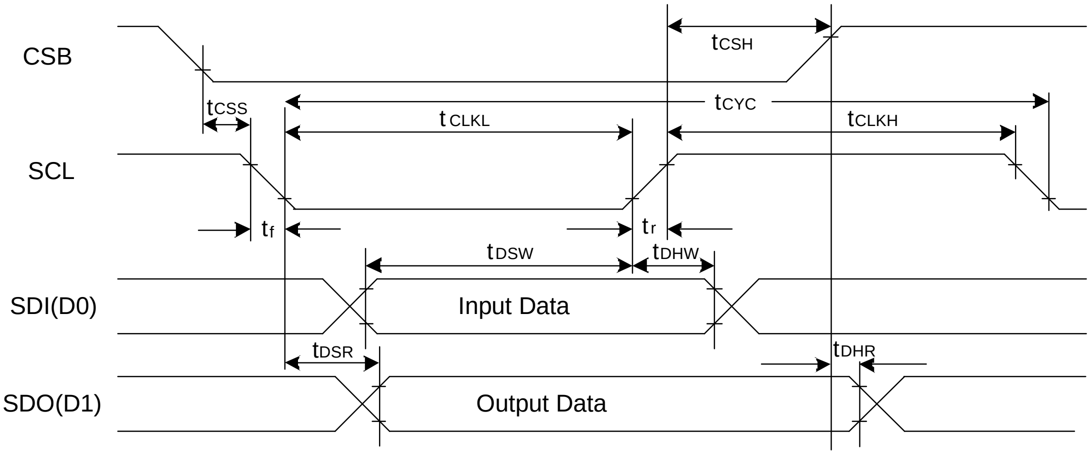


Figure 54. Clock Synchronized Serial Interface Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYCW}	Serial write clock cycle	0.1	-	-	µs	
t_{CYCR}	Serial read clock cycle	0.25	-	-	µs	
t_{CLKHW}	Serial write clock H pulse	40	-	-	ns	
t_{CLKLW}	Serial write clock L pulse	40	-	-	ns	
t_{CLKHR}	Serial read clock H pulse	120	-	-	ns	
t_{CLKLR}	Serial read clock L pulse	120	-	-	ns	
t_{CSS}	Chip select setup time	20	-	-	ns	
t_{CSH}	Chip select hold time	60	-	-	ns	
t_r / t_f	Rise time / Fall time	-	-	20	ns	
t_{DSW}	Write data setup time	30	-	-	ns	
t_{DHW}	Write data hold time	30	-	-	ns	
t_{DSR}	Read data setup time	-	-	130	ns	
t_{DHR}	Read data hold time	5	-	-	ns	

6. Serial Interface

(VDD = 2.4 ~ 3.6V, VCC = VDDR = 1.9±0.1V, TA = -40 ~ 85°C) (Single power supply mode)

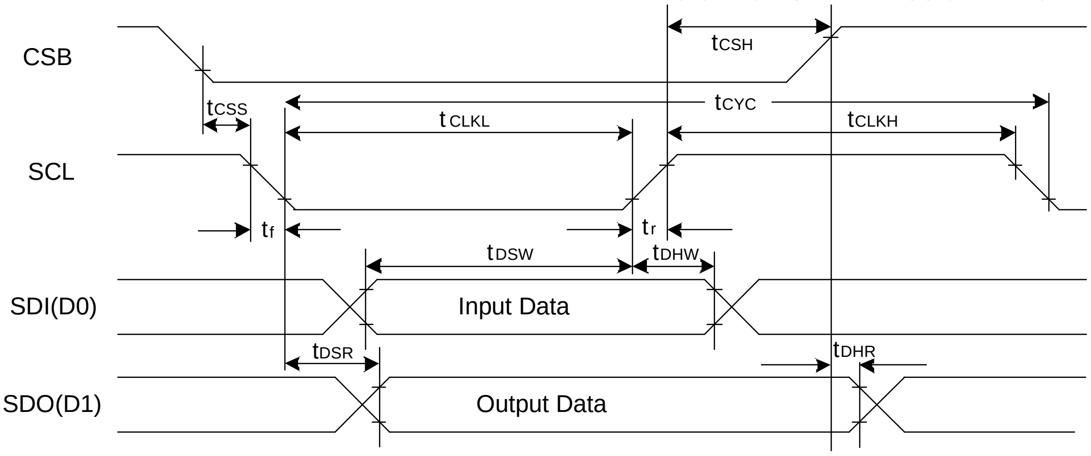


Figure 55. Clock Synchronized Serial Interface Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYCW}	Serial write clock cycle	0.076	-	-	μs	
t_{CYCR}	Serial read clock cycle	0.15	-	-	μs	
t_{CLKHW}	Serial write clock H pulse	40	-	-	ns	
t_{CLKLW}	Serial write clock L pulse	35	-	-	ns	
t_{CLKHR}	Serial read clock H pulse	70	-	-	ns	
t_{CLKLR}	Serial read clock L pulse	70	-	-	ns	
t_{CSS}	Chip select setup time	20	-	-	ns	
t_{CSH}	Chip select hold time	60	-	-	ns	
t_r / t_f	Rise time / Fall time	-	-	20	ns	
t_{DSW}	Write data setup time	30	-	-	ns	
t_{DHW}	Write data hold time	30	-	-	ns	
t_{DSR}	Read data setup time	-	-	130	ns	
t_{DHR}	Read data hold time	5	-	-	ns	

NOTE: *1. All timing is specified using VIL and VIH as the reference.

*2. t**CSLW** and t**CSLR** are specified as the overlap between CSB is "L" when WRB or RDB is at "L" level, or E is at the "H" level.

7. Reset Timing

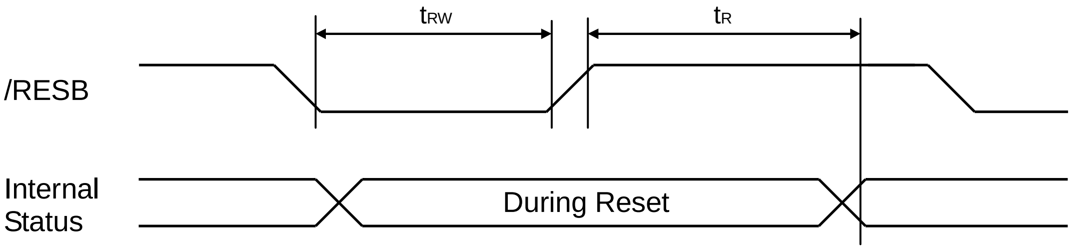
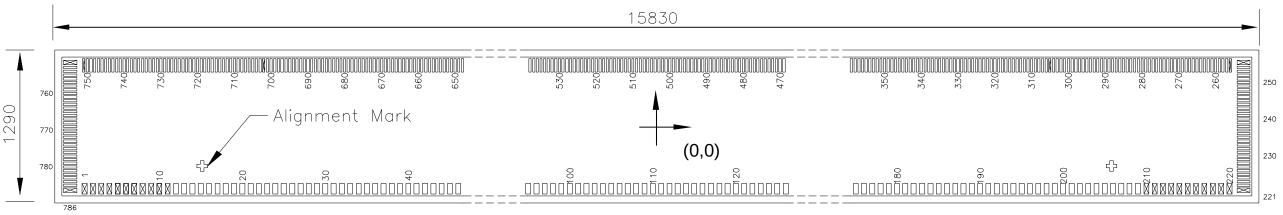


Figure 56. Reset Timing

(VDD = 1.6 ~ 3.6V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_R	Reset Time	-	-	10	ms	
t_{RW}	Reset low pulse width	100	-	-	µs	/RESB

Bonding Diagram



Unit: μm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	DUMMY1	-7665	-525	34	C23+	-5355	-525
2	DUMMY2	-7595	-525	35	C23+	-5285	-525
3	DUMMY3	-7525	-525	36	C23+	-5215	-525
4	DUMMY4	-7455	-525	37	C23-	-5145	-525
5	DUMMY5	-7385	-525	38	C23-	-5075	-525
6	DUMMY6	-7315	-525	39	C23-	-5005	-525
7	DUMMY7	-7245	-525	40	C23-	-4935	-525
8	DUMMY8	-7175	-525	41	C22+	-4865	-525
9	DUMMY9	-7105	-525	42	C22+	-4795	-525
10	DUMMY10	-7035	-525	43	C22+	-4725	-525
11	DUMMY11	-6965	-525	44	C22+	-4655	-525
12	RESB1	-6895	-525	45	C22-	-4585	-525
13	CEP	-6825	-525	46	C22-	-4515	-525
14	CEP	-6755	-525	47	C22-	-4445	-525
15	CEP	-6685	-525	48	C22-	-4375	-525
16	CEP	-6615	-525	49	C21+	-4305	-525
17	CEP	-6545	-525	50	C21+	-4235	-525
18	CEM	-6475	-525	51	C21+	-4165	-525
19	CEM	-6405	-525	52	C21+	-4095	-525
20	CEM	-6335	-525	53	C21-	-4025	-525
21	CEM	-6265	-525	54	C21-	-3955	-525
22	CEM	-6195	-525	55	C21-	-3885	-525
23	VCL	-6125	-525	56	C21-	-3815	-525
24	VCL	-6055	-525	57	VCI2	-3745	-525
25	VCL	-5985	-525	58	VCI2	-3675	-525
26	VCL	-5915	-525	59	VCI2	-3605	-525
27	VCL	-5845	-525	60	VCI2	-3535	-525
28	VCH	-5775	-525	61	TEST1	-3465	-525
29	VCH	-5705	-525	62	TEST1	-3395	-525
30	VCH	-5635	-525	63	TEST2	-3325	-525
31	VCH	-5565	-525	64	TEST2	-3255	-525
32	VCH	-5495	-525	65	TEST3	-3185	-525
33	C23+	-5425	-525	66	TEST3	-3115	-525

Bonding Dimensions (Continued) Unit: µm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
67	D15	-3045	-525	108	D2	-175	-525
68	D15	-2975	-525	109	D1	-105	-525
69	D15	-2905	-525	110	D1	-35	-525
70	D14	-2835	-525	111	D1	35	-525
71	D14	-2765	-525	112	D0	105	-525
72	D14	-2695	-525	113	D0	175	-525
73	D13	-2625	-525	114	D0	245	-525
74	D13	-2555	-525	115	R/WB	315	-525
75	D13	-2485	-525	116	R/WB	385	-525
76	D12	-2415	-525	117	R/WB	455	-525
77	D12	-2345	-525	118	E	525	-525
78	D12	-2275	-525	119	E	595	-525
79	D11	-2205	-525	120	E	665	-525
80	D11	-2135	-525	121	A0	735	-525
81	D11	-2065	-525	122	A0	805	-525
82	D10	-1995	-525	123	A0	875	-525
83	D10	-1925	-525	124	CSB	945	-525
84	D10	-1855	-525	125	CSB	1015	-525
85	D9	-1785	-525	126	CSB	1085	-525
86	D9	-1715	-525	127	VDDR	1155	-525
87	D9	-1645	-525	128	VDDR	1225	-525
88	D8	-1575	-525	129	VDDR	1295	-525
89	D8	-1505	-525	130	VCC	1365	-525
90	D8	-1435	-525	131	VCC	1435	-525
91	D7	-1365	-525	132	VCC	1505	-525
92	D7	-1295	-525	133	VCC	1575	-525
93	D7	-1225	-525	134	VDD	1645	-525
94	D6	-1155	-525	135	VDD	1715	-525
95	D6	-1085	-525	136	VDD	1785	-525
96	D6	-1015	-525	137	VDD2	1855	-525
97	D5	-945	-525	138	VDD2	1925	-525
98	D5	-875	-525	139	VDD2	1995	-525
99	D5	-805	-525	140	VDD3	2065	-525
100	D4	-735	-525	141	VDD3	2135	-525
101	D4	-665	-525	142	VDD3	2205	-525
102	D4	-595	-525	143	VDD3	2275	-525
103	D3	-525	-525	144	VSS	2345	-525
104	D3	-455	-525	145	VSS	2415	-525
105	D3	-385	-525	146	VSS	2485	-525
106	D2	-315	-525	147	VSS2	2555	-525
107	D2	-245	-525	148	VSS2	2625	-525

Bonding Dimensions (Continued)

Unit: μm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
149	VSS2	2695	-525	190	C12+	5565	-525
150	VSS3	2765	-525	191	C12+	5635	-525
151	VSS3	2835	-525	192	C12+	5705	-525
152	VSS3	2905	-525	193	C12-	5775	-525
153	VSS3	2975	-525	194	C12-	5845	-525
154	RESB2	3045	-525	195	C12-	5915	-525
155	RESB2	3115	-525	196	C12-	5985	-525
156	OSCO	3185	-525	197	C11+	6055	-525
157	OSCO	3255	-525	198	C11+	6125	-525
158	OSCI	3325	-525	199	C11+	6195	-525
159	OSCI	3395	-525	200	C11+	6265	-525
160	VDD1	3465	-525	201	C11-	6335	-525
161	REGENB	3535	-525	202	C11-	6405	-525
162	REGENB	3605	-525	203	C11-	6475	-525
163	VSS1	3675	-525	204	C11-	6545	-525
164	S/P	3745	-525	205	VCI1	6615	-525
165	S/P	3815	-525	206	VCI1	6685	-525
166	VDD1	3885	-525	207	VCI1	6755	-525
167	C86	3955	-525	208	VCI1	6825	-525
168	C86	4025	-525	209	RESB3	6895	-525
169	VSS1	4095	-525	210	DUMMY12	6965	-525
170	S8/16	4165	-525	211	DUMMY13	7035	-525
171	S8/16	4235	-525	212	DUMMY14	7105	-525
172	VDD1	4305	-525	213	DUMMY15	7175	-525
173	VREFL	4375	-525	214	DUMMY16	7245	-525
174	VREFL	4445	-525	215	DUMMY17	7315	-525
175	VREFM	4515	-525	216	DUMMY18	7385	-525
176	VREFM	4585	-525	217	DUMMY19	7455	-525
177	VM	4655	-525	218	DUMMY20	7525	-525
178	VM	4725	-525	219	DUMMY21	7595	-525
179	VM	4795	-525	220	DUMMY22	7665	-525
180	VM	4865	-525	221	DUMMY23	7785	-536.5
181	VSH	4935	-525	222	COM2	7785	-496
182	VSH	5005	-525	223	COM4	7785	-465
183	VSH	5075	-525	224	COM6	7785	-434
184	VSH	5145	-525	225	COM8	7785	-403
185	VOUT	5215	-525	226	COM10	7785	-372
186	VOUT	5285	-525	227	COM12	7785	-341
187	VOUT	5355	-525	228	COM14	7785	-310
188	VOUT	5425	-525	229	COM16	7785	-279
189	C12+	5495	-525	230	COM18	7785	-248

Bonding Dimensions (Continued)

Unit: μm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
231	COM20	7785	-217	272	COM98	7176.5	515
232	COM22	7785	-186	273	COM100	7145.5	515
233	COM24	7785	-155	274	COM102	7114.5	515
234	COM26	7785	-124	275	COM104	7083.5	515
235	COM28	7785	-93	276	COM106	7052.5	515
236	COM30	7785	-62	277	COM108	7021.5	515
237	COM32	7785	-31	278	COM110	6990.5	515
238	COM34	7785	0	279	COM112	6959.5	515
239	COM36	7785	31	280	COM114	6928.5	515
240	COM38	7785	62	281	COM116	6897.5	515
241	COM40	7785	93	282	COM118	6866.5	515
242	COM42	7785	124	283	COM120	6835.5	515
243	COM44	7785	155	284	COM122	6804.5	515
244	COM46	7785	186	285	COM124	6773.5	515
245	COM48	7785	217	286	COM126	6742.5	515
246	COM50	7785	248	287	COM128	6711.5	515
247	COM52	7785	279	288	COM130	6680.5	515
248	COM54	7785	310	289	COM132	6649.5	515
249	COM56	7785	341	290	COM134	6618.5	515
250	COM58	7785	372	291	COM136	6587.5	515
251	COM60	7785	403	292	COM138	6556.5	515
252	COM62	7785	434	293	COM140	6525.5	515
253	COM64	7785	465	294	COM142	6494.5	515
254	COM66	7785	496	295	COM144	6463.5	515
255	DUMMY24	7785	536.5	296	COM146	6432.5	515
256	DUMMY25	7672.5	515	297	COM148	6401.5	515
257	COM68	7641.5	515	298	COM150	6370.5	515
258	COM70	7610.5	515	299	COM152	6339.5	515
259	COM72	7579.5	515	300	COM154	6308.5	515
260	COM74	7548.5	515	301	COM156	6277.5	515
261	COM76	7517.5	515	302	COM158	6246.5	515
262	COM78	7486.5	515	303	COM160	6215.5	515
263	COM80	7455.5	515	304	COM162	6184.5	515
264	COM82	7424.5	515	305	DUMMY26	6153.5	515
265	COM84	7393.5	515	306	SEG396	6122.5	515
266	COM86	7362.5	515	307	SEG395	6091.5	515
267	COM88	7331.5	515	308	SEG394	6060.5	515
268	COM90	7300.5	515	309	SEG393	6029.5	515
269	COM92	7269.5	515	310	SEG392	5998.5	515
270	COM94	7238.5	515	311	SEG391	5967.5	515
271	COM96	7207.5	515	312	SEG390	5936.5	515

Bonding Dimensions (Continued)

Unit: µm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
313	SEG389	5905.5	515	354	SEG348	4634.5	515
314	SEG388	5874.5	515	355	SEG347	4603.5	515
315	SEG387	5843.5	515	356	SEG346	4572.5	515
316	SEG386	5812.5	515	357	SEG345	4541.5	515
317	SEG385	5781.5	515	358	SEG344	4510.5	515
318	SEG384	5750.5	515	359	SEG343	4479.5	515
319	SEG383	5719.5	515	360	SEG342	4448.5	515
320	SEG382	5688.5	515	361	SEG341	4417.5	515
321	SEG381	5657.5	515	362	SEG340	4386.5	515
322	SEG380	5626.5	515	363	SEG339	4355.5	515
323	SEG379	5595.5	515	364	SEG338	4324.5	515
324	SEG378	5564.5	515	365	SEG337	4293.5	515
325	SEG377	5533.5	515	366	SEG336	4262.5	515
326	SEG376	5502.5	515	367	SEG335	4231.5	515
327	SEG375	5471.5	515	368	SEG334	4200.5	515
328	SEG374	5440.5	515	369	SEG333	4169.5	515
329	SEG373	5409.5	515	370	SEG332	4138.5	515
330	SEG372	5378.5	515	371	SEG331	4107.5	515
331	SEG371	5347.5	515	372	SEG330	4076.5	515
332	SEG370	5316.5	515	373	SEG329	4045.5	515
333	SEG369	5285.5	515	374	SEG328	4014.5	515
334	SEG368	5254.5	515	375	SEG327	3983.5	515
335	SEG367	5223.5	515	376	SEG326	3952.5	515
336	SEG366	5192.5	515	377	SEG325	3921.5	515
337	SEG365	5161.5	515	378	SEG324	3890.5	515
338	SEG364	5130.5	515	379	SEG323	3859.5	515
339	SEG363	5099.5	515	380	SEG322	3828.5	515
340	SEG362	5068.5	515	381	SEG321	3797.5	515
341	SEG361	5037.5	515	382	SEG320	3766.5	515
342	SEG360	5006.5	515	383	SEG319	3735.5	515
343	SEG359	4975.5	515	384	SEG318	3704.5	515
344	SEG358	4944.5	515	385	SEG317	3673.5	515
345	SEG357	4913.5	515	386	SEG316	3642.5	515
346	SEG356	4882.5	515	387	SEG315	3611.5	515
347	SEG355	4851.5	515	388	SEG314	3580.5	515
348	SEG354	4820.5	515	389	SEG313	3549.5	515
349	SEG353	4789.5	515	390	SEG312	3518.5	515
350	SEG352	4758.5	515	391	SEG311	3487.5	515
351	SEG351	4727.5	515	392	SEG310	3456.5	515
352	SEG350	4696.5	515	393	SEG309	3425.5	515
353	SEG349	4665.5	515	394	SEG308	3394.5	515

Bonding Dimensions (Continued)

Unit: μm

Pad No.	Designation	X	Y
395	SEG307	3363.5	515
396	SEG306	3332.5	515
397	SEG305	3301.5	515
398	SEG304	3270.5	515
399	SEG303	3239.5	515
400	SEG302	3208.5	515
401	SEG301	3177.5	515
402	SEG300	3146.5	515
403	SEG299	3115.5	515
404	SEG298	3084.5	515
405	SEG297	3053.5	515
406	SEG296	3022.5	515
407	SEG295	2991.5	515
408	SEG294	2960.5	515
409	SEG293	2929.5	515
410	SEG292	2898.5	515
411	SEG291	2867.5	515
412	SEG290	2836.5	515
413	SEG289	2805.5	515
414	SEG288	2774.5	515
415	SEG287	2743.5	515
416	SEG286	2712.5	515
417	SEG285	2681.5	515
418	SEG284	2650.5	515
419	SEG283	2619.5	515
420	SEG282	2588.5	515
421	SEG281	2557.5	515
422	SEG280	2526.5	515
423	SEG279	2495.5	515
424	SEG278	2464.5	515
425	SEG277	2433.5	515
426	SEG276	2402.5	515
427	SEG275	2371.5	515
428	SEG274	2340.5	515
429	SEG273	2309.5	515
430	SEG272	2278.5	515
431	SEG271	2247.5	515
432	SEG270	2216.5	515
433	SEG269	2185.5	515
434	SEG268	2154.5	515
435	SEG267	2123.5	515
436	SEG266	2092.5	515
437	SEG265	2061.5	515
438	SEG264	2030.5	515
439	SEG263	1999.5	515
440	SEG262	1968.5	515
441	SEG261	1937.5	515
442	SEG260	1906.5	515
443	SEG259	1875.5	515
444	SEG258	1844.5	515
445	SEG257	1813.5	515
446	SEG256	1782.5	515
447	SEG255	1751.5	515
448	SEG254	1720.5	515
449	SEG253	1689.5	515
450	SEG252	1658.5	515
451	SEG251	1627.5	515
452	SEG250	1596.5	515
453	SEG249	1565.5	515
454	SEG248	1534.5	515
455	SEG247	1503.5	515
456	SEG246	1472.5	515
457	SEG245	1441.5	515
458	SEG244	1410.5	515
459	SEG243	1379.5	515
460	SEG242	1348.5	515
461	SEG241	1317.5	515
462	SEG240	1286.5	515
463	SEG239	1255.5	515
464	SEG238	1224.5	515
465	SEG237	1193.5	515
466	SEG236	1162.5	515
467	SEG235	1131.5	515
468	SEG234	1100.5	515
469	SEG233	1069.5	515
470	SEG232	1038.5	515
471	SEG231	1007.5	515
472	SEG230	976.5	515
473	SEG229	945.5	515
474	SEG228	914.5	515
475	SEG227	883.5	515
476	SEG226	852.5	515

Bonding Dimensions (Continued) Unit: µm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
477	SEG225	821.5	515	519	SEG183	-480.5	515
478	SEG224	790.5	515	520	SEG182	-511.5	515
479	SEG223	759.5	515	521	SEG181	-542.5	515
480	SEG222	728.5	515	522	SEG180	-573.5	515
481	SEG221	697.5	515	523	SEG179	-604.5	515
482	SEG220	666.5	515	524	SEG178	-635.5	515
483	SEG219	635.5	515	525	SEG177	-666.5	515
484	SEG218	604.5	515	526	SEG176	-697.5	515
485	SEG217	573.5	515	527	SEG175	-728.5	515
486	SEG216	542.5	515	528	SEG174	-759.5	515
487	SEG215	511.5	515	529	SEG173	-790.5	515
488	SEG214	480.5	515	530	SEG172	-821.5	515
489	SEG213	449.5	515	531	SEG171	-852.5	515
490	SEG212	418.5	515	532	SEG170	-883.5	515
491	SEG211	387.5	515	533	SEG169	-914.5	515
492	SEG210	356.5	515	534	SEG168	-945.5	515
493	SEG209	325.5	515	535	SEG167	-976.5	515
494	SEG208	294.5	515	536	SEG166	-1007.5	515
495	SEG207	263.5	515	537	SEG165	-1038.5	515
496	SEG206	232.5	515	538	SEG164	-1069.5	515
497	SEG205	201.5	515	539	SEG163	-1100.5	515
498	SEG204	170.5	515	540	SEG162	-1131.5	515
499	SEG203	139.5	515	541	SEG161	-1162.5	515
500	SEG202	108.5	515	542	SEG160	-1193.5	515
501	SEG201	77.5	515	543	SEG159	-1224.5	515
502	SEG200	46.5	515	544	SEG158	-1255.5	515
503	SEG199	15.5	515	545	SEG157	-1286.5	515
504	SEG198	-15.5	515	546	SEG156	-1317.5	515
505	SEG197	-46.5	515	547	SEG155	-1348.5	515
506	SEG196	-77.5	515	548	SEG154	-1379.5	515
507	SEG195	-108.5	515	549	SEG153	-1410.5	515
508	SEG194	-139.5	515	550	SEG152	-1441.5	515
509	SEG193	-170.5	515	551	SEG151	-1472.5	515
510	SEG192	-201.5	515	552	SEG150	-1503.5	515
511	SEG191	-232.5	515	553	SEG149	-1534.5	515
512	SEG190	-263.5	515	554	SEG148	-1565.5	515
513	SEG189	-294.5	515	555	SEG147	-1596.5	515
514	SEG188	-325.5	515	556	SEG146	-1627.5	515
515	SEG187	-356.5	515	557	SEG145	-1658.5	515
516	SEG186	-387.5	515	558	SEG144	-1689.5	515
517	SEG185	-418.5	515	559	SEG143	-1720.5	515
518	SEG184	-449.5	515	560	SEG142	-1751.5	515

Bonding Dimensions (Continued) Unit: μm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
561	SEG141	-1782.5	515	602	SEG100	-3053.5	515
562	SEG140	-1813.5	515	603	SEG99	-3084.5	515
563	SEG139	-1844.5	515	604	SEG98	-3115.5	515
564	SEG138	-1875.5	515	605	SEG97	-3146.5	515
565	SEG137	-1906.5	515	606	SEG96	-3177.5	515
566	SEG136	-1937.5	515	607	SEG95	-3208.5	515
567	SEG135	-1968.5	515	608	SEG94	-3239.5	515
568	SEG134	-1999.5	515	609	SEG93	-3270.5	515
569	SEG133	-2030.5	515	610	SEG92	-3301.5	515
570	SEG132	-2061.5	515	611	SEG91	-3332.5	515
571	SEG131	-2092.5	515	612	SEG90	-3363.5	515
572	SEG130	-2123.5	515	613	SEG89	-3394.5	515
573	SEG129	-2154.5	515	614	SEG88	-3425.5	515
574	SEG128	-2185.5	515	615	SEG87	-3456.5	515
575	SEG127	-2216.5	515	616	SEG86	-3487.5	515
576	SEG126	-2247.5	515	617	SEG85	-3518.5	515
577	SEG125	-2278.5	515	618	SEG84	-3549.5	515
578	SEG124	-2309.5	515	619	SEG83	-3580.5	515
579	SEG123	-2340.5	515	620	SEG82	-3611.5	515
580	SEG122	-2371.5	515	621	SEG81	-3642.5	515
581	SEG121	-2402.5	515	622	SEG80	-3673.5	515
582	SEG120	-2433.5	515	623	SEG79	-3704.5	515
583	SEG119	-2464.5	515	624	SEG78	-3735.5	515
584	SEG118	-2495.5	515	625	SEG77	-3766.5	515
585	SEG117	-2526.5	515	626	SEG76	-3797.5	515
586	SEG116	-2557.5	515	627	SEG75	-3828.5	515
587	SEG115	-2588.5	515	628	SEG74	-3859.5	515
588	SEG114	-2619.5	515	629	SEG73	-3890.5	515
589	SEG113	-2650.5	515	630	SEG72	-3921.5	515
590	SEG112	-2681.5	515	631	SEG71	-3952.5	515
591	SEG111	-2712.5	515	632	SEG70	-3983.5	515
592	SEG110	-2743.5	515	633	SEG69	-4014.5	515
593	SEG109	-2774.5	515	634	SEG68	-4045.5	515
594	SEG108	-2805.5	515	635	SEG67	-4076.5	515
595	SEG107	-2836.5	515	636	SEG66	-4107.5	515
596	SEG106	-2867.5	515	637	SEG65	-4138.5	515
597	SEG105	-2898.5	515	638	SEG64	-4169.5	515
598	SEG104	-2929.5	515	639	SEG63	-4200.5	515
599	SEG103	-2960.5	515	640	SEG62	-4231.5	515
600	SEG102	-2991.5	515	641	SEG61	-4262.5	515
601	SEG101	-3022.5	515	642	SEG60	-4293.5	515

Bonding Dimensions (Continued) Unit: µm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
643	SEG59	-4324.5	515	685	SEG17	-5626.5	515
644	SEG58	-4355.5	515	686	SEG16	-5657.5	515
645	SEG57	-4386.5	515	687	SEG15	-5688.5	515
646	SEG56	-4417.5	515	688	SEG14	-5719.5	515
647	SEG55	-4448.5	515	689	SEG13	-5750.5	515
648	SEG54	-4479.5	515	690	SEG12	-5781.5	515
649	SEG53	-4510.5	515	691	SEG11	-5812.5	515
650	SEG52	-4541.5	515	692	SEG10	-5843.5	515
651	SEG51	-4572.5	515	693	SEG9	-5874.5	515
652	SEG50	-4603.5	515	694	SEG8	-5905.5	515
653	SEG49	-4634.5	515	695	SEG7	-5936.5	515
654	SEG48	-4665.5	515	696	SEG6	-5967.5	515
655	SEG47	-4696.5	515	697	SEG5	-5998.5	515
656	SEG46	-4727.5	515	698	SEG4	-6029.5	515
657	SEG45	-4758.5	515	699	SEG3	-6060.5	515
658	SEG44	-4789.5	515	700	SEG2	-6091.5	515
659	SEG43	-4820.5	515	701	SEG1	-6122.5	515
660	SEG42	-4851.5	515	702	DUMMY27	-6153.5	515
661	SEG41	-4882.5	515	703	COM161	-6184.5	515
662	SEG40	-4913.5	515	704	COM159	-6215.5	515
663	SEG39	-4944.5	515	705	COM157	-6246.5	515
664	SEG38	-4975.5	515	706	COM155	-6277.5	515
665	SEG37	-5006.5	515	707	COM153	-6308.5	515
666	SEG36	-5037.5	515	708	COM151	-6339.5	515
667	SEG35	-5068.5	515	709	COM149	-6370.5	515
668	SEG34	-5099.5	515	710	COM147	-6401.5	515
669	SEG33	-5130.5	515	711	COM145	-6432.5	515
670	SEG32	-5161.5	515	712	COM143	-6463.5	515
671	SEG31	-5192.5	515	713	COM141	-6494.5	515
672	SEG30	-5223.5	515	714	COM139	-6525.5	515
673	SEG29	-5254.5	515	715	COM137	-6556.5	515
674	SEG28	-5285.5	515	716	COM135	-6587.5	515
675	SEG27	-5316.5	515	717	COM133	-6618.5	515
676	SEG26	-5347.5	515	718	COM131	-6649.5	515
677	SEG25	-5378.5	515	719	COM129	-6680.5	515
678	SEG24	-5409.5	515	720	COM127	-6711.5	515
679	SEG23	-5440.5	515	721	COM125	-6742.5	515
680	SEG22	-5471.5	515	722	COM123	-6773.5	515
681	SEG21	-5502.5	515	723	COM121	-6804.5	515
682	SEG20	-5533.5	515	724	COM119	-6835.5	515
683	SEG19	-5564.5	515	725	COM117	-6866.5	515
684	SEG18	-5595.5	515	726	COM115	-6897.5	515

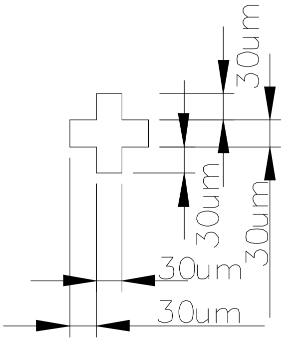
Bonding Dimensions (Continued) Unit: µm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
727	COM113	-6928.5	515	768	COM35	-7785	31
728	COM111	-6959.5	515	769	COM33	-7785	0
729	COM109	-6990.5	515	770	COM31	-7785	-31
730	COM107	-7021.5	515	771	COM29	-7785	-62
731	COM105	-7052.5	515	772	COM27	-7785	-93
732	COM103	-7083.5	515	773	COM25	-7785	-124
733	COM101	-7114.5	515	774	COM23	-7785	-155
734	COM99	-7145.5	515	775	COM21	-7785	-186
735	COM97	-7176.5	515	776	COM19	-7785	-217
736	COM95	-7207.5	515	777	COM17	-7785	-248
737	COM93	-7238.5	515	778	COM15	-7785	-279
738	COM91	-7269.5	515	779	COM13	-7785	-310
739	COM89	-7300.5	515	780	COM11	-7785	-341
740	COM87	-7331.5	515	781	COM9	-7785	-372
741	COM85	-7362.5	515	782	COM7	-7785	-403
742	COM83	-7393.5	515	783	COM5	-7785	-434
743	COM81	-7424.5	515	784	COM3	-7785	-465
744	COM79	-7455.5	515	785	COM1	-7785	-496
745	COM77	-7486.5	515	786	DUMMY30	-7785	-536.5
746	COM75	-7517.5	515				
747	COM73	-7548.5	515				
748	COM71	-7579.5	515				
749	COM69	-7610.5	515				
750	COM67	-7641.5	515				
751	DUMMY28	-7672.5	515				
752	DUMMY29	-7785	536.5				
753	COM65	-7785	496				
754	COM63	-7785	465				
755	COM61	-7785	434				
756	COM59	-7785	403				
757	COM57	-7785	372				
758	COM55	-7785	341				
759	COM53	-7785	310				
760	COM51	-7785	279				
761	COM49	-7785	248				
762	COM47	-7785	217				
763	COM45	-7785	186				
764	COM43	-7785	155				
765	COM41	-7785	124				
766	COM39	-7785	93				
767	COM37	-7785	62				

Alignment Mark Location (Total: 2) [Unit: µm]

No.	Designation	X	Y
AL_L	Alignment Mark (Button Left)	-6672	-334
AL_R	Alignment Mark (Button Right)	6672	-334

Alignment Mark (Button Left side and Button Right side)



Pad Dimensions

	PAD NO.	SIZE		UNIT
		X	Y	
Chip Size	-	15830	1290	µm
Chip thickness	-	525		µm
Pad Pitch	1~220	70		µm
	221~222,254~255,752~753,785~786	40.5		µm
	222~254,256~751,753~785	31		µm
Bump Size	1~220	42	90	µm
	221,255,752,786	38	110	µm
	222~254,256~751,753~785	19	110	µm
Bump Height	All pads	15 ± 3		µm

Ordering Information

Part No.	Packages
NT7553H-BDT	Gold Bump on Chip Tray

Cautions

1. The contents of this document will be subjected to change without notice.
2. Precautions against light projection:

   Light has the effect of causing the electrons of semiconductor to move; so light projection may change the characteristics of semiconductor devices. For this reason, it is necessary to take account of effective protection measures for the packages (such as COB, COG, TCP and COF, etc.) causing chip to be exposed to a light environment in order to isolate the projection of light on any part of the chip, including top, bottom and the area around the chip.

   Observe the following instructions in using this product:

   a. During the design stage, it is necessary to notice and confirm the light sensitivity and preventive measures for using IC on substrate (PCB, Glass or Film) or product.
   b. Test and inspect the product under an environment free of light source penetration.
   c. Confirm that all surfaces around the IC will not be exposed to light source.