NOVATEK
聯 詠 科 技

Data Sheet

NT7508

128 x 129 RAM-Map LCD Controller/Driver

V1.0

Revision History

NT7508 Specification Revision History				
Version	**Content**	**Prepared by**	**Checked by**	**Date**
1.0	Original	Jacky Chang	Johnny Hsiao	2008/7/1

Features

- 128 x 128 dots graphics LCD driver for 4 level grayscale with separated Icon line
- RAM capacity: 129 x 128 x 2 = 33,024bits
- 8-bit parallel bi-directional interface with 6800-series or 8080-series
- SPI (serial peripheral interface) available (only write operation)
- Power supply voltage:
  - VDD = 1.65 ~ 3.6V
  - VDDA = 2.4 ~ 3.6V
  - VCI = 2.4 ~ 3.6V
  - VLCD (V0-VSS2) = 4.0 ~ 15.0V
- 3x, 4x, 5x, 6x, 7x, 8x on chip DC-DC converter
- On-chip Voltage Generator
- 64 level internal contrast control
- Programmable bias ratio from 1/5 ~ 1/12
- Programmable Multiplex Ratio in dot-matrix display area from 16Mux ~ 129Mux
- On-Chip Oscillator circuit
- Temperature coefficient: -0.125 or -0.05%/°C
- Various partial display
- Partial window moving
- Vertical Scrolling
- Shift change of segment and common driver
- N-raster-row AC liquid-crystal drive (C-pattern waveform drive)
- Low power consumption
- CMOS Process
- Available in COG

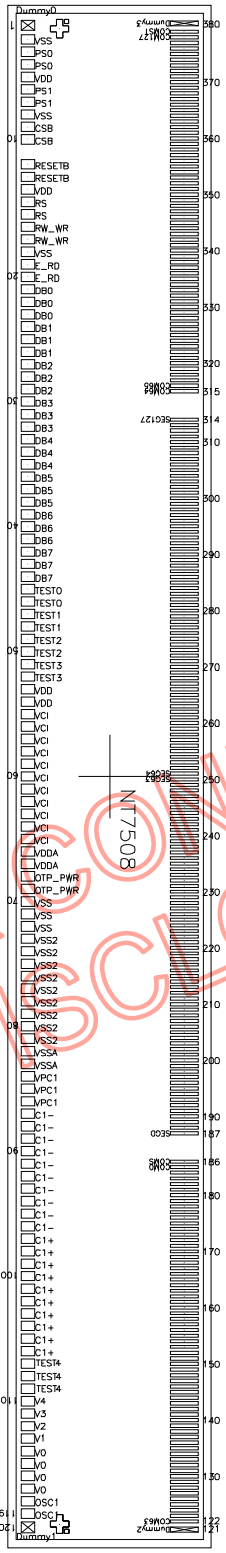
General Description

The NT7508 is a single chip with driver & controller LSI for dot matrix liquid crystal displays, which is display 128 x 129 dot graphics for 4 level grayscale. It accepts serial peripheral interface (SPI) or 8 bit parallel display data directly sent from a microcomputer and stores it in an on chip display RAM of 128 x 129 x 2 bits.

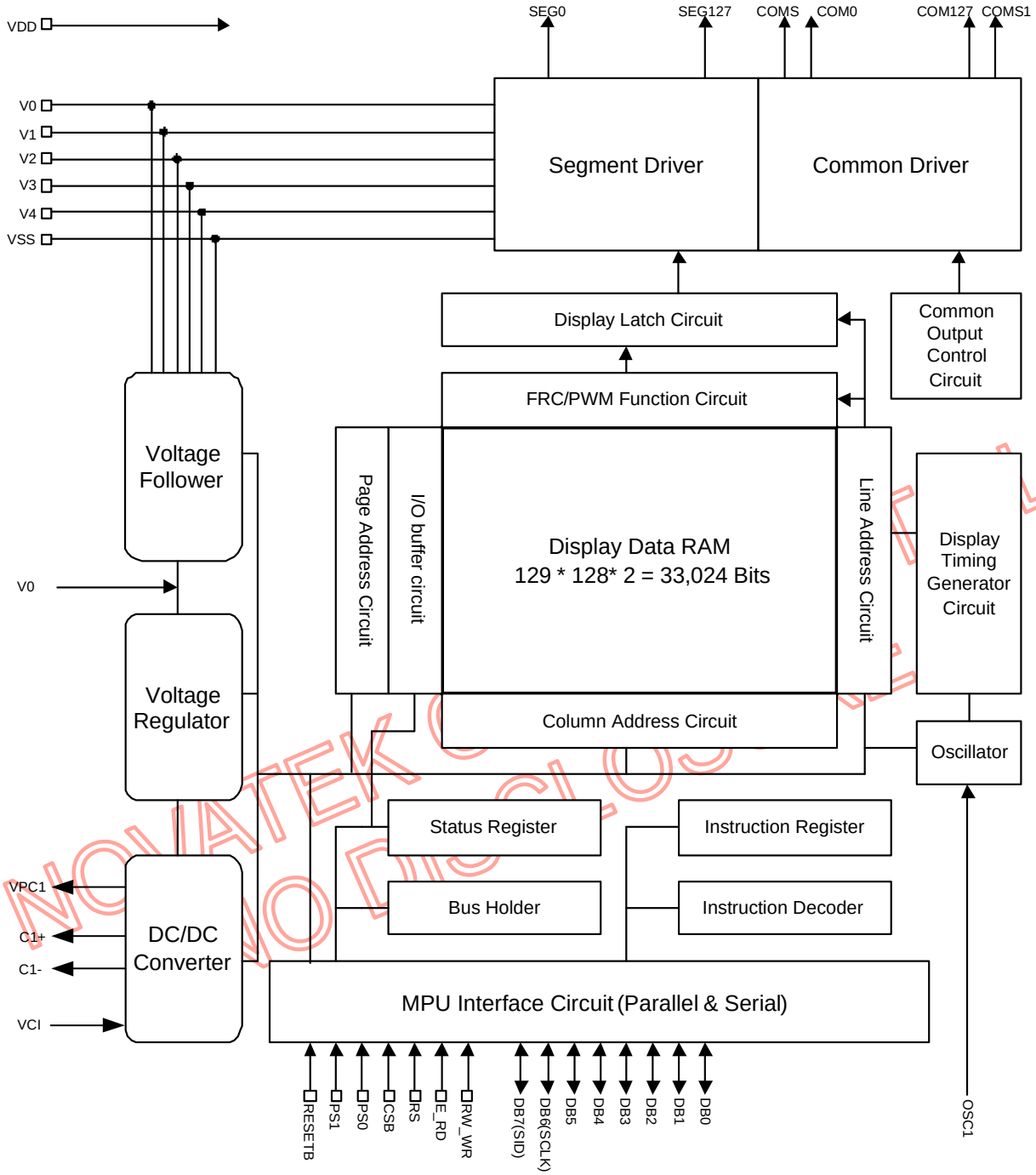
NT7508 embeds a DC/DC converter, an LCD voltage regulator, an on-chip bias divider and an on-chip Oscillator, which reduce the number of external components. NT7508 is suitable for any portable battery-driven applications requiring a long operation and compact size.

No external operation clock is required for RAM read/write operations. Accordingly, this driver can be operated with a minimum current consumption and its on board low current consumption liquid crystal power supply can implement a high performance handy display system with a minimum current consumption and a smallest LSI configuration.

Pad Configuration



Block Diagram



Pin and Pad Descriptions

Power Supply

Pad No.	Designation	I/O	Description
53~54	VDD	Supply	1.65~3.6V power supply Logic
55~65	VCI	Supply	2.4~3.6V Voltage converter input voltage pin
66~67	VDDA	Supply	2.4~3.6V power supply input for analog
5,13	VDD	O	Power supply output for pad option
68~69	OTP_PWR	Supply	Power supply for OTP programming, When not used, these pins should be left open.
70~72	VSS	Supply	Ground for Logic
73~81	VSS2	Supply	Ground input for DC-DC converter
82~83	VSSA	Supply	Ground input for analog
2,8,18	VSS	O	Power supply output for pad option
110 111 112 113 114~ 117	V4 V3 V2 V1 V0	O	LCD driver supply voltages. The voltage determined by LCD pixel is impedance-converted by an operational amplifier for application. Voltages should have the following relationship: V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS2. When the on-chip operating power circuit is on, the following voltages are given to V1 to V4 by the on-chip power circuit. Voltage selection is performed by the set LCD bias command.

LCD bias	V1	V2	V3	V4
1/N bias	(N-1)/N×V0	(N-2)/N×V0	(2/N)×V0	(1/N)×V0
Note: N= 5 to 12				

LCD Driver Supply

Pad No.	Designation	I/O	Description
87~96	C1-	O	Capacitor 1- pad for internal DC/DC voltage converter.
97~106	C1+	O	Capacitor 1+ pad for internal DC/DC voltage converter.
84~86	VPC1	O	This pin is connected to VSS2 with stabilization capacitor

System Control

Pad No.	Designation	I/O	Description
118~119	OSC1	I	When using internal clock Oscillator, open this pin. When using external clock Oscillator, external OSC input pin.

Microprocessor Interface

<table>
<tr><th>Pad No.</th><th>Designation</th><th>I/O</th><th>Description</th></tr>
<tr><td>11~12</td><td>RESETB</td><td>I</td><td>Reset input pin
When RESETB is “L”, initialization is executed.</td></tr>
<tr><td>3~4</td><td>PS0</td><td>I</td><td>Parallel / Serial data select input.
<table>
<tr><th>PS0</th><th>Interface Mode</th><th>Chip Select</th><th>Data / Instruction</th><th>Data</th><th>Read / Write</th><th>Serial Clock</th></tr>
<tr><td>H</td><td>Parallel</td><td>CSB</td><td>RS</td><td>DB7 to DB0</td><td>E_/RD, RW_WR</td><td>—</td></tr>
<tr><td>L</td><td>Serial</td><td>CSB</td><td>RS</td><td>DB7(SID)</td><td>Write Only</td><td>DB6 (SCLK)</td></tr>
</table>
Note: In serial mode, it cannot read data from the on-chip RAM. And DB0 to DB5 are high impedance and E_RD and RW_WR must be fixed to either “H” or “L”.</td></tr>
<tr><td>6~7</td><td>PS1</td><td>I</td><td>Microprocessor interface select input pin
<table>
<tr><th>Interface Select</th><th>6800 series</th><th>8080 series</th><th>4 pin SPI</th><th>3 pin SPI</th></tr>
<tr><td>PS0</td><td>H</td><td>H</td><td>L</td><td>L</td></tr>
<tr><td>PS1</td><td>H</td><td>L</td><td>H</td><td>L</td></tr>
</table></td></tr>
<tr><td>9~10</td><td>CSB</td><td>I</td><td>Chip Select input pins
Data/Instruction I/O is enabled only when CSB is “L”. When chip select s non-active, DB0 to DB7 are control data.</td></tr>
<tr><td>14~15</td><td>RS</td><td>I</td><td>Register select input pins
RS=”H”: DB0 to DB7 are display data
RS=”L”: DB0 to DB7 are control data
When the serial interface is selected, fix RS pads to VSS level.</td></tr>
<tr><td>16~17</td><td>RW_WR</td><td>I</td><td>Read / Write execution control pin
<table>
<tr><th>PS1</th><th>MPU Type</th><th>RW_WR</th><th>Description</th></tr>
<tr><td>H</td><td>6800 series</td><td>E</td><td>Read / Write control input pin
-RW="H": read
-RW="L": write</td></tr>
<tr><td>L</td><td>8080 series</td><td>/RD</td><td>Read enable clock input pin
The data on DB0 to DB7 are latched at the rising edge of the /WR signal</td></tr>
</table></td></tr>
</table>

<table>
<tr>
<td>19~20</td>
<td>E_RD</td>
<td>I</td>
<td>Read / Write execution control pin
<table>
<tr><th>PS1</th><th>MPU Type</th><th>E_RD</th><th>Description</th></tr>
<tr><td>H</td><td>6800 series</td><td>E</td><td>Read / Write control input pin
-RW="H": when E is "H", DB0 to DB7 are in an output status.
-RW="L": The data on DB0 to DB7 are latched at the falling edge of the E signal.</td></tr>
<tr><td>L</td><td>8080 series</td><td>/RD</td><td>Read enable clock input pin
When /RD is "L", DB0 to DB7 are in an output status.</td></tr>
</table></td>
</tr>
<tr>
<td>21~44</td>
<td>DB0 to DB7</td>
<td>I/O</td>
<td>8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus.
When the serial interface selected (PS0=”L”);
DB0 to DB5: high impedance
DB6: serial input clock (SCLK)
DB7: serial input data (SID)
When the serial interface is selected, fix D0~D5 pads to VSS level.
When chip select is not active, DB0 to DB7 may be high impedance.</td>
</tr>
</table>

Liquid Crystal Drive Pads

<table>
<tr><th>Pad No.</th><th>Designation</th><th>I/O</th><th>Description</th></tr>
<tr><td>187~314</td><td>SEG 0
to
SEG127</td><td>O</td><td>LCD segment drive outputs
The display data and the M signal control the output voltage of segment driver.
<table>
<tr><th rowspan="2">Display Data</th><th rowspan="2">M(Intrnal)</th><th colspan="2">Segment driver output voltage</th></tr>
<tr><th>Normal display</th><th>Reverse display</th></tr>
<tr><td>H</td><td>H</td><td>V0</td><td>V2</td></tr>
<tr><td>H</td><td>L</td><td>VSS2</td><td>V3</td></tr>
<tr><td>L</td><td>H</td><td>V2</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V3</td><td>VSS2</td></tr>
<tr><td colspan="2">Power Save Mode</td><td>VSS2</td><td>VSS2</td></tr>
</table></td></tr>
<tr><td>122~185
315~378</td><td>COM 0
to
COM127</td><td>O</td><td>LCD common driver outputs
The internal scanning data and M signal control the output voltage of common driver.
<table>
<tr><th>Scan data</th><th>M(Internal)</th><th>Common driver output voltage</th></tr>
<tr><td>H</td><td>H</td><td>VSS2</td></tr>
<tr><td>H</td><td>L</td><td>V0</td></tr>
<tr><td>L</td><td>H</td><td>V1</td></tr>
<tr><td>L</td><td>L</td><td>V4</td></tr>
<tr><td colspan="2">Power Save Mode</td><td>VSS2</td></tr>
</table></td></tr>
<tr><td>186,379</td><td>COMS
(COMS1)</td><td>O</td><td>Common output for the icons
The output signals of two pins are same. When not used, these pins should be left open.</td></tr>
</table>

Test Pads

Pad No.	Designation	I/O	Description
45~52 107~109	TEST0~4	-	Test pads, no connection for user.
1,120, 121,380	Dummy0~4	-	Must be no connection.

Functional Description

1. Microprocessor Interface

1.1 Chip Select Input

The NT7508 has one chip select pads can interface to a microprocessor wheh CSB is “L”. When these pins are set to any others combinatins, RS, E_RD, and RW_RW inputs are disabled and DB0 to DB7 are to be high impedance. And , in case of serial interface, the internal shift register and the counter are reset.

1.2 Parallel / Serial Interface

The NT7508 has four types of interface with an MPU, which are two serial and two parallel interface.This parallel or serial interface is determined by PS0 pin as shown in table 1.

PS0	Type	PS1	CSB	Interface Mode
H	Parallel	H	CSB	6800-series MPU mode
		L		8080-series MPU mode
L	Serial	H	CSB	4-pin SPI mode
		L		3-pin SPI mode

Table 1. Parallel / Serial Interface Mode

1.3 Parallel Interface (PS0=“H”)

The 8 bit bi-direction data bus is used in parallel interface and the type of MPU is selected by PS1 as shown in table 2.

PS1	MPU Bus Type	CSB	RS	E_RD	RW_WR	DB0 to DB7
H	6800-series	CSB	RS	E	RW	DB0 to DB7
L	8080-series	CSB	RS	/RD	/WR	DB0 to DB7

Table 2. Microprocessor Selection for Parallel Interface

The type of data transfer is determined by signals at RS,E_RD, and RW_WR as shown in table 3.

Common	6800 series		8080 series		Description
RS	E_RD	RW_WR	/RD	RW_WR	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register (instruction)

Table 3. Parallel Data Transfer

When E_RD pin is always pulled high for 6800 series interface, it can be used CSB for enable signal.

1.4 Serial Interface (PS0="L")

When the NT7508 is active at serial interface, serial data (DB7) and serial clock(DB6) inputs are enabled. If not, the internal 8 bit shift register and the 3 bit counter are reset.The display data / command indication may be controlled either via software or the Register Select (RS)pin, based on the setting of PS1. In 4 pin SPI mode,data is display data when RS is "H" and Common data when RS is "L".
In 3 pin SPI mode, the LCD driver will reveive command from MCU by default. If message on the data pin are data rather than command, MCU should send data direction command(11101000) to control the data direction and then one more command to define the number of data bytes will be write.After these two contunuous commands are send, the following messages will be data rather than command.
Serial data can be read on the rising edge of serial clock going into DB6. And the DDRAM column address pointer will be increased by one automatically. The next bytes after the display data string is handled as command data.

Serial mode	PS0	PS1	CSB	RS
4 pin SPI mode	L	H	CSB	Uesd
3 pin SPI mode	L	L	CSB	Fix to VSS

4 pin SPI Mode (PS0="L",PS1="H")

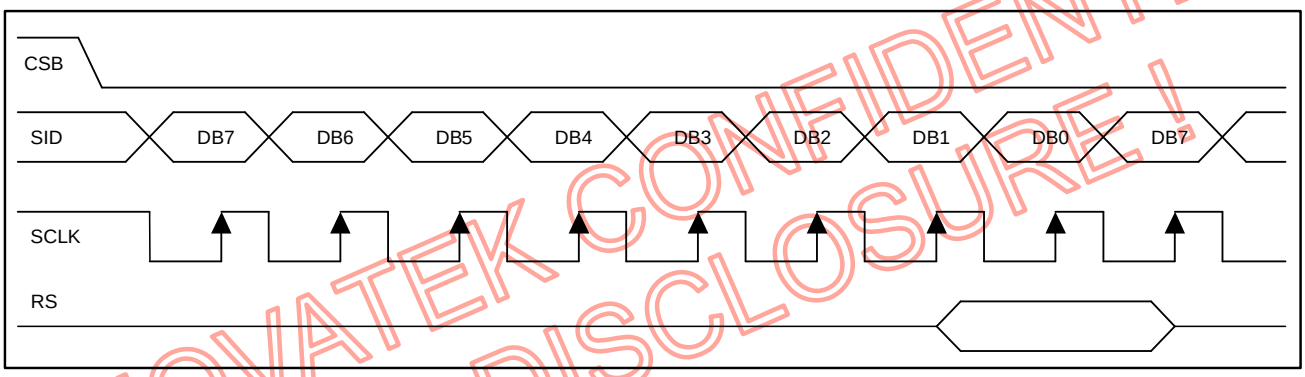


Figure 1. 4 pin SPI Timing (RS is used)

3 pin SPI Mode (PS0="L" , PS1="L")

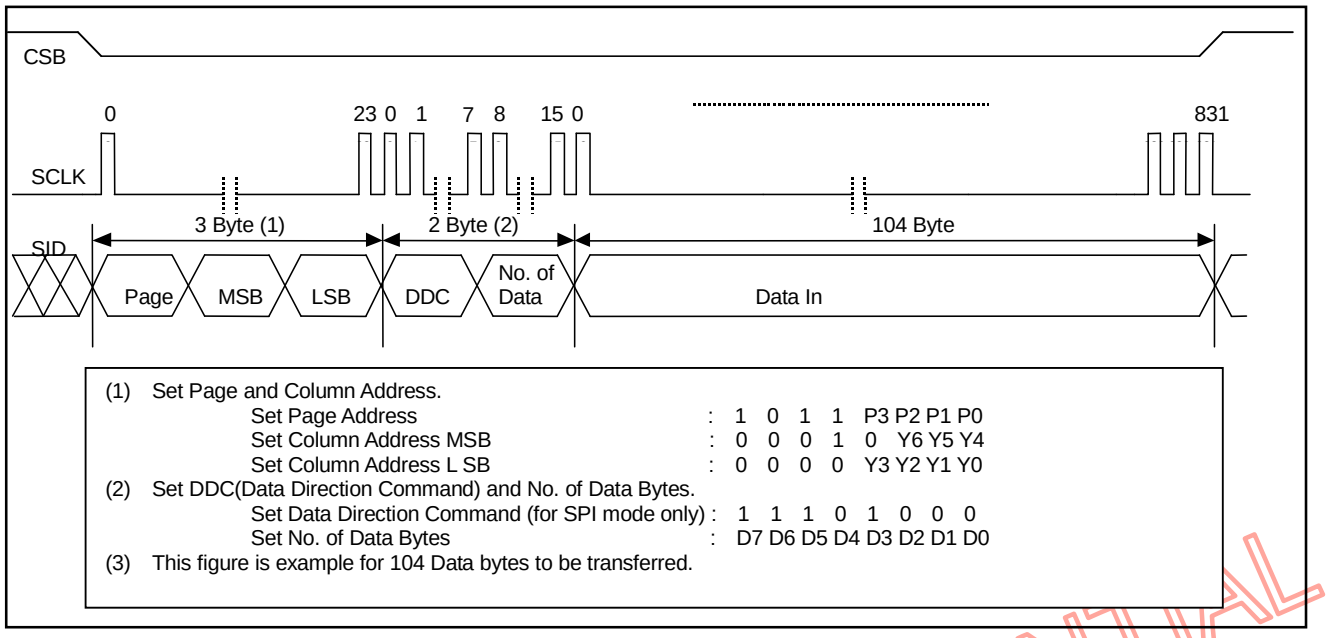


Figure 2. 3-pin SPI Timing (RS is not used)

This command is used in 3 pin SPI mode only. It will be continuous commands, the first byte controls the data direction and informs the LCD driver the second byte will be number of data bytes will be write. After these two commands sending out, the following messages will be data. If data is stopped in transmitting, it is not valid data.New data will be transferred serially with most significant bit first.

Note: In spite of transmission of data, if CSB will be disable, state terminates abnormally. Next state is initialized.

1.5 Busy Flag

The Busy Flag indicatges whether the NT7508 is operating or not.When DB7 is "H" in read status operstion, this device is in busy status and will accept only read status instruction. If the cycle time is correct, the microprocessor needs not to check this flag before each informationm which improves the MPU performance.

1.6 Data Transfer

NT7508 uses bus holder and internal data bus for data transfer with the MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in figure 3. And when reading data from on-chip RAM to th MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in figure 4. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

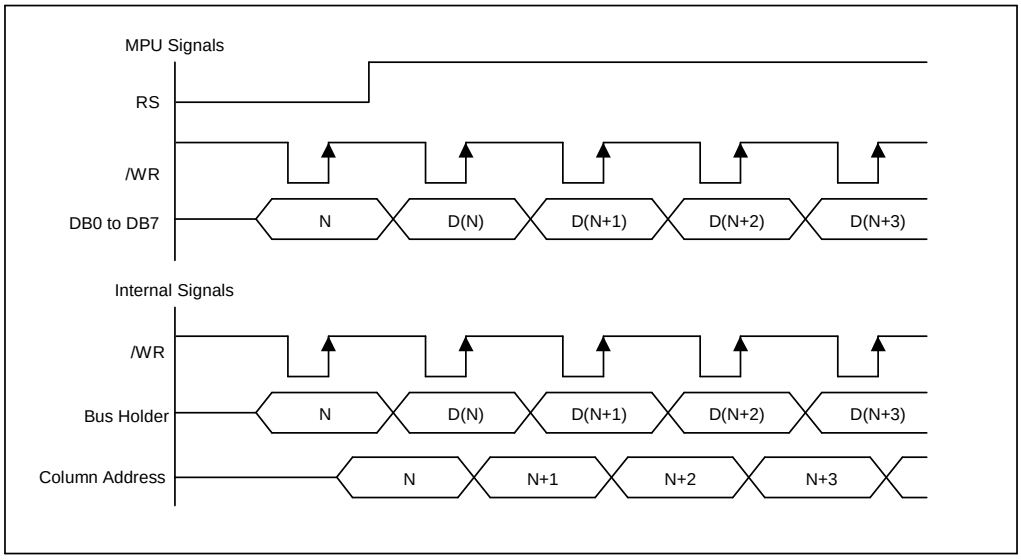


Figure 3. Write Timing

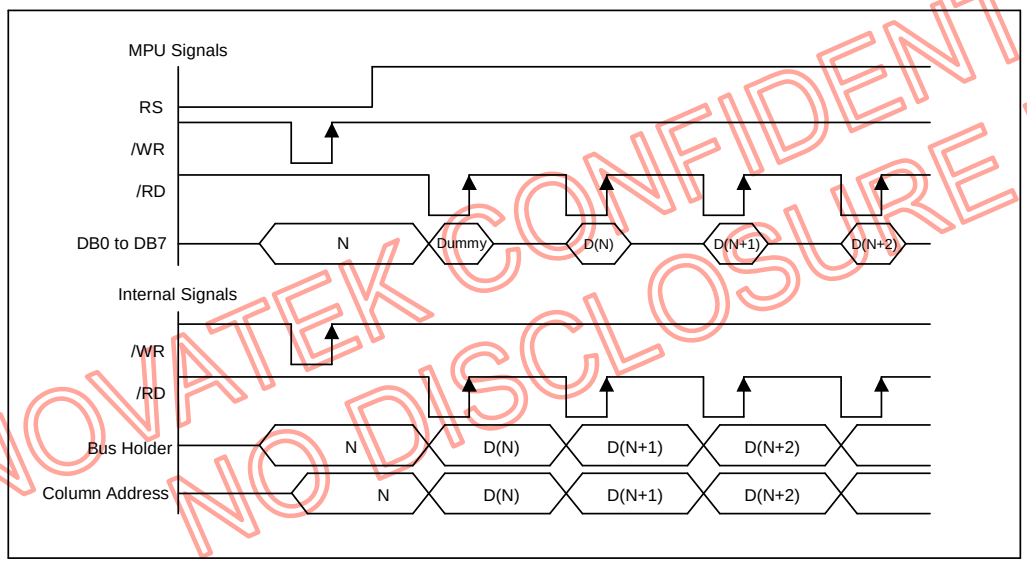


Figure 4. Read Timing

2. Display Data RAM

The Display Data RAM stores pixel data for the LCD. It is 129-row(17 page by 8 bits) by 128-column addressable array. Each pixel can be selected when the page and column addresses are specified. The 129 rows are divided into 16 pages of 8 lines and the icon page with a single line(DB0 only). Data is read from or written to the 8 lines of each page directly through DB0 to DB7.The display data of DB0 to DB7 from the microprocessor correspond to the LCD common lines. The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independenlty, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

3. Page Address Circuit

The circuit is for providing a Page Address to Display Data RAM shown in figure 6. It incorporates 4-bit Page Address register changed by only the “Set Page” instruction. Page Address 16 is a special RAM area for the icons and display data DB0 in only valid.

4. Line Address Circuit

This circuit assigns DDRAM a Line Address corresponding to the first line (COM0) of the display. Therefore, by setting Line Adddress repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on chip RAM as shown in figure 6. It incorporates 7-bit Line Address register changed by only the initial display line instruction and 7-bit counter circuit. At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by CL signal and generates the line address for transferring the 128 bit RAM data to the display data latch circuit. When icon is enabled by setting icon control register, display data of icons are not scrolled because the MPU can not access Line Address of icons.

5. Column Address Circuit

Column Address Circuit has a 8 bit preset counter that provides Column Address to the Display Data RAM as shown in figure 6. When set Column Address MSB/LSB instruction is issued, 7-bit [Y7 : Y1] are set and lowest bit, Y0 is set to “0”. Since this address is increased by 1 each a read or write data instruction, microprocessor can access the display data continuously. However, the counteris not increased and locked of a non-existing address above 7EH. It counter is independent of page address register.

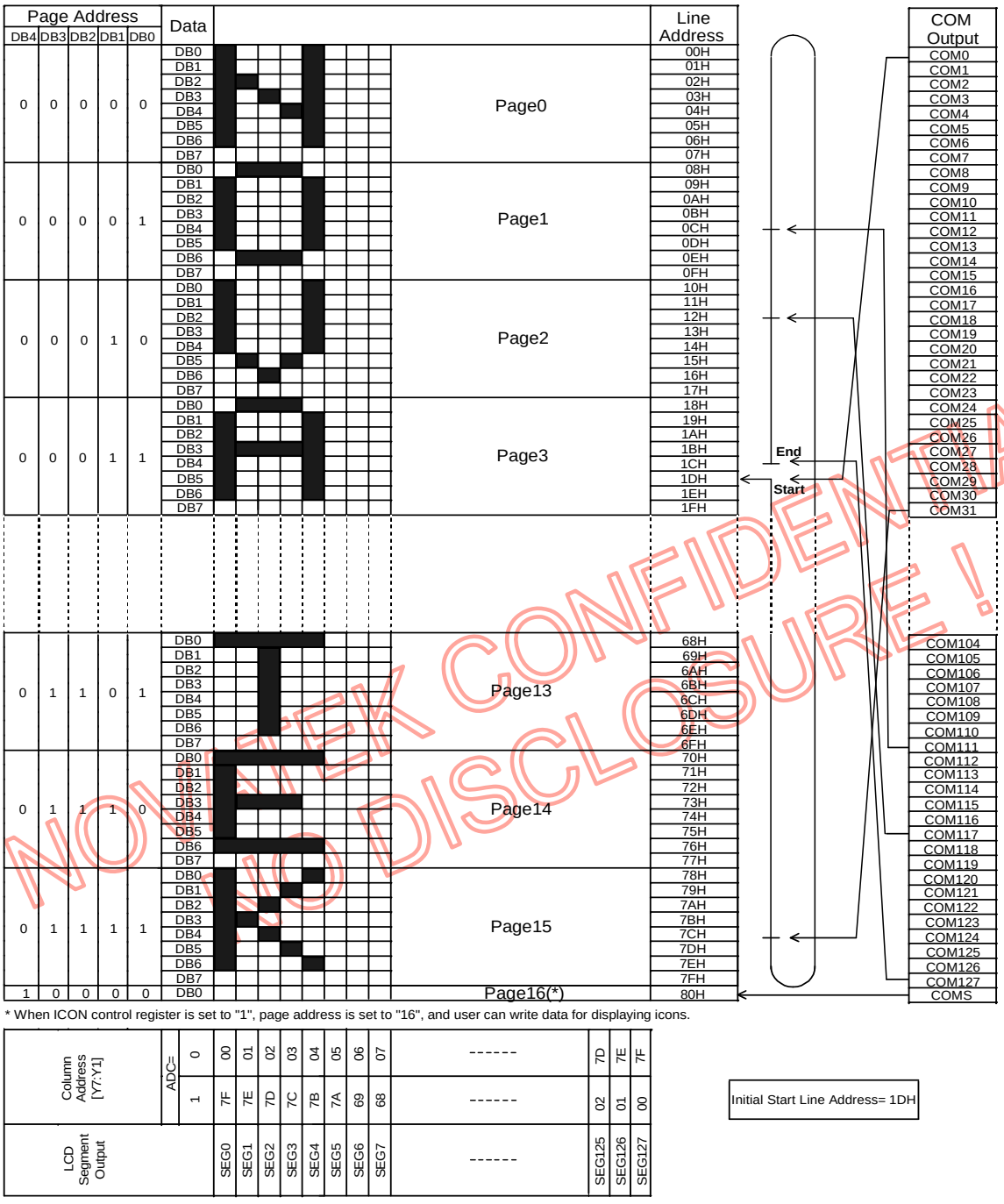
ADC select instruction makes it possible to invert the relationship between the Column Address and the segment outputs.It is necessary to rewrite the display data on built in RAM after issuing ADC select instruciton.Refer to the following figure 5.

SEG Output	SEG 0		SEG 1		SEG 2		SEG 3		…	SEG 124		SEG 125		SEG 126		SEG 127	
Column Address[Y7:Y1]	00H		01H		02H		03H		…	7CH		7DH		7EH		7FH	
Internal Column Address[Y7:Y1]	00H	01H	02H	03H	04H	05H	06H	07H	…	F8H	F9H	FAH	FBH	FCH	FDH	FEH	FFH
Display Data(ADC=0)	1	1	1	0	0	0	0	1	…	1	1	0	0	1	0	0	1
LCD Panel Display									…								
Display Data(ADC=1)	0	1	1	0	0	0	1	1	…	0	1	0	0	1	0	1	1
LCD Panel Display									…								

Figure 5. The Relationship between the Column Address and the Segment Outputs

6. Segment Control Circuit

This circuit controls the display data by the display ON/OFF, reverse display ON/OFF and entire display ON/OFF instructions wihtout changing the data in the display data RAM.



* When ICON control register is set to "1", page address is set to "16", and user can write data for displaying icons.

Figure 6. Display Data RAM Map

7. LCD Display Circuit

FRC(Frame Rate Control) and PWM(Pulse Width Modulation) Function Circuit

NT7508 incorporates an FRC function and a PWM function circuit to display a 4 level gran scale. The FRC function and PWM utilize liquid crystal characteristics whose transmittance is changed by an effective value of applied voltage. The NT7508 provides four 4 bit palette-registers to assign the desired gray level. Thses registers are set by the instrucitons and the RESETB.

-Gray Scale Table of 4 FRC(Frame Rate Control)

Gray Scale Level	MSB (DB7 to DB4)	LSB (DB3 to DB0)
White	2nd FR (FR2)	1st FR (FR1)
	4th FR (FR4)	3rd FR (FR3)
Light Gray	2nd FR (FR2)	1st FR (FR1)
	4th FR (FR4)	3rd FR (FR3)
Dark Gray	2nd FR (FR2)	1st FR (FR1)
	4th FR (FR4)	3rd FR (FR3)
Black	2nd FR (FR2)	1st FR (FR1)
	4th FR (FR4)	3rd FR (FR3)

-Gray Scale Table of 3 FRC(Frame Rate Control)

Gray Scale Level	MSB (DB7 to DB4)	LSB (DB3 to DB0)
White	2nd FR (FR2)	1st FR (FR1)
	× × × ×	3rd FR (FR3)
Light Gray	2nd FR (FR2)	1st FR (FR1)
	× × × ×	3rd FR (FR3)
Dark Gray	2nd FR (FR2)	1st FR (FR1)
	× × × ×	3rd FR (FR3)
Black	2nd FR (FR2)	1st FR (FR1)
	× × × ×	3rd FR (FR3)

-Gray Scale Table of 15 PWM(Pulse Width Modulation)

Dec	Hex	4-bits	PWM(on width)	Note
0	00	0000	0 (0/15)	Brighter
1	01	0001	1/15	↑
2	02	0010	2/15	
3	03	0011	3/15	
4	04	0100	4/15	
5	05	0101	5/15	
6	06	0110	6/15	
7	07	0111	7/15	
8	08	1000	8/15	
9	09	1001	9/15	
10	0A	1010	10/15	↓

11	0B	1011	11/15	
12	0C	1100	12/15	
13	0D	1101	13/15	
14	0E	1110	14/15	
15	0F	1111	1 (15/15)	Darker

-Gray Scale Table of 12 PWM(Pulse Width Modulation)

Dec	Hex	4-bits	PWM(on width)	Note
0	00	0000	0 (0/12)	Brighter
1	01	0001	1/12	
2	02	0010	2/12	
3	03	0011	3/12	
4	04	0100	4/12	
5	05	0101	5/12	
6	06	0110	6/12	
7	07	0111	7/12	
8	08	1000	8/12	
9	09	1001	9/12	
10	0A	1010	10/12	
11	0B	1011	11/12	
12	0C	1100	1 (12/12)	Darker
13	0D	1101	0/12	This area is selected to OFF level (0/12 level)
14	0E	1110	0/12	
15	0F	1111	0/12	

-Gray Scale Table of 9PWM(Pulse Width Modulation)

Dec	Hex	4-bits	PWM(on width)	Note
0	00	0000	0 (0/9	Brighter
1	01	0001	1/9	
2	02	0010	2/9	
3	03	0011	3/9	
4	04	0100	4/9	
5	05	0101	5/9	
6	06	0110	6/9	
7	07	0111	7/9	
8	08	1000	8/9	
9	09	1001	1 (9/9)	Darker
10	0A	1010	0/9	This area is selected to OFF level (0/9 level)
11	0B	1011	0/9	
12	0C	1100	0/9	
13	0D	1101	0/9	
14	0E	1110	0/9	
15	0F	1111	0/9	

8. Oscillator

This is on-chip Oscillator. When external OSC mode, the oscillation stops, and the display clock is input through the OSC1 terminal.

9. Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock,CL(internal),generated by Oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal(M) which enables the LCD driver to make a AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. The frame signal or the line signal changes the M by setting internal instruction. Driving waveform and internal timing signal are shown in Figure 7.

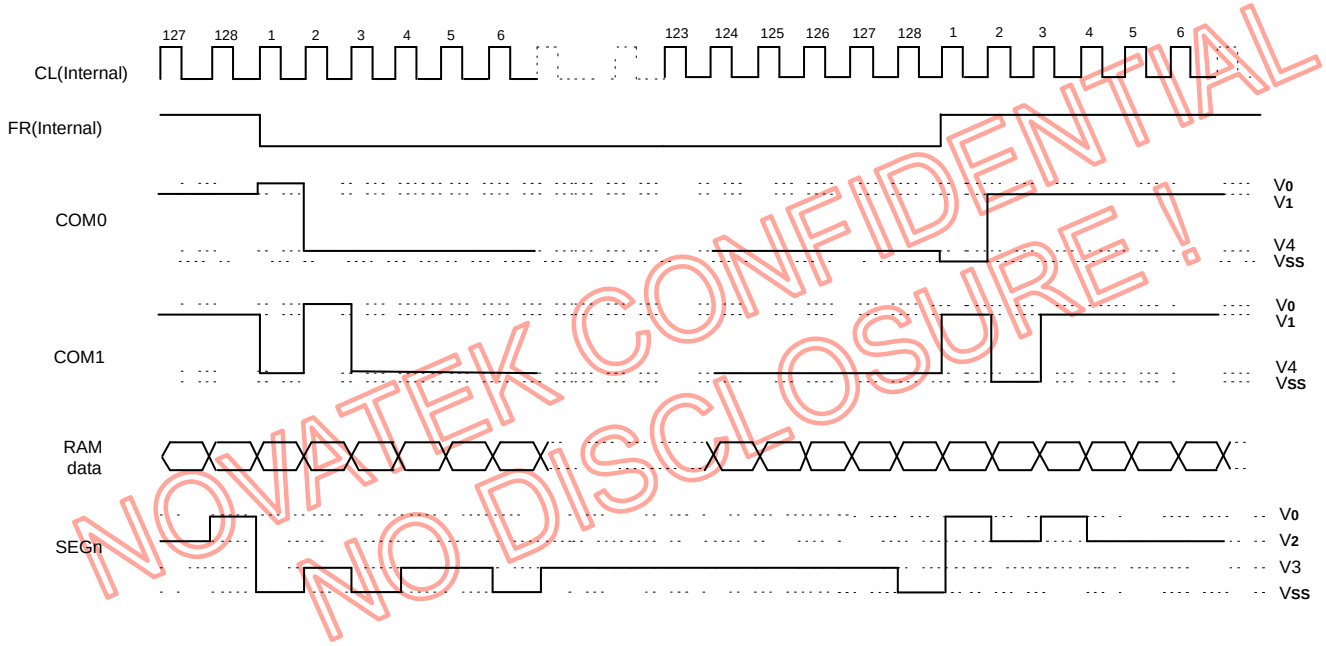


Figure 7. 2-frame AC Driving Waveform (Duty Ratio = 1/128)

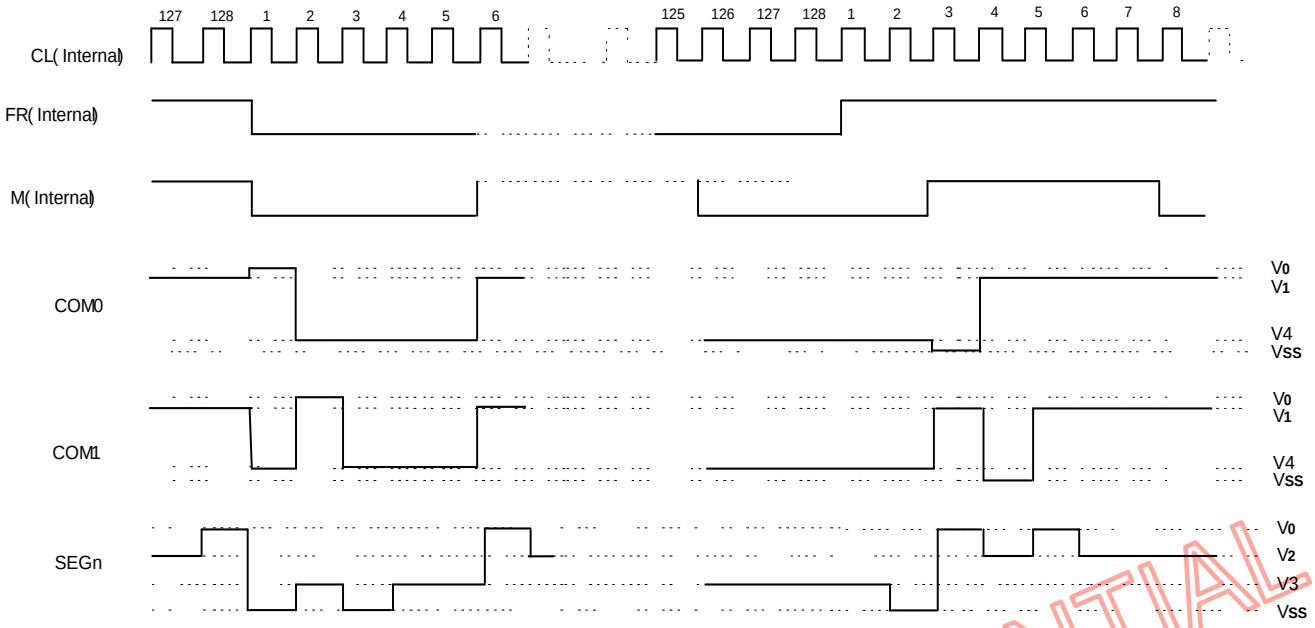


Figure 8. N-Line Inversion Driving Waveform (N = 5, Duty Ratio = 1/128)

10. LCD Driver Circuit

This driver circuit is configured by 129-channel common drivers and 128-channel segment drivers. This LCD panel driver voltage depends on the combination of display data and M signal.

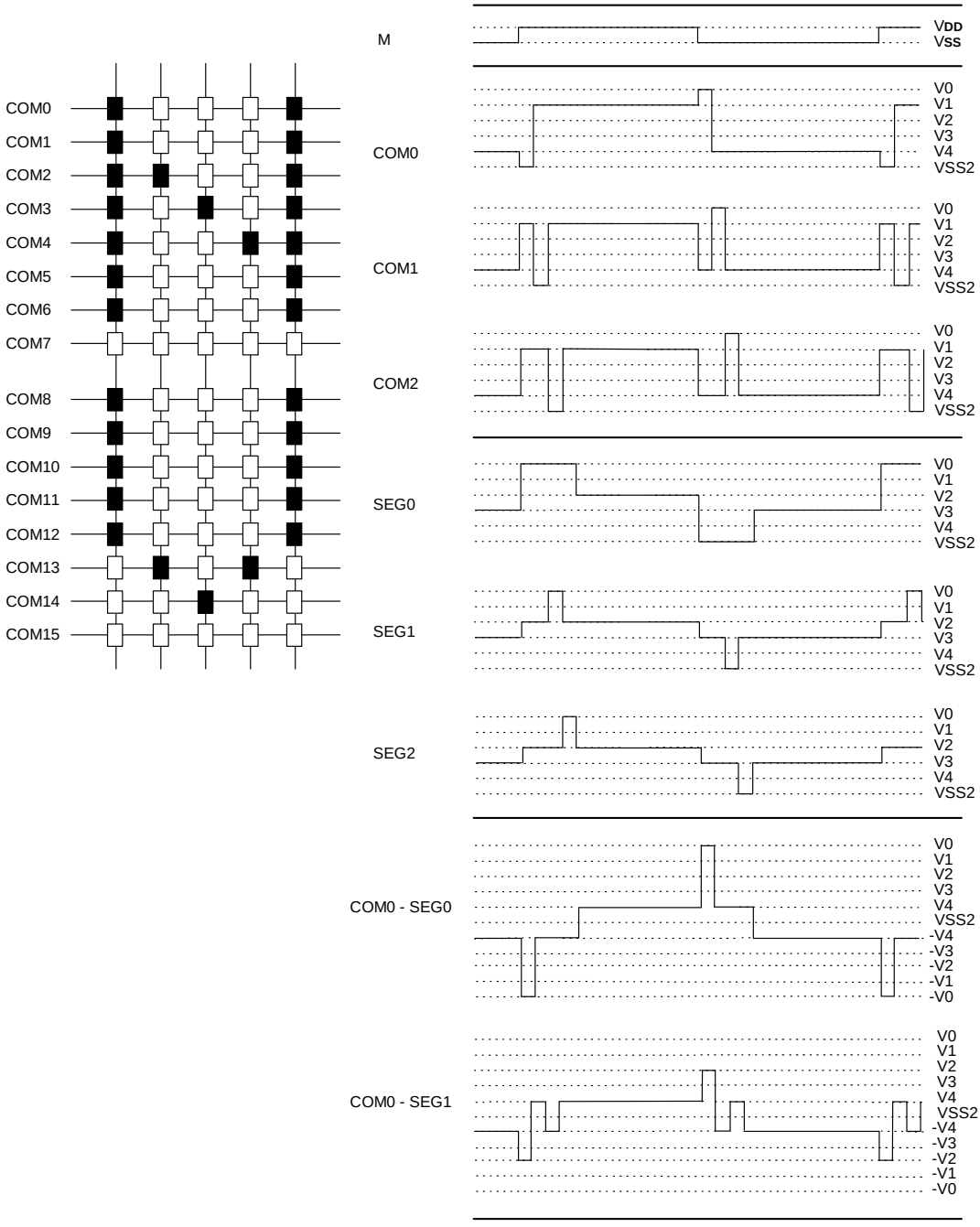


Figure 9. Segment and Common Timing

11. Partial Display On LCD

The NT7508 realizes the Partial Display function on LCD with low-duty driving for saving power consumption and showing the various display duty. To show the various display duty on LCD, LCD driving duty and bias are programmable via the instruction. And, built-in power supply circuits are controlled by the instruction for adjusting the LCD driving voltages.

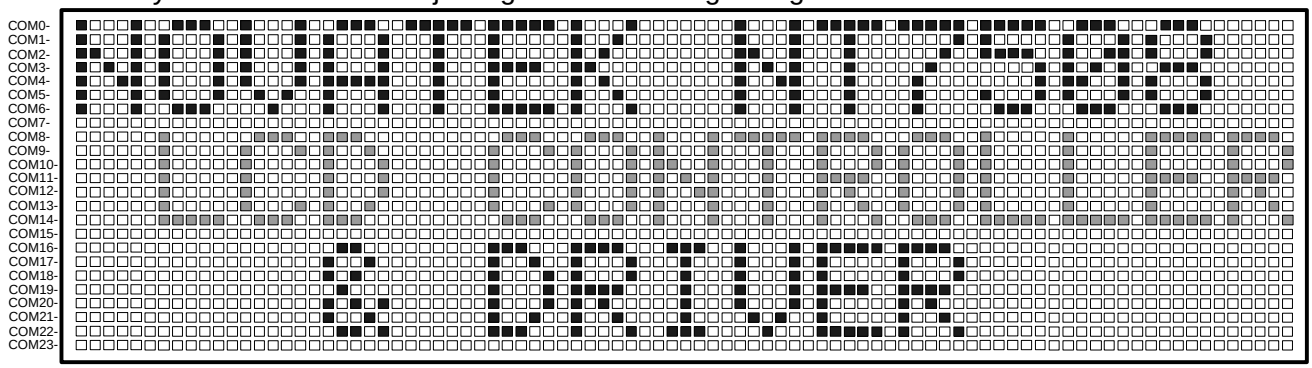


Figure 10. Reference Example for Partial Display

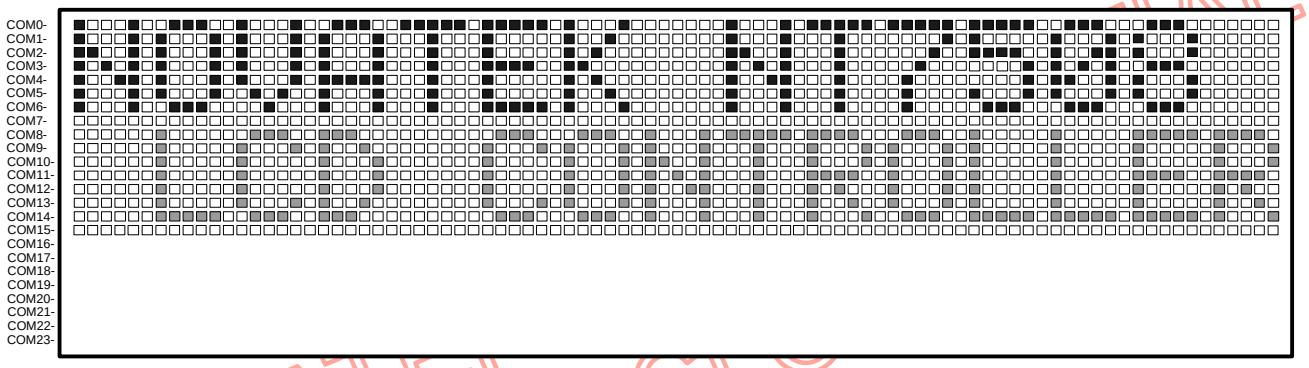


Figure 11. Partial Display (Partial Display Duty = 16, Initial COM0 = 0)

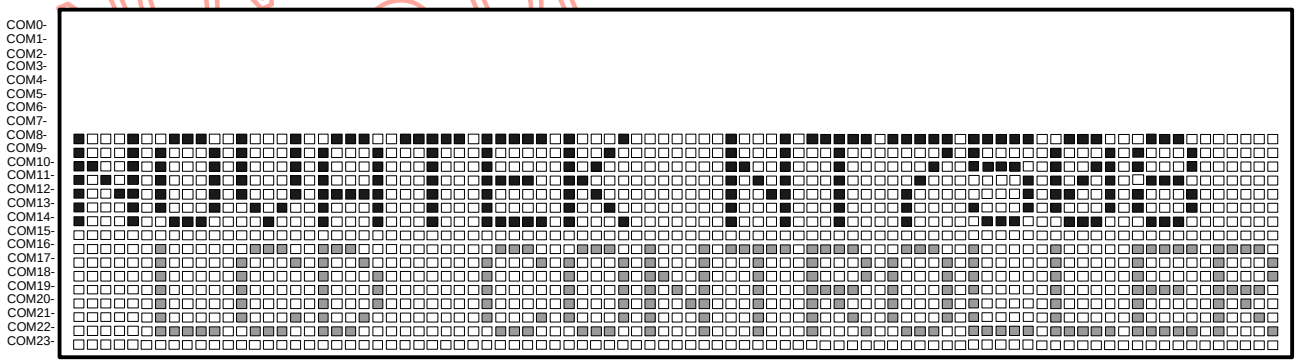


Figure 12. Moving Display (Partial Display Duty = 16, Initial COM0 = 8)

12. Power Supply Circuit

The power supply circuit generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are controllerd by power control instruction. For details, refers to “Instruction Description”. Table 4 shows the referenced combinations in using Power Supply circuits.

User setup	Power control (V/C V/R V/F)	V/C circuits	V/R circuits	V/F circuits	V0	V1 to V4
The internal power supply circuits are used	1 1 1	ON	ON	ON	Open	Open

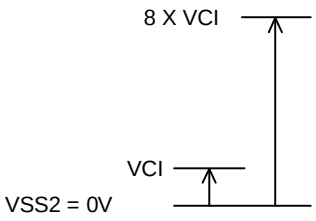
Table 4. Recommended Power Supply Combinations

13. Voltage Convertor Circuit

Using the step-up voltage circuits within the NT7508 chips it is possible to product 8X, 7X, 6X, 5X, 4X, 3X step-ups of the VCI-VSS2 voltage levels. The signal is internal pumping voltage, please keep the relationship: (VCI * times) > VLCD + Temperature Compensation Voltage + 3.0V.

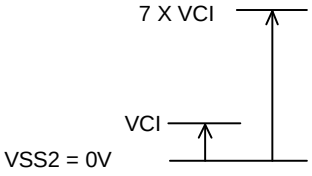
Figure 13

8x step-up voltage



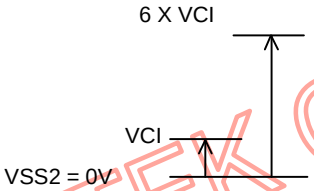
8x step-up voltage relationships

7x step-up voltage



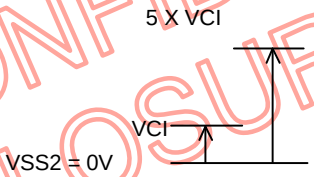
7x step-up voltage relationships

6x step-up voltage



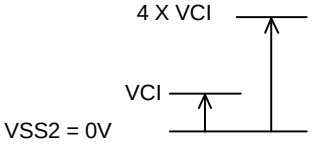
6x step-up voltage relationships

5x step-up voltage



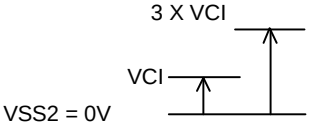
5x step-up voltage relationships

4x step-up voltage



4x step-up voltage relationships

3x step-up voltage



3x step-up voltage relationships

14. The Voltage Regulator Circuit

The function of the internal voltage regulator circuits is to determine liquid crystal operating voltage, V0 by adjusting resistor, Ra and Rb, within the range of V0. Because V0 is the operating voltage of operational-amplifier circuits shown in figure14, it is necessary to be applied internally.
For the Eq.1, we determine V0 by Ra,Rb and VEV. The Ra and Rb are connected internally. And VEV called the voltage of electronic volume is determined by Eq.2, where the parameter α is the value selected by instruction, “Set Reference Voltage Register”, within the range 0 to 63. VREF voltage at Ta=25℃ is shown in Table 5.

$$V0 = (1+\frac{Rb}{Ra}) \times VEV \text{ ---------- (Eq.1)}$$

$$VEV = (1-\frac{63-\alpha}{210}) \times VREF \text{ -------- (Eq.2)}$$

REF	Temp. coefficient	VREF(V)
Internal	-0.125 or -0.05%/°C	1.4

Table 5. VREF Voltage at Ta = 25℃

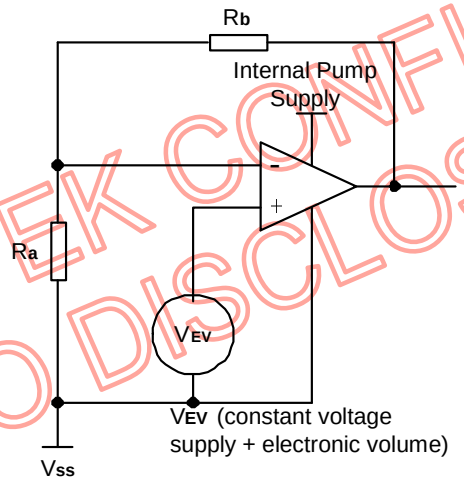


Figure 14. Internal Voltage Regulator Circuit

In Case of Using Internal Resistors, Ra and Rb

Resistor Ra is connected internally between VR and VSS, and Rb is connected between V0 and VR. We determine V0 by two instructions, “Regulator Resistor Select“ and “Set Reference Voltage”.

	3-bit data settings (R2 R1 R0)							
	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
1+ (Rb / Ra)	3.45	4.5	5.55	6.6	7.65	8.7	9.75	10.8

Table 6. Internal Rb / Ra Ratio depending on 3-bit Data (R2 R1 R0)

Figure 15 shows V0 voltage measured by adjusting internal regulator register ratio(Rb / Ra) and 6-bit electronic volume registers for each temperature coefficient at Ta = 25 °C.

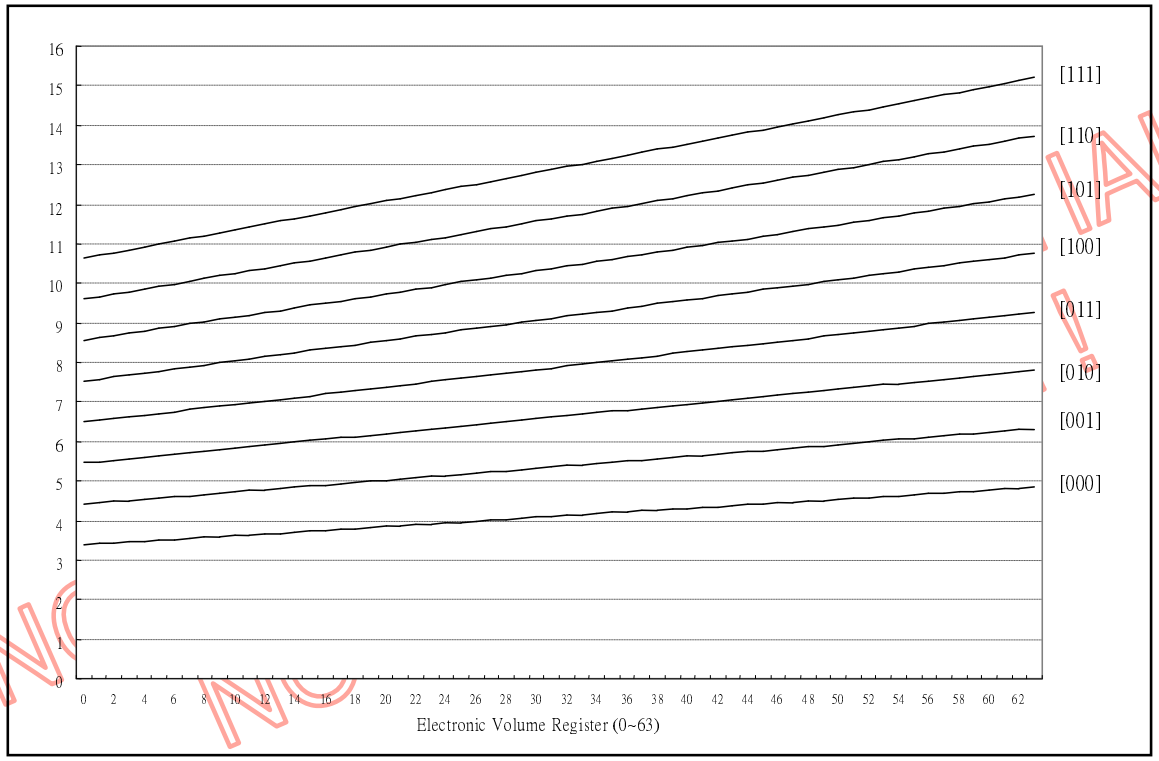


Figure 15. Electronic Volume Level (Temperature = 25 ℃)

15. Voltage Follower Circuit

VLCD voltage (V0) is resistively divided into four voltage levels (V1, V2, V3 and V4), and those output impedance are converted by the voltage follower for increasing drive capability. Table ** shows the relationship between V1 to V4 level and each duty ratio.

LCD bias	V1	V2	V3	V4	Remarks
1 / N	(N-1) / N × V0	(N-2) / N × V0	2 / N × V0	1 /N × V0	N = 5 to 12

Table 7. The Relationship between V1 to V4 Level and Each Duty Ratio

16. Reference Power Supply Circuit for Driving LCD Panel

[C1, C2, C3 = 1.0 ~ 2.2 (μF)]

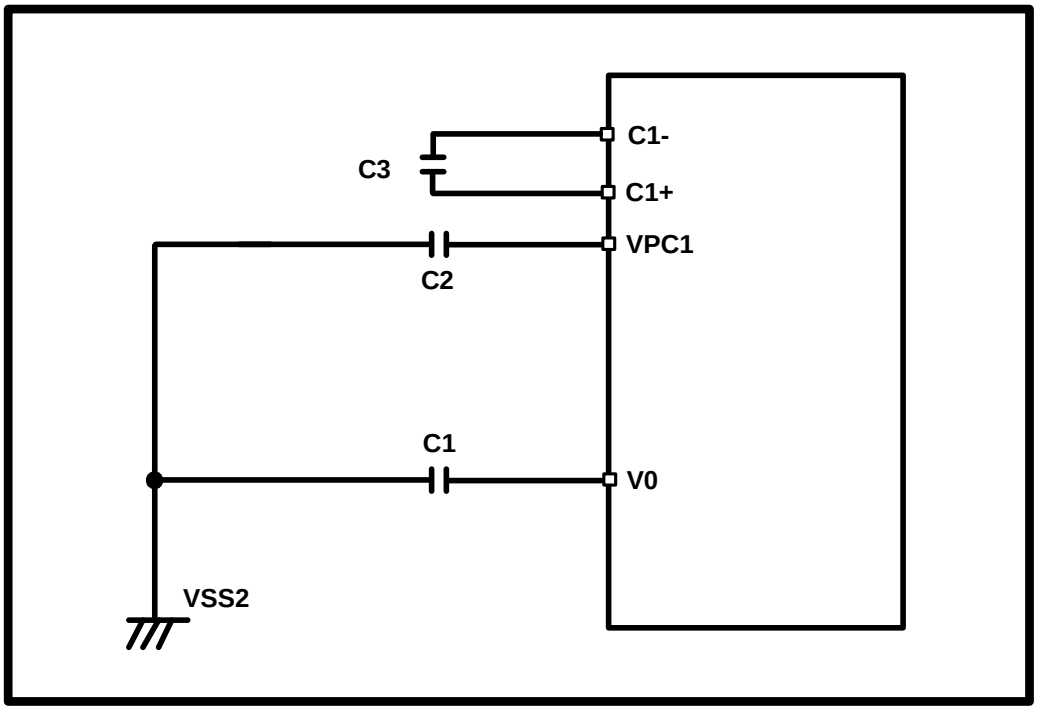


Figure 16. When using all LCD Power Circuits (V/C: ON, V/R: ON, V/F: ON)

17. Reset Circuit

Setting RESETB to “L” or Reset instruction can initialize internal function.
When RESETB becomes “L” , following procedure is occurred.

Page address : 0
Column address : 0
Read-modify-write : OFF
Display ON / OFF : OFF
Initial display line : 0 (first)
Initial COM0 register : 0 (COM 0)
Partial display duty ratio : 1/128
Reverse display ON/OFF : OFF (normal)
N-line inversion register : 0 (disable)
Entire display ON/OFF : OFF (Icon disable)
Icon control register ON/OFF : OFF (Icon disable)
Power control register (VC, VR, VF)= (0,0,0)
DC-DC converter circuit (DC2,DC1,DC0) = (0,0,0)
Regulator resistor select register : (R2,R1,R0) = (0, 0, 0)
Contrast Level : 32
LCD bias ratio : 1/12
COM scan Direction : 0
ADC select : 0
Oscillator : OFF
Power Save Mode : Release
Display Data Length register : 0 (for SPI mode)
White mode set : OFF
White palette register (WG3,WG2,WG1,WG0) = (0, 0, 0, 0)
Light gray mode set : OFF
Light gray palette register (LG3,LG2,LG1,LG0) = (0, 0, 0, 0)
Dark gray mode set : OFF
Dark gray palette register (DG3,DG2,DG1,DG0) = (1, 1, 1, 1)
Black mode set : OFF
Black palette register (BG3,BG2,BG1,BG0) = (1, 1, 1, 1)
FRC, PWM mode : 4FRC, 9PWM
Temperature coefficient set to –0.125%/℃
Select Oscillator Source : Internal OSC, RC Mode 0

When RESET instruction is issued, following procedure is occurred.

Page address : 0
Column address : 0
Read-modify-write : OFF
Initial display line : 0 (first)
Regulator resistor select register: (R2,R1,R0) = (0, 0, 0,)
Contrast Level : 32
Display Data Length register : 0 (for SPI mode)
White mode set : OFF
White palette register (WG3,WG2,WG1,WG0) = (0, 0, 0, 0)
Light gray mode set : OFF
Light gray palette register (LG3,LG2,LG1,LG0) = (0, 0, 0, 0)
Dark gray mode set : OFF
Dark gray palette register (DG3,DG2,DG1,DG0) = (1, 1, 1, 1)
Black mode set : OFF
Black palette register (BG3,BG2,BG1,BG0) = (1, 1, 1, 1)
FRC, PWM mode : 4FRC, 9PWM

While RESETB is “L” or reset instruciton is executed, no instruction except read status can be accepted. Reset status appears at DB5. After DB5 becomes “ L”,any instruction can be accepted. RESETB must be connected to the reset pin of the MPU, and initialize the MPU and this LSI at the same time. The initialization by RESETB is essential before used.

18. Instruction Description

Table 8. Instruction Table

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex	Description
Read display data	1	1	Read data								-	Read data from DDRAM
Write display data	1	0	Write data								-	Write data into DDRAM
Read status	0	1	BUSY	ON	RES	0	0	0	1	0	-	Read the internal status
Icon control register ON/OFF	0	0	1	0	1	0	0	0	1	ICON	A2h A3h	ICON=0: ICON disable (default) ICON=1: Icon enable & set the page address to icon page
Set page address	0	0	1	0	1	1	P3	P2	P1	P0	B0h ~ BFh	Set page address
Set column address MSB	0	0	0	0	0	1	0	Y7	Y6	Y5	10h ~ 17h	Set column address MSB
Set column address LSB	0	0	0	0	0	0	Y4	Y3	Y2	Y1	00h ~ 0Fh	Set column address LSB
Set modify-read	0	0	1	1	1	0	0	0	0	0	E0h	Set modify-read mode
Reset modify-read	0	0	1	1	1	0	1	1	1	0	EEh	Release modify-read mode
Display ON/OFF	0	0	1	0	1	0	1	1	1	D	AE AF	D=0:disply OFF D=1:display ON
Set initial display line register	0	0	0	1	0	0	0	0	×	×	40h ~ 43h	2-byte instruction to specify the initial display line to realize vertical scrolling
	0	0	×	S6	S5	S4	S3	S2	S1	S0		
Set initial COM0 Register	0	0	0	1	0	0	0	1	×	×	44h ~ 47h	2-byte instruction to specify the initial COM0 to realize vertical scrolling
	0	0	×	C6	C5	C4	C3	C2	C1	C0		
Set partial display duty ratio	0	0	0	1	0	0	1	0	×	×	48h ~ 4Bh	2-byte instruction to set partial display duty ratio
	0	0	D7	D6	D5	D4	D3	D2	D1	D0		
Set N-line inversion	0	0	0	1	0	0	1	1	×	×	4Ch ~ 4Fh	2-byte instruction to set N-line inversion register
	0	0	×	×	×	N4	N3	N2	N1	N0		
Release N-line inversion	0	0	1	1	1	0	0	1	0	0	E4h	Release N-line inversion mode
Reverse display ON/OFF	0	0	1	0	1	0	0	1	1	REV	A6h A7h	REV=0: normal display REV=1:reverse display
Entire display ON/OFF	0	0	1	0	1	0	0	1	0	EON	A4h A5h	EON=0:normal display EON=1:entire display ON

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex	Description
Power control	0	0	0	0	1	0	1	VC	VR	VF	28h ~ 2Fh	Control power circuit operation
Select DC-DC step-up	0	0	0	1	1	0	DC2	1	DC1	DC0	64h ~ 6Fh	Select the step-up of the internal voltage converter
Select regulator resistor	0	0	0	0	1	0	0	R2	R1	R0	20h ~ 27h	Select internal resistance ratio of the regulator resistor
Set electronic volume register	0	0	1	0	0	0	0	0	0	1	81h	2-byte instruction to specify the reference voltage
	0	0	×	×	EV5	EV4	EV3	EV2	EV1	EV0		
Select LCD bias	0	0	0	1	0	1	0	B2	B1	B0	50h ~ 57h	Select LCD bias
SHL select	0	0	1	1	0	0	SHL	×	×	×	C0h ~ CFh	COM bi-directional selection SHL=0: normal direction SHL=1: reverse direction
ADC select	0	0	1	0	1	0	0	0	0	ADC	A0h A1h	SEG bi-directional selection ADC=0: normal direction ADC=1: reverse direction
Oscillator on start	0	0	1	0	1	0	1	0	1	1	ABh	Start the built-in Oscillator
Set power save mode	0	0	1	0	1	0	1	0	0	P	A8h A9h	P=0: normal mode P=1: power save mode
Release power save mode	0	0	1	1	1	0	0	0	0	1	E1h	Release power save mode
Reset	0	0	1	1	1	0	0	0	1	0	E2h	Initialize the internal functions
Set data direction & display data length (DDL)	×	×	1	1	1	0	1	0	0	0	E8h	2-byte instruction to specify the number of data bytes
	×	×	D7	D6	D5	D4	D3	D2	D1	D0		
NOP	0	0	1	1	1	0	0	0	1	1	E3h	No operation
Test Instruction	0	0	1	1	1	1	×	×	×	×	F0h ~ FFh	Don't use this instruction
Set FRC and PWM	0	0	1	0	0	1	0	FRC	PWM 1	PWM 0	90h ~ 97h	FRC (1: 3 FRC, 0: 4 FRC) PWM1 PWM0 0 0 9PWM 0 1 9PWM 1 0 12PWM 1 1 15PWM

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex	Description
Set white mode and 1st/2nd frame, set pulse width	0	0	1	0	0	0	1	0	0	0	88h	Set white mode and 1st/2nd frame
	0	0	WB3	WB2	WB1	WB0	WA3	WA2	WA1	WA0		
Set white mode and 3rd/4th frame, set pulse width	0	0	1	0	0	0	1	0	0	1	89h	Set white mode and 3rd/4th frame
	0	0	WD3	WD2	WD1	WD0	WC3	WC2	WC1	WC0		
Set light gray mode and 1st/2nd frame, set pulse width	0	0	1	0	0	0	1	0	1	0	8Ah	Set light gray mode and 1st/2nd frame
	0	0	LB3	LB2	LB1	LB0	LA3	LA2	LA1	LA0		
Set light gray mode and 3rd/4th frame, set pulse width	0	0	1	0	0	0	1	0	1	1	8Bh	Set light gray mode and 3rd/4th frame
	0	0	LD3	LD2	LD1	LD0	LC3	LC2	LC1	LC0		
Set dark gray mode and 1st/2nd frame, set pulse width	0	0	1	0	0	0	1	1	0	0	8Ch	Set dark gray mode and 1st/2nd frame
	0	0	DB3	DB2	DB1	DB0	DA3	DA2	DA1	DA0		
Set dark gray mode and 3rd/4th frame, set pulse width	0	0	1	0	0	0	1	1	0	1	8Dh	Set dark gray mode and 3rd/4th frame
	0	0	DD3	DD2	DD1	DD0	DC3	DC2	DC1	DC0		
Set black mode and 1st/2nd frame, set pulse width	0	0	1	0	0	0	1	1	1	0	8Eh	Set black mode and 1st/2nd frame
	0	0	BB3	BB2	BB1	BB0	BA3	BA2	BA1	BA0		
Set black mode and 3rd/4th frame, set pulse width	0	0	1	0	0	0	1	1	1	1	8Fh	Set black mode and 3rd/4th frame
	0	0	BD3	BD2	BD1	BD0	BC3	BC2	BC1	BC0		
Set Temperature Coefficient Value	0	0	1	1	1	1	0	0	0	1	F1h	0: -0.125%/℃ 1: -0.05%/℃
	0	0	0	0	0	0	0	0	0	TC		
Select Oscillator Source	0	0	1	1	1	1	0	1	1	1	F7h	RC: 0: Internal OSC 1: External OSC FR Mode: 0: Mode 0 1: Mode 1
	0	0	0	0	0	0	0	0	FR Mode	RC		
Frame Frequency Adjust	0	0	1	1	1	1	0	1	1	0	F6h	OSC frequency select and frame divider select
	0	0	0	0	0	F4	F3	F2	F1	F0		
OTP Calibration Set	0	0	1	1	1	1	0	0	1	1	F3h	Set V0 OTP Data
	0	0	0	0	0	0	V0 OTP Data [3:0]					
Programming Set	0	0	1	1	1	1	0	1	0	0	F4h	OTP Programming
	0	0	0	0	0	0	0	0	PG	EN		

1. Read Display Data

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Read Data							

8-bit data from Display Data RAM specified by the column address and page address can be read by this instruction. As the column address is increased by 1 automatically after each this instruction, the microprocessor can continuously read data from the addressed page. A dummy read is required after loading an address into the column address register. Display Data cannot be red through the serial interface.

2. Write Display Data

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	Write Data							

8-bit data of Display Data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page.During auto-increasement, the column address wraps to 0 after the last column is written.

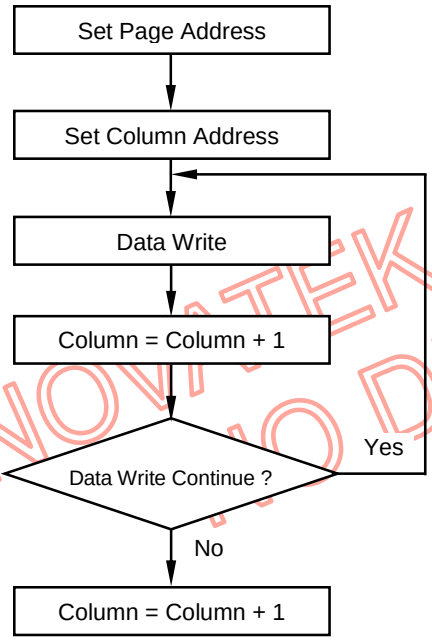


Figure 17. Sequence for Writing Display Data

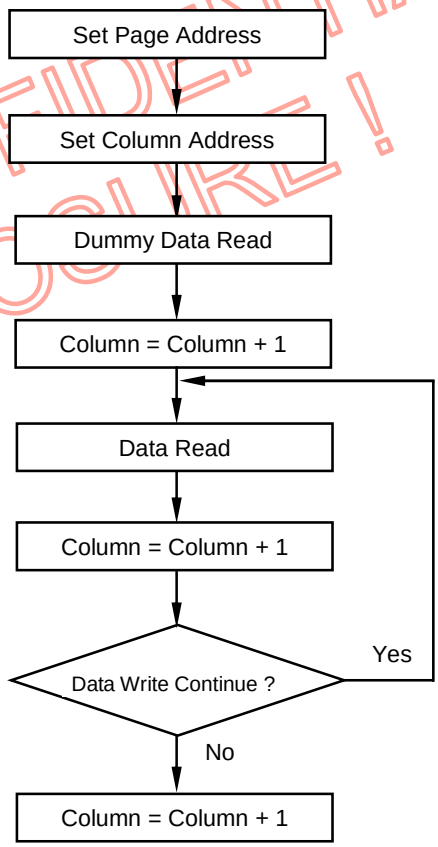


Figure 18. Sequence for Reading Display Data

3. Read Status

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BUSY	ON/OFF	RES	0	0	0	1	0

Flag	Description
BUSY	The device is busy when internal operation or reset. Any instruction is rejected until BUSY goes Low. 0:Chip is active, 1:Chip is being busy.
ON / OFF	Indicates display ON/OFF status. 0: display OFF, 1:display ON
RESET	Indicates the initialization is in progress by RESET signal. 0: Chip is active, 1:Chip is being reset.

Indicates the internal staus of the NT7508

4. ICON Control Register ON/OFF

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	1	Icon

This instruciton makes icon enable or disable. By default, icon display is disabled (ICON = 0). When icon control register is set to “1”, icon display is enabled and page address is set to icon page. Then user can write data for icons. When writing data for icons, icon control register ON instruction would be used to set the page address to icon page. When icon control register is set to “0” (ICON=0), icon display is disabled.
ICON=0: Icon disable (default)
ICON=1: Icon enable & set the page address to icon address

5. Set Page Address

Sets the Page Address of display data RAM from the microprocessor into the page address register. Any RAM data bit can be accessed when its Page Address and column address are specified. Along with the column address, the Page Address defines the address of the display RAM to write or read display data. Changing the Page Address doesn’t effect to the display status. Set Page Address instruction can not be used to set the page address to icon page. Use ICON control register ON/OFF instruction to set the page address to icon address.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	P3	P2	P1	P0

P3	P2	P1	P0	Page
0	0	0	0	0
0	0	0	1	1
:	:	:	:	:
1	1	1	0	14
1	1	1	1	15

6. Set Column Address

Sets the column address of display RAM from the microprocessor into the column address register. Along with the column address, the column address defines the address of the display RAM to write or read display data. When the microprocessor reads or writes display datra to or from display RAM, column address are automatically increased.

Set Column Address MSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	0	Y7	Y6	Y5

Set Column Address LSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	Y4	Y3	Y2	Y1

Y7	Y6	Y5	Y4	Y3	Y2	Y1	Column Address [Y7:Y1]
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	126
1	1	1	1	1	1	1	127

7. Set Modify – Read

The instruction stops the automatic increment of the column address by the read display data instruction, but the column address is still increased by the write display data instruction. And it reduces the load of microprocessor when the data of a specific area is repeatedly changed during cursor blinking or others. This mode is canceled by the reset Modify-Read instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	0

8. Reset Modify – Read

The instruction cancels the modify-read mode. And makes the column address return to its initial value just before the set modify-read instruction is started.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	1	1	0

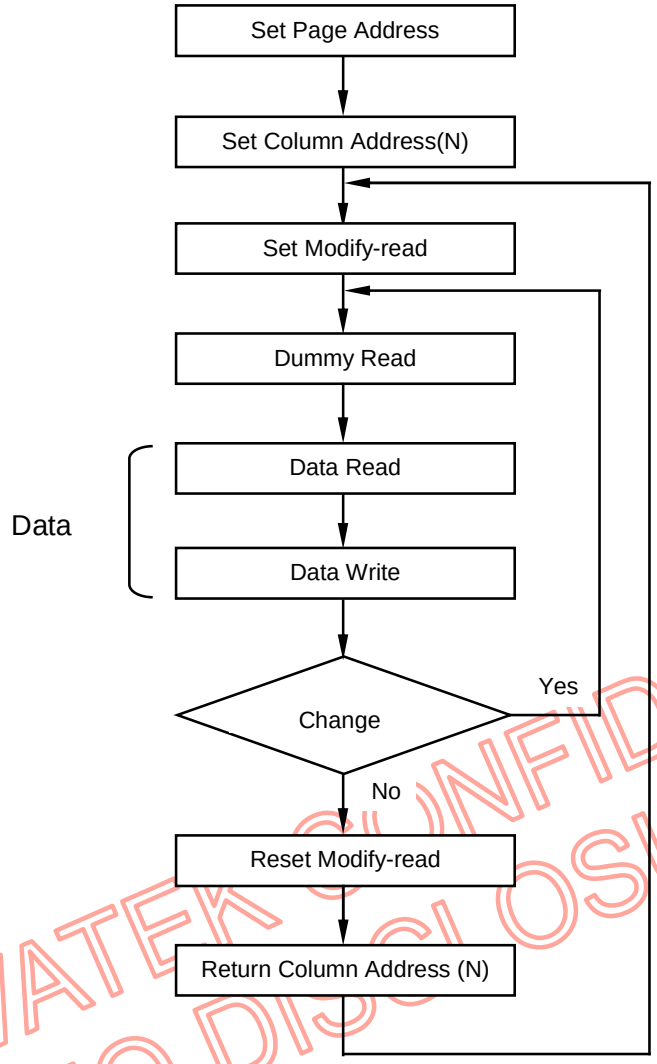


Figure 19. Sequence for Cursor Display

9. Display ON/OFF

Turns the display ON or OFF
This command has priority over Entire Display On/Off and Reverse Display On/Off. Commands are accepted while the display is off, but the visual state of the display does not change.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	1	DON

DON = 1 : Display ON
DON = 0 : Display OFF

10. Set Initial Display Line Register

Set the line address of display RAM to determine the initial display line using 2-byte instruciton. The RAM display data is displayed at the top of row(Com0) of LCD panel.

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	0	0	×	×

The 2nd instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	S6	S5	S4	S3	S2	S1	S0

S6	S5	S4	S3	S2	S1	S0	Line Address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
:	:	:	:	:	:	:	:
1	1	1	1	1	0	0	124
1	1	1	1	1	0	1	125
1	1	1	1	1	1	0	126
1	1	1	1	1	1	1	127

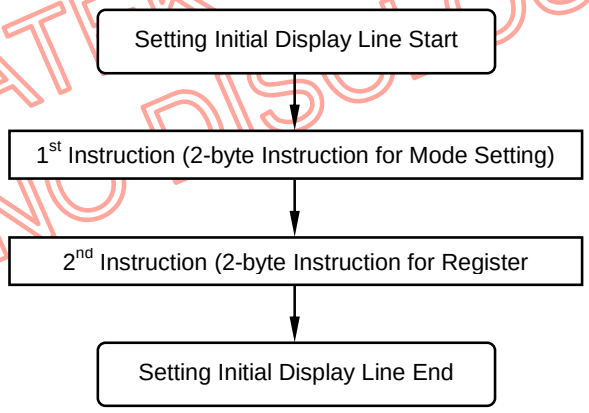


Figure 20. The Sequence for setting the Initial Display Line

11. Set Initial COM0 Register

Sets the initila row (com) of the LCD panel using the 2-byte instruction. By using this instruction, it is possible to realize the window moving without the change of display data.

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	0	1	×	×

The 2nd instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	C6	C5	C4	C3	C2	C1	C0

C6	C5	C4	C3	C2	C1	C0	Line Address
0	0	0	0	0	0	0	COM 0
0	0	0	0	0	0	1	COM 1
0	0	0	0	0	1	0	COM 2
0	0	0	0	0	1	1	COM 3
:	:	:	:	:	:	:	:
1	1	1	1	1	0	0	COM 124
1	1	1	1	1	0	1	COM 125
1	1	1	1	1	1	0	COM 126
1	1	1	1	1	1	1	COM 127

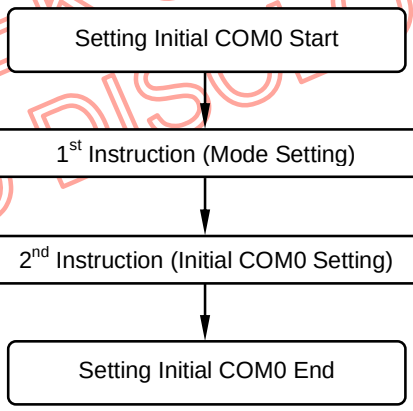


Figure 21. Sequence for Setting the Initial COM0

12. Set Partial Display Duty Ratio

Sets the duty ratio within range of 16 to 128 (ICON=0) or 17 to 129 (ICON=1) to realize partial display by using the 2-byte instruction.

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	1	0	×	×

The 2nd instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	D7	D6	D5	D4	D3	D2	D1	D0

D7	D6	D5	D4	D3	D2	D1	D0	Selected partial duty ratio (ICON=0)	Selected partial duty ratio (ICON=1)
0	0	0	0	0	0	0	0	No Operation	No Operation
:	:	:	:	:	:	:	:		
0	0	0	0	1	1	1	1		
0	0	0	1	0	0	0	0	1/16	1/17
0	0	0	1	0	0	0	1	1/17	1/18
:	:	:	:	:	:	:	:	:	:
0	1	1	1	1	1	1	1	1/127	1/128
1	0	0	0	0	0	0	0	1/128	1/129
1	0	0	0	0	0	0	1	No operation	No operation
:	:	:	:	:	:	:	:		
1	1	1	1	1	1	1	1		

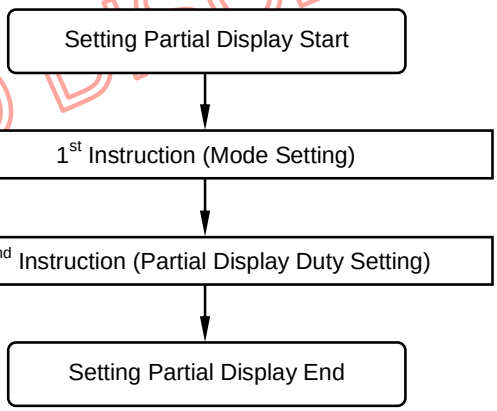


Figure 22. Sequence for Setting Partial Display

13. Set N-line Inversion Registr

Sets the inverted line number within range of 3 to 33 to improve the display quality by controlling the phase of the internal LCD AC signal (M) by using the 2-byte instruction.
The DC-bias problem could be occourred if K is even number. So, we recommend customers to set K to be odd number.
K : D / N
D : The number of display duty ratio (D is selectable by customers)
N : N for N-line inversion (N is selectable by customers)

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	1	1	×	×

The 2nd instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	×	×	N4	N3	N2	N1	N0

N4	N3	N2	N1	N0	Selected n-line inversion
0	0	0	0	0	0-line inversion (frame inversion)
0	0	0	0	1	3-line inversion
0	0	0	1	0	4-line inversion
0	0	0	1	1	5-line inversion
:	:	:	:	:	:
1	1	1	0	1	31-line inversion
1	1	1	1	0	32-line inversion
1	1	1	1	1	33-line inversion

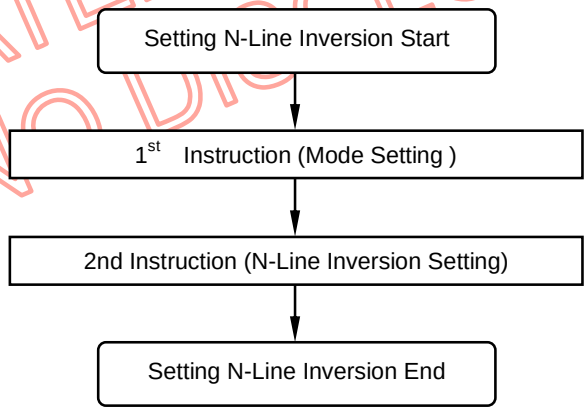


Figure 23. Sequence for N-line Inversion

14. Release N-line Inversion

Returns to the frame inversion condition from the n-line inversion condition.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	1	0	0

15. Reverse Display ON/OFF

Reverses the display status on LCD panel without rewriting the contents of the display data RAM.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	1	REV

REV	DD RAM data = “00” (White)	DD RAM data = “01” (Light Gray)	DD RAM data = ”10” (Dark Gray)	DD RAM data = “ 11” (Dark)
0 (normal)	White (“00”)	Light Gray (“01”)	Dark Gray (“10”)	Dark (“11”)
1 (reverse)	Dark (“11”)	Dark Gray (“10”)	Light Gray (“01”)	White (“00”)

16. Entire Display ON/OFF

Forces the whole LCD points to be turned on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held. This instruction has priorty over the Reverse Display ON/OFF instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	0	EON

EON	DD RAM data = “00” (White)	DD RAM data = “01” (Light Gray)	DD RAM data = ”10” (Dark Gray)	DD RAM data = “ 11” (Dark)
0 (normal)	White (“00”)	Light Gray (“01”)	Dark Gray (“10”)	Black (“11”)
1 (entire)	Black (“11”)	Black (“11”)	Black (“11”)	Black (“11”)

17. Power Control

Select one of eight power circuit functions by using 3-bit register.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	1	VC	VR	VF

V/C	V/R	V/F	Status of internal power supply circuits
0 1			Internal voltage converter circuit is OFF Internal voltage converter circuit is ON
	0 1		Internal voltage regulator circuit is OFF Internal voltage regulator circuit is ON
		0 1	Internal voltage follower circuit is OFF Internal voltage follower circuit is ON

18. Select DC-DC Set-Up

Selects one of 6 DC-DC step-up to reduce the power consumption by this instruction. It is very useful to realize the partial display function.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	0	DC2	1	DC1	DC0

DC2	DC1	DC0	Select DC-DC converter circuit
0	0	0	3 times boosting circuit
0	0	1	4 times boosting circuit
0	1	0	5 times boosting circuit
0	1	1	6 times boosting circuit
1	0	0	7 times boosting circuit
1	0	1	8 times boosting circuit
1	1	0	8 times boosting circuit
1	1	1	8 times boosting circuit

19. Select Regulator Resistor

Selects resistance ratio of the internal resistor used in the internal voltage regulator. See voltage regulator section in power supply circuit. Refer to the table **.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	0	R2	R1	R0

R2	R1	R0	1 + (Rb / Ra)
0	0	0	3.45
0	0	1	4.50
0	1	0	5.55
0	1	1	6.60
1	0	0	7.65
1	0	1	8.70
1	1	0	9.75
1	1	1	10.80

20. Set Electronic Volumn Register

Consist of 2-byte instructins
The 1st instruction set Reference Voltage mode, the 2nd one updates the contents of reference voltage register. After second instruction, Reference Voltage mode is released.
The 1st Instruction: Set Reference Voltage Select Mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	1

The 2nd instruction :Set Reference Voltage Register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	×	EV5	EV4	EV3	EV2	EV1	EV0

EV5	EV4	EV3	EV2	EV1	EV0	Reference voltage parameter (α)
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

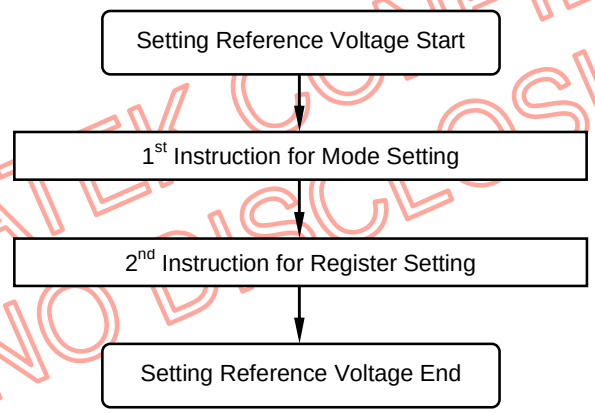


Figure 24. Sequence for Setting the Electronic Volume

21. Select LCD Bias

Selects LCD bias ratio of the voltage required for driving the LCD.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	1	0	B2	B1	B0

B2	B1	B0	LCD bias
0	0	0	1/5
0	0	1	1/6
0	1	0	1/7
0	1	1	1/8
1	0	0	1/9
1	0	1	1/10
1	1	0	1/11
1	1	1	1/12

22. SHL Select

COM output scanning direction is select by this instruction which determines the LCD driver output staus.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	SHL	×	×	×

SHL = “0” : normal direction (COM0 → COM127)
SHL = “1” : reverse direction (COM127 → COM0)

23. ADC Select

Changes the relationship between RAM column address and segment driver. The direction of segment driver output pins could be reversed by software. This makes IC layout flexible in LCD module assembly.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	ADC

ADC = “0” : normal direction (SEG0 → SEG127)
ADC = “1” : reverse direction (SEG127 → SEG0)

24. Oscilliator On Start

This instruction enales the built in Oscillator circuit.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	1

25. Power Save

The NT7508 enters the power save status to reduce the power consumption to the static power consumption value and returns to the normal operation status by the following instructions.

Set Power Save Mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	P

P = “0” : Normal mode
P = “1” : Power save mode

Release Power Save Mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	1

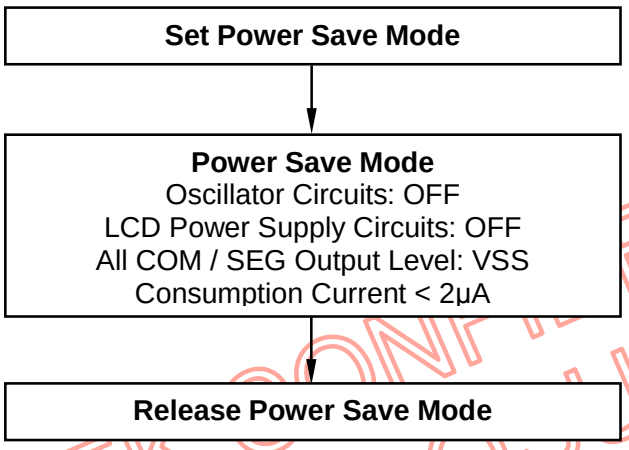


Figure 25. Power Save Routine

26. Reset

This instruction resets initial display line, column address, page address, and common output status select to their initial status, but does not affect the contents of display data RAM. This instruction cannot initialize the LCD power supply, which is initialized by the RESETB pin.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	0

27. Set Data Direction & Display Data Length (3-PIN SPI Mode)

Consists of 2 bytes instruciton.
This command is used in 3-pin SPI mode only(PS0 = “L” and PS1 = “L”). It will be two continuous commands, the first byte control the data direction(write mode only) and inform the LCD driver the second byte will be number of data bytes will be write. When RS is not used, the Display Data Length instruction is used to indicate that a specified number of display data bytes are to be transmitted. The next byte after the display string is handled as command data.

The 1st Instruction: Set Data Direction (Only Write Mode)

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
×	×	1	1	1	0	1	0	0	0

The 2nd Instruction: Set Display Data Length (DDL) Register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
×	×	D7	D6	D5	D4	D3	D2	D1	D0

D7	D6	D5	D4	D3	D2	D1	D0	Display Data Length
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	1	0	3
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	1	254
1	1	1	1	1	1	1	0	255
1	1	1	1	1	1	1	1	256

28. Nop

No operation

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	1

29. Test I Instruction

This instruction is for testing IC. Please do not use this instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	×	×	×	×

30. Set PWM & FRC mode

Select 3 / 4 FRC and 9 / 12 / 15 PWM.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	FRC	PWM1	PWM0

FRC	PWM1	PWM0	Status of PWM & FRC
0			4 FRC
1			3 FRC
	0	0	9 PWM
	0	1	9 PWM
	1	0	12 PWM
	1	1	15 PWM

31. Set Gray Scale Mode & Register

Consists of 2 bytes instruction. The first byte sets grayscale mode and the second byte updates the contents of gray scale register without issuing any other instruction.
Set Gray Scale Mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	1	GM2	GM1	GM0

GM2	GM1	GM0	Description
0	0	0	In case of setting white mode and 1st/2nd frame
0	0	1	In case of setting white mode and 3rd /4th frame
0	1	0	In case of setting light gray mode and 1st/2nd frame
0	1	1	In case of setting light gray mode and 3rd /4th frame
1	0	0	In case of setting dark gray mode and 1st/2nd frame
1	0	1	In case of setting dark gray mode and 3rd /4th frame
1	1	0	In case of setting black mode and 1st/2nd frame
1	1	1	In case of setting black mode and 3rd /4th frame

Set Gray Scale Register

RS	RW	DB 7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	GB3	GB2	GB1	GB0	GA3	GA2	GA1	GA0
0	0	GD3	GD2	GD1	GD0	GC3	GC2	GC1	GC0

GA3, GB3 GC3, GD3	GA2, GB2 GC2, GD2	GA1, GB1 GC1, GD1	GA0, GB0 GC0, GD0	Pulse width (9PWM)	Pulse width (12PWM)	Pulse width (15PWM)
0	0	0	0	0 / 9	0 / 12	0 / 15
0	0	0	1	1 / 9	1 / 12	1 / 15
:	:	:	:	:	:	:
1	0	0	1	9 / 9	9 / 12	9 / 15
1	0	1	0	0 / 9	10 / 12	10 / 15
1	0	1	1	0 / 9	11 / 12	11 / 15
1	1	0	0	0 / 9	12 / 12	12 / 15
1	1	0	1	0 / 9	0 / 12	13 / 15
1	1	1	0	0 / 9	0 / 12	14 / 15
1	1	1	1	0 / 9	0 / 12	15 / 15

GA3= WA3, LA3, DA3, BA3 GA2= WA2, LA2, DA3, BA2 GA1=WA1, LA1, DA1, BA1 GA0= WA0, LA0, DA0, BA0
GB3= WB3, LB3, DB3, BB3 GA2= WB2, LB2, DB2, BB2 GA1=WB1, LB1, DB1, BB1 GA0= WB0, LB0, DB0, BB0
GC3= WC3, LC3, DC3, BC3 GA2= WC2, LC2, DC2, BC2 GA1=WC1, LC1, DC1, BC1 GA0= WD0, LD0, DD0, BD0
GD3= WD3, LD3, DD3, BD3 GA2=WD2, LD2, DD2, BD2 GA1=WD1, LD1, DD1, BD1 GA0= WD0, LD0, DD0, BD0

32. Set Temperature Compensation

This command can select the average temperature compensation coefficients. The default value of the temperature compensation coefficients is -0.125%/℃ .

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	0	0	1
0	0	0	0	0	0	0	0	0	TC

There are four sets of temperature compensation coefficients can be selected as follow.

TC	Temperature Compensation Coefficient (at 25℃)
0	-0.125%/℃
1	-0.05%/℃

33. Select Oscillator Source

This command can select the Internal/External Oscillator. The default value of the oscillator source is internal mode.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	1	1	1
0	0	0	0	0	0	0	0	FR	RC

RC	Select Oscillator Source
0	Internal Oscillator
1	External Oscillator from OSC1 pin

FR	Frame Mode Select	Frame
0	Mode 0	9PWM:112Hz, 12PWM:84Hz, 15PWM:67.2Hz
1	Mode 1	Frame = Fosc / [Duty x (FrameFQ+1) x PWM]

34. Set Frame Frequency Adjust (FR Mode 1)

This command can set Frame Frequency.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	1	1	0
0	0	0	0	0	F4	F3	F2	F1	F0

F4 F3	Fosc
00	92KHz
01	122KHz
10	147KHz
11	184KHz

F2 F1 F0	FrameFQ
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

Frame Frequency = Fosc / [Duty x (FrameFQ+1) x PWM]

35. Set V0 OTP Data

This command can adjust V0 OTP Data.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	0	1	1
0	0	0	0	0	0	V0_OTP Data [3:0]			

The Setting of the offset value of contrast.

V0_OTP_Data	Step	V0_OTP_Data	Step
1000	-8	0000	0
1001	-7	0001	1
1010	-6	0010	2
1011	-5	0011	3
1100	-4	0100	4
1101	-3	0101	5
1110	-2	0110	6
1111	-1	0111	7

36. OTP Programming

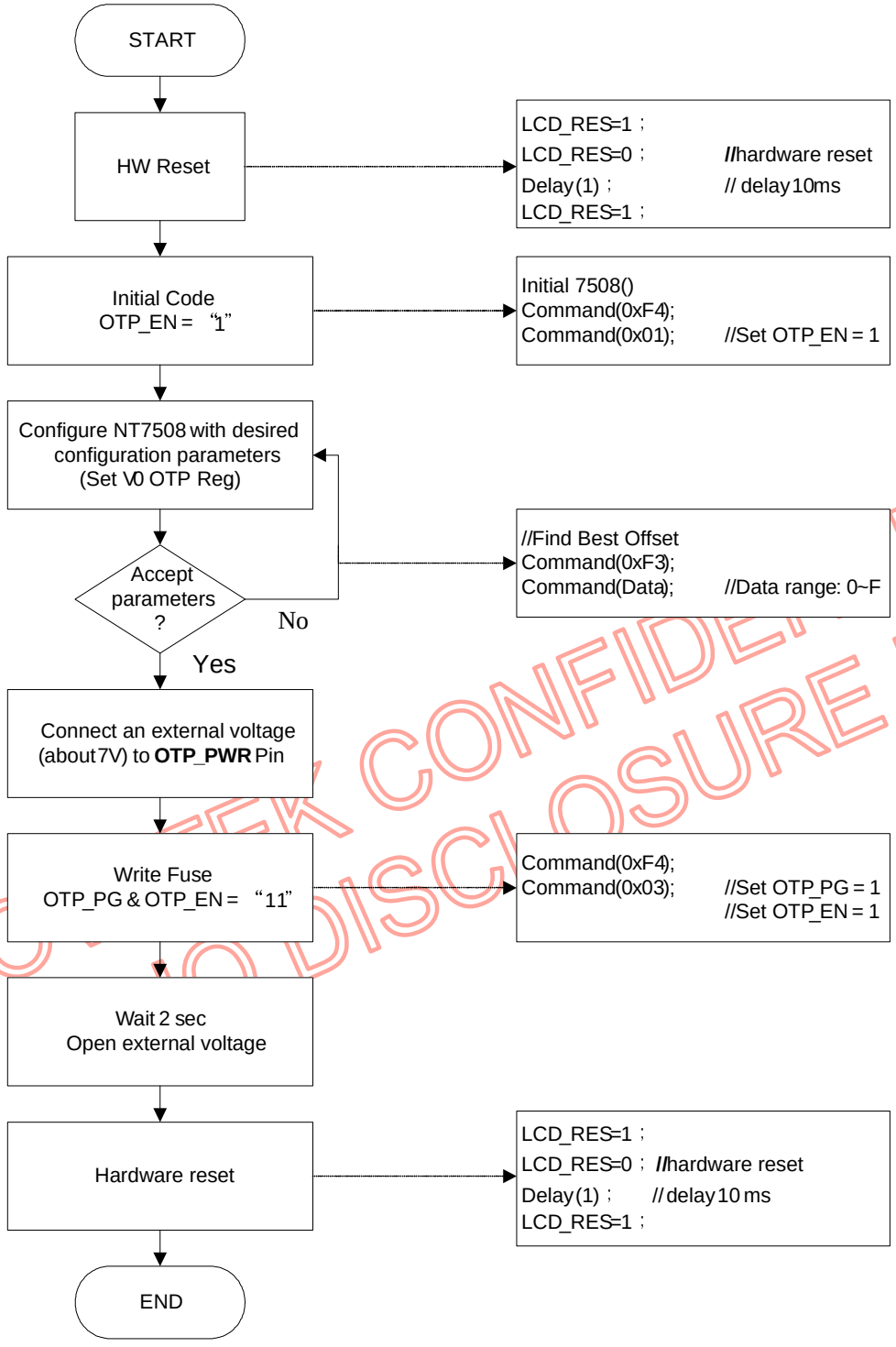
This command can set OTP programming mode.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	1	0	0
0	0	0	0	0	0	0	0	OTP_PG	OTP_EN

The Setting of the V0 OTP programming mode.

OTP_PG	OTP_EN	OTP Programming Mode
0	0	Normal Mode
0	1	Test Mode
1	1	Fusing

NT7508 OTP Fusing Flow



Referential Instruction Set-up Flow: Initializing with the built-in Power Supply Circuits

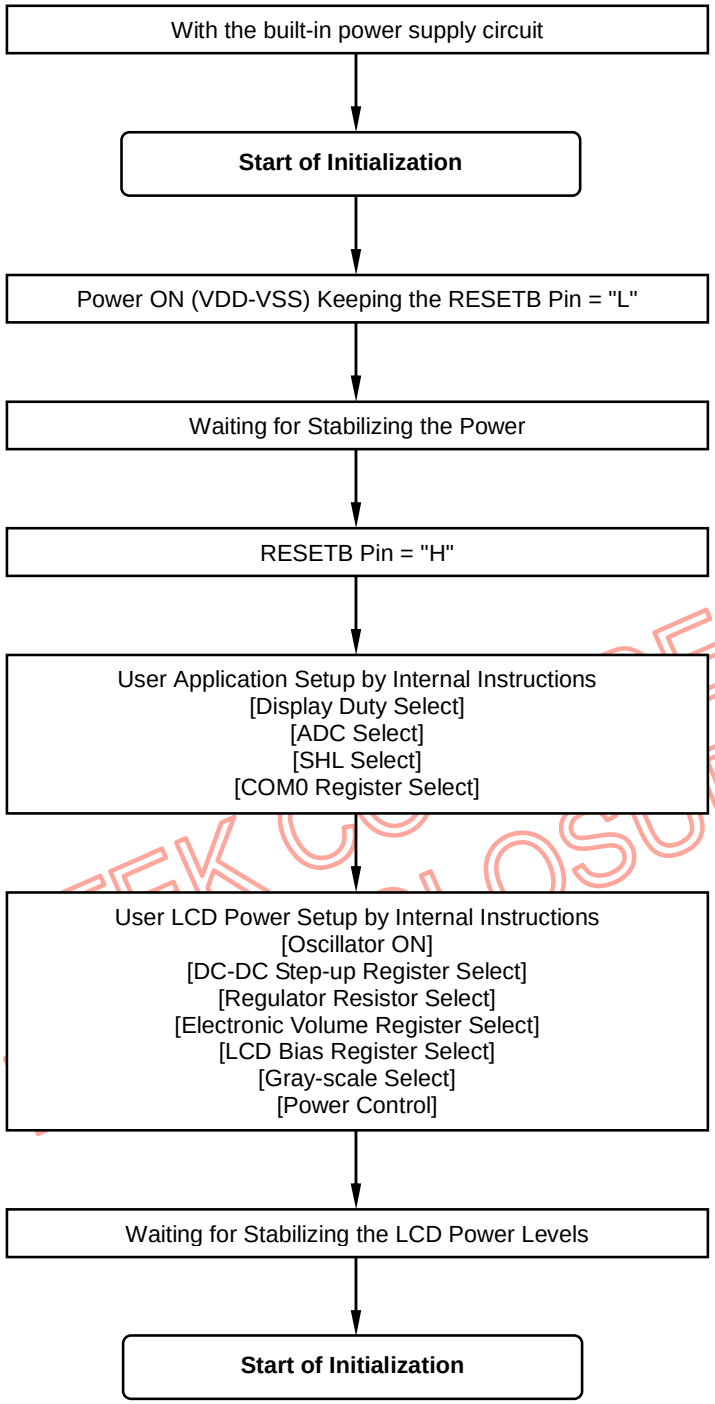


Figure 26. Initializing with the Built-in Power Supply Circuits

Referential Instruction Set-up Flow: Partial Duty Changing

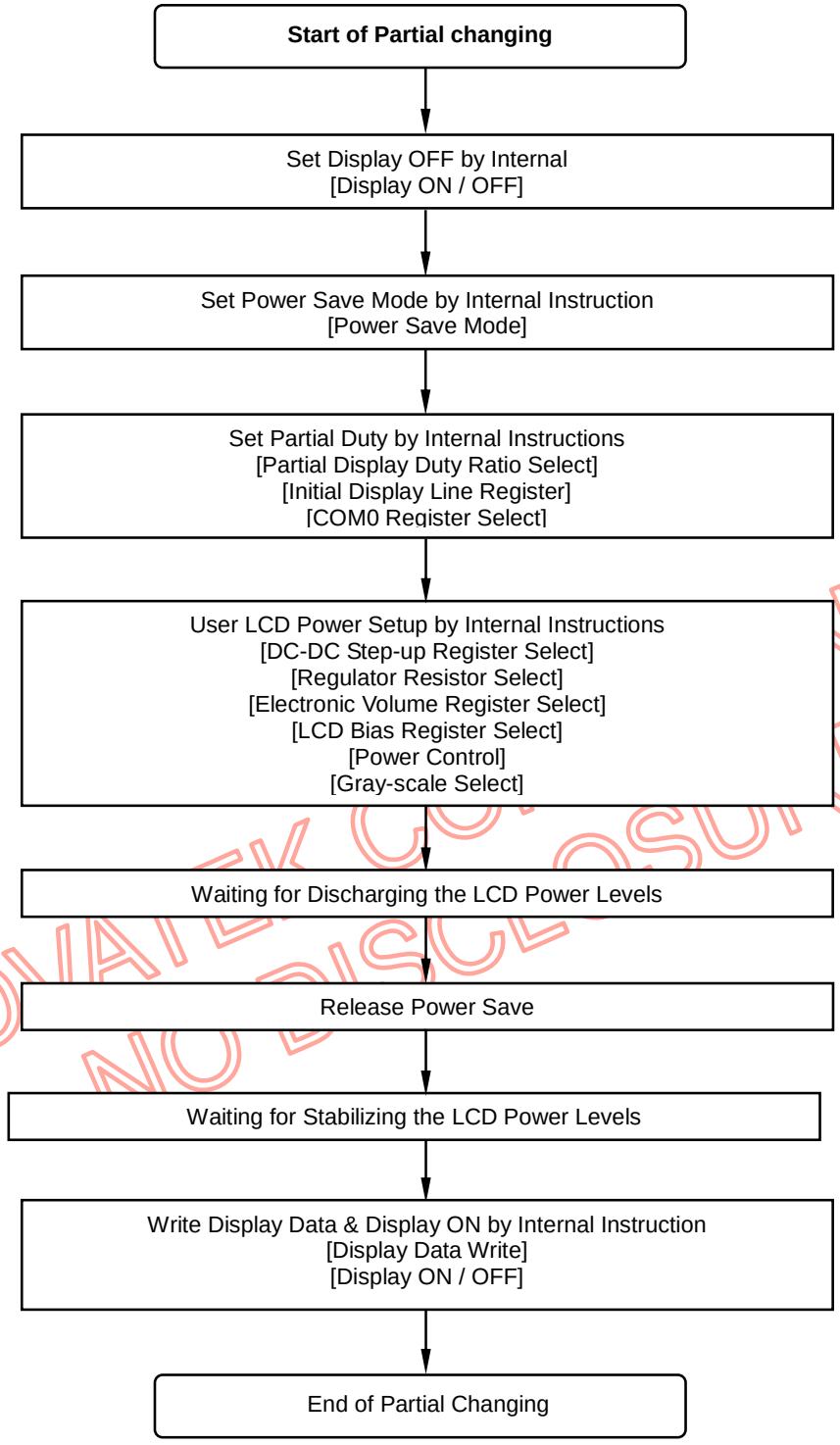
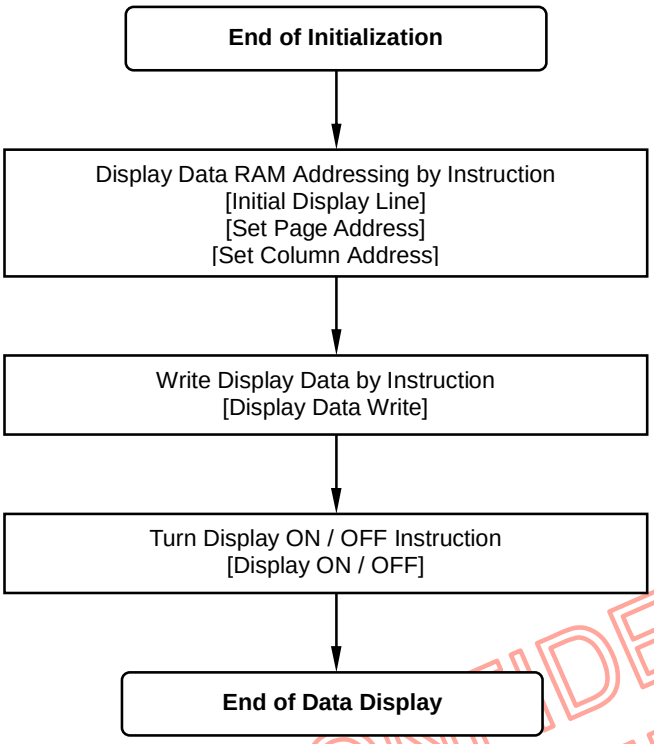
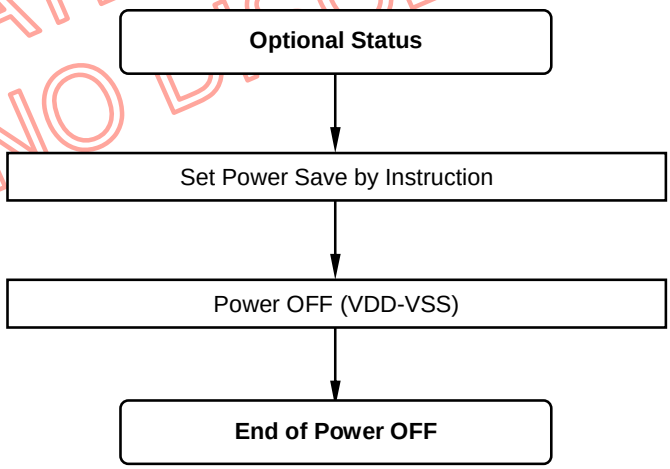


Figure 27. Partial Duty Changing

Referential Instruction Set-up Flow: Data Displaying



Referential Instruction Set-up Flow: Power OFF



Absolute Maximum Rating*

Supply Voltage Range (VDD)	-0.3V to +4.0V
Supply Voltage Range (V0)	-0.3V to +16.0V
Supply Voltage Range (V1, V2, V3, V4)	-0.3V to V0+0.3V
External Reference Voltage	+0.3V to VDD
Input Voltage Range	–0.3 to VDD+0.3V
Operating Temperature Range	-30°C to +85°C
Storage Temperature Range	-55°C to +125°C

Notes:
1. VCI, V0, V1 to V4 and VEXT based on VSS2=0V
2. Voltage V0≧V1≧V2≧V3≧V4≧VSS2 must always be satisfied. (VLCD=V0-VSS2)
3. If supply voltage exceeds its absolute maximum range, this LSI may be damaged permanently. It is desirable to use this LSI under electrical characteristic conditions during general operation. Otherwise, this LSI may malfunction or reduced LSI reliability may result.

DC Characteristics

Symbol	Parameters	Min.	Typ.	Max.	Unit	Conditions
VDD	Operating Voltage (*1)	1.65	-	3.6	V	
VDDA	Analog Operating Voltage	2.4	-	3.6	V	
VCI	Voltage Converter Input Voltage	2.4	-	3.6	V	
V_0	Operating Voltage	4.0	-	15.0	V	
V_{IH}	Input Voltage(*2)	0.8 VDD	-	VDD	V	
V_{IL}		VSS	-	0.2 VDD		
V_{OH}	Output Voltage(*3)	0.8 VDD	-	VDD	V	IOH = -0.5mA
V_{OL}		VSS	-	0.2 VDD		IOL = -0.5mA
I_{IL}	Input Leakage Current(*2)	-1.0	-	+1.0	μA	Vin=VDD or VSS
I_{OZ}	Output Leakage Current(*4)	-3.0	-	+3.0	μA	Vin=VDD or VSS
R_{ON}	LCD Drive ON Resistance(*5)	-	2.0	3.0	KΩ	Ta=25℃,V0=8V
f_{FR}	Operating Frequency(*6)	109	112	115	Hz	Ta=25°C 1/128Duty,9PWM
V_0	Voltage Follower Operating Voltage(*7)	4.0	-	15.0	V	
△V_0	VLCD Voltage Accuracy	-0.1	-	+0.1	V	Ta = 25°C

Table 9. DC Characteristics

Dynamic Current Consumption When The Internal Power Supply is ON

Symbol	Parameters	Min.	Typ.	Max.	Unit	Conditions
IDD	Current Consumption (*8)	-	250	300	μA	VDD=3.0V, V0-VSS=12.0V, x5 Boosting, Duty=1/128, Normal Mode (Display off)
		-	300	400	μA	VDD=3.0V, V0-VSS=12.0V, x5 Boosting, Duty=1/128, Normal Mode (Display on, Checker Pattern)

Table 10. Dynamic Current 2 (Internal Power)

Current Consumption during Power Save Mode

Symbol	Parameters	Min.	Typ.	Max.	Unit	Conditions
IDDS1	Power save mode current	-	-	2	μA	During power save mode

Table 11. Power Save Mode Current

Relationship between Oscillation Frequency and Frame Frequency

Duty Ratio	Item	fCL	fOSC1
I / N	On-Chip Oscillator circuit is used	$f_{FR} \times N$	$f_{FR} \times PWM \times N$

(fOSC1: Oscillation frequency, fCL: display clock frequency, fFR: frame frequency, N = 16 to 129)

12. The Relationship between Oscillation Frequency and Frame Frequency

[Remark Solves]
1. Though the wide range of operating voltages is guaranteed, a spike voltage change may affect the voltage assurance during access from the MPU.
2. CSB, RS, DB0 to DB7, E_RD, RW_WR, RESETB, PS0, PS1
3. DB0 to DB7
4. Applies when the DB0 to DB7 pins are in high impedance.
5. Resistance value when -0.1[mA] is applied during the ON status of the output pin SEGn or COMn.
   RON [kΩ] = ΔV[V] / 0.1[mA] (ΔV : voltage change when -0.1[mA] is applied in the ON status.)
6. See Table 12 for the relationship between Oscillation frequency and frame frequency.
7. The voltage regulator circuit adjusts V0 within the voltage follower operating voltage range.
8. Applies to the case where the on-chip Oscillation circuit is used and no access is made from the MPU.
   The current consumption, when the built-in power supply circuit is ON.
   The current flowing through voltage regulation resistors (Rb and Ra) is not included.
   It does not include the current of the LCD panel capacity, wiring capacity, etc.
   Other conditions are 1/12 bias, 3 FRC, 9 PWM, Frame inversion, Frame freq. = 112HZ, BL=(9,9,9,0), DG=(6,6,6,0), LG=(3,3,3,0), WH=(0,0,0,0).

AC Characteristics

Read / Write Characteristics (8080-series MPU)

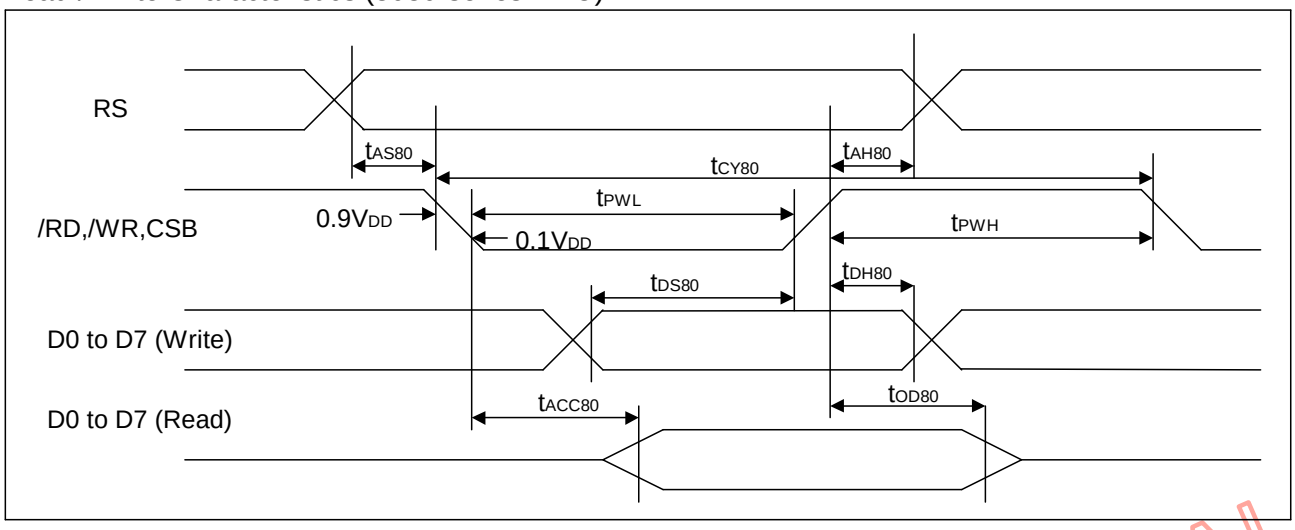


Figure 28. Read / Write Characteristics (8080-series MPU)

(VDD = 1.65V~2.7V, Ta= -30 ~ 70°C)

Symbol	Signal	Parameters	Min.	Typ.	Max.	Unit	Conditions
t_{AS80}	RS	Address setup time	0		-	ns	
t_{AH80}		Address hold time	0		-	ns	
t_{CY80}	/WR /RD	System cycle time for write	120		-	ns	
t_{CY80}		System cycle time for read	180		-	ns	
t_{PWL}		Pulse width low	70		-	ns	
t_{PWH}		Pulse width time	50		-	ns	
t_{DS80}	DB0 to DB7	Data setup time	30		-	ns	
t_{DH80}		Data hold time	0		-	ns	
t_{ACC80}		Read access time	-		90	ns	CL=100pF
t_{OD80}		Output disable time	10		50	ns	

(VDD = 2.7V~3.6V, Ta= -30 ~ 70°C)

Symbol	Signal	Parameters	Min.	Typ.	Max.	Unit	Conditions
t_{AS80}	RS	Address setup time	0		-	ns	
t_{AH80}		Address hold time	0		-	ns	
t_{CY80}		System cycle time for write	60		-	ns	
t_{CY80}		System cycle time for read	90		-	ns	
t_{PWL}	/WR	Pulse width low	30		-	ns	
t_{PWH}	/RD	Pulse width time	30		-	ns	
t_{DS80}	DB0 to DB7	Data setup time	20		-	ns	
t_{DH80}		Data hold time	0		-	ns	
t_{ACC80}		Read access time	-		50	ns	CL=100pF
t_{OD80}		Output disable time	10		50	ns	

Read / Write Characteristics (6800-series MPU)

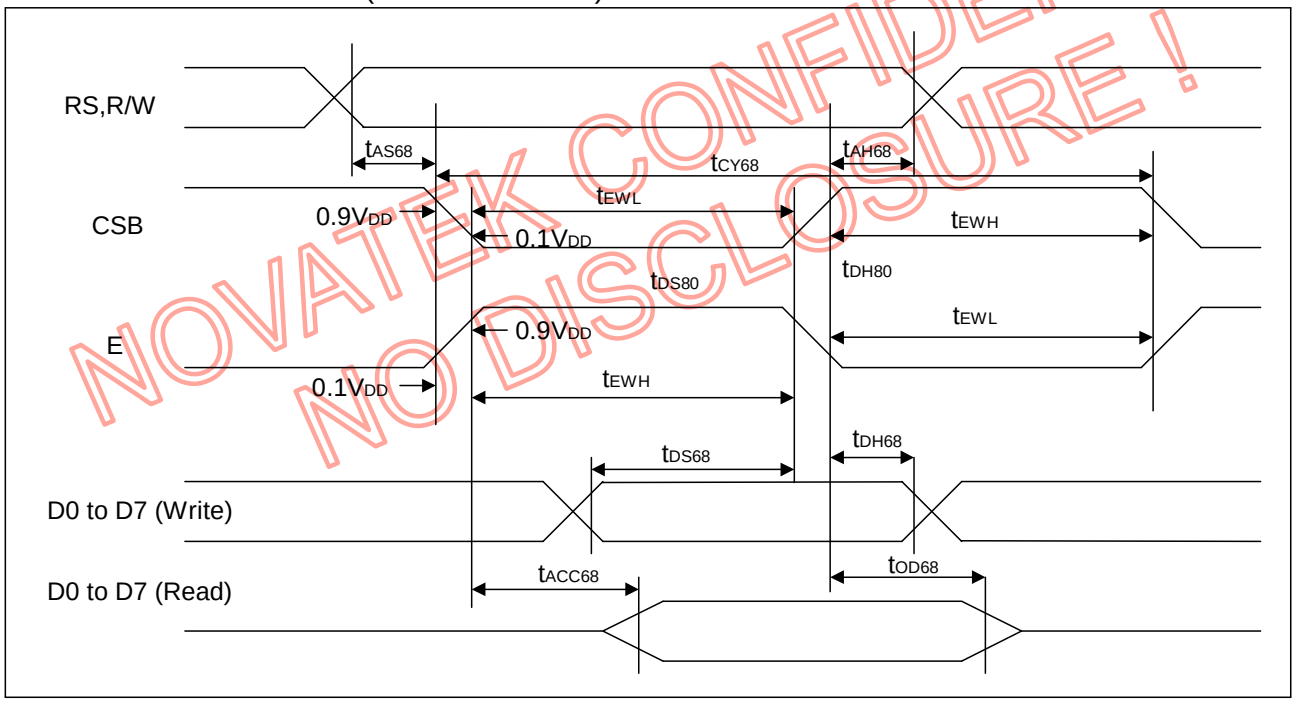


Figure 29. Read / Write Characteristics (6800-series Microprocessor)

(VDD = 1.65V~2.7V, Ta= -30 ~ 70℃)

Symbol	Signal	Parameters	Min.	Typ.	Max.	Unit	Conditions
t_{AS68}	RS	Address setup time	0		-	ns	
t_{AH68}	RW	Address hold time	0		-	ns	
t_{CY68}		System cycle time for write	120		-	ns	
t_{CY68}		System cycle time for read	180		-	ns	
t_{EWH}	E_RD	Pulse width low	70		-	ns	
t_{EWL}	(E)	Pulse width time	50		-	ns	
t_{DS68}		Data setup time	30		-	ns	
t_{DH68}	DB0 to DB7	Data hold time	0		-	ns	
t_{ACC68}		Read access time	-		90	ns	CL=100pF
t_{OD68}		Output disable time	10		50	ns	

(VDD = 2.7V~3.6V, Ta=-30 ~ 70℃)

Symbol	Signal	Parameters	Min.	Typ.	Max.	Unit	Conditions
t_{AS68}	RS	Address setup time	0		-	ns	
t_{AH68}	RW	Address hold time	0		-	ns	
t_{CY68}		System cycle time for write	60		-	ns	
t_{CY68}		System cycle time for read	90		-	ns	
t_{EWH}	E_RD	Pulse width low	30		-	ns	
t_{EWL}	(E)	Pulse width time	30		-	ns	
t_{DS68}		Data setup time	20		-	ns	
t_{DH68}	DB0 to DB7	Data hold time	0		-	ns	
t_{ACC68}		Read access time	-		50	ns	CL=100pF
t_{OD68}		Output disable time	10		50	ns	

Serial Interface Characteristics

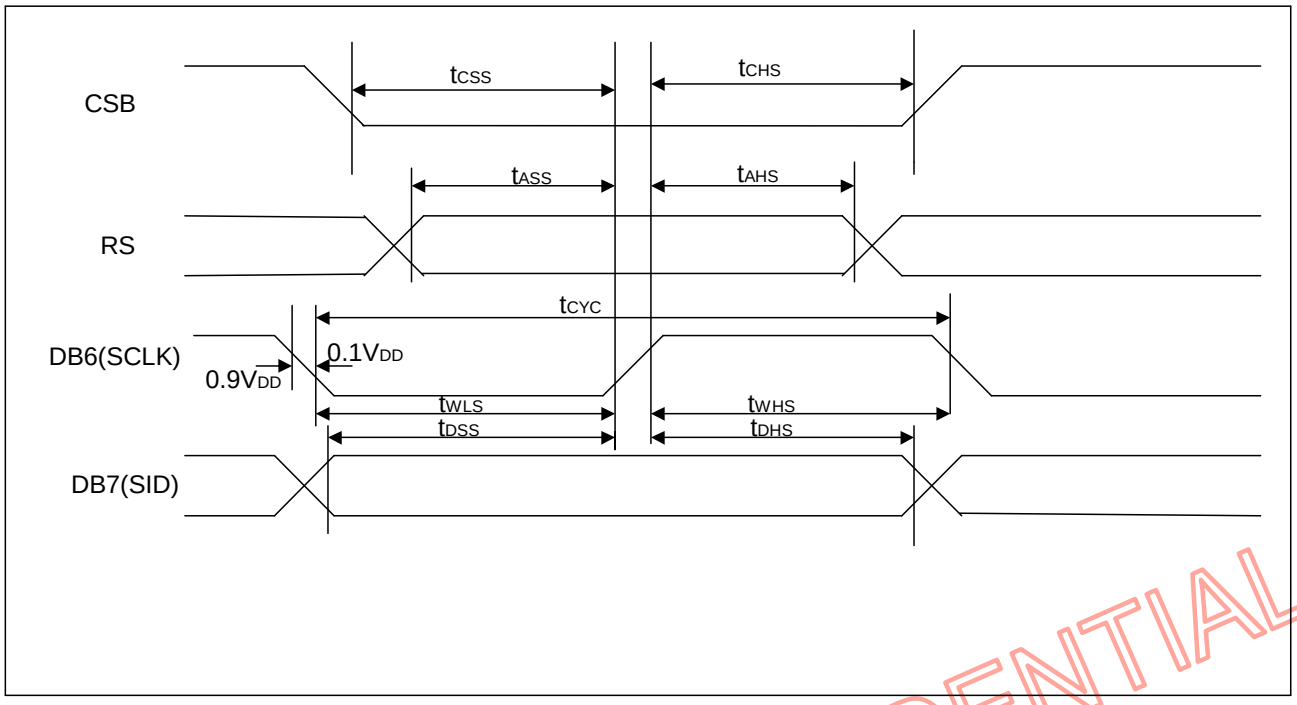


Figure 30. Serial Interface Characteristics

(VDD = 1.65V~2.7V, Ta= -30 ~ 70℃)

Symbol	Signal	Parameters	Min.	Typ.	Max.	Unit	Conditions
tCYS	DB6 (SCLK)	Serial clock cycle	120		-	ns	
tWHS		SCLK high pulse width	60		-	ns	
tWLS		SCLK low pulse width	60		-	ns	
tASS	RS	Address setup time	60		-	ns	
tAHS		Address hold time	80		-	ns	
tDSS	DB7 (SID)	Data setup time	60		-	ns	
tdhs		Data hold time	60		-	ns	
tCCS	CSB	CSB setup time	60		-	ns	
tCHS		CSB hold time	1/2 * tCYS		-	ns	

(VDD = 2.7V~3.6V, Ta= -30 ~ 70℃)

Symbol	Signal	Parameters	Min.	Typ.	Max.	Unit	Conditions
t_{CYS}	DB6 (SCLK)	Serial clock cycle	60		-	ns	
t_{WHS}		SCLK high pulse width	30		-	ns	
t_{WLS}		SCLK low pulse width	30		-	ns	
t_{ASS}	RS	Address setup time	30		-	ns	
t_{AHS}		Address hold time	30		-	ns	
t_{DSS}	DB7 (SID)	Data setup time	30		-	ns	
tdhs		Data hold time	30		-	ns	
t_{CCS}	CSB	CSB setup time	30		-	ns	
t_{CHS}		CSB hold time	1/2 * t_{CYS}		-	ns	

Reset Input Timing

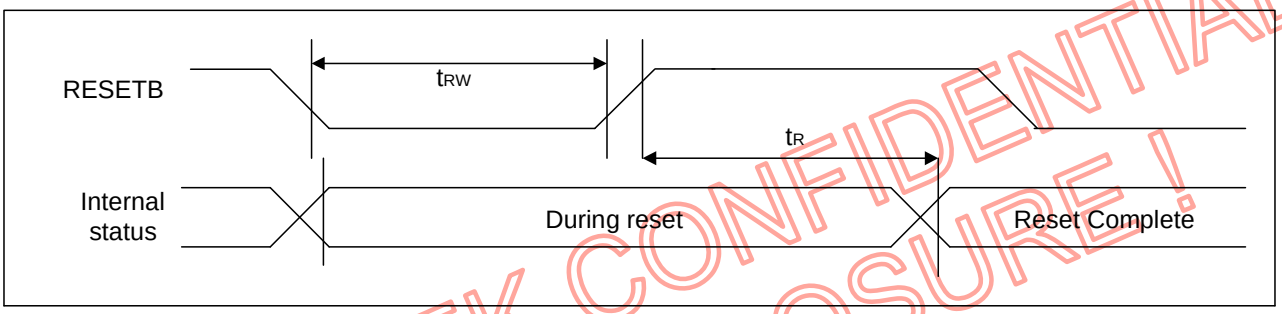


Figure 31. Reset Input Timing

(VDD=1.65 ~ 2.7V, Ta= -30~+70℃)

Symbol	Signal	Parameters	Min.	Typ.	Max.	Unit	Conditions
t_{RW}	RESETB	Reset low pulse width	20		-	μs	
t_R	-	Reset time	-		1	μs	

(VDD=2.7 ~ 3.6V, Ta=-30~+70℃)

Symbol	Signal	Parameters	Min.	Typ.	Max.	Unit	Conditions
t_{RW}	RESETB	Reset low pulse width	10		-	μs	
t_R	-	Reset time	-		1	μs	

Microprocessor Interface (for reference only)

In Case of Interfacing with 8080-series (PS0 = “H”, PS1 = “L”)

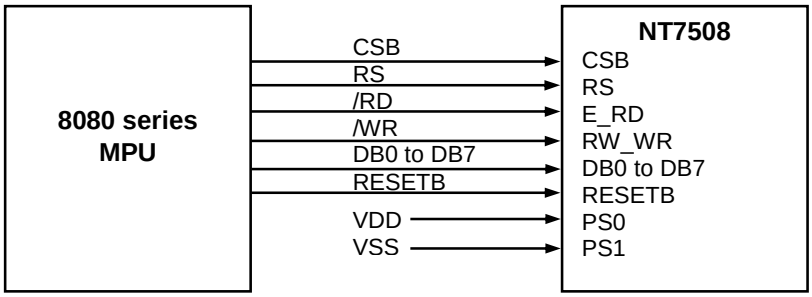


Figure 32. Interfacing with 8080-series (PS0 = “H”, PS1 = “L”)

In Case of Interfacing with 6800-series (PS0 = “H”, PS1 = “H”)

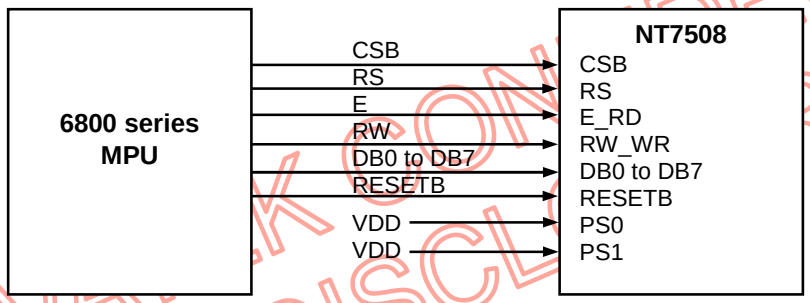


Figure 33. Interfacing with 6800-series (PS0 = “H”, PS1 = “H”)

In Case of 4-pin SPI mode (PS0 = "L" , PS1 = "H")

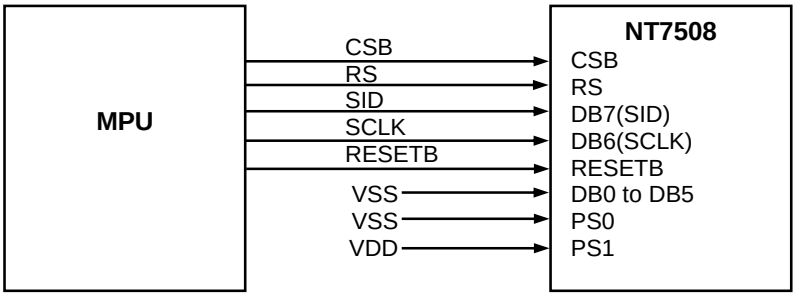


Figure 34. Serial Interface (PS0 = “L”, PS1 = “H”)

In Case of 3-pin SPI mode (PS0 = "L" , PS1 = "L")

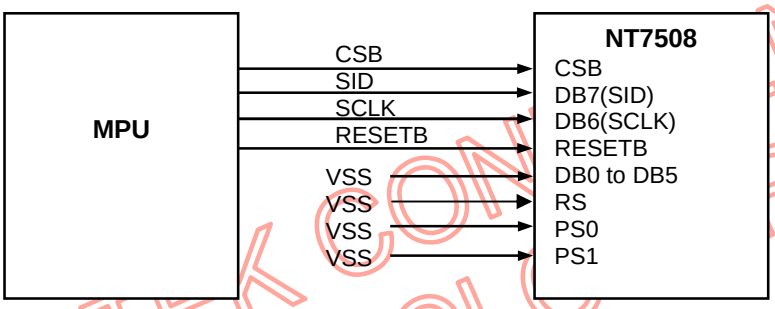


Figure 35. Serial Interface (PS0 = “L”, PS1 = “L”)

Connections Between NT7508 And LCD Panel
Single Chip Configuration (1/129 Duty Configurations)

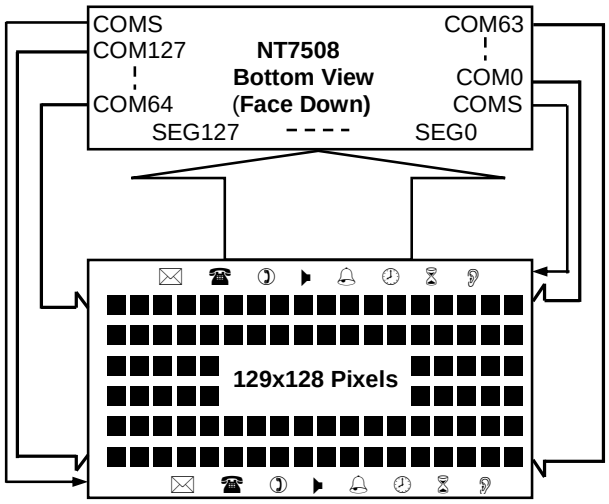


Figure 36. SHL = 0, ADC = 1

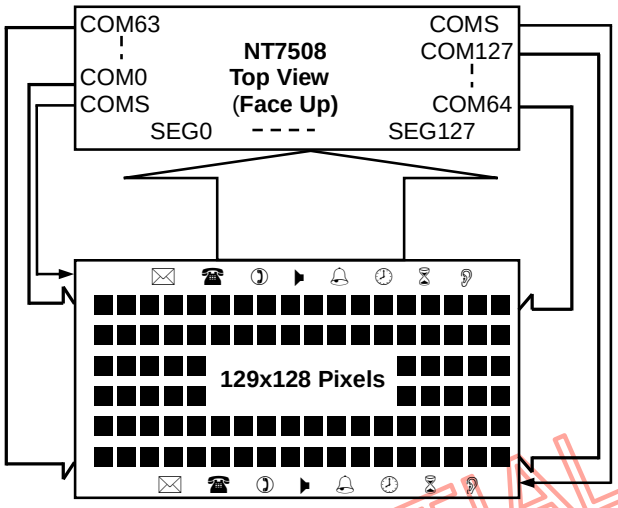


Figure 37. SHL = 0, ADC = 0

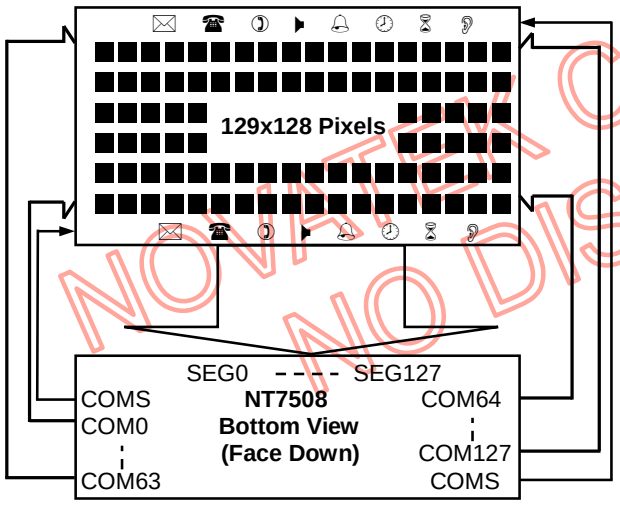


Figure 38. SHL = 1, ADC = 0

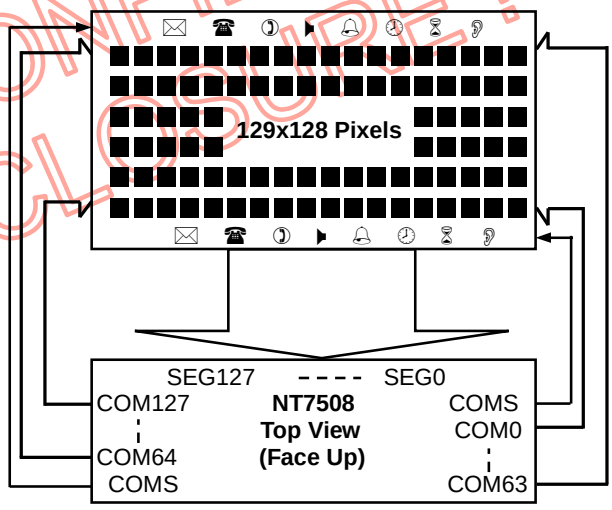
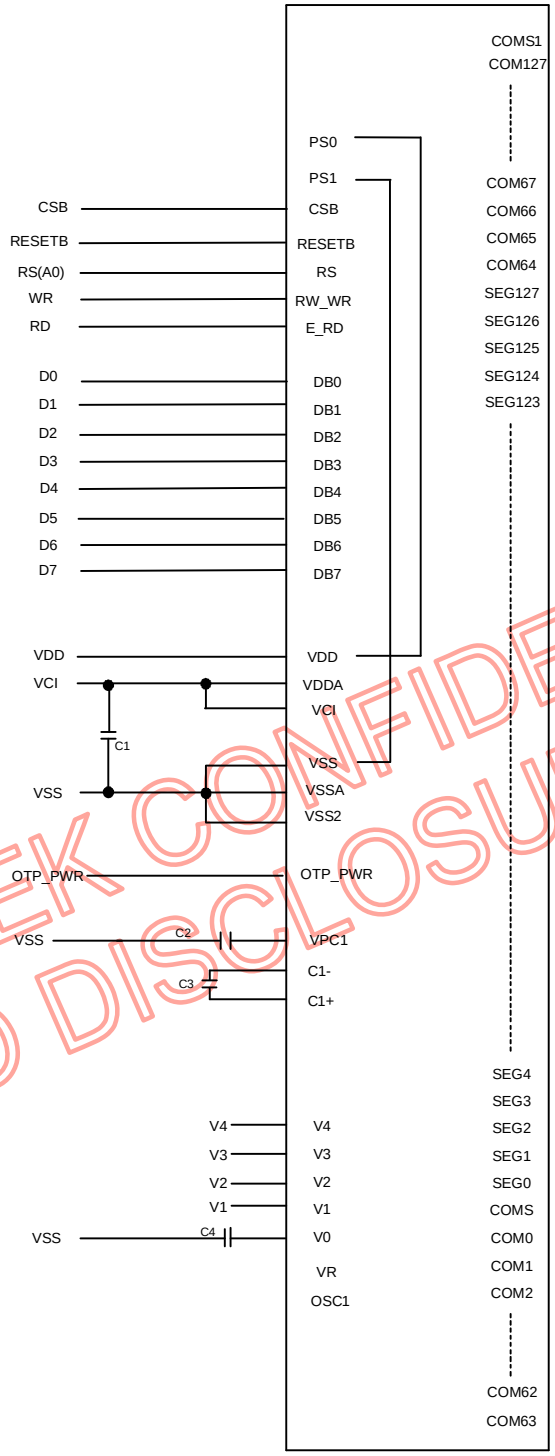


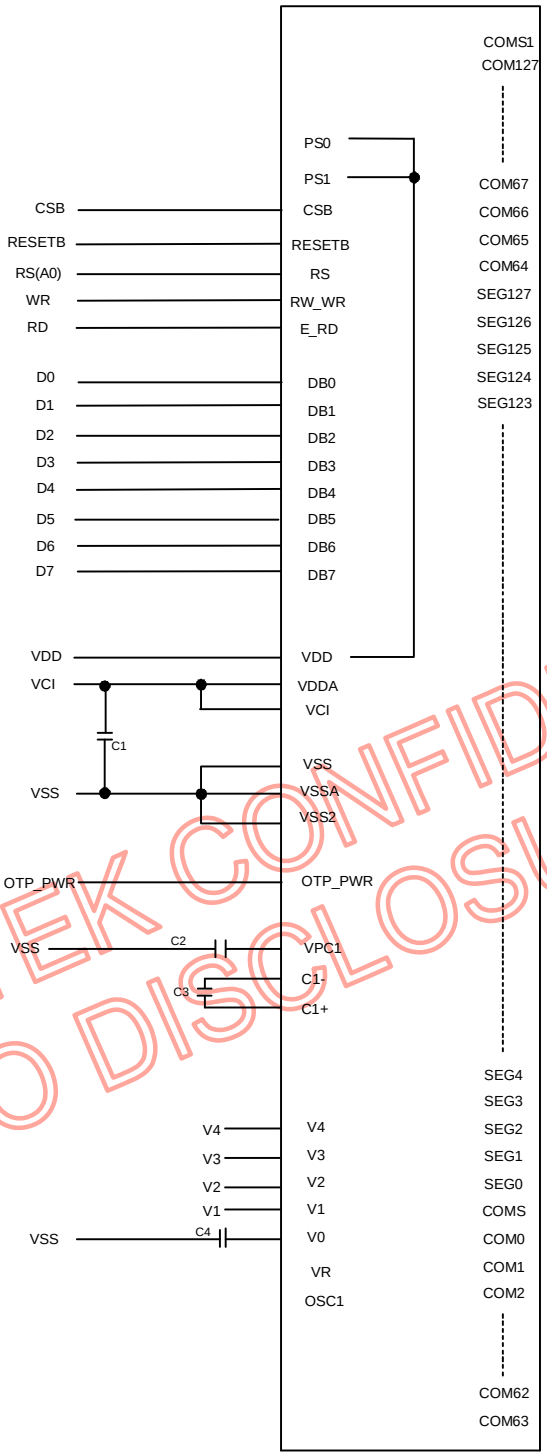
Figure 39. SHL = 1, ADC = 1

Application information for Pin Connection to MPU (for reference only)

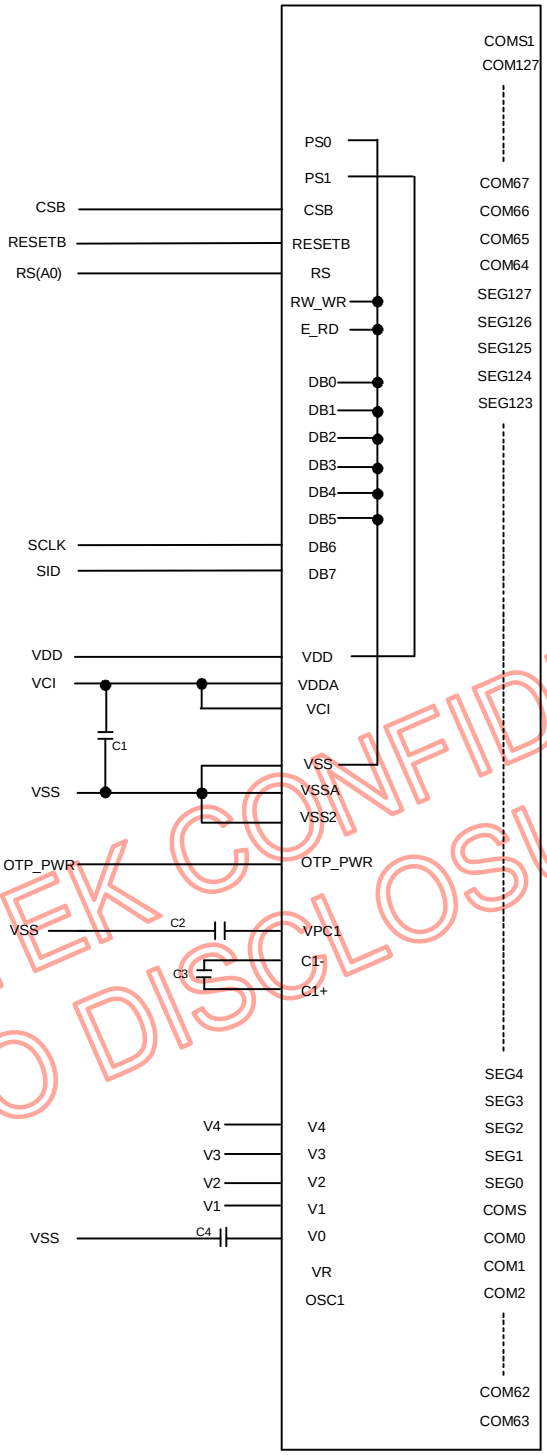
1. 8080 MPU Mode: (PS0=1, PS1=0,, 1/128duty, Internal OSC, C1~C4 = 1.0 ~ 2.2 μF)



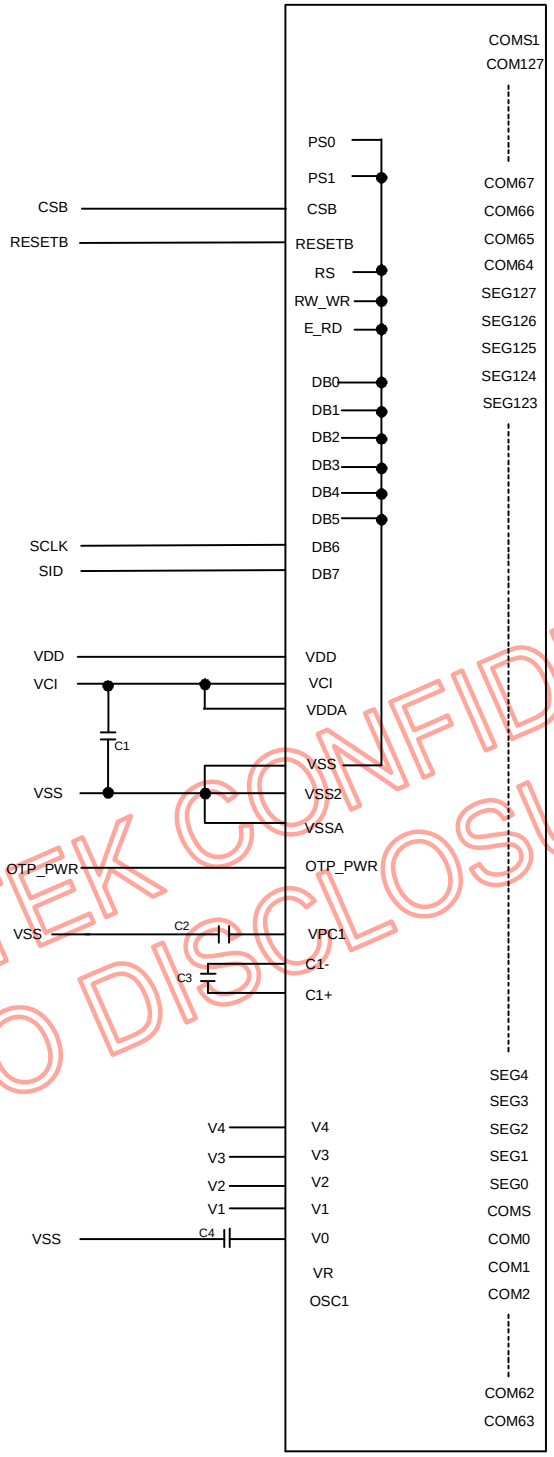
2. 6800 MPU Mode: (PS0=1, PS1=1, 1/128duty, Internal OSC, C1~C4 = 1.0 ~ 2.2 μF)



3. 4 pin Serial Mode: (PS0=0, PS1=1, 1/128duty, Internal OSC, C1~C4 = 1.0 ~ 2.2 μF)



4. 3 pin Serial Mode: (PS0=0, PS1=0, 1/128duty, Internal OSC, C1~C4 = 1.0 ~ 2.2 μF)



Application Notice

1. Power: VDD, VDDA, VCI ≤ 3.6V; V0 ≤ 15.0V.
2. Keep the relationship of power supply: VDDA, VCI ≥ VDD.
3. Keep the relationship of LCD driving voltage: V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS2.
4. Use VDD (pad 5, 13) for power supply input, and don't use VDDA VCI output for pad option to power supply input pad.
5. Use VSS (pad 2, 8, 18) for ground input, and don't use VSSA VSS2 output for pad option to ground input pad.
6. Open pads TEST0~TEST3 with no connection.
7. The reset pin of NT7508 is floating inside the IC. Please make sure the reset pin of the customer's system is in a fixed status ("H" or "L") while operating this pin.
8. If using serial mode, please make sure /RD, /WR, D0 ~ D5 pads must be fixed "H" or "L". If using 3SPI mode, please to make sure A0 pad must be fixed "H" or "L".
9. Note that all capacitors must have proper capacitance and voltage rating.

Item	Capacitance	Max. Rating	Remark
VDD, VDDA, VCI	1.0μF ~ 4.7μF	6V	-
C1+ to C1-	1.0μF ~ 2.2μF	6V	-
VPCI to VSS	1.0μF ~ 2.2μF	10V	
V0 to VSS	1.0μF ~ 2.2μF	16V	V0 ≤ 12.0V.
		25V	V0 >12.0V

10. Recommendation of choosing times of pump: According to the characteristics of LCM and black or gray display application, 3~8 times can be chosen of PUMP times. We suggestion that user can adjust pump times by self to get better display quality and current consumption.

    There is a recommendation table as below:

V0	Pump times	VCI	Remark
V0 ≤ 13.0V.	3x ~ 6x	2.4V~3.6V	Black & White
	7x ~ 8x	2.4V~3.6V	4 Gray
V0 >13.0V	6x	2.4V~3.6V	Black & White
	7x ~ 8x	2.8V~3.6V	4 Gray

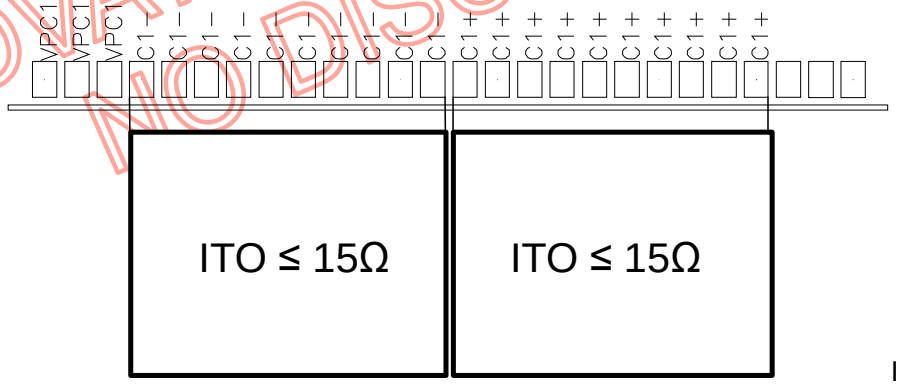
ITO Layout Notice

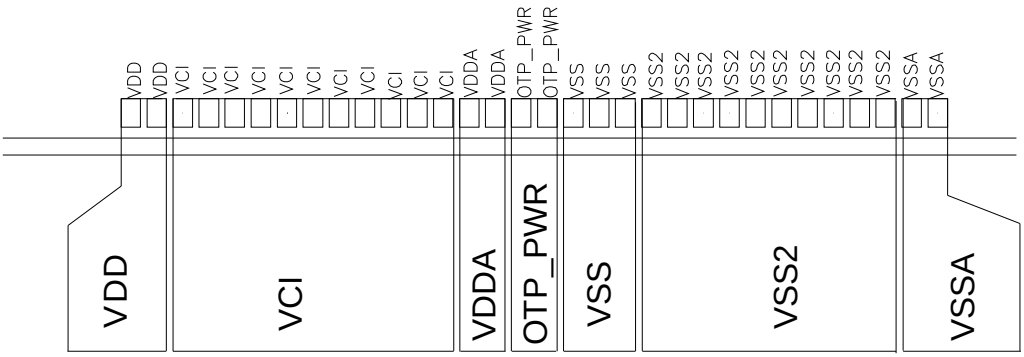
1. Specifically with COG application, it is important to reduce the resistance of the ITO path. To make the overall display performance of the LCM better, there are some suggestions for ITO layout described as below :
   a) Please keep the resistance of VDD & VSS path between PCB and corresponding pads of IC ≤ 50Ω. This value includes the ITO resistors' values, the FPC/Heat seal resistor; the ACF contact resistors between IC and Glass, Glass and FPC/Heat seal, FPC/Heat seal and PCB.
   b) The resistance of V0 ≤ 100Ω
   c) The value of the other pins of the interface ≤300Ω

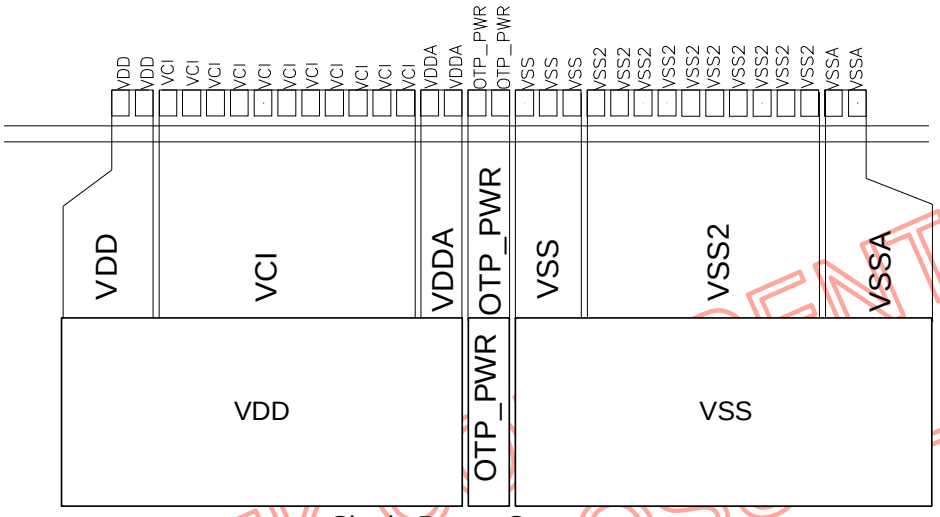
ITO Path	Max. Resistance
C1+, C1-, VCI, VSS2	15Ω
VDD, VDDA, VSS, VSSA, VPC1	50Ω
V0, OTP_PWR	100Ω
RESETB	300Ω
CSB, RS, RW_WR, E_RD, DB0 ~ DB7	300Ω

2. To meet the value demanded above while laying out ITO, users may accept the rules below:
   a) In order to keep the ITO resistance to a minimum, the vary pitch and position of the module connection to the outside should be selected to make the power lines go as straight as possible.
   b) The distance between NT7508 and FPC is the shorter the better. Then the length of ITO will be the shortest and you can get a smaller resistor value.
   c) The ITO interface may fill the blank area on the LCD Panel to reduce the ITO resistance.

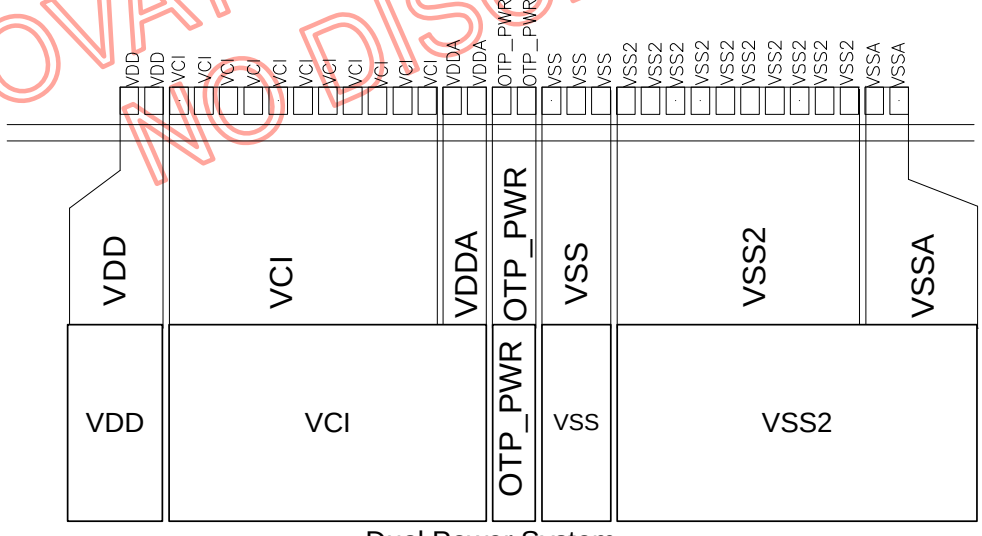
3. In order to improve display quality, the ITO trace for VDD、VDDA、VCI、VSS、VSSA and VSS2 should be separated and it can be connected in FPC. (Below figure for reference only)
4. Dummy pad: Must be no connection.
5. The resistance of C1+, C1-, VCI, VSS2 ≤ 15Ω to get a better pump efficiency.





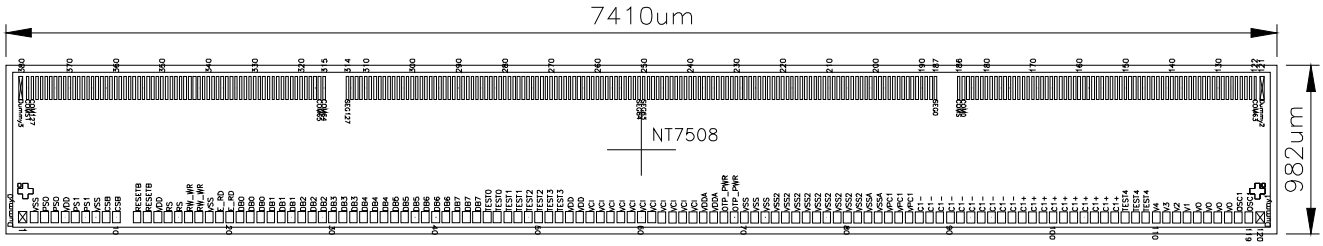


Single Power System



Dual Power System

Bonding Diagram



[Unit: um]

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	Dummy0	-3607.5	-394.0	31	DB3	-1740.0	-394.0
2	VSS	-3540.0	-394.0	32	DB3	-1680.0	-394.0
3	PS0	-3480.0	-394.0	33	DB4	-1620.0	-394.0
4	PS0	-3420.0	-394.0	34	DB4	-1560.0	-394.0
5	VDD	-3360.0	-394.0	35	DB4	-1500.0	-394.0
6	PS1	-3300.0	-394.0	36	DB5	-1440.0	-394.0
7	PS1	-3240.0	-394.0	37	DB5	-1380.0	-394.0
8	VSS	-3180.0	-394.0	38	DB5	-1320.0	-394.0
9	CSB	-3120.0	-394.0	39	DB6	-1260.0	-394.0
10	CSB	-3060.0	-394.0	40	DB6	-1200.0	-394.0
11	RESETB	-2940.0	-394.0	41	DB6	-1140.0	-394.0
12	RESETB	-2880.0	-394.0	42	DB7	-1080.0	-394.0
13	VDD	-2820.0	-394.0	43	DB7	-1020.0	-394.0
14	RS	-2760.0	-394.0	44	DB7	-960.0	-394.0
15	RS	-2700.0	-394.0	45	TEST0	-900.0	-394.0
16	RW_WR	-2640.0	-394.0	46	TEST0	-840.0	-394.0
17	RW_WR	-2580.0	-394.0	47	TEST1	-780.0	-394.0
18	VSS	-2520.0	-394.0	48	TEST1	-720.0	-394.0
19	E_RD	-2460.0	-394.0	49	TEST2	-660.0	-394.0
20	E_RD	-2400.0	-394.0	50	TEST2	-600.0	-394.0
21	DB0	-2340.0	-394.0	51	TEST3	-540.0	-394.0
22	DB0	-2280.0	-394.0	52	TEST3	-480.0	-394.0
23	DB0	-2220.0	-394.0	53	VDD	-420.0	-394.0
24	DB1	-2160.0	-394.0	54	VDD	-360.0	-394.0
25	DB1	-2100.0	-394.0	55	VCI	-300.0	-394.0
26	DB1	-2040.0	-394.0	56	VCI	-240.0	-394.0
27	DB2	-1980.0	-394.0	57	VCI	-180.0	-394.0
28	DB2	-1920.0	-394.0	58	VCI	-120.0	-394.0
29	DB2	-1860.0	-394.0	59	VCI	-60.0	-394.0
30	DB3	-1800.0	-394.0	60	VCI	0.0	-394.0

Bonding Diagram (continued)

[Unit: um]

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
61	VCI	60.0	-394.0	98	C1+	2280.0	-394.0
62	VCI	120.0	-394.0	99	C1+	2340.0	-394.0
63	VCI	180.0	-394.0	100	C1+	2400.0	-394.0
64	VCI	240.0	-394.0	101	C1+	2460.0	-394.0
65	VCI	300.0	-394.0	102	C1+	2520.0	-394.0
66	VDDA	360.0	-394.0	103	C1+	2580.0	-394.0
67	VDDA	420.0	-394.0	104	C1+	2640.0	-394.0
68	OTP_PWR	480.0	-394.0	105	C1+	2700.0	-394.0
69	OTP_PWR	540.0	-394.0	106	C1+	2760.0	-394.0
70	VSS	600.0	-394.0	107	TEST4	2820.0	-394.0
71	VSS	660.0	-394.0	108	TEST4	2880.0	-394.0
72	VSS	720.0	-394.0	109	TEST4	2940.0	-394.0
73	VSS2	780.0	-394.0	110	V4	3000.0	-394.0
74	VSS2	840.0	-394.0	111	V3	3060.0	-394.0
75	VSS2	900.0	-394.0	112	V2	3120.0	-394.0
76	VSS2	960.0	-394.0	113	V1	3180.0	-394.0
77	VSS2	1020.0	-394.0	114	V0	3240.0	-394.0
78	VSS2	1080.0	-394.0	115	V0	3300.0	-394.0
79	VSS2	1140.0	-394.0	116	V0	3360.0	-394.0
80	VSS2	1200.0	-394.0	117	V0	3420.0	-394.0
81	VSS2	1260.0	-394.0	118	OSC1	3480.0	-394.0
82	VSSA	1320.0	-394.0	119	OSC1	3540.0	-394.0
83	VSSA	1380.0	-394.0	120	Dummy3	3607.5	-394.0
84	VPC1	1440.0	-394.0	121	Dummy2	3617.5	360.0
85	VPC1	1500.0	-394.0	122	COM[63]	3577.5	360.0
86	VPC1	1560.0	-394.0	123	COM[62]	3550.5	360.0
87	C1-	1620.0	-394.0	124	COM[61]	3523.5	360.0
88	C1-	1680.0	-394.0	125	COM[60]	3496.5	360.0
89	C1-	1740.0	-394.0	126	COM[59]	3469.5	360.0
90	C1-	1800.0	-394.0	127	COM[58]	3442.5	360.0
91	C1-	1860.0	-394.0	128	COM[57]	3415.5	360.0
92	C1-	1920.0	-394.0	129	COM[56]	3388.5	360.0
93	C1-	1980.0	-394.0	130	COM[55]	3361.5	360.0
94	C1-	2040.0	-394.0	131	COM[54]	3334.5	360.0
95	C1-	2100.0	-394.0	132	COM[53]	3307.5	360.0
96	C1-	2160.0	-394.0	133	COM[52]	3280.5	360.0
97	C1+	2220.0	-394.0	134	COM[51]	3253.5	360.0

Bonding Diagram (continued)

[Unit: um]

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
135	COM[50]	3226.5	360.0	172	COM[13]	2227.5	360.0
136	COM[49]	3199.5	360.0	173	COM[12]	2200.5	360.0
137	COM[48]	3172.5	360.0	174	COM[11]	2173.5	360.0
138	COM[47]	3145.5	360.0	175	COM[10]	2146.5	360.0
139	COM[46]	3118.5	360.0	176	COM[9]	2119.5	360.0
140	COM[45]	3091.5	360.0	177	COM[8]	2092.5	360.0
141	COM[44]	3064.5	360.0	178	COM[7]	2065.5	360.0
142	COM[43]	3037.5	360.0	179	COM[6]	2038.5	360.0
143	COM[42]	3010.5	360.0	180	COM[5]	2011.5	360.0
144	COM[41]	2983.5	360.0	181	COM[4]	1984.5	360.0
145	COM[40]	2956.5	360.0	182	COM[3]	1957.5	360.0
146	COM[39]	2929.5	360.0	183	COM[2]	1930.5	360.0
147	COM[38]	2902.5	360.0	184	COM[1]	1903.5	360.0
148	COM[37]	2875.5	360.0	185	COM[0]	1876.5	360.0
149	COM[36]	2848.5	360.0	186	COMS	1849.5	360.0
150	COM[35]	2821.5	360.0	187	SEG[0]	1714.5	360.0
151	COM[34]	2794.5	360.0	188	SEG[1]	1687.5	360.0
152	COM[33]	2767.5	360.0	189	SEG[2]	1660.5	360.0
153	COM[32]	2740.5	360.0	190	SEG[3]	1633.5	360.0
154	COM[31]	2713.5	360.0	191	SEG[4]	1606.5	360.0
155	COM[30]	2686.5	360.0	192	SEG[5]	1579.5	360.0
156	COM[29]	2659.5	360.0	193	SEG[6]	1552.5	360.0
157	COM[28]	2632.5	360.0	194	SEG[7]	1525.5	360.0
158	COM[27]	2605.5	360.0	195	SEG[8]	1498.5	360.0
159	COM[26]	2578.5	360.0	196	SEG[9]	1471.5	360.0
160	COM[25]	2551.5	360.0	197	SEG[10]	1444.5	360.0
161	COM[24]	2524.5	360.0	198	SEG[11]	1417.5	360.0
162	COM[23]	2497.5	360.0	199	SEG[12]	1390.5	360.0
163	COM[22]	2470.5	360.0	200	SEG[13]	1363.5	360.0
164	COM[21]	2443.5	360.0	201	SEG[14]	1336.5	360.0
165	COM[20]	2416.5	360.0	202	SEG[15]	1309.5	360.0
166	COM[19]	2389.5	360.0	203	SEG[16]	1282.5	360.0
167	COM[18]	2362.5	360.0	204	SEG[17]	1255.5	360.0
168	COM[17]	2335.5	360.0	205	SEG[18]	1228.5	360.0
169	COM[16]	2308.5	360.0	206	SEG[19]	1201.5	360.0
170	COM[15]	2281.5	360.0	207	SEG[20]	1174.5	360.0
171	COM[14]	2254.5	360.0	208	SEG[21]	1147.5	360.0

Bonding Diagram (continued)

[Unit: um]

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
209	SEG[22]	1120.5	360.0	246	SEG[59]	121.5	360.0
210	SEG[23]	1093.5	360.0	247	SEG[60]	94.5	360.0
211	SEG[24]	1066.5	360.0	248	SEG[61]	67.5	360.0
212	SEG[25]	1039.5	360.0	249	SEG[62]	40.5	360.0
213	SEG[26]	1012.5	360.0	250	SEG[63]	13.5	360.0
214	SEG[27]	985.5	360.0	251	SEG[64]	-13.5	360.0
215	SEG[28]	958.5	360.0	252	SEG[65]	-40.5	360.0
216	SEG[29]	931.5	360.0	253	SEG[66]	-67.5	360.0
217	SEG[30]	904.5	360.0	254	SEG[67]	-94.5	360.0
218	SEG[31]	877.5	360.0	255	SEG[68]	-121.5	360.0
219	SEG[32]	850.5	360.0	256	SEG[69]	-148.5	360.0
220	SEG[33]	823.5	360.0	257	SEG[70]	-175.5	360.0
221	SEG[34]	796.5	360.0	258	SEG[71]	-202.5	360.0
222	SEG[35]	769.5	360.0	259	SEG[72]	-229.5	360.0
223	SEG[36]	742.5	360.0	260	SEG[73]	-256.5	360.0
224	SEG[37]	715.5	360.0	261	SEG[74]	-283.5	360.0
225	SEG[38]	688.5	360.0	262	SEG[75]	-310.5	360.0
226	SEG[39]	661.5	360.0	263	SEG[76]	-337.5	360.0
227	SEG[40]	634.5	360.0	264	SEG[77]	-364.5	360.0
228	SEG[41]	607.5	360.0	265	SEG[78]	-391.5	360.0
229	SEG[42]	580.5	360.0	266	SEG[79]	-418.5	360.0
230	SEG[43]	553.5	360.0	267	SEG[80]	-445.5	360.0
231	SEG[44]	526.5	360.0	268	SEG[81]	-472.5	360.0
232	SEG[45]	499.5	360.0	269	SEG[82]	-499.5	360.0
233	SEG[46]	472.5	360.0	270	SEG[83]	-526.5	360.0
234	SEG[47]	445.5	360.0	271	SEG[84]	-553.5	360.0
235	SEG[48]	418.5	360.0	272	SEG[85]	-580.5	360.0
236	SEG[49]	391.5	360.0	273	SEG[86]	-607.5	360.0
237	SEG[50]	364.5	360.0	274	SEG[87]	-634.5	360.0
238	SEG[51]	337.5	360.0	275	SEG[88]	-661.5	360.0
239	SEG[52]	310.5	360.0	276	SEG[89]	-688.5	360.0
240	SEG[53]	283.5	360.0	277	SEG[90]	-715.5	360.0
241	SEG[54]	256.5	360.0	278	SEG[91]	-742.5	360.0
242	SEG[55]	229.5	360.0	279	SEG[92]	-769.5	360.0
243	SEG[56]	202.5	360.0	280	SEG[93]	-796.5	360.0
244	SEG[57]	175.5	360.0	281	SEG[94]	-823.5	360.0
245	SEG[58]	148.5	360.0	282	SEG[95]	-850.5	360.0

Bonding Diagram (continued)

[Unit: um]

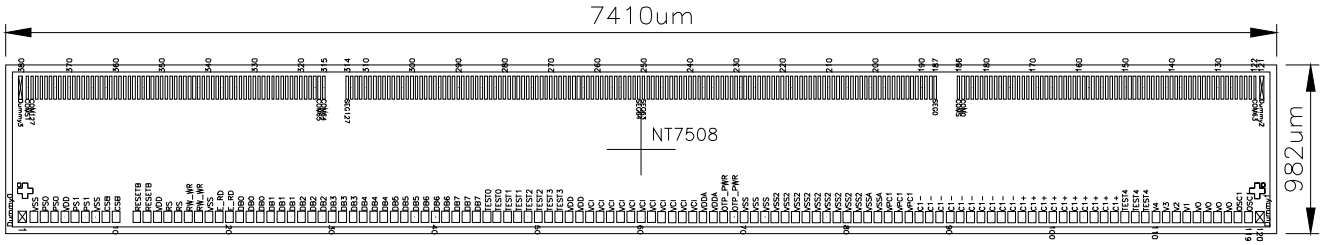
Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
283	SEG[96]	-877.5	360.0	320	COM[69]	-1984.5	360.0
284	SEG[97]	-904.5	360.0	321	COM[70]	-2011.5	360.0
285	SEG[98]	-931.5	360.0	322	COM[71]	-2038.5	360.0
286	SEG[99]	-958.5	360.0	323	COM[72]	-2065.5	360.0
287	SEG[100]	-985.5	360.0	324	COM[73]	-2092.5	360.0
288	SEG[101]	-1012.5	360.0	325	COM[74]	-2119.5	360.0
289	SEG[102]	-1039.5	360.0	326	COM[75]	-2146.5	360.0
290	SEG[103]	-1066.5	360.0	327	COM[76]	-2173.5	360.0
291	SEG[104]	-1093.5	360.0	328	COM[77]	-2200.5	360.0
292	SEG[105]	-1120.5	360.0	329	COM[78]	-2227.5	360.0
293	SEG[106]	-1147.5	360.0	330	COM[79]	-2254.5	360.0
294	SEG[107]	-1174.5	360.0	331	COM[80]	-2281.5	360.0
295	SEG[108]	-1201.5	360.0	332	COM[81]	-2308.5	360.0
296	SEG[109]	-1228.5	360.0	333	COM[82]	-2335.5	360.0
297	SEG[110]	-1255.5	360.0	334	COM[83]	-2362.5	360.0
298	SEG[111]	-1282.5	360.0	335	COM[84]	-2389.5	360.0
299	SEG[112]	-1309.5	360.0	336	COM[85]	-2416.5	360.0
300	SEG[113]	-1336.5	360.0	337	COM[86]	-2443.5	360.0
301	SEG[114]	-1363.5	360.0	338	COM[87]	-2470.5	360.0
302	SEG[115]	-1390.5	360.0	339	COM[88]	-2497.5	360.0
303	SEG[116]	-1417.5	360.0	340	COM[89]	-2524.5	360.0
304	SEG[117]	-1444.5	360.0	341	COM[90]	-2551.5	360.0
305	SEG[118]	-1471.5	360.0	342	COM[91]	-2578.5	360.0
306	SEG[119]	-1498.5	360.0	343	COM[92]	-2605.5	360.0
307	SEG[120]	-1525.5	360.0	344	COM[93]	-2632.5	360.0
308	SEG[121]	-1552.5	360.0	345	COM[94]	-2659.5	360.0
309	SEG[122]	-1579.5	360.0	346	COM[95]	-2686.5	360.0
310	SEG[123]	-1606.5	360.0	347	COM[96]	-2713.5	360.0
311	SEG[124]	-1633.5	360.0	348	COM[97]	-2740.5	360.0
312	SEG[125]	-1660.5	360.0	349	COM[98]	-2767.5	360.0
313	SEG[126]	-1687.5	360.0	350	COM[99]	-2794.5	360.0
314	SEG[127]	-1714.5	360.0	351	COM[100]	-2821.5	360.0
315	COM[64]	-1849.5	360.0	352	COM[101]	-2848.5	360.0
316	COM[65]	-1876.5	360.0	353	COM[102]	-2875.5	360.0
317	COM[66]	-1903.5	360.0	354	COM[103]	-2902.5	360.0
318	COM[67]	-1930.5	360.0	355	COM[104]	-2929.5	360.0
319	COM[68]	-1957.5	360.0	356	COM[105]	-2956.5	360.0

Bonding Diagram (continued)

[Unit: um]

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
357	COM[106]	-2983.5	360.0	370	COM[119]	-3334.5	360.0
358	COM[107]	-3010.5	360.0	371	COM[120]	-3361.5	360.0
359	COM[108]	-3037.5	360.0	372	COM[121]	-3388.5	360.0
360	COM[109]	-3064.5	360.0	373	COM[122]	-3415.5	360.0
361	COM[110]	-3091.5	360.0	374	COM[123]	-3442.5	360.0
362	COM[111]	-3118.5	360.0	375	COM[124]	-3469.5	360.0
363	COM[112]	-3145.5	360.0	376	COM[125]	-3496.5	360.0
364	COM[113]	-3172.5	360.0	377	COM[126]	-3523.5	360.0
365	COM[114]	-3199.5	360.0	378	COM[127]	-3550.5	360.0
366	COM[115]	-3226.5	360.0	379	COMS1	-3577.5	360.0
367	COM[116]	-3253.5	360.0	380	Dummy3	-3617.5	360.0
368	COM[117]	-3280.5	360.0		ALK_L	-3591.0	-242.0
369	COM[118]	-3307.5	360.0		ALK_R	3591.0	-242.0

Package Information



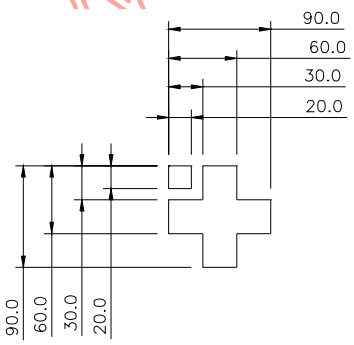
Pad Dimensions

[Unit: um]

	Pad No.	Size	
		X	**Y**
Chip size	-	7410	982
Chip Thickness	-	525 / 400 / 300	
Pad pitch	1~2,119~120	67.5	-
	2~10,11~119	60	-
	10~11	120	-
	122~186,187~314, 315~379	27	-
	186~187,314~315	135	-
	121~122,379~380	40	-
Bump size	1,120	50	66
	2~119	45	66
	121,380	23	134
	122~379	15	134
Bump height	All pads	15±3	

Alignment Mark Dimensions

[Unit: um]



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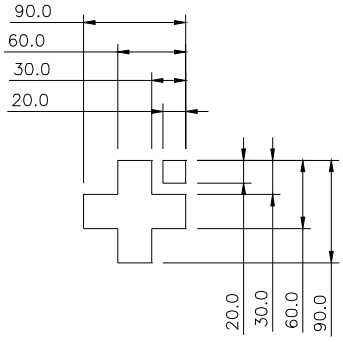

ALK_R

Ordering Information

Part No.	Temperature coefficient (%/°C)	IC thickness (um)	Packages
NT7508H-D/3E	-0.125	300	Gold Bump on Chip Tray (Face up)
NT7508H-D01/3E	-0.05	300	Gold Bump on Chip Tray (Face up)

Cautions

1. The contents of this document will be subjected to change without notice.
2. Precautions against light projection:
   Light has the effect of causing the electrons of semiconductor to move; so light projection may change the characteristics of semiconductor devices. For this reason, it is necessary to take account of effective protection measures for the packages (such as COB, COG, TCP and COF, etc.) causing chip to be exposed to a light environment in order to isolate the projection of light on any part of the chip, including top, bottom and the area around the chip.
   Observe the following instructions in using this product:
   a. During the design stage, it is necessary to notice and confirm the light sensitivity and preventive measures for using IC on substrate (PCB, Glass or Film) or product.
   b. Test and inspect the product under an environment free of light source penetration.
   c. Confirm that all surfaces around the IC will not be exposed to light source.