NOVATEK
聯 詠 科 技

Data Sheet

NT7506

128 x 129 RAM-Map LCD Controller/Driver

V0.02

Preliminary

Revision History

NT7506 Specification Revision History		
Version	**Content**	**Data**
0.01	Original	Dec. 2003
0.02	1. Reduce chip Size and Modify Bonding Diagram. (Page 70~75) 2. Modify pad configuration and descriptions. (Page 5, Page 7~10) 3. Modify package information. (Page 76) 4. Modify reset low pulse width. (Page 61) 5. Added Application information for Pin Connection to MPU. (Page 65~68) 6. Added Ordering Information and Caution. (Page 77)	Aug. 2004

Features

- 128 x 128 dots graphics LCD driver for 4 level grayscale with separated Icon line
- RAM capacity: 129 x 128 x 2 = 33,024bits
- 8-bit parallel bi-directional interface with 6800-series or 8080-series
- SPI (serial peripheral interface) available (only write operation)
- Power supply voltage:
  VDD: 1.8 ~ 3.3V
  VLCD(V0-VSS): 4.0~15.0V
- 3x, 4x, 5x, 6x on chip DC-DC converter
- On-chip Voltage Generator or external LCD driving power supply selectable
- 64 level internal contrast control or external contrast control
- Programmable bias ratio from 1/5 ~ 1/12
- Programmable Multiplex Ratio in dot-matrix display area from 16Mux ~ 129Mux
- On-Chip Oscillator with external resistor
- Temperature coefficient:-0.125%/°C, or external input
- Various partial display
- Partial window moving
- Vertical Scrolling
- Shift change of segment and common driver
- N-raster-row AC liquid-crystal drive (C-pattern waveform drive)
- Low power consumption
  300μA Max. (Operation)
  2μA Max. (Sleep mode)
- CMOS Process
- Available in COG and TCP package

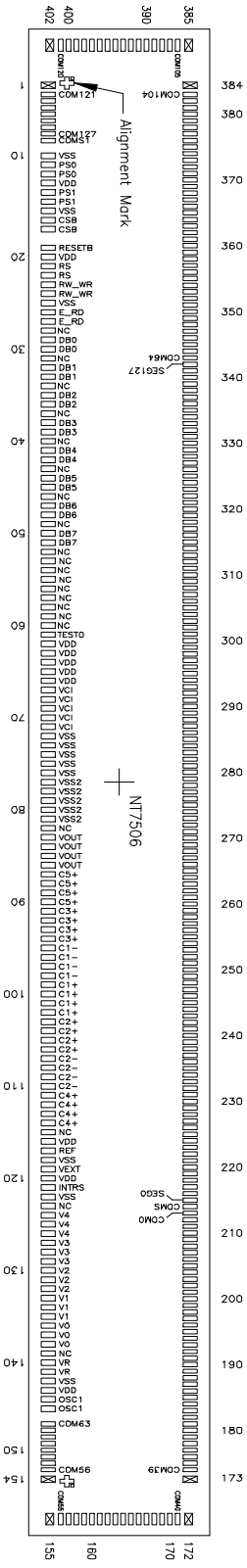
General Description

The NT7506 is a single chip with driver & controller LSI for dot matrix liquid crystal displays, which is display 128 x 129 dot graphics for 4 level grayscale. It accepts serial peripheral interface (SPI) or 8 bit parallel display data directly sent from a microcomputer and stores it in an on chip display RAM of 128 x 129 x 2 bits.

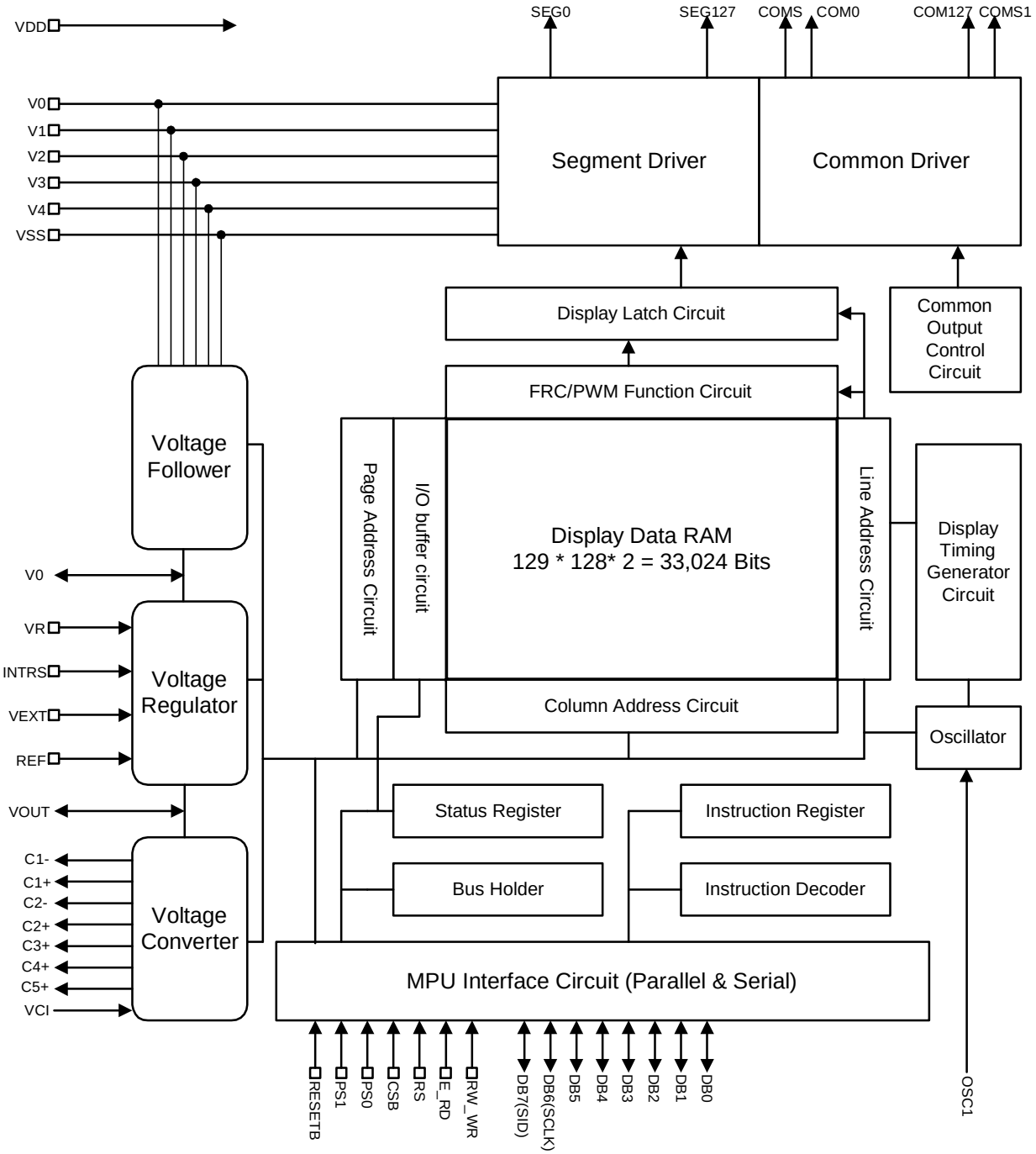
NT7506 embeds a DC/DC converter, an LCD voltage regulator, an on-chip bias divider and an on-chip Oscillator, which reduce the number of external components. NT7506 is suitable for any portable battery-driven applications requiring a long operation and compact size.

No external operation clock is required for RAM read/write operations. Accordingly, this driver can be operated with a minimum current consumption and its on board low current consumption liquid crystal power supply can implement a high performance handy display system with a minimum current consumption and a smallest LSI configuration.

Pad Configuration



Block Diagram



Pin and Pad Descriptions

Power Supply

Pad No.	Designation	I/O	Description
13, 20, 62 – 66, 116, 120, 143	VDD	Supply	1.8～3.3V power supply input
10, 16, 25, 72 – 76, 118, 122, 142	VSS	Supply	Ground input
77 – 81	VSS2	Supply	Ground input
124 – 126 V4 127 – 129 V3 130 – 132 V2 133 – 135 V1 136 – 138 V0		I/O	LCD driver supply voltages. The voltage determined by LCD pixel is impedance-converted by an operational amplifier for application. Voltages should have the following relationship: V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS, When the on-chip operating power circuit is on, the following voltages are given to V1 to V4 by the on-chip power circuit. Voltage selection is performed by the set LCD bias command. When the amplifiers are not used, V0 to V4 voltage can be supplied to these pins externally.

LCD bias	V1	V2	V3	V4
1/N bias	(N-1)/N×V0	(N-2)/N×V0	(2/N)×V0	(1/N)×V0
Note: N= 5 to 12				

LCD Driver Supply

Pad No.	Designation	I/O	Description
95 – 98	C1-	O	Capacitor 1- pad for internal DC/DC voltage converter
99 – 102	C1+	O	Capacitor 1+ pad for internal DC/DC voltage converter
107 – 110	C2-	O	Capacitor 2- pad for internal DC/DC voltage converter
103 – 106	C2+	O	Capacitor 2+ pad for internal DC/DC voltage converter
91 – 94	C3+	O	Capacitor 3+ pad for internal DC/DC voltage converter
111 – 114	C4+	O	Capacitor 4+ pad for internal DC/DC voltage converter
87 – 90	C5+	O	Capacitor 5+ pad for internal DC/DC voltage converter
83 – 86	VOUT	I/O	Voltage converter input / output pin
67 – 71	VCI	I	Voltage converter input voltage pin

140 – 141	VR	I	V0 Voltage adjustment pin. INTRS="H": internal resistors is used, open this pin INTRS="L": using external resistors (Ra/Rb) to adjustment.
117	REF	I	Select the external VREF voltage via the VEXT pin REF="H": using the internal VREF REF="L": using the external VREF
119	VEXT	I	Externally input reference voltage (VREF) for the internal regulator. It is valid only when REF is "L". When using internal voltage regulator, connect to VDD, VSS or open this pin.
144 – 145	OSC1	I	When using internal clock Oscillator, connect a resistor between OSC1 and VDD.

System Control

Pad No.	Designation	I/O	Description
121	INTRS	I	Selects the resistors for adjusting V0 voltage level INTRS="H": use the internal resistors. INTRS="L": use the external resistors.

Microprocessor Interface

Pad No.	Designation	I/O	Description
19	RESETB	I	Reset input pin When RESETB is "L", initialization is executed.
11– 12	PS0	I	Parallel / Serial data select input. PS0 | Interface Mode | Chip Select | Data / Instruction | Data | Read / Write | Serial Clock H | Parallel | CSB | RS | DB7 to DB0 | E_/RD, RW_WR | — L | Serial | CSB | RS | DB7(SID) | Write Only | DB6 (SCLK) Note : In serial mode, it cannot read data from the on-chip RAM. And DB0 to DB5 are high impedance and E_RD and RW_WR must be fixed to either "H" or "L".
14 – 15	PS1	I	Microprocessor interface select input pin Interface Select | 6800 series | 8080 series | 4 pin SPI | 3 pin SPI PS0 | H | H | L | L PS1 | H | L | H | L
17 – 18	CSB	I	Chip Select input pins Data/Instruction I/O is enabled only when CSB is "L". When chip select s non-active, DB0 to DB7 are control data.

<table>
<tr><td>21 – 22</td><td>RS</td><td>I</td><td>Register select input pins
RS=”H”: DB0 to DB7 are display data
RS=”L”: DB0 to DB7 are control data</td></tr>
<tr><td>23 – 24</td><td>RW_WR</td><td>I</td><td>Read / Write execution control pin
<table>
<tr><th>C86</th><th>MPU Type</th><th>RW_WR</th><th>Description</th></tr>
<tr><td>H</td><td>6800 series</td><td>RW</td><td>Read/Write control input pin
-RW="H":read
-RW="L":write</td></tr>
<tr><td>L</td><td>8080 series</td><td>/WR</td><td>Write enable clock input pin
The data on DB0 to DB7 are latched at the rising edge of the /WR signal.</td></tr>
</table></td></tr>
<tr><td>26 – 27</td><td>E_RD</td><td>I</td><td>Read / Write execution control pin
<table>
<tr><th>PS1</th><th>MPU Type</th><th>E_RD</th><th>Description</th></tr>
<tr><td>H</td><td>6800 series</td><td>E</td><td>Read / Write control input pin
-RW="H": when E is "H", DB0 to DB7 are in an output status.
-RW="L": The data on DB0 to DB7 are latched at the falling edge of the E signal.</td></tr>
<tr><td>L</td><td>8080 series</td><td>/RD</td><td>Read enable clock input pin
When /RD is "L", DB0 to DB7 are in an output status.</td></tr>
</table></td></tr>
<tr><td>29 – 30,
32 – 33
35 – 36,
38 – 39
41 – 42,
44 – 45
47 – 48,
50 – 51</td><td>DB0 to DB7</td><td>I/O</td><td>8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus.
When the serial interface selected (PS0=”L”);
DB0 to DB5: high impedance
DB6: serial input clock (SCLK)
DB7: serial input data (SID)
When chip select is not active, DB0 to DB7 may be high impedance.</td></tr>
</table>

Liquid Crystal Drive Pads

<table>
<tr><th>Pad No.</th><th>Designation</th><th>I/O</th><th>Description</th></tr>
<tr><td>215 – 342</td><td>SEG 0
to
SEG127</td><td>O</td><td>LCD segment drive outputs
The display data and the M signal control the output voltage of segment driver.
<table>
<tr><td>H</td><td>H</td><td>V0</td><td>V2</td></tr>
<tr><td>H</td><td>L</td><td>VSS</td><td>V3</td></tr>
<tr><td>L</td><td>H</td><td>V2</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V3</td><td>VSS</td></tr>
<tr><td colspan="2">Power Save Mode</td><td>VSS</td><td>VSS</td></tr>
</table></td></tr>
</table>

<table>
<tr>
<td>2 – 8
146 – 153
156 – 171
174 – 213
343 – 383
386 – 401</td>
<td>COM 0
to
COM127</td>
<td>O</td>
<td>LCD common driver outputs
The internal scanning data and M signal control the output voltage of common driver.
<table>
<tr><th>Scan data</th><th>M(Internal)</th><th>Common driver output voltage</th></tr>
<tr><td>H</td><td>H</td><td>VSS</td></tr>
<tr><td>H</td><td>L</td><td>V0</td></tr>
<tr><td>L</td><td>H</td><td>V1</td></tr>
<tr><td>L</td><td>L</td><td>V4</td></tr>
<tr><td colspan="2">Power Save Mode</td><td>VSS</td></tr>
</table>
</td>
</tr>
<tr>
<td>214
(9)</td>
<td>COMS
(COMS1)</td>
<td>O</td>
<td>Common output for the icons
The output signals of two pins are same. When not used, these pins should be left open.</td>
</tr>
</table>

Test Pads

Pad No.	Designation	I/O	Description
61	TEST0	I	Test pads, and must be connected to VDD
28, 31, 34, 37, 40, 43, 46, 49, 52 – 60, 82, 115, 123, 139	NC	-	NC pads, no connection for user
1, 154, 155, 172, 173, 384, 385,402	DUMMY0 to DUMMY7	-	Dummy pads, no connection for user

Functional Description

1. Microprocessor Interface

1.1 Chip Select Input

The NT7506 has one chip select pads can interface to a microprocessor wheh CSB is “L”. When these pins are set to any others combinatins, RS, E_RD, and RW_RW inputs are disabled and DB0 to DB7 are to be high impedance. And , in case of serial interface, the internal shift register and the counter are reset.

1.2 Parallel / Serial Interface

The NT7506 has four types of interface with an MPU, which are two serial and two parallel interface.This parallel or serial interface is determined by PS0 pin as shown in table 1.

PS0	Type	PS1	CSB	Interface Mode
H	Parallel	H	CSB	6800-series MPU mode
		L		8080-series MPU mode
L	Serial	H	CSB	4-pin SPI mode
		L		3-pin SPI mode

Table 1. Parallel / Serial Interface Mode

1.3 Parallel Interface (PS0=“H”)

The 8 bit bi-direction data bus is used in parallel interface and the type of MPU is selected by PS1 as shown in table 2.

PS1	MPU Bus Type	CSB	RS	E_RD	RW_WR	DB0 to DB7
H	6800-series	CSB	RS	E	RW	DB0 to DB7
L	8080-series	CSB	RS	/RD	/WR	DB0 to DB7

Table 2. Microprocessor Selection for Parallel Interface

The type of data transfer is determined by signals at RS,E_RD, and RW_WR as shown in table 3.

Common	6800 series		8080 series		Description
RS	E_RD	RW_WR	/RD	RW_WR	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register (instruction)

Table 3. Parallel Data Transfer

When E_RD pin is always pulled high for 6800 series interface, it can be used CSB for enable signal.

1.4 Serial Interface (PS0="L")

When the NT7506 is active at serial interface, serial data (DB7) and serial clock(DB6) inputs are enabled. If not, the internal 8 bit shift register and the 3 bit counter are reset.The display data / command indication may be controlled either via software or the Register Select (RS)pin, based on the setting of PS1. In 4 pin SPI mode,data is display data when RS is "H" and Common data when RS is "L".

In 3 pin SPI mode, the LCD driver will reveive command from MCU by default. If message on the data pin are data rather than command, MCU should send data direction command(11101000) to control the data direction and then one more command to define the number of data bytes will be write.After these two contunuous commands are send, the following messages will be data rather than command.

Serial data can be read on the rising edge of serial clock going into DB6. And the DDRAM column address pointer will be increased by one automatically. The next bytes after the display data string is handled as command data.

Serial mode	PS0	PS1	CSB	RS
4 pin SPI mode	L	H	CSB	Uesd
3 pin SPI mode	L	L	CSB	Not Used

4 pin SPI Mode (PS0="L",PS1="H")

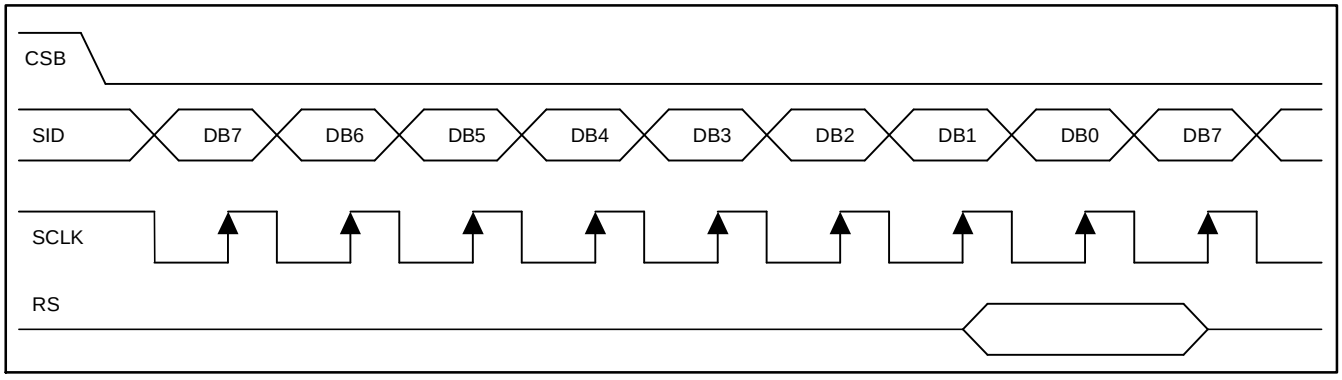


Figure 1. 4 pin SPI Timing (RS is used)

3 pin SPI Mode (PS0="L" , PS1="L")

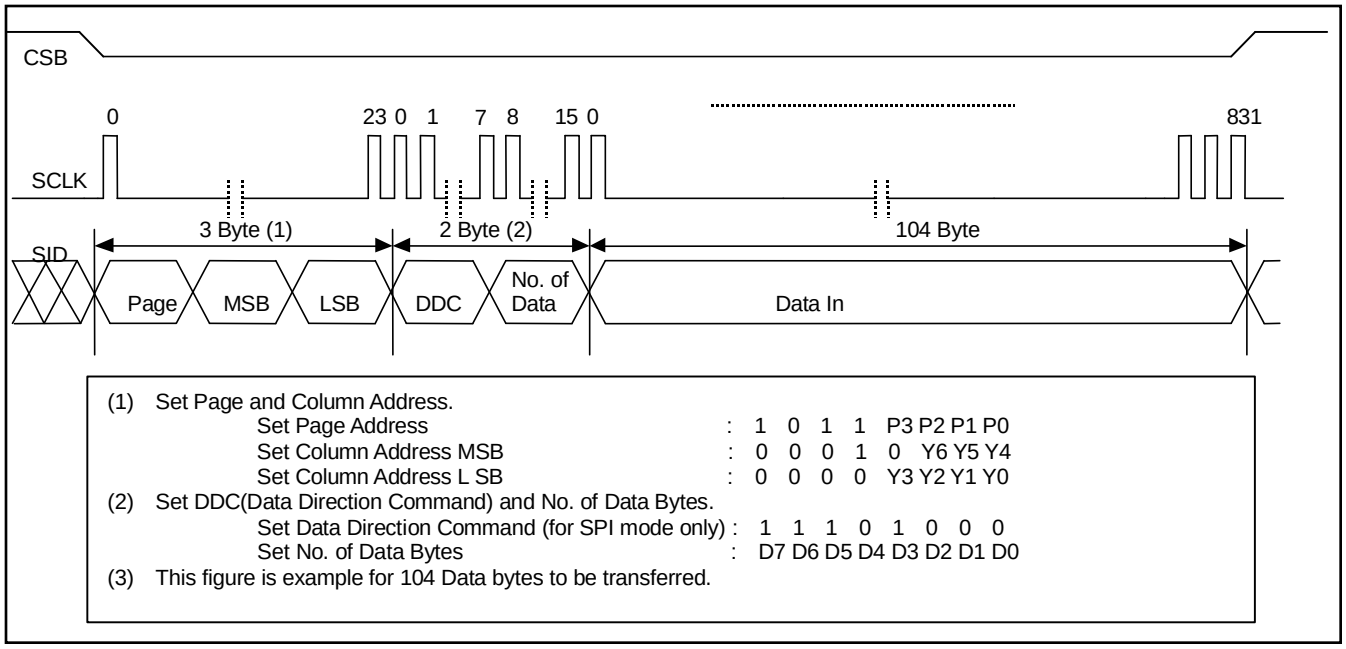


Figure 2. 3-pin SPI Timing (RS is not used)

This command is used in 3 pin SPI mode only. It will be continuous commands, the first byte controls the data direction and informs the LCD driver the second byte will be number of data bytes will be write. After these two commands sending out, the following messages will be data. If data is stopped in transmitting, it is not valid data.New data will be transferred serially with most significant bit first.

Note: In spite of transmission of data, if CSB will be disable, state terminates abnormally. Next state is initialized.

1.5 Busy Flag

The Busy Flag indicatges whether the NT7506 is operating or not.When DB7 is "H" in read status operstion, this device is in busy status and will accept only read status instruction. If the cycle time is correct, the microprocessor needs not to check this flag before each informationm which improves the MPU performance.

1.6 Data Transfer

NT7506 uses bus holder and internal data bus for data transfer with the MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in figure 3. And when reading data from on-chip RAM to th MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in figure 4. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

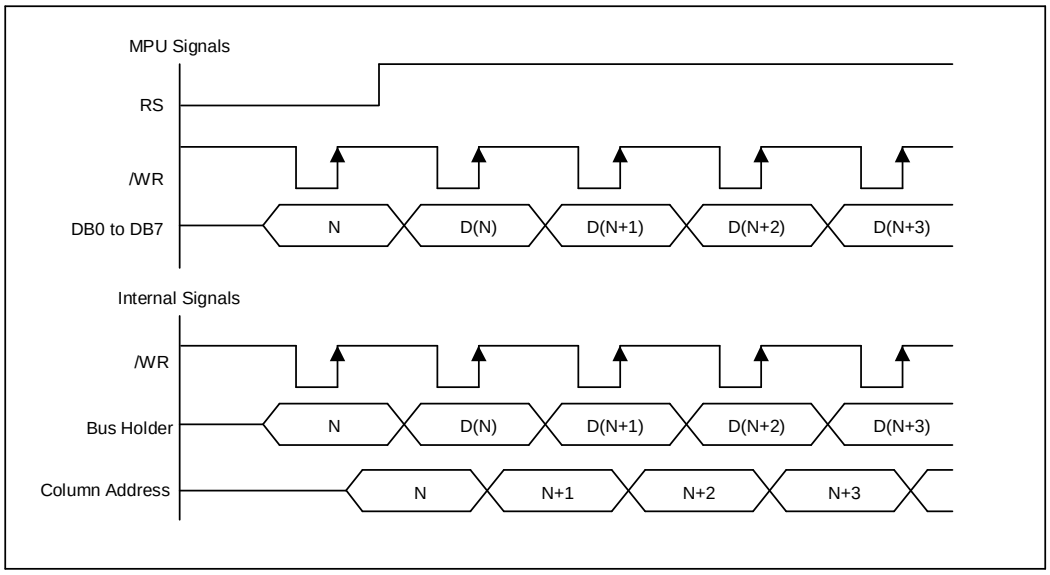


Figure 3. Write Timing

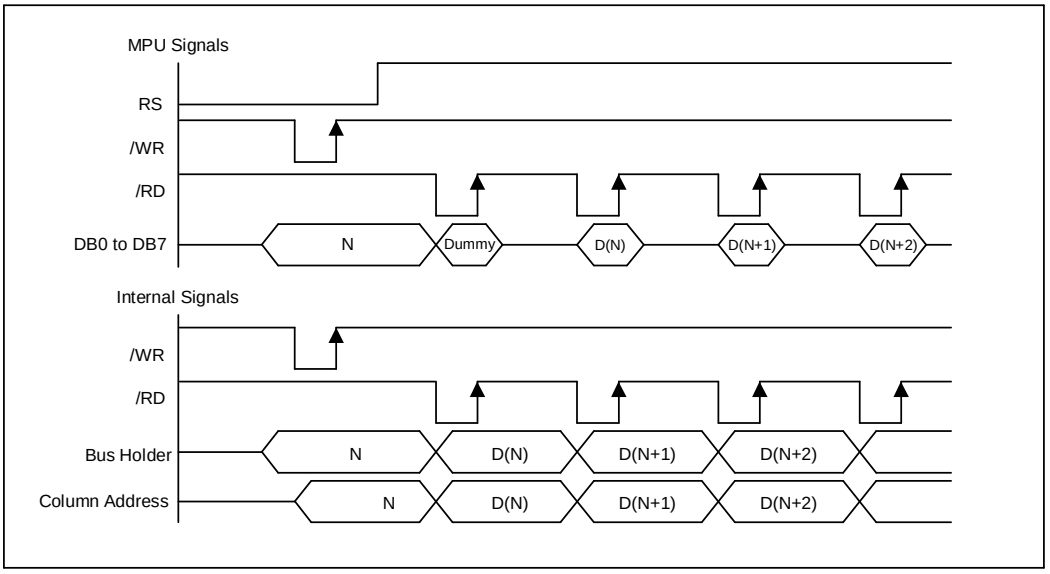


Figure 4. Read Timing

2. Display Data RAM

The Display Data RAM stores pixel data for the LCD. It is 129-row(17 page by 8 bits) by 128-column addressable array. Each pixel can be selected when the page and column addresses are specified. The 129 rows are divided into 16 pages of 8 lines and the 17th page with a single line(DB0 only). Data is read from or written to the 8 lines of each page directly through DB0 to DB7.The display data of DB0 to DB7 from the microprocessor correspond to the LCD common lines. The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independenlty, dat can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

3. Page Address Circuit

The circuit is for providing a Page Address to Display Data RAM shown in figure 8. It incorporates 4-bit Page Address register changed by only the “Set Page” instruction. Page Address 16 is a special RAM area for the icons and display data DB0 in only valid.

4. Line Address Circuit

This circuit assigns DDRAM a Line Address corresponding to the first line (COM0) of the display. Therefore, by setting Line Adddress repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on chip RAM as shown in figure 6. It incorporates 7-bit Line Address register changed by only the initial display line instruction and 7 bit counter circuit. At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by CL signal and generates the line address for transferring the 128 bit RAM data to the display data latch circuit. When icon is enabled by setting icon control register, display data of icons are not scrolled because the MPU can not access Line Address of icons.

5. Column Address Circuit

Column Address Circuit has a 8 bit preset counter that provides Column Address to the Display Data RAM as shown in figure 6. When set Column Address MSB/LSB instruction is issued, 7-bit [Y7 : Y1] are set and lowest bit, Y0 is set to “0”. Since this address is increased by 1 each a read or write data instruction, microprocessor can access the display data continuously. However, the counteris not increased and locked of a non-existing address above 7EH. It counter is independent of page address register.

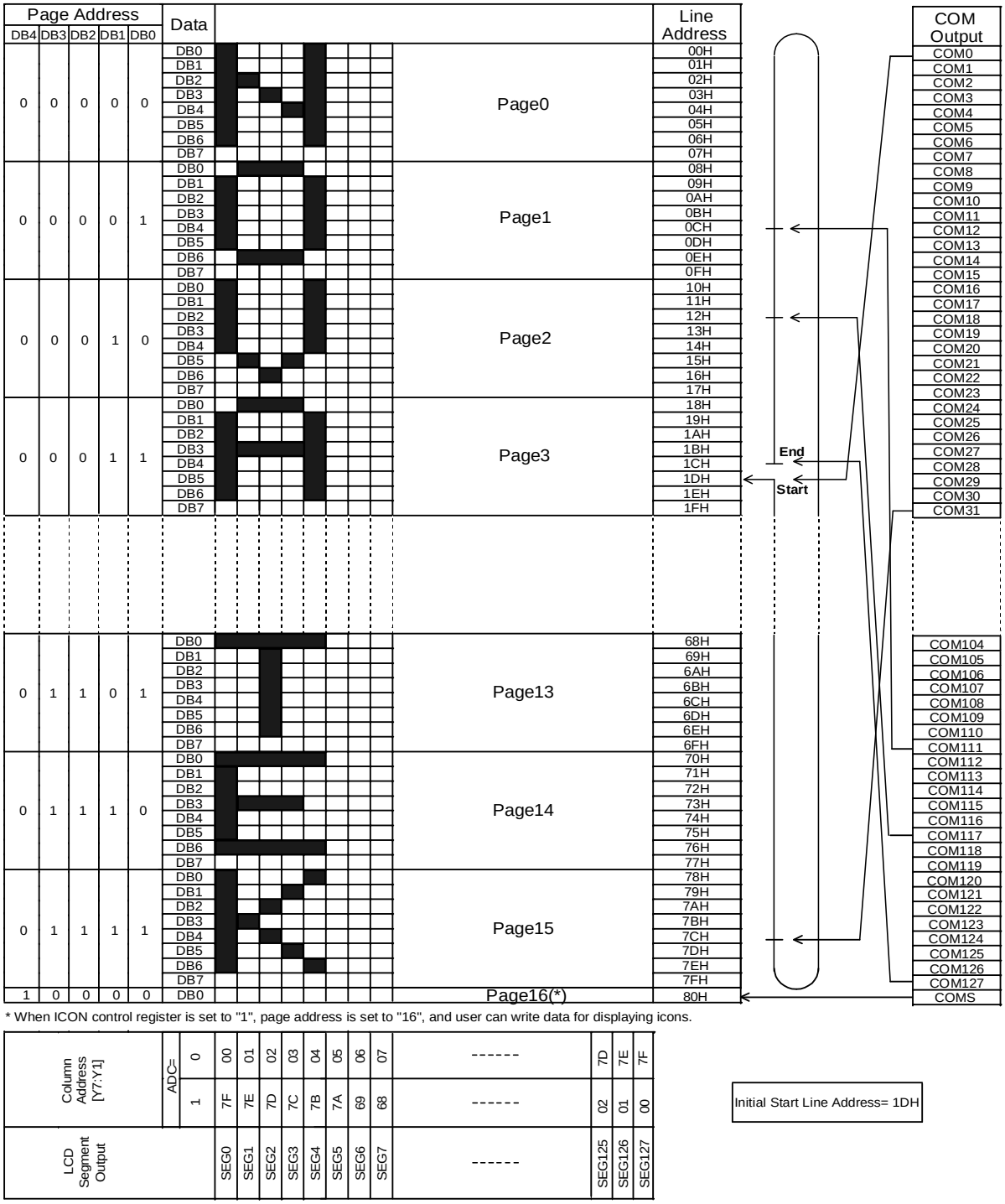
ADC select instruction makes it possible to invert the relationship between the Column Address and the segment outputs.It is necessary to rewrite the display data on built in RAM after issuing ADC select instruciton.Refer to the following figure 5.

SEG Output	SEG 0		SEG 1		SEG 2		SEG 3		…	SEG 124		SEG 125		SEG 126		SEG 127	
Column Address[Y7:Y1]	00H		01H		02H		03H		…	7CH		7DH		7EH		7FH	
Internal Column Address[Y7:Y1]	00H	01H	02H	03H	04H	05H	06H	07H	…	F8H	F9H	FAH	FBH	FCH	FDH	FEH	FFH
Display Data(ADC=0)	1	1	1	0	0	0	0	1	…	1	1	0	0	1	0	0	1
LCD Panel Display									…								
Display Data(ADC=1)	0	1	1	0	0	0	1	1	…	0	1	0	0	1	0	1	1
LCD Panel Display									…								

Figure 5. The Relationship between the Column Address and The Segment Outputs

6. Segment Control Circuit

This circuit controls the display data by the display ON/OFF, reverse display ON/OFF and entire display ON/OFF instructions wihtout changing the data in the display data RAM.



* When ICON control register is set to "1", page address is set to "16", and user can write data for displaying icons.

Figure 6. Display Data RAM Map

7. LCD Display Circuit

FRC(Frame Rate Control) and PWM(Pulse Width Modulation) Function Circuit

NT7506 incorporates an FRC function and a PWM function circuit to display a 4 level gran scale. The FRC function and PWM utilize liquid crystal characteristics whose transmittance is changed by an effective value of applied voltage. The NT7506 provides four 4 bit palette-registers to assign the desired gray level. Thses registers are set by the instrucitons and the RESETB.

-Gray Scake Table of 4 FRC(Frame Rate Control)

Gray Scale Level	MSB (DB7 to DB4)	LSB (DB3 to DB0)
White	2nd FR (FR2)	1st FR (FR1)
	4th FR (FR4)	3rd FR (FR3)
Light Gray	2nd FR (FR2)	1st FR (FR1)
	4th FR (FR4)	3rd FR (FR3)
Dark Gray	2nd FR (FR2)	1st FR (FR1)
	4th FR (FR4)	3rd FR (FR3)
Black	2nd FR (FR2)	1st FR (FR1)
	4th FR (FR4)	3rd FR (FR3)

-Gray Scake Table of 3 FRC(Frame Rate Control)

Gray Scale Level	MSB (DB7 to DB4)	LSB (DB3 to DB0)
White	2nd FR (FR2)	1st FR (FR1)
	× × × ×	3rd FR (FR3)
Light Gray	2nd FR (FR2)	1st FR (FR1)
	× × × ×	3rd FR (FR3)
Dark Gray	2nd FR (FR2)	1st FR (FR1)
	× × × ×	3rd FR (FR3)
Black	2nd FR (FR2)	1st FR (FR1)
	× × × ×	3rd FR (FR3)

-Gray Scake Table of 15 PWM(Pulse Width Modulation)

Dec	Hex	4-bits	PWM(on width)	Note
0	00	0000	0 (0/15)	Brighter
1	01	0001	1/15	↑
2	02	0010	2/15	↑
3	03	0011	3/15	↑
4	04	0100	4/15	↑
5	05	0101	5/15	↑
6	06	0110	6/15	↑
7	07	0111	7/15	↑
8	08	1000	8/15	↑
9	09	1001	9/15	↑
10	0A	1010	10/15	↑
11	0B	1011	11/15	↑

12	0C	1100	12/15	
13	0D	1101	13/15	
14	0E	1110	14/15	
15	0F	1111	1 (15/15)	Darker

-Gray Scake Table of 12 PWM(Pulse Width Modulation)

Dec	Hex	4-bits	PWM(on width)	Note
0	00	0000	0 (0/12)	Brighter
1	01	0001	1/12	
2	02	0010	2/12	
3	03	0011	3/12	
4	04	0100	4/12	
5	05	0101	5/12	
6	06	0110	6/12	
7	07	0111	7/12	
8	08	1000	8/12	
9	09	1001	9/12	
10	0A	1010	10/12	
11	0B	1011	11/12	
12	0C	1100	1 (12/12)	Darker
13	0D	1101	0/12	This area is selected to OFF level (0/12 level)
14	0E	1110	0/12	
15	0F	1111	0/12	

-Gray Scake Table of 9PWM(Pulse Width Modulation)

Dec	Hex	4-bits	PWM(on width)	Note
0	00	0000	0 (0/9	Brighter
1	01	0001	1/9	
2	02	0010	2/9	
3	03	0011	3/9	
4	04	0100	4/9	
5	05	0101	5/9	
6	06	0110	6/9	
7	07	0111	7/9	
8	08	1000	8/9	
9	09	1001	1 (9/9)	Darker
10	0A	1010	0/9	This area is selected to OFF level (0/9 level)
11	0B	1011	0/9	
12	0C	1100	0/9	
13	0D	1101	0/9	
14	0E	1110	0/9	
15	0F	1111	0/9	

8. Oscillator

This is on-chip Oscillator with external resistor. Its frequency is controlled by external resistor between OSC1 and VDD. This Oscillator signal is used in the voltage converter and display timing generation circuit.

9. Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock,CL(internal),generated by Oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal(M) which enables the LCD driver to make a AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. The frame signal or the line signal changes the M by setting internal instruction. Driving waveform and internal timing signal are shown in Figure 7.

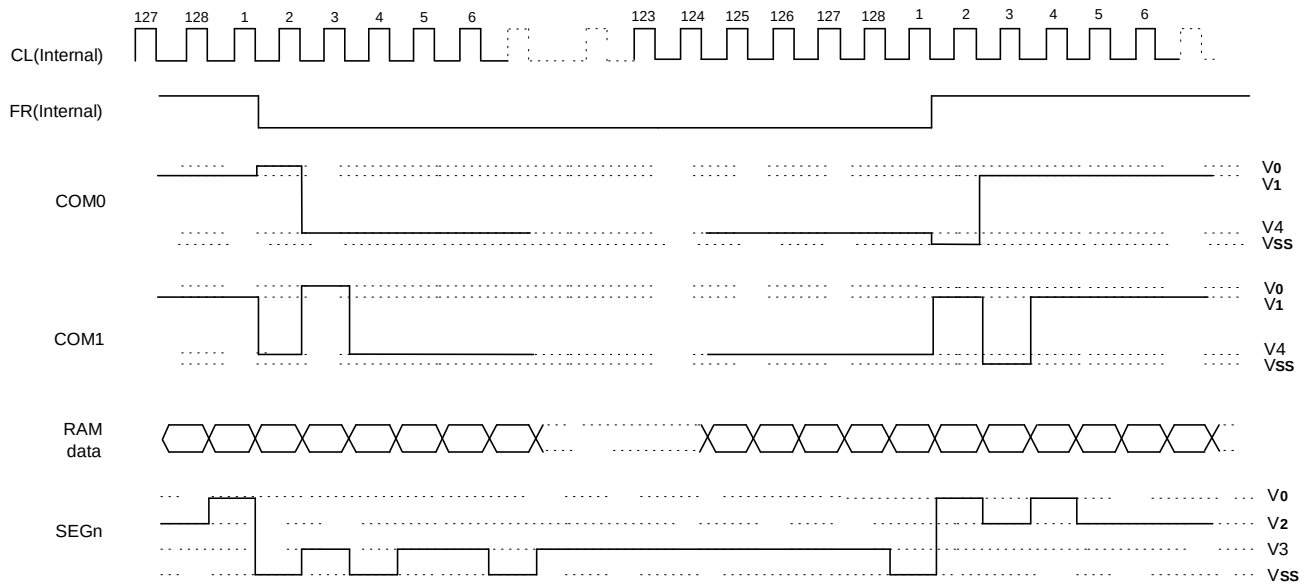


Figure 7. 2-frame AC Driving Waveform (Duty Ratio = 1/128)

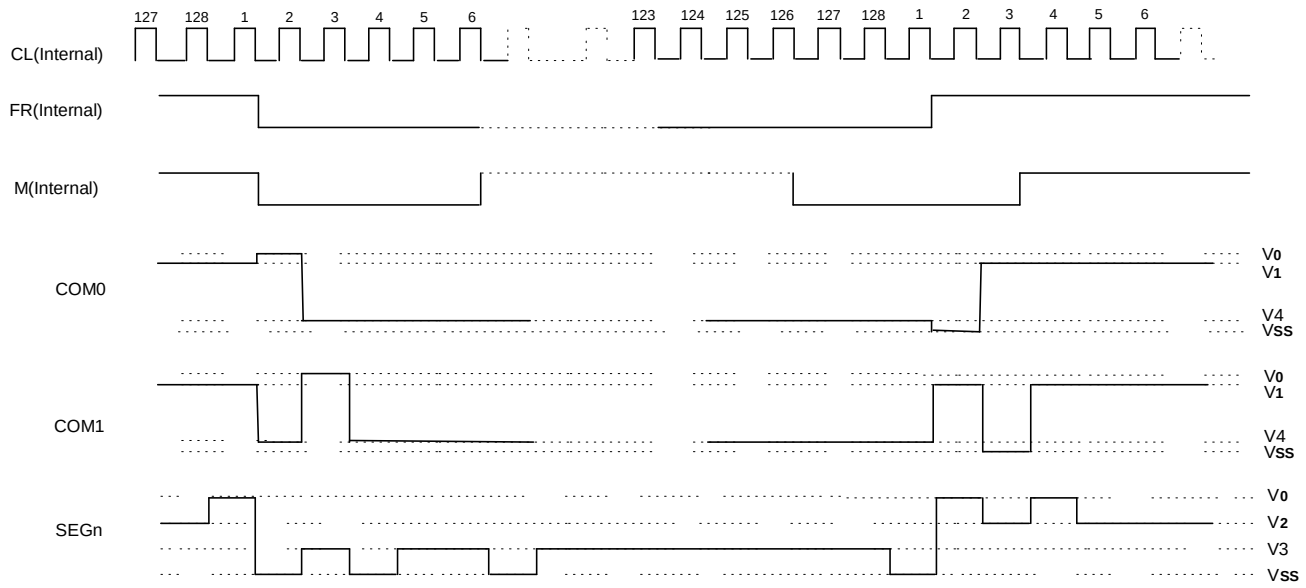


Figure 8. N-Line Inversion Driving Waveform (N = 5, Duty Ratio = 1/128)

10. LCD Driver Circuit

This driver circuit is configured by 129-channel common drivers and 128-channel segment drivers. This LCD panel driver voltage depends on the combination of display data and M signal.

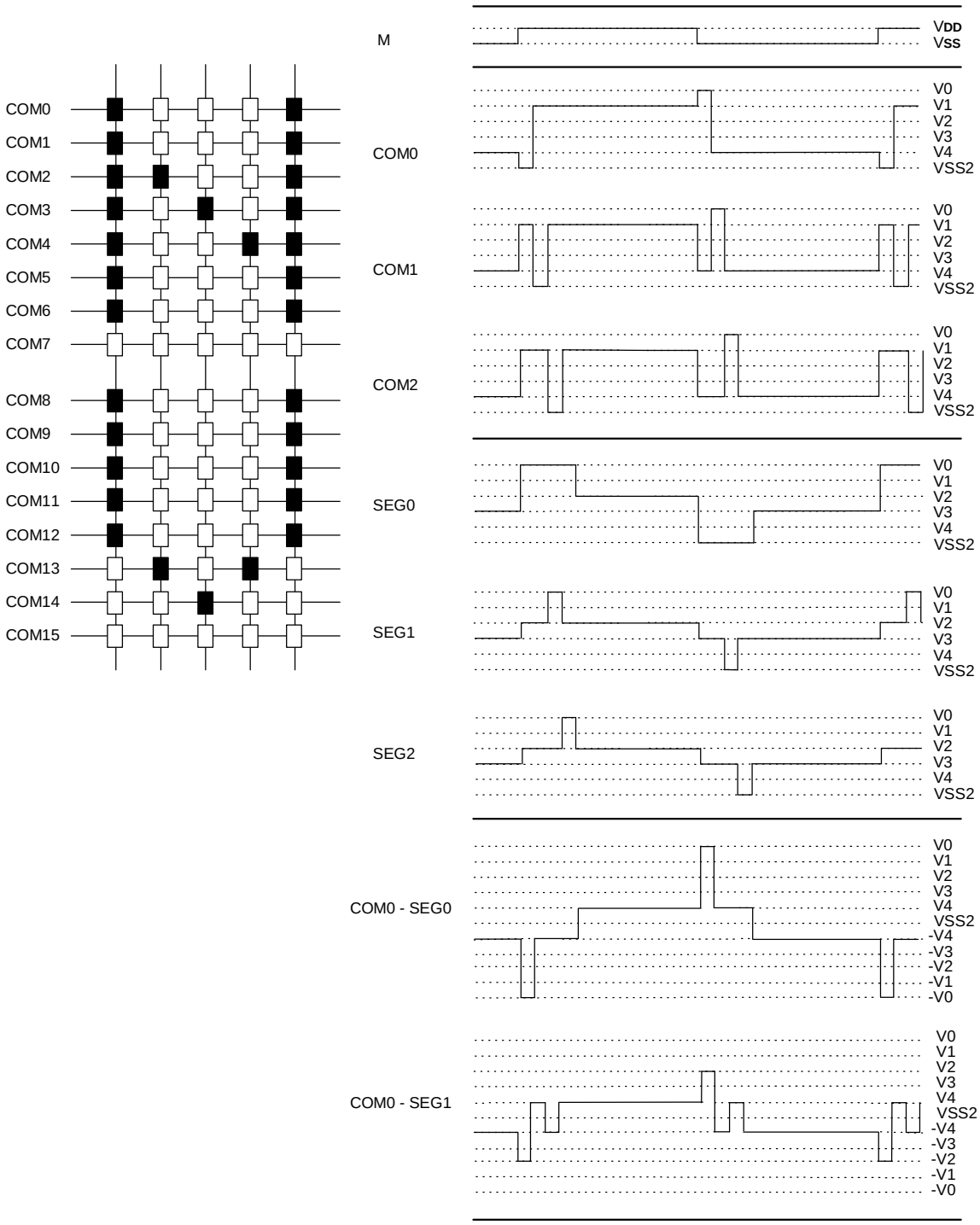


Figure 9. Segment and Common Timing

11. Partial Display On LCD

The NT7506 realizes the Partial Display function on LCD with low-duty driving for saving power consumption and showing the various display duty. To show the various display duty on LCD, LCD driving duty and bias are programmable via the instruction. And, built-in power supply circuits are controlled by the instruction for adjusting the LCD driving voltages.

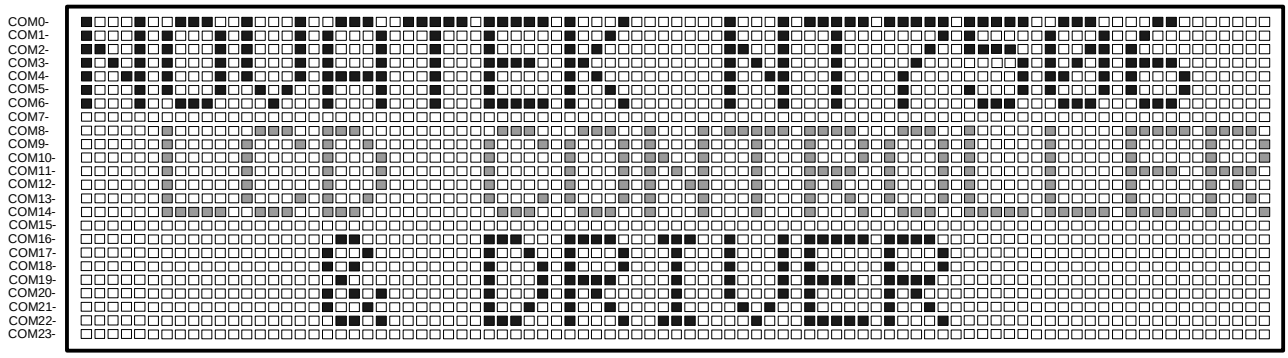


Figure 10. Reference Example for Partial Display

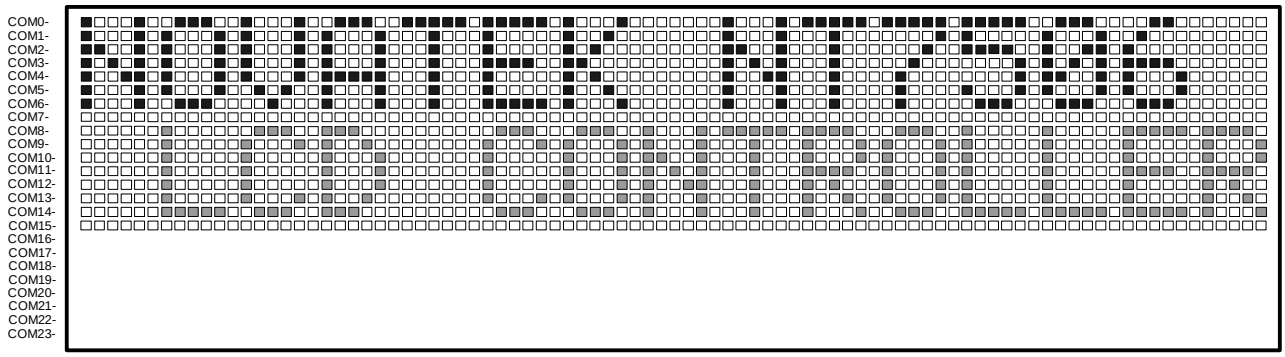


Figure 11. Partial Display (Partial Display Duty = 16, Initial COM0 = 0)

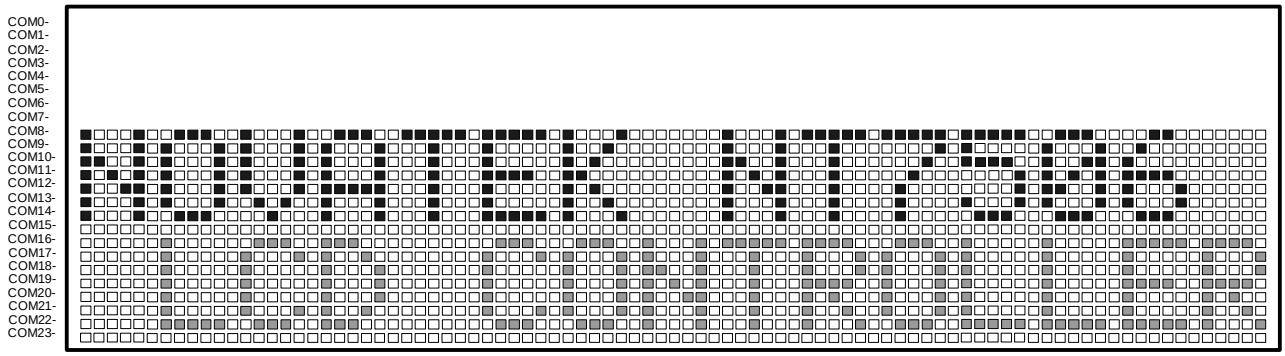


Figure 12. Moving Display (Partial Display Duty = 16, Initial COM0 = 8)

12. Power Supply Circuit

The power Supply circuit generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are controllerd by power control instruction. For details, refers to “Instruction Description”. Table 4 shows the referenced combinations in using Power Supply circuits.

User setup	Power control (V/C V/R V/F)	V/C circuits	V/R circuits	V/F circuits	VOUT	Vo	V1 to V4
Only the internal power supply circuits are used	1 1 1	ON	ON	ON	Open	Open	Open
Only the voltage regulator circuits and voltage follower circuits are used	0 1 1	OFF	ON	ON	External Input	Open	Open
Only the voltage follower circuit are used	0 0 1	OFF	OFF	ON	Open	External input	Open
Only the external power supply circuit are used	0 0 0	OFF	OFF	OFF	Open	External input	External input

Table 4. Recommended Power Supply Combinations

13. Voltage Convertor Circuit

These circuit boost up the electric potential between VCI and Vss to 3,4,5 or 6 times toward positive side and boosted voltage is outputted from VOUT pin. It is possible to select the lower boosting level in any boosting circuit by “Set DC-DC Step-up” instruction. When the higher level is selected by instruction, VOUT voltage is not valid.

[C1 = 1.0 to 4.7 (μF)]

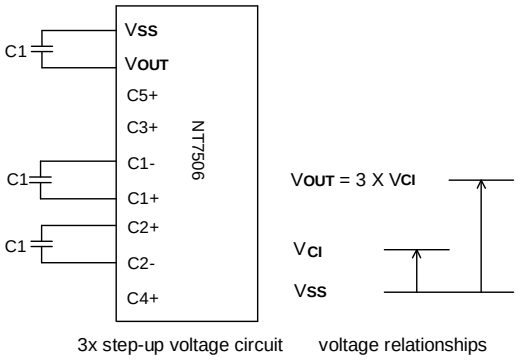


Figure 13. Three Times Boosting Circuit

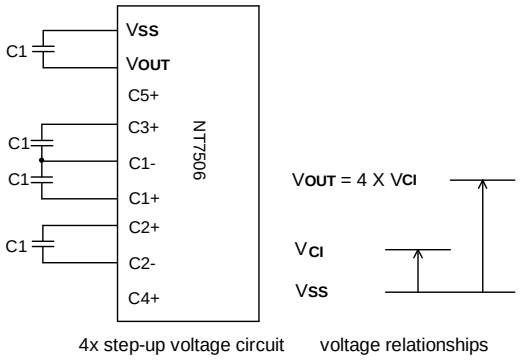


Figure 14. Four Times Boosting Circuit

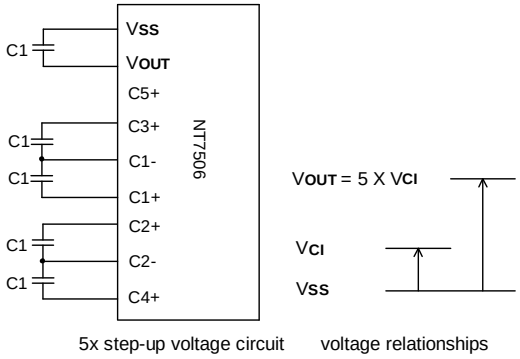


Figure 15. Five Times Boosting Circuit

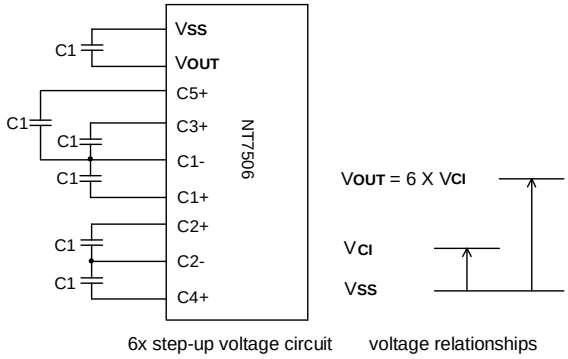


Figure 16. Six Times Boosting Circuit

14. The Voltage Regulator Circuit

The function of the internal voltage regulator circuits is to determine liquid crystal operating voltage, V0 by adjusting resistor, Ra and Rb, within the range of |VOl < |VOUTl. Because VOUT is the operating voltage of operational-amplifier circuits shown in figure17, it is necessary to be applied internally or externally.

For the Eq.1, we determine V0 by Ra,Rb and VEV. The Ra and Rb are connected internally or externally by INTRS pin. And VEV called the voltage of electronic volume is determined by Eq.2, where the parameter α is the value selected by instruction, “Set Reference Voltage Register”, within the range 0 to 63. VREF voltage at Ta=25℃ is shown in Table 5.

$V0 = (1+ Rb/Ra) \times VEV$----------(Eq.1)

$VEV = (1- (63-\alpha)/210) \times VREF$--------(Eq.2)

REF	Temp. coefficient	VREF(V)
1	-0.125% /°C	2.1
0	External input	VEXT

Table 5 . VREF Voltage at Ta = 25°C

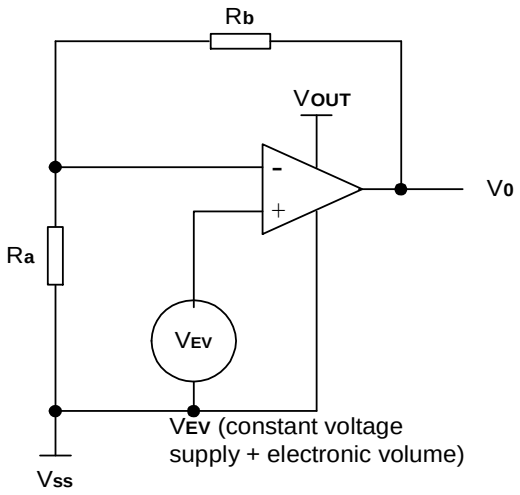


Figure 17. Internal Voltage Regulator Circuit

In Case of Using Internal Resistors, Ra and Rb (INTRS = "H")

When INTRS pin is "H", resistor Ra is connected internally between VR pin and VSS, and Rb is connected between V0 and VR. We determine V0 by two instructions, "Regulator Resistor Select" and "Set Reference Voltage".

	3-bit data settings (R2 R1 R0)							
	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
1+ (Rb / Ra)	2.3	3.0	3.7	4.4	5.1	5.8	6.5	7.2

Table 6. Internal Rb / Ra Ratio depending on 3-bit Data (R2 R1 R0)

Figure 18 shows V0 voltage measured by adjusting internal regulator register ratio(Rb / Ra) and 6-bit electronic volume registers for each temperature coefficient at Ta = 25 °C.

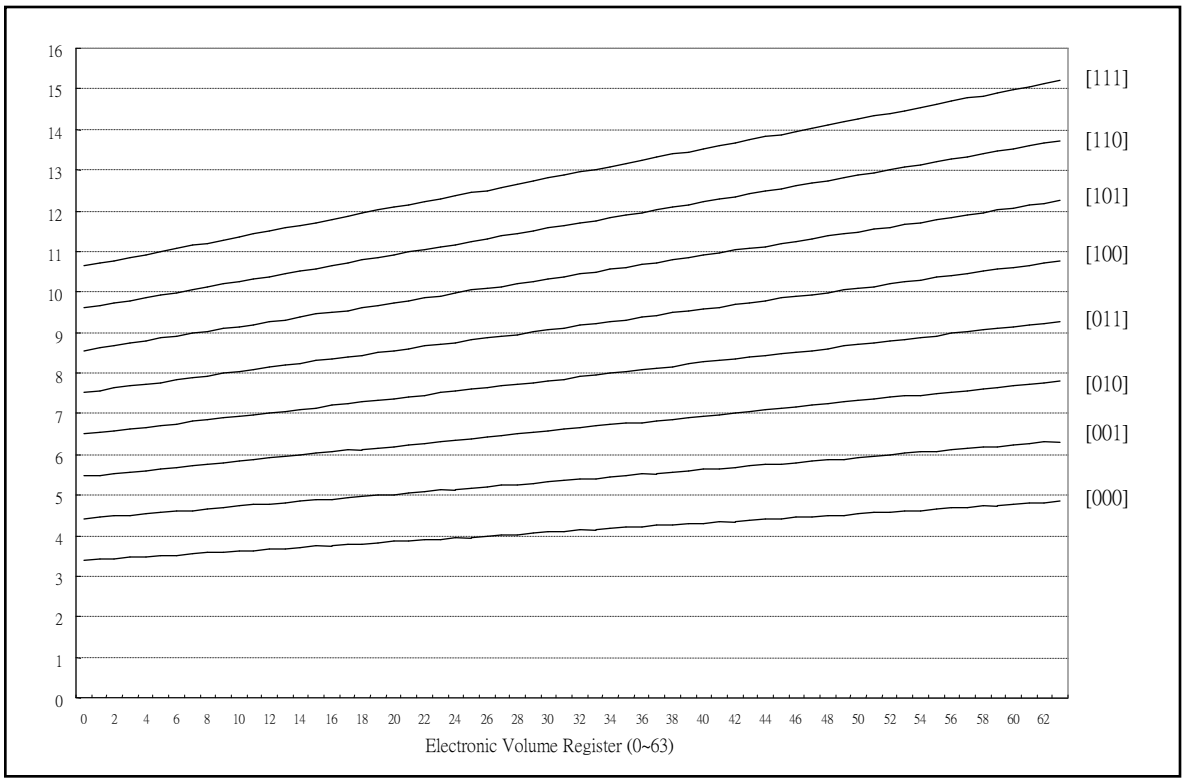


Figure 18. Electronic Volume Level (Temp. Coefficient = -0.125% / °C)

In Case of Using External Resistors, Ra and Rb (INTRS = "L")

When INTRS pin is "L", it is necessary to connect external regulator Ra between VR and VSS, and Rb between V0 and VR.

Example: For the following requirements

1. LCD driver voltage, V0 = 10V
2. 6-bit reference voltage register = (1, 0, 0, 0, 0, 0)
3. Maximum current flowing Ra, Rb = 1μA

From Eq.1
$10 = (1+ Rb/Ra) \times VEV$ [V]--------(Eq.3)

From Eq.1
$VEV = (1+ (63-32)/210) \times 2.1 = 1.79$ [V]--------(Eq.4)

From requirement 3.
$10 / (Ra +Rb) = 1$ [μA] --------(Eq.5)

From equations Eq. 3, 4 and 5
Ra = 1.79 [MΩ]
Rb = 8.21 [MΩ]

	Electronic volume level				
	0	……	32	……	63
V0	8.21	……	10.00	……	11.73

Table 7. The Range of V0

15. Voltage Follower Circuit

VLCD voltage (V0) is resistively divided into four voltage levels (V1, V2, V3 and V4), and those output impedance are converted by the voltage follower for increasing drive capability. Table ** shows the relationship between V1 to V4 level and each duty ratio.

LCD bias	V1	V2	V3	V4	Remarks
1 / N	(N-1) / N × V0	(N-2) / N × V0	2 / N × V0	1 /N × V0	N = 5 to 12

Table 8. The Relationship between V1 to V4 Level and Each Duty Ratio

16. Reference Power Supply Circuit for Driving LCD Panel

[C1 = 1.0 ~ 4.7 (μF), C2 = 0.47 ~ 2.0 (μF)]

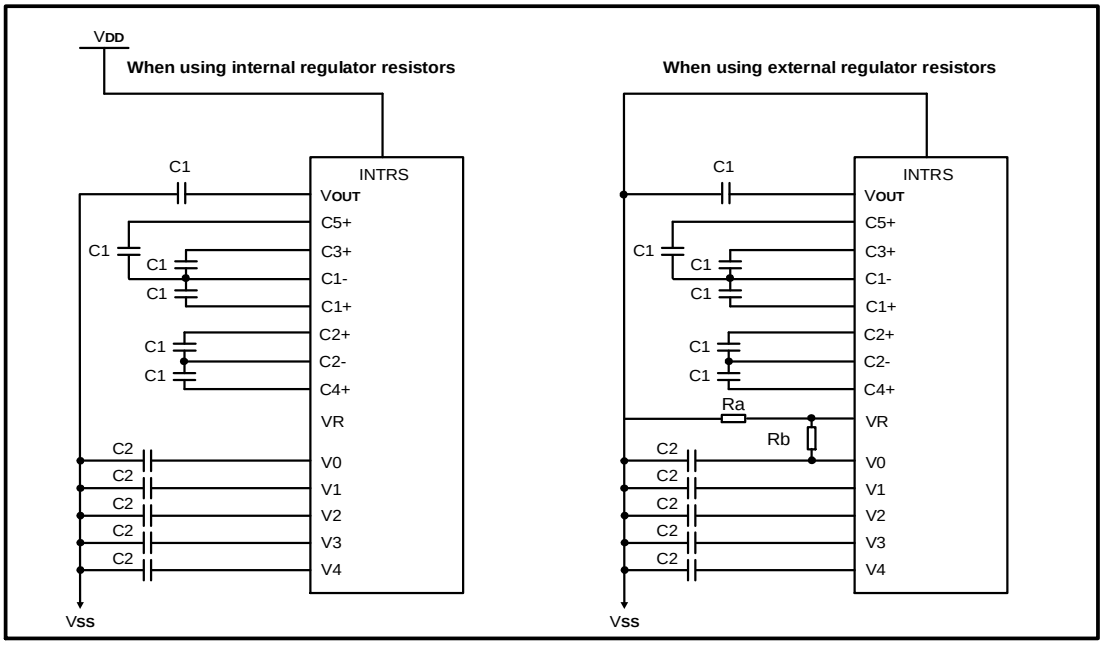


Figure 19. When Using all LCD Power Circuits (6-Time V/C: ON, V/R: ON, V/F: ON)

[C2 = 0.47 ~ 2.0 (μF)]

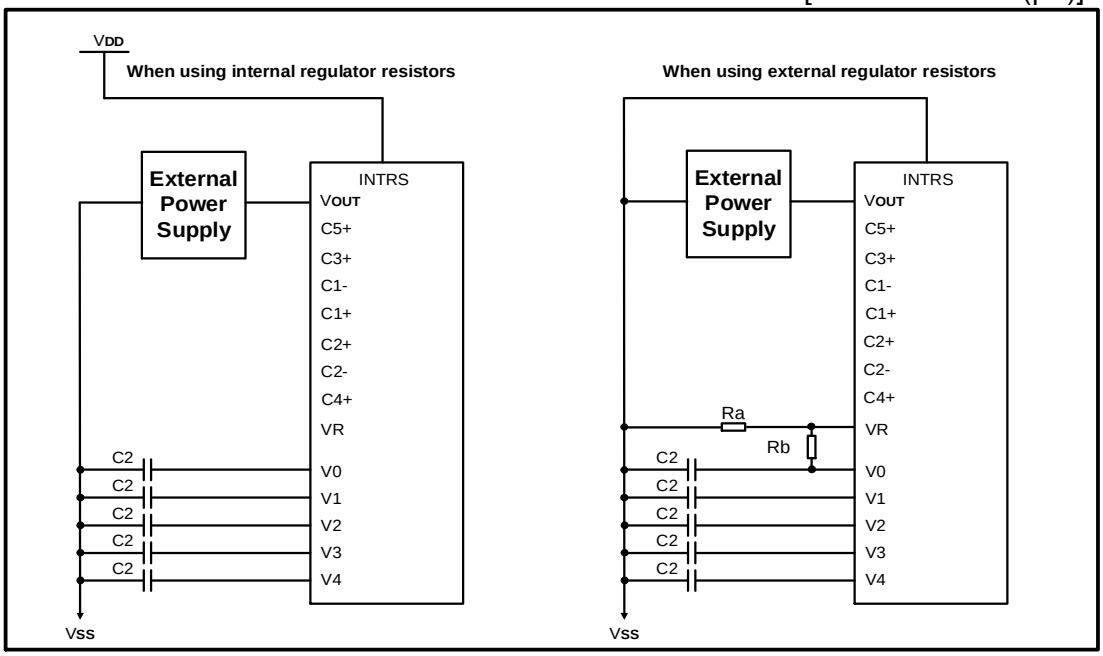


Figure 20. When Using some LCD Power Circuits (V/C: OFF, V/R: ON, V/F: ON)

[C2 = 0.47 ~ 2.0 (μF)]

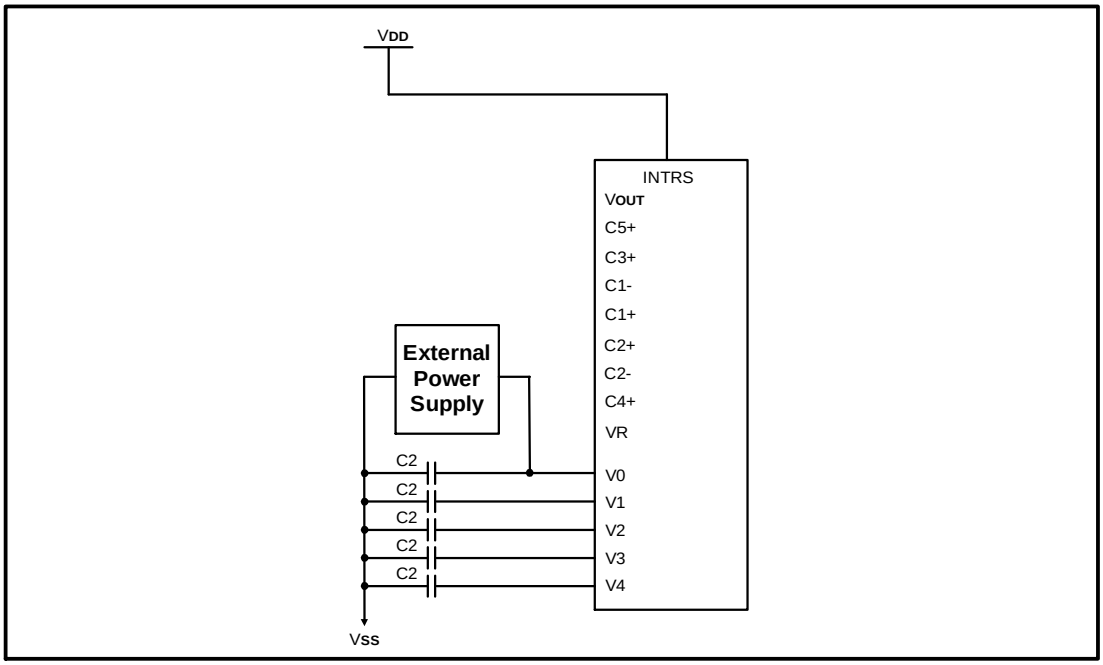


Figure 21. When Using some LCD Power Circuits (V/C: OFF, V/R: OFF, V/F: ON)

[C2 = 0.47 ~ 2.0 (μF)]

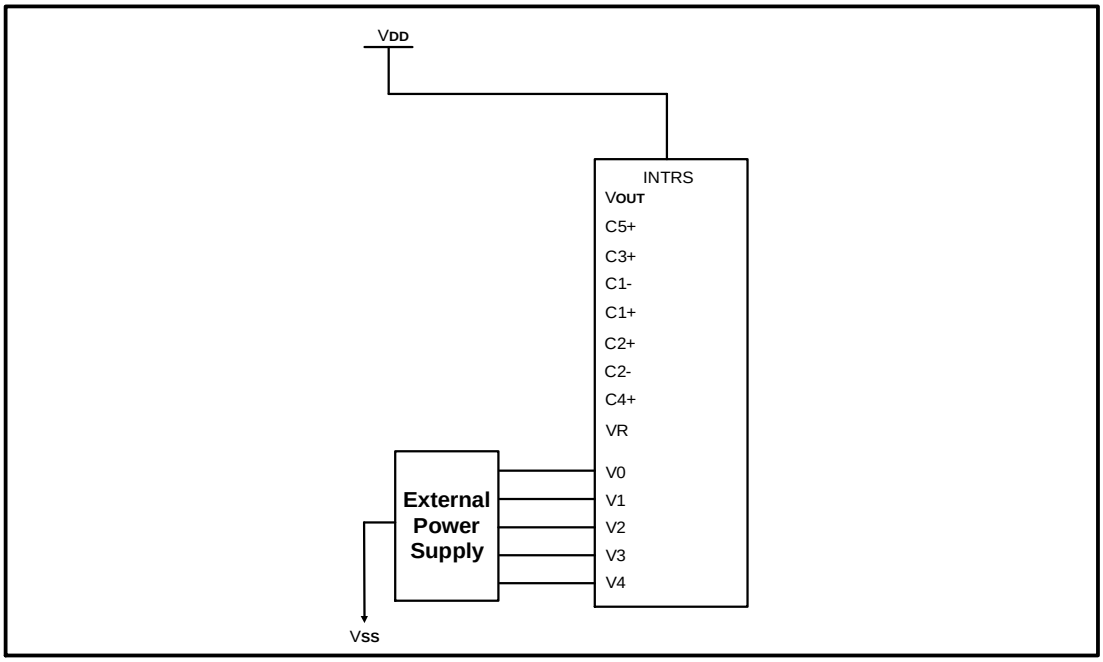


Figure 22. When Not Using any Internal LCD Power Supply Circuits (V/C: OFF, V/R: OFF, V/F: OFF)

17. Reset Circuit

Setting RESETB to “L” or Reset instruction can initialize internal function.
When RESETB becomes “L” , following procedure is occurred.

Page address : 0
Column address : 0
Read-modify-write : OFF
Display ON / OFF : OFF
Initial display line : 0 (first)
Initial COM0 register : 0 (COM 0)
Partial display duty ratio : 1/128
Reverse display ON/OFF : OFF (normal)
N-line inversion register : 0 (disable)
Entire display ON/OFF : OFF (Icon disable)
Icon control register ON/OFF : OFF (Icon disable)
Power control register (VC, VR, VF)= (0,0,0)
DC-DC converter circuit = (0,0)
Regulator resistor select register : (R2,R1,R0) = (0, 0, 0)
Contrast Level : 32
LCD bias ratio : 1/12
COM scan Direction : 0
ADC select : 0
Oscillator : OFF
Power Save Mode : Release
Display Data Length register : 0 (for SPI mode)
White mode set : OFF
White palette register (WG3,WG2,WG1,WG0) = (0, 0, 0, 0)
Light gray mode set : OFF
Light gray palette register (LG3,LG2,LG1,LG0) = (0, 0, 0, 0)
Dark gray mode set : OFF
Dark gray palette register (DG3,DG2,DG1,DG0) = (1, 1, 1, 1)
Black mode set : OFF
Black palette register (BG3,BG2,BG1,BG0) = (1, 1, 1, 1)
FRC, PWM mode : 4FRC, 9PWM

When RESET instruction is issued, following procedure is occurred.

Page address : 0
Column address : 0
Read-modify-write : OFF
Initial display line : 0 (first)
Regulator resistor select register: (R2,R1,R0) = (0, 0, 0,)
Contrast Level : 32
Display Data Length register : 0 (for SPI mode)
White mode set : OFF
White palette register (WG3,WG2,WG1,WG0) = (0, 0, 0, 0)
Light gray mode set : OFF
Light gray palette register (LG3,LG2,LG1,LG0) = (0, 0, 0, 0)
Dark gray mode set : OFF
Dark gray palette register (DG3,DG2,DG1,DG0) = (1, 1, 1, 1)
Black mode set : OFF
Black palette register (BG3,BG2,BG1,BG0) = (1, 1, 1, 1)
FRC, PWM mode : 4FRC, 9PWM

While RESETB is “L” or reset instruciton is executed, no instruction except read status can be accepted. Reset status appears at DB4. After DB4 becomes “ L”,any instruction can be accepted. RESETB must be connected to the reset pin of the MPU, and initialize the MPU and this LSI at the same time. The initialization by RESETB is essential before used.

18. Instruction Description

Table 9. Instruction Table

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Read display data	1	1	Read data								Read data from DDRAM
Write display data	1	0	Write data								Write data into DDRAM
Read status	0	1	BUSY	ON	RES	MF2	MF1	MF0	DS1	DS0	Read the internal status
ICON control register ON/OFF	0	0	1	0	1	0	0	0	1	ICON	ICON=0: ICON disable (default) ICON=1: ICON enable & set the page address to 16
Set page address	0	0	1	0	1	1	P3	P2	P1	P0	Set page address
Set column address MSB	0	0	0	0	0	1	0	Y7	Y6	Y5	Set column address MSB
Set column address LSB	0	0	0	0	0	0	Y4	Y3	Y2	Y1	Set column address LSB
Set modify-read	0	0	1	1	1	0	0	0	0	0	Set modify-read mode
Reset modify-read	0	0	1	1	1	0	1	1	1	0	Release modify-read mode
Display ON/OFF	0	0	1	0	1	0	1	1	1	D	D=0:disply OFF D=1:display ON
Set initial display line register	0	0	0	1	0	0	0	0	×	×	2-byte instruction to specify the initial display line to realize vertical scrolling
	0	0	×	S6	S5	S4	S3	S2	S1	S0	
Set initial COM0 Register	0	0	0	1	0	0	0	1	×	×	2-byte instruction to specify the initial COM0 to realize vertical scrolling
	0	0	×	C6	C5	C4	C3	C2	C1	C0	
Set partial display duty ratio	0	0	0	1	0	0	1	0	×	×	2-byte instruction to set partial display duty ratio
	0	0	D7	D6	D5	D4	D3	D2	D1	D0	
Set N-line inversion	0	0	0	1	0	0	1	1	×	×	2-byte instruction to set N-line inversion register
	0	0	×	×	×	N4	N3	N2	N1	N0	
Release N-line inversion	0	0	1	1	1	0	0	1	0	0	Release N-line inversion mode
Reverse display ON/OFF	0	0	1	0	1	0	0	1	1	REV	REV=0: normal display REV=1:reverse display
Entire display ON/OFF	0	0	1	0	1	0	0	1	0	EON	EON=0:normal display EON=1:entire display ON
Power control	0	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation
Select DC-DC step-up	0	0	0	1	1	0	0	1	DC1	DC0	Select the step-up of the internal voltage converter
Select regulator resistor	0	0	0	0	1	0	0	R2	R1	R0	Select internal resistance ratio of the regulator resistor

Set electronic volume register	0	0	1	0	0	0	0	0	0	1	2-byte instruction to specify the reference voltage
	0	0	×	×	EV5	EV4	EV3	EV2	EV1	EV0	
Select LCD bias	0	0	0	1	0	1	0	B2	B1	B0	Select LCD bias
SHL select	0	0	1	1	0	0	SHL	×	×	×	COM bi-directional selection SHL=0: normal direction SHL=1: reverse direction
ADC select	0	0	1	0	1	0	0	0	0	ADC	SEG bi-directional selection ADC=0: normal direction ADC=1: reverse direction
Oscillator on start	0	0	1	0	1	0	1	0	1	1	Start the built-in Oscillator
Set power save mode	0	0	1	0	1	0	1	0	0	P	P=0: normal mode P=1: sleep mode
Release power save mode	0	0	1	1	1	0	0	0	0	1	Release power save mode
Reset	0	0	1	1	1	0	0	0	1	0	Initialize the internal functions
Set data direction & display data length (DDL)	×	×	1	1	1	0	1	0	0	0	2-byte instruction to specify the number of data bytes
	×	×	D7	D6	D5	D4	D3	D2	D1	D0	
NOP	0	0	1	1	1	0	0	0	1	1	No operation
Test Instruction	0	0	1	1	1	1	×	×	×	×	Don't use this instruction
Set FRC and PWM	0	0	1	0	0	1	0	FRC	PWM1	PWM0	FRC (1:3 FRC,0:4 FRC) PWM1 PWM0 0 0 9PWM 0 1 9PWM 1 0 12PWM 1 1 15PWM
Set white mode and 1st/2nd frame, set pulse width	0	0	1	0	0	0	1	0	0	0	Set white mode and 1st/2nd frame
	0	0	WB3	WB2	WB1	WB0	WA3	WA2	WA1	WA0	
Set white mode and 3rd/4th frame, set pulse width	0	0	1	0	0	0	1	0	0	1	Set white mode and 3rd/4th frame
	0	0	WD3	WD2	WD1	WD0	WC3	WC2	WC1	WC0	
Set light gray mode and 1st/2nd frame, set pulse width	0	0	1	0	0	0	1	0	1	0	Set light gray mode and 1st/2nd frame
	0	0	LB3	LB2	LB1	LB0	LA3	LA2	LA1	LA0	
Set light gray mode and 3rd/4th frame, set pulse width	0	0	1	0	0	0	1	0	1	1	Set light gray mode and 3rd/4th frame
	0	0	LD3	LD2	LD1	LD0	LC3	LC2	LC1	LC0	

Set dark gray mode and 1st/2nd frame, set pulse width	0	0	1	0	0	0	1	1	0	0	Set dark gray mode and 1st/2nd frame
	0	0	DB3	DB2	DB1	DB0	DA3	DA2	DA1	DA0	
Set dark gray mode and 3rd/4th frame, set pulse width	0	0	1	0	0	0	1	1	0	1	Set dark gray mode and 3rd/4th frame
	0	0	DD3	DD2	DD1	DD0	DC3	DC2	DC1	DC0	
Set black mode and 1st/2nd frame, set pulse width	0	0	1	0	0	0	1	1	1	0	Set black mode and 1st/2nd frame
	0	0	BB3	BB2	BB1	BB0	BA3	BA2	BA1	BA0	
Set black mode and 3rd/4th frame, set pulse width	0	0	1	0	0	0	1	1	1	1	Set black mode and 3rd/4th frame
	0	0	BD3	BD2	BD1	BD0	BC3	BC2	BC1	BC0	

1. Read Display Data

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Read Data							

8-bit data from Display Data RAM specified by the column address and page address can be read by this instruction. As the column address is increased by 1 automatically after each this instruction, the microprocessor can continuously read data from the addressed page. A dummy read is required after loading an address into the column address register. Display Data cannot be red through the serial interface.

2. Write Display Data

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	Write Data							

8-bit data of Display Data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page.During auto-increasement, the column address wraps to 0 after the last column is written.

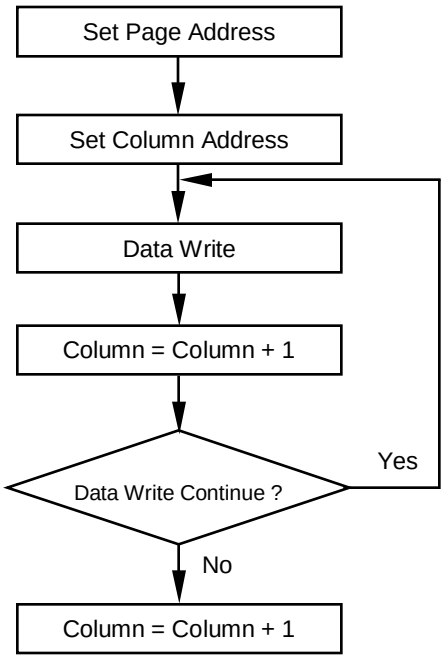


Figure 23. Sequence for Writing Display Data

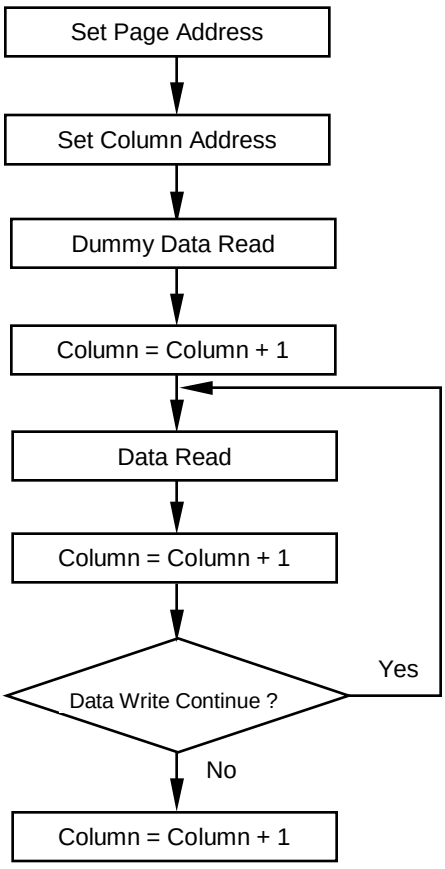


Figure 24. Sequence for Reading Display Data

3. Read Status

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BUSY	ON/OFF	RES	0	0	0	1	0

Flag	Description
BUSY	The device is busy when internal operation or reset. Any instruction is rejected until BUSY goes Low. 0:Chip is active, 1:Chip is being busy.
ON / OFF	Indicates display ON/OFF status. 0: display OFF, 1:display ON
RESET	Indicates the initialization is in progress by RESET signal. 0: Chip is active, 1:Chip is being reset.

Indicates the internal staus of the NT7506

4. ICON Control Register ON/OFF

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	1	Icon

This instruciton makes ICON enable or Disable. By default, ICON display is disabled (ICON = 0). When ICON control register is set to “1”, ICON display is enabled and page address is set to “16”. Then user can write data for icons. It is impossible toet the page address to “16” by Set Page Address instruction. Therefore, when writing data for icons, ICON control register ON instruction would be used to set the page address to “16”. When ICON control register is set to “0”, Icon display is disabled.
ICON=0: ICON disable (default)
ICON=1: ICON enable & set the page address to 16

5. Set Page Address

Sets the Page Address of display data RAM from the microprocessor into the page address register. Any RAM data bit can be accessed when its Page Address and column address are specified. Along with the column address, the Page Address defines the address of the display RAM to write or read display data. Changing the Page Address doesn’t effect to the display status. Set Page Address instruction can not be used to set the page address to “16”. Use ICON control register ON/OFF instruction to set the page address to “16” .

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	P3	P2	01	P0

P3	P2	P1	P0	Page
0	0	0	0	0
0	0	0	1	1
:	:	:	:	:
1	1	1	0	14
1	1	1	1	15

6. Set Column Address

Sets the column address of display RAM from the microprocessor into the column address register. Along with the column address, the column address defines the address of the display RAM to write or read display data. When the microprocessor reads or writes display datra to or from display RAM, column address are automatically increased.

Set Column Address MSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	0	Y7	Y6	Y5

Set Column Address LSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	Y4	Y3	Y2	Y1

Y7	Y6	Y5	Y4	Y3	Y2	Y1	Column Address [Y7:Y1]
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	126
1	1	1	1	1	1	1	127

7. Set Modify – Read

The instruction stops the automatic increment of the column address by the read display data instruction, but the column address is still increased by the write display data instruction. And it reduces the load of microprocessor when the data of a specific area is repeatedly changed during cursor blinking or others. This mode is canceled by the reset Modify-Read instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	0

8. Reset Modify – Read

The instruction cancels the modify-read mode. And makes the column address return to its initial value just before the set modify-read instruction is started.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	1	1	0

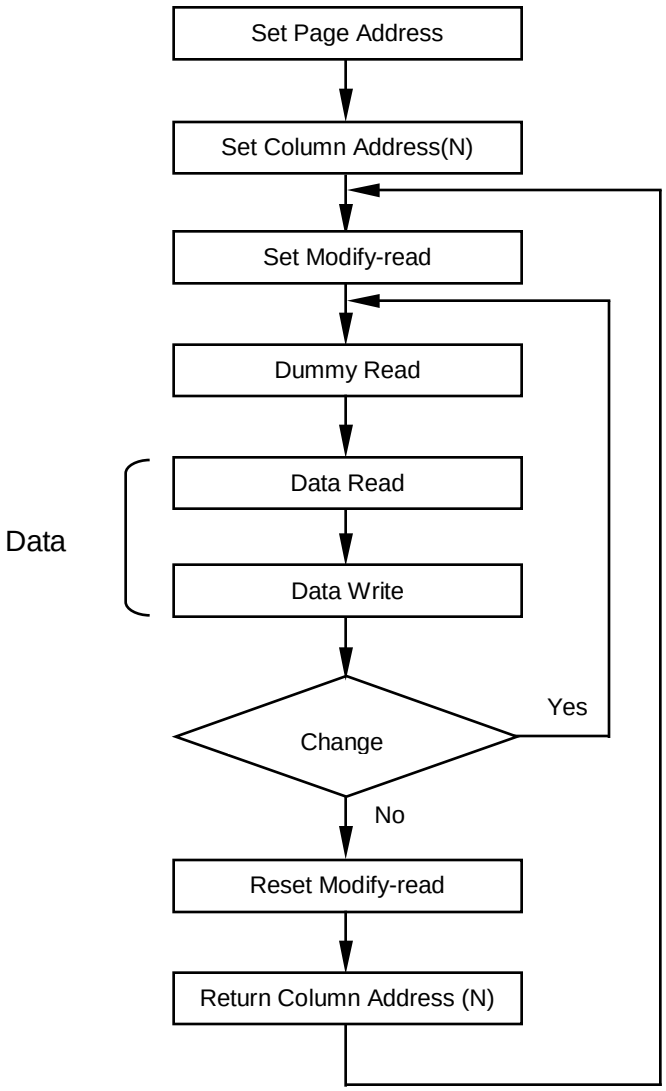


Figure 25. Sequence for Cursor Display

9. Display ON/OFF

Turns the display ON or OFF
This command has priority over Entire Display On/Off and Reverse Display On/Off. Commands are accepted while the display is off, but the visual state of the display does not change.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	1	DON

DON = 1 : Display ON
DON = 0 : Display OFF

10. Set Initial Display Line Register

Set the line address of display RAM to determine the initial display line using 2-byte instruciton. The RAM display data is displayed at the top of row(Com0) of LCD panel.

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	0	0	×	×

The 2nd instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	S6	S5	S4	S3	S2	S1	S0

S6	S5	S4	S3	S2	S1	S0	Line Address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
:	:	:	:	:	:	:	:
1	1	1	1	1	0	0	124
1	1	1	1	1	0	1	125
1	1	1	1	1	1	0	126
1	1	1	1	1	1	1	127

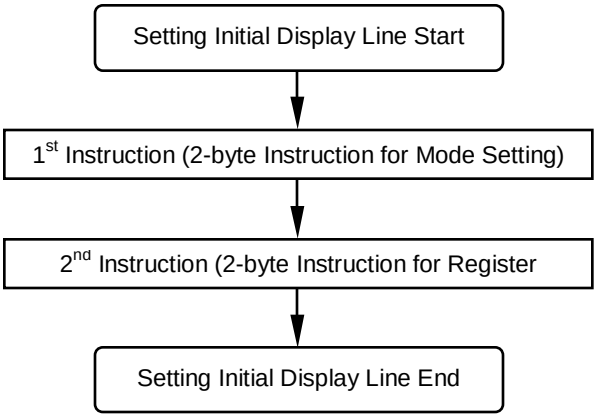


Figure 26. The Sequence for setting the Initial Display Line

11. Set Initial COM0 Register

Sets the initila row (com) of the LCD panel using the 2-byte instruction. By using this instruction, it is possible to realize the window moving without the change of display data.

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	0	1	×	×

The 2nd instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	C6	C5	C4	C3	C2	C1	C0

C6	C5	C4	C3	C2	C1	C0	Line Address
0	0	0	0	0	0	0	COM 0
0	0	0	0	0	0	1	COM 1
0	0	0	0	0	1	0	COM 2
0	0	0	0	0	1	1	COM 3
:	:	:	:	:	:	:	:
1	1	1	1	1	0	0	COM 124
1	1	1	1	1	0	1	COM 125
1	1	1	1	1	1	0	COM 126
1	1	1	1	1	1	1	COM 127

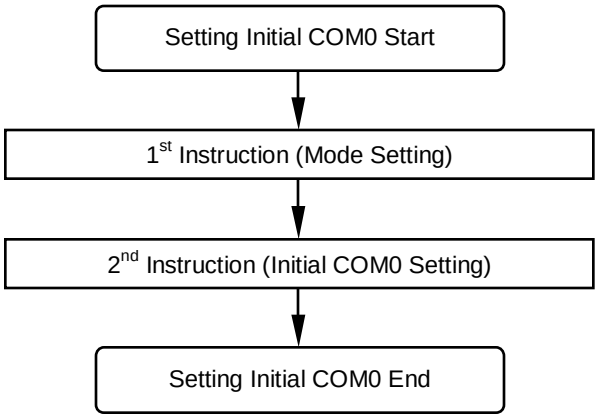


Figure 27. Sequence for Setting the Initial COM0

12. Set Partial Display Duty Ratio

Sets the duty ratio within range of 16 to 128 (ICON disabled) or 17 to 129 (ICON enabled) to realize partial display by using the 2-byte instruction.

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	1	0	×	×

The 2nd instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	D7	D6	D5	D4	D3	D2	D1	D0

D7	D6	D5	D4	D3	D2	D1	D0	Selected partial duty ratio (ICON disabled)	Selected partial duty ratio (ICON enabled)
0	0	0	0	0	0	0	0	No Operation	No Operation
:	:	:	:	:	:	:	:		
0	0	0	0	1	1	1	1		
0	0	0	1	0	0	0	0	1/16	1/17
0	0	0	1	0	0	0	1	1/17	1/18
:	:	:	:	:	:	:	:	:	:
0	1	1	1	1	1	1	1	1/127	1/128
1	0	0	0	0	0	0	0	1/128	1/129
1	0	0	0	0	0	0	1	No operation	No operation
:	:	:	:	:	:	:	:		
1	1	1	1	1	1	1	1		

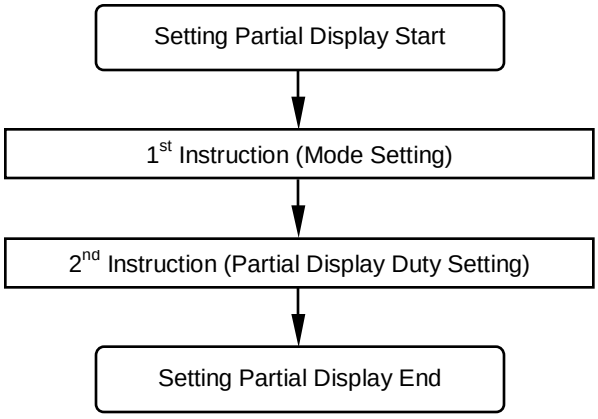


Figure 28. Sequence for Setting Partial Display

13. Set N-line Inversion Registr

Sets the inverted line number within range of 3 to 33 to improve the display quality by controlling the phase of the internal LCD AC signal (M) by using the 2-byte instruction.
The DC-bias problem could be occourred if K is even number. So, we recommend customers to set K to be odd number.
K : D / N
D : The number of display duty ratio (D is selectable by customers)
N : N for N-line inversion (N is selectable by customers)

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	1	1	×	×

The 2nd instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	×	×	N4	N3	N2	N1	N0

N4	N3	N2	N1	N0	Selected n-line inversion
0	0	0	0	0	0-line inversion (frame inversion)
0	0	0	0	1	3-line inversion
0	0	0	1	0	4-line inversion
0	0	0	1	1	5-line inversion
:	:	:	:	:	:
1	1	1	0	1	31-line inversion
1	1	1	1	0	32-line inversion
1	1	1	1	1	33-line inversion

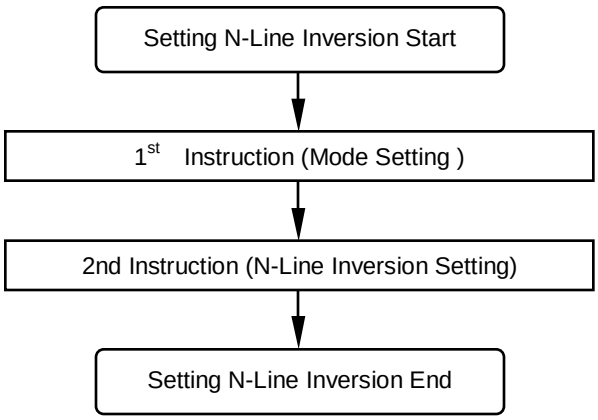


Figure 29. Sequence for N-line Inversion

14. Release N-line Inversion

Returns to the frame inversion condition from the n-line inversion condition.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	1	0	0

15. Reverse Display ON/OFF

Reverses the display status on LCD panel without rewriting the contents of the display data RAM.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	1	REV

REV	DD RAM data = “00” (White)	DD RAM data = “01” (Light Gray)	DD RAM data = ”10” (Dark Gray)	DD RAM data = “ 11” (DARK)
0 (normal)	White (“00”)	Light Gray (“01”)	Dark Gray (“10”)	Dark (“11”)
1 (reverse)	Dark (“11”)	Dark Gray (“10”)	Light Gray (“01”)	White (“00”)

16. Entire Display ON/OFF

Forces the whole LCD points to be turned on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held. This instruction has priorty over the Reverse Display ON/OFF instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	0	EON

EON	DD RAM data = “00” (White)	DD RAM data = “01” (Light Gray)	DD RAM data = ”10” (Dark Gray)	DD RAM data = “ 11” (DARK)
0 (normal)	White (“00”)	Light Gray (“01”)	Dark Gray (“10”)	Black (“11”)
1 (entire)	Black (“11”)	Black (“11”)	Black (“11”)	Black (“11”)

17. Power Control

Select one of eight power circuit functions by using 3-bit register. An external power supply and part of internal power supply functions can be used simultaneously.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	1	VC	VR	VF

V/C	V/R	V/F	Status of internal power supply circuits
0			Internal voltage converter circuit is OFF
1			Internal voltage converter circuit is ON
	0		Internal voltage regulator circuit is OFF
	1		Internal voltage regulator circuit is ON
		0	Internal voltage follower circuit is OFF
		1	Internal voltage follower circuit is ON

18. Select DC-DC Set-Up

Selects one of 4 DC-DC step-up to reduce the power consumption by this instruction. It is very useful to realize the partial display functin.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	0	0	1	DC1	DC0

DC1	DC0	Select DC-DC converter circuit
0	0	3 times boosting circuit
0	1	4 times boosting circuit
1	0	5 times boosting circuit
1	1	6 times boosting circuit

19. Select Regulator Resistor

Selects resistance ratio of the internal resistor used in the internal voltage regulator. See voltage regulator section in power supply circuit. Refer to the table **.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	0	R2	R1	R0

R2	R1	R0	1 + (Rb / Ra)
0	0	0	2.3
0	0	1	3.0
0	1	0	3.7
0	1	1	4.4
1	0	0	5.1
1	0	1	5.8
1	1	0	6.5
1	1	1	7.2

20. Set Electronic Volumn Register

Consist of 2-byte instructins
The 1st instruction set Reference Voltage mode, the 2nd one updates the contents of reference voltage register. After second instruction, Reference Voltage mode is released.
The 1st Instruction: Set Reference Voltage Select Mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	1

The 2nd instruction :Set Reference Voltage Register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	×	EV5	EV4	EV3	EV2	EV1	EV0

EV5	EV4	EV3	EV2	EV1	EV0	Reference voltage parameter (α)
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

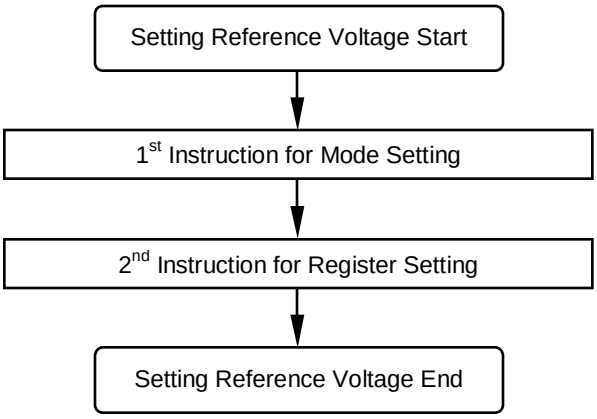


Figure 30. Sequence for Setting the Electronic Volume

21. Select LCD Bias

Selects LCD bias ratio of the voltage required for driving the LCD.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	1	0	B2	B1	B0

B2	B1	B0	LCD bias
0	0	0	1/5
0	0	1	1/6
0	1	0	1/7
0	1	1	1/8
1	0	0	1/9
1	0	1	1/10
1	1	0	1/11
1	1	1	1/12

22. SHL Select

COM output scanning direction is select by this instruction which determines the LCD driver output staus.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	SHL	×	×	×

SHL = “0” : normal direction (COM0 → COM127)
SHL = “1” : reverse direction (COM127 → COM0)

23. ADC Select

Changes the relationship between RAM column address and segment driver. The direction of segment driver output pins could be reversed by software. This makes IC layout flexible in LCD module assembly.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	ADC

ADC = “0” : normal direction (SEG0 → SEG127)
ADC = “1” : reverse direction (SEG127 → SEG0)

24. Oscilliator On Start

This instruction enales the built in Oscillator circuit.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	1

25. Power Save

The NT7506 enters the power save status to reduce the power consumption to the static power consumption value and returns to the normal operation status by the following instructions.

Set Power Save Mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	P

P = “0” : normal mode
P = “1” : sleep mode

Release Power Save Mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	1

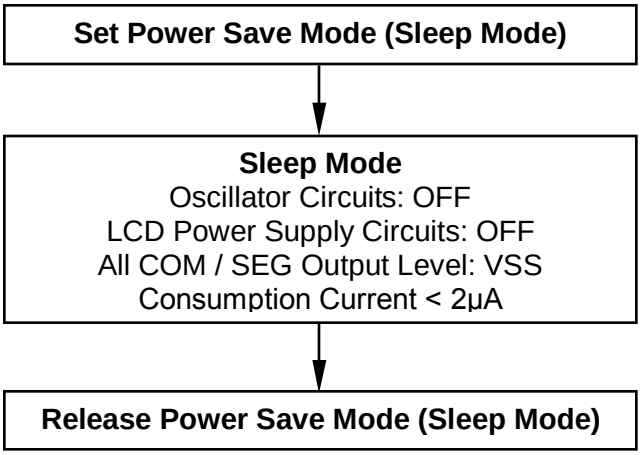


Figure 31. Power Save Routine

26. Reset

This instruction resets initial display line, column address, page address, and common output status select to their initial status, but does not affect the contents of display data RAM. This instruction cannot initialize the LCD power supply, which is initialized by the RESETB pin.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	0

27. Set Data Direction & Display Data Length (3-PIN SPI Mode)

Consists of 2 bytes instruciton.
This command is used in 3-pin SPI mode only(PS0 = “L” and PS1 = “L”). It will be two continuous commands, the first byte control the data direction(write mode only) and inform the LCD driver the second byte will be number of data bytes will be write. When RS is not used, the Display Data Length instruction is used to indicate that a specified number of display data bytes are to be transmitted. The next byte after the display string is handled as command data.

The 1st Instruction: Set Data Direction (Only Write Mode)

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
×	×	1	1	1	0	1	0	0	0

The 2nd Instruction: Set Display Data Length (DDL) Register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
×	×	D7	D6	D5	D4	D3	D2	D1	D0

D7	D6	D5	D4	D3	D2	D1	D0	Display Data Length
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	1	0	3
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	1	254
1	1	1	1	1	1	1	0	255
1	1	1	1	1	1	1	1	256

28. Nop

No operation

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	1

29. Test I Instruction

This instruction is for testing IC. Please do not use this pin.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	×	×	×	×

30. Set PWM & FRC mode

Select 3 / 4 FRC and 9 / 12 / 15 PWM.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	FRC	PWM1	PWM0

FRC	PWM1	PWM0	Status of PWM & FRC
0			4 FRC
1			3 FRC
	0	0	9 PWM
	0	1	9 PWM
	1	0	12 PWM
	1	1	15 PWM

31. Set Gray Scale Mode & Register

Consists of 2 bytes instruction. The first byte sets grayscale mode and the second byte updates the contents of gray scale register without issuing any other instruction.
Set Gray Scale Mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	1	GM2	GM1	GM0

GM2	GM1	GM0	Description
0	0	0	In case of setting white mode and 1st/2nd frame
0	0	1	In case of setting white mode and 3rd /4th frame
0	1	0	In case of setting light gray mode and 1st/2nd frame
0	1	1	In case of setting light gray mode and 3rd /4th frame
1	0	0	In case of setting dark gray mode and 1st/2nd frame
1	0	1	In case of setting dark gray mode and 3rd /4th frame
1	1	0	In case of setting black mode and 1st/2nd frame
1	1	1	In case of setting black mode and 3rd /4th frame

Set Gray Scale Register

RS	RW	DB 7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	GB3	GB2	GB1	GB0	GA3	GA2	GA1	GA0
0	0	GD3	GD2	GD1	GD0	GC3	GC2	GC1	GC0

GA3, GB3 GC3, GD3	GA2, GB2 GC2, GD2	GA1, GB1 GC1, GD1	GA0, GB0 GC0, GD0	Pulse width (9PWM)	Pulse width (12PWM)	Pulse width (15PWM)
0	0	0	0	0 / 9	0 / 12	0 / 15
0	0	0	1	1 / 9	1 / 12	1 / 15
:	:	:	:	:	:	:
1	0	0	1	9 / 9	9 / 12	9 / 15
1	0	1	0	0 / 9	10 / 12	10 / 15
1	0	1	1	0 / 9	11 / 12	11 / 15
1	1	0	0	0 / 9	12 / 12	12 / 15
1	1	0	1	0 / 9	0 / 12	13 / 15
1	1	1	0	0 / 9	0 / 12	14 / 15
1	1	1	1	0 / 9	0 / 12	15 / 15

GA3= WA3, LA3, DA3, BA3 GA2= WA2, LA2, DA3, BA2 GA1=WA1, LA1, DA1, BA1 GA0= WA0, LA0, DA0, BA0
GB3= WB3, LB3, DB3, BB3 GA2= WB2,LB2,DB2,BB2 GA1=WB1, LB1, DB1, BB1 GA0= WB0, LB0, DB0, BB0
GC3= WC3, LC3, DC3, BC3 GA2= WC2,LC2,DC2,BC2 GA1=WC1,LC1,DC1,BC1 GA0= WD0,LD0, DD0, BD0
GD3= WD3, LD3, DD3, BD3 GA2=WD2,LD2,DD2,BD2 GA1=WD1, LD1, DD1, BD1 GA0= WD0,LD0, DD0, BD0

Referential Instruction Set-up Flow: Initializing with the built-in Power Supply Circuits

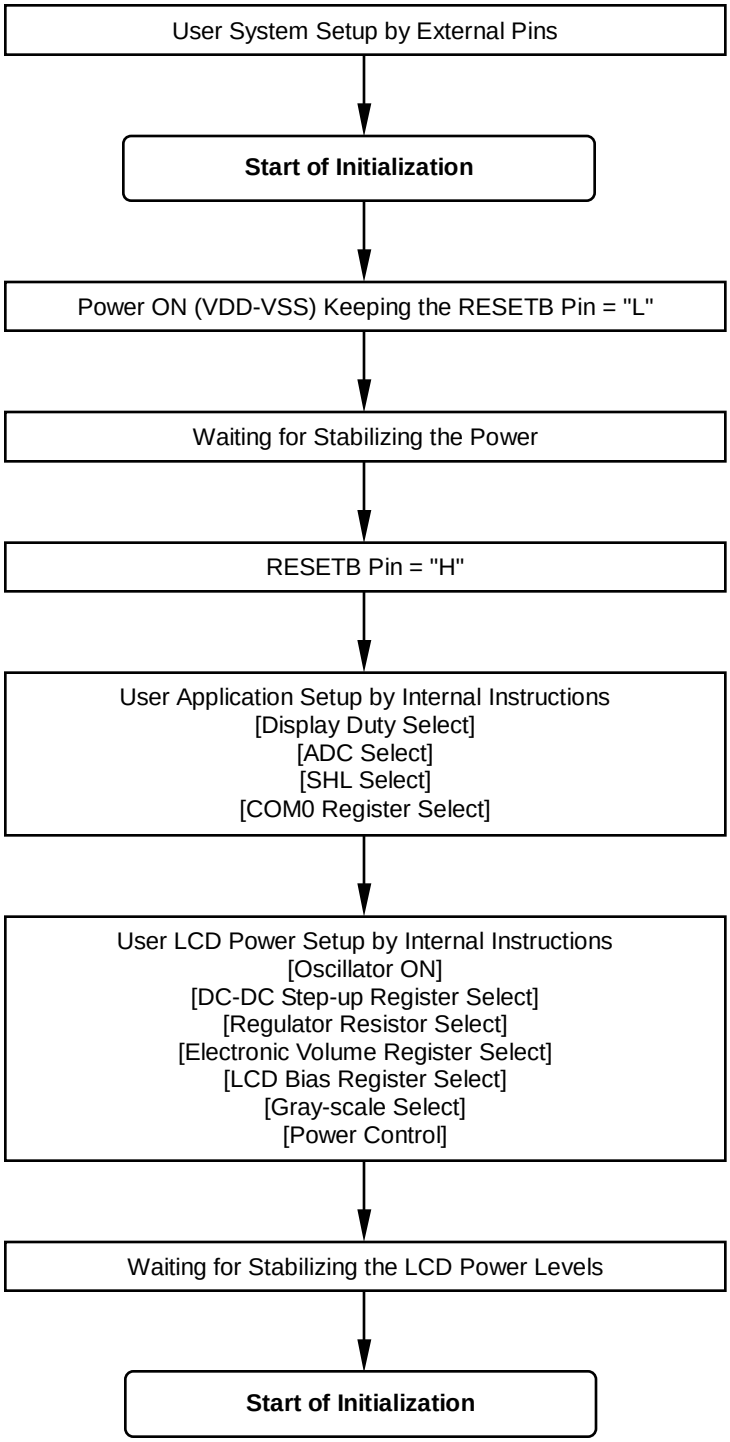


Figure 32. Initializing with the Built-in Power Supply Circuits

Referential Instruction Set-up Flow: Initializing without the built-in Power Supply Circuits

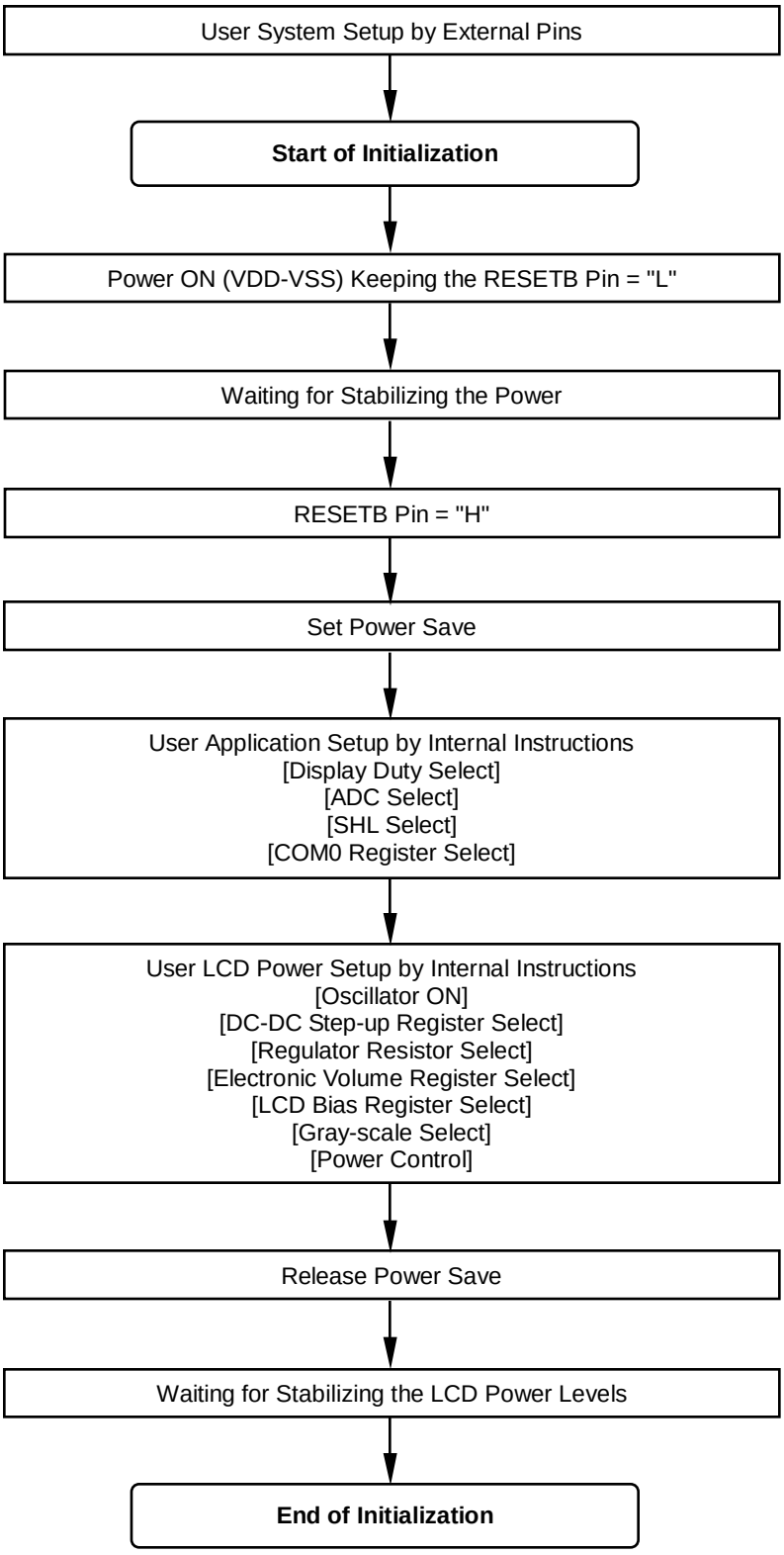


Figure 33. Initializing without the Built-in Power Supply Circuits

Referential Instruction Set-up Flow: Data Displaying

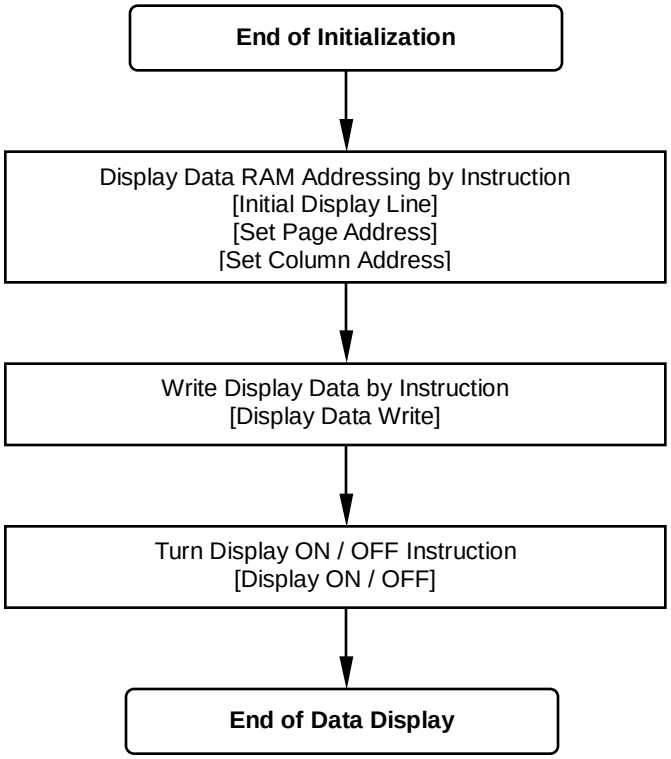


Figure 34. Data Displaying

Referential Instruction Set-up Flow: Power OFF

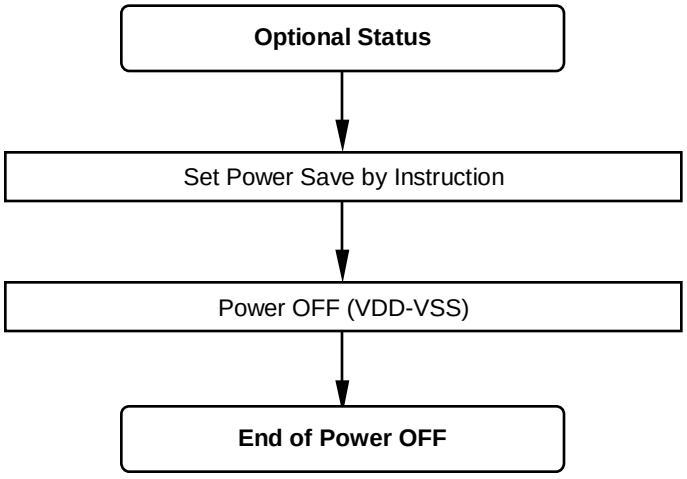


Figure 35. Power OFF

Referential Instruction Set-up Flow: Partial Duty Changing

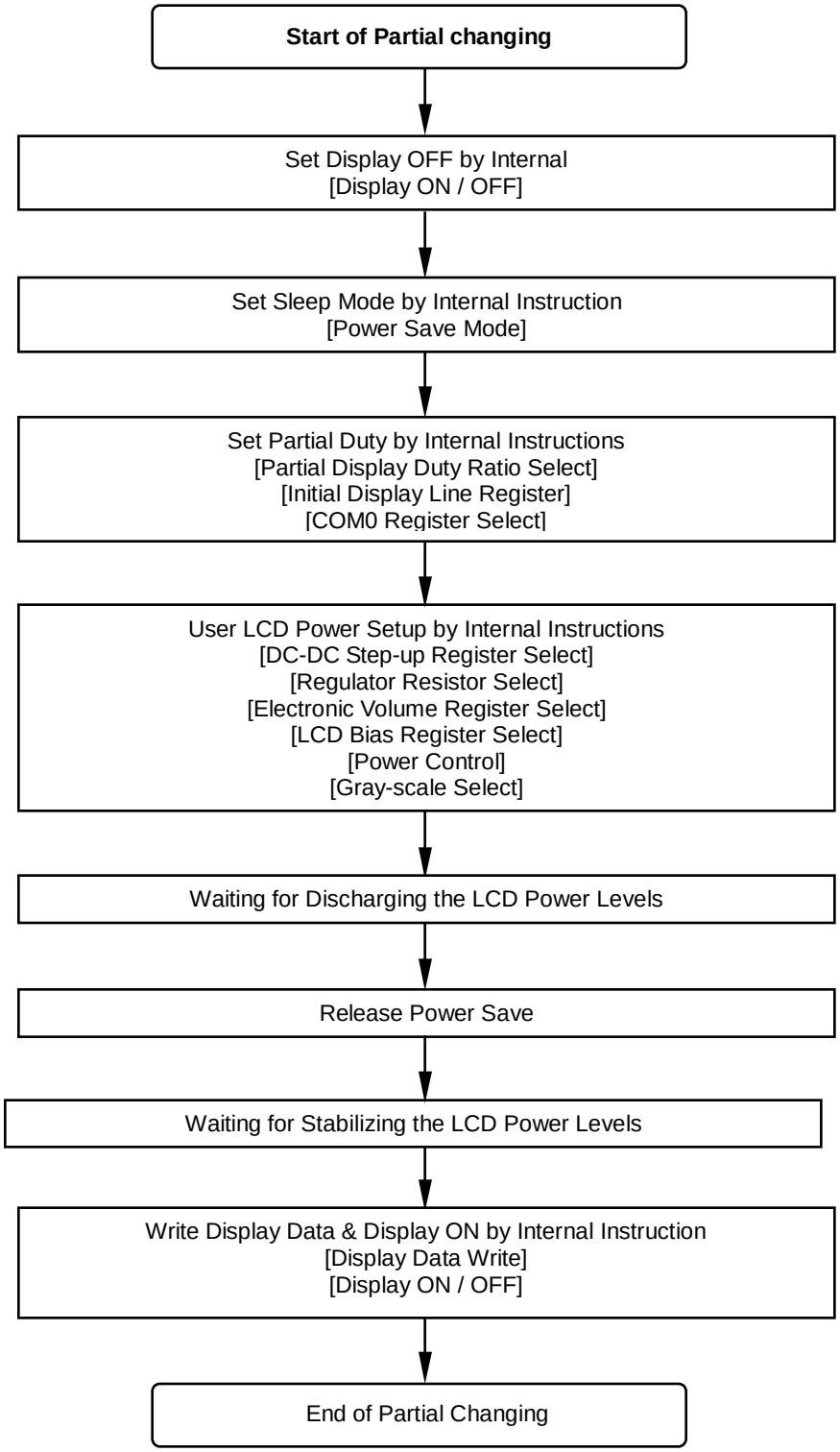


Figure 36. Partial Duty Changing

Absolute Maximum Rating*

Supply Voltage Range (VDD). . . . . -0.3V to +7.0V

Supply Voltage Range (V0,VOUT). . . . . -0.3V to +17.0V

Supply Voltage Range (V1,V2,V3,V4). . . . . -0.3V to V0+0.3V

External Reference Voltage . . . . . +0.3V to VDD

Input Voltage Range . . . . . –0.3 to VDD+0.3V

Operating Temperature Range . . . . . -40°C to +85°C

Storage Temperature Range . . . . . -55°C to +125°C

Notes:
1. VDD, V0, VOUT, V1 to V4 and VEXT based on VSS=0V
2. Voltage V0≧V1≧V2≧V3≧V4≧VSS must always be satisfied. (VLCD=V0-VSS)
3. If supply voltage exceeds its absolute maximum range, this LSI may be damaged permanently. It is desirable to use this LSI under electrical characteristic conditions during general operation. Otherwise, this LSI may malfunction or reduced LSI reliability may result.

DC Characteristics

Symbol	Parameters	Min.	Typ.	Max.	Unit	Conditions
VDD	Operating Voltage (1)	1.8	-	3.3	V	
V_0	Operating Voltage(2)	4.0	-	15.0	V	
V_{IH}	Input Voltage	0.8VDD	-	VDD	V	
V_{IL}		VSS	-	0.2 VDD		
V_{OH}	Output Voltage	0.8 VDD	-	VDD	V	IOH = -0.5mA
V_{OL}		VSS	-	0.2 VDD		IOL = -0.5mA
I_{IL}	Input Leakage Current	-1.0	-	+1.0	μA	VIN=VDD or VSS
I_{OZ}	Output Leakage Current	-3.0	-	+3.0	μA	VIN=VDD or VSS
R_{ON}	LCD Drive ON Resistance	-	2.0	3.0	KΩ	Ta=25℃,V0=8V
f_{FR}	Operating Frequency	90	105	120	Hz	Ta=25°C 1/128Duty,9PWM REXT=620KΩ
V_{CI}	Voltage Converter Input Voltage	1.8	-	5.0	V	×3
		1.8	-	3.75		×4
		1.8	-	3.0		×5
		1.8	-	2.5		×6
V_{OUT}	Voltage Converter Output Voltage	95	99	-	%	×3/×4/×5/×6 voltage conversion (no load)
V_{OUT}	Voltage Regulator Operating Voltage	5.4	-	15.0	V	
V_0	Voltage Follower Operating Voltage	4.0	-	15.0	V	
V_{REF}	Reference Voltage	2.04	2.10	2.16	V	Ta = 25°C

Table 11. DC Characteristics

Dynamic Current Consumption When The Internal Power Supply is ON

Symbol	Parameters	Min.	Typ.	Max.	Unit	Conditions
IDD	Dynamic Current Consumption	-	100	150	μA	V0-VSS=12.0V,x5 Boosting, Duty=1/128, Normal Mode (Display off)
		-	200	300	μA	V0-VSS=12.0V,x5 Boosting, Duty=1/128, Normal Mode (Display on, Checker Pattern)

Table 12. Dynamic Current 2 (Internal Power)

Current Consumption during Power Save Mode

Symbol	Parameters	Min.	Typ.	Max.	Unit	Conditions
IDDS1	Sleep mode current	-	-	2	μA	During Sleep

Table 13. Power Save Mode Current

Relationship between Oscillation Frequency and Frame Frequency

Duty Ratio	Item	fCL	fOSC1
I / N	On-Chip Oscillator circuit is used	$f_{FR} \times N$	$f_{FR} \times PWM \times 2 \times N$

(fOSC1: Oscillation frequency, fCL: display clock frequency, fFR: frame frequency, N = 16 to 129)

Table 14. The Relationship between Oscillation Frequency and Frame Frequency

[Remark Solves]

1. Though the wide range of operating voltages is guaranteed, a spike voltage change may affect the voltage assurance during access from the MPU.
2. In case of external power supply is applied.
3. CSB, RS, DB0 to DB7, E_RD, RW_WR, RESETB, PS0, PS1, INTRS and REF
4. DB0 to DB7
5. Applies when the DB0 to DB7 pins are in high impedance.
6. Resistance value when -0.1[mA] is applied during the ON status of the output pin SEGn or COMn.
   RON [kΩ] = ΔV[V] / 0.1[mA] (ΔV : voltage change when -0.1[mA] is applied in the ON status.)
7. See Table 23 for the relationship between Oscillation frequency and frame frequency.
8. The voltage regulator circuit adjusts V0 within the voltage follower operating voltage range.
9. On-chip reference voltage source of the voltage regulator circuit to adjust V0.
10. Applies to the case where the on-chip Oscillation circuit is used and no access is made from the MPU.
    The current consumption, when the built-in power supply circuit is ON.
    The current flowing through voltage regulation resistors (Rb and Ra) is not included.
    It does not include the current of the LCD panel capacity, wiring capacity, etc.
    Other conditions are 1/12 bias, 3 FRC, 9 PWM, Frame inversion, Frame freq. = 105HZ, BL=(9,9,9,0), DG=(6,6,6,0), LG=(3,3,3,0), WH=(0,0,0,0).
11. Applies when PWM method is used.
    When both PWM and FRC method are used, frame frequency should be increased up to more than 130Hz. So, Oscillator resistor value between OSC1 and VDD pin should be reduced.

AC Characteristics

Read / Write Characteristics (8080-series MPU)

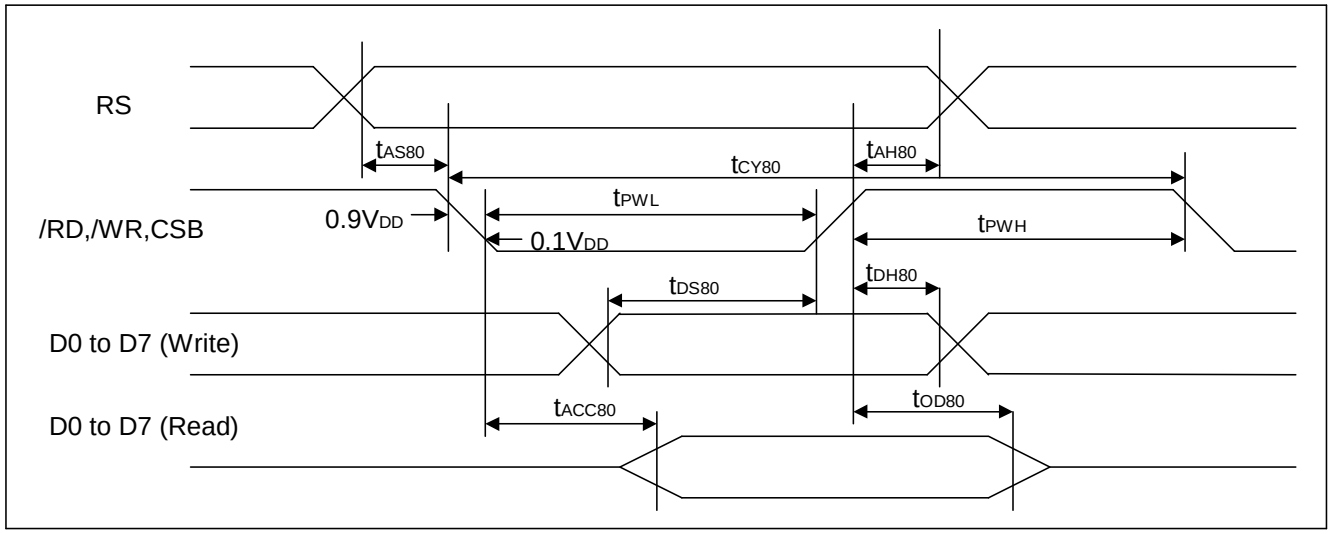


Figure 37. Read / Write Characteristics (8080-series MPU)

(VDD = 1.8V, Ta=-40 ~ 85°C)

Symbol	Signal	Parameters	Min.	Typ.	Max.	Unit	Conditions
t_{AS80}	RS	Address setup time	0		-	ns	
t_{AH80}		Address hold time	0		-	ns	
t_{CY80}		System cycle time for write	150		-	ns	
t_{CY80}		System cycle time for read	330		-	ns	
t_{PWL}	/WR	Pulse width low	60		-	ns	
t_{PWH}	/RD	Pulse width time	60		-	ns	
t_{DS80}	DB0 to DB7	Data setup time	40		-	ns	
t_{DH80}		Data hold time	10		-	ns	
t_{ACC80}		Read access time	15		-	ns	CL=100pF
t_{OD80}		Output disable time	10		50	ns	

(VDD = 2.7V, Ta=-40 ~ 85°C)

Symbol	Signal	Parameters	Min.	Typ.	Max.	Unit	Conditions
t_{AS80}	RS	Address setup time	0		-	ns	
t_{AH80}		Address hold time	0		-	ns	
t_{CY80}		System cycle time for write	100		-	ns	
t_{CY80}		System cycle time for read	166		-	ns	
t_{PWL}	/WR /RD	Pulse width low	40		-	ns	
t_{PWH}		Pulse width time	40		-	ns	
t_{DS80}	DB0 to DB7	Data setup time	30		-	ns	
t_{DH80}		Data hold time	5		-	ns	
t_{ACC80}		Read access time	15		-	ns	CL=100pF
t_{OD80}		Output disable time	10		50	ns	

Read / Write Characteristics (6800-series MPU)

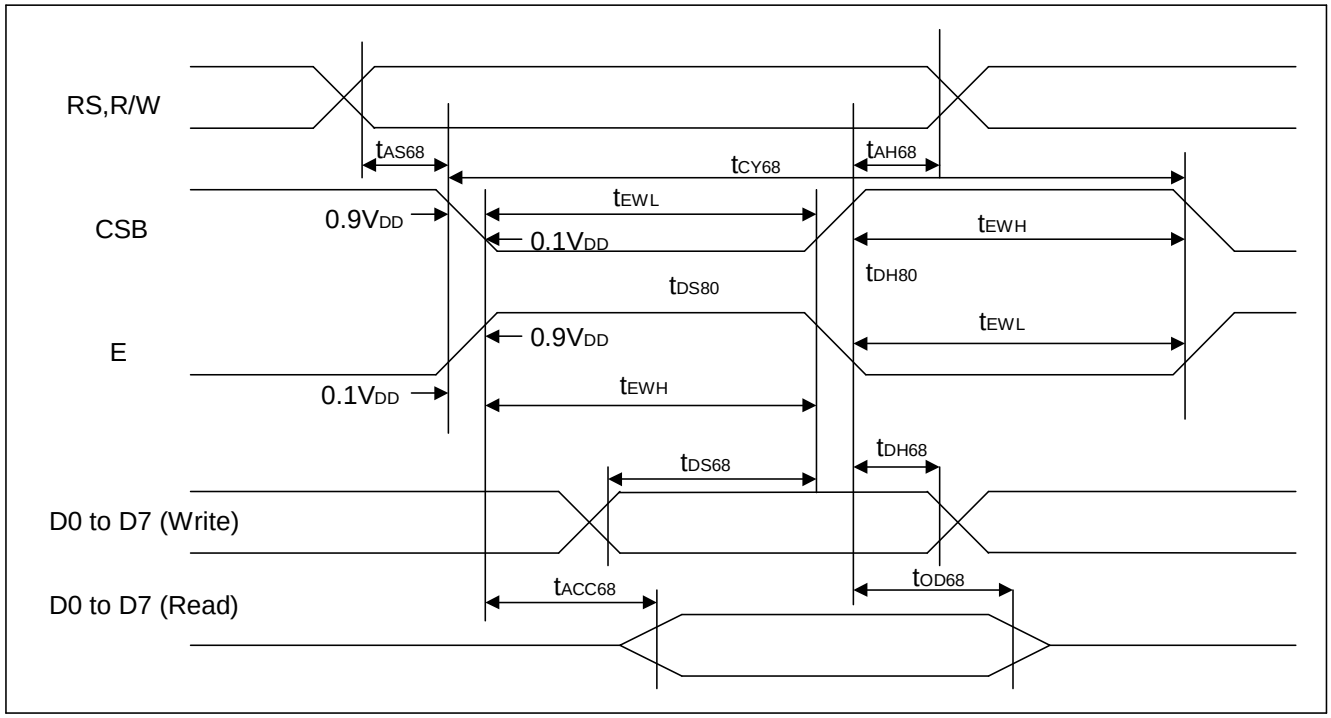


Figure 38. Read / Write Characteristics (6800-series Microprocessor)

(VDD = 1.8V, Ta=-40 ~ 85℃)

Symbol	Signal	Parameters	Min.	Typ.	Max.	Unit	Conditions
t_{AS68}	RS	Address setup time	0		-	ns	
t_{AH68}	RW	Address hold time	0		-	ns	
t_{CY68}		System cycle time for write	150		-	ns	
t_{CY68}		System cycle time for read	330		-	ns	
t_{EWH}	E_RD	Pulse width low	60		-	ns	
t_{EWL}	(E)	Pulse width time	60		-	ns	
t_{DS68}	DB0 to DB7	Data setup time	40		-	ns	
t_{DH68}		Data hold time	10		-	ns	
t_{ACC68}		Read access time	15		-	ns	CL=100pF
t_{OD68}		Output disable time	10		50	ns	

(VDD = 2.7V, Ta=-40 ~ 85℃)

Symbol	Signal	Parameters	Min.	Typ.	Max.	Unit	Conditions
t_{AS68}	RS	Address setup time	0		-	ns	
t_{AH68}	RW	Address hold time	0		-	ns	
t_{CY68}		System cycle time for write	100		-	ns	
t_{CY68}		System cycle time for read	166		-	ns	
t_{EWH}	E_RD	Pulse width low	40		-	ns	
t_{EWL}	(E)	Pulse width time	40		-	ns	
t_{DS68}	DB0 to DB7	Data setup time	30		-	ns	
t_{DH68}		Data hold time	5		-	ns	
t_{ACC68}		Read access time	15		-	ns	CL=100pF
t_{OD68}		Output disable time	10		50	ns	

Serial Interface Characteristics

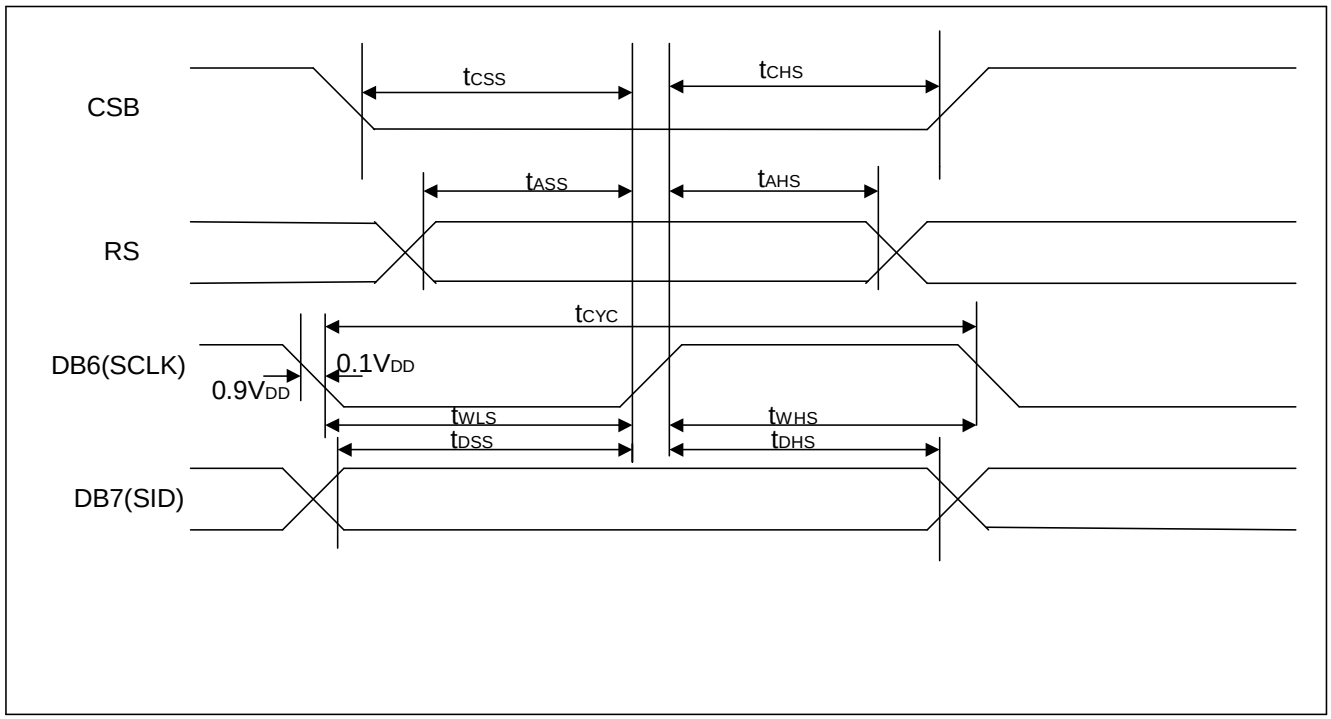


Figure 39. Serial Interface Characteristics

(VDD = 1.8V, Ta=-40 ~ 85℃)

Symbol	Signal	Parameters	Min.	Typ.	Max.	Unit	Conditions
t_{CYS}	DB6 (SCLK)	Serial clock cycle	111		-	ns	
t_{WHS}		SCLK high pulse width	60		-	ns	
t_{WLS}		SCLK low pulse width	60		-	ns	
t_{ASS}	RS	Address setup time	60		-	ns	
t_{AHS}		Address hold time	60		-	ns	
t_{DSS}	DB7 (SID)	Data setup time	60		-	ns	
T_{dhs}		Data hold time	60		-	ns	
t_{CCS}	CSB	CSB setup time	60		-	ns	
t_{CHS}		CSB hold time	1/2 * t_{CYS}		-	ns	

(VDD = 2.7V, Ta=-40 ~ 85℃)

Symbol	Signal	Parameters	Min.	Typ.	Max.	Unit	Conditions
t_{CYS}	DB6 (SCLK)	Serial clock cycle	53.8		-	ns	
t_{WHS}		SCLK high pulse width	30		-	ns	
t_{WLS}		SCLK low pulse width	30		-	ns	
t_{ASS}	RS	Address setup time	30		-	ns	
t_{AHS}		Address hold time	30		-	ns	
t_{DSS}	DB7 (SID)	Data setup time	30		-	ns	
T_{dhs}		Data hold time	30		-	ns	
t_{CCS}	CSB	CSB setup time	30		-	ns	
t_{CHS}		CSB hold time	1/2 * t_{CYS}		-	ns	

Reset Input Timing

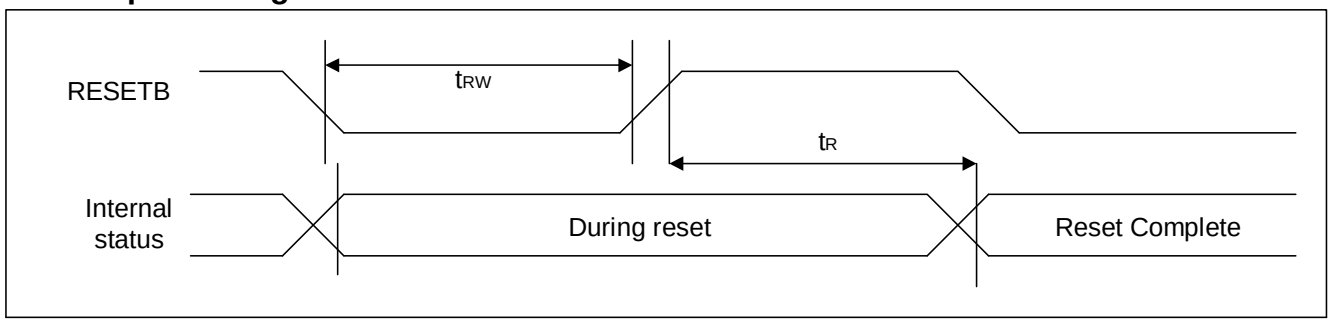


Figure 40. Reset Input Timing

(VDD=1.8 ~ 3.3V, Ta=-40~+85℃)

Symbol	Signal	Parameters	Min.	Typ.	Max.	Unit	Conditions
t_{RW}	RESETB	Reset low pulse width	10		-	μs	
t_R	-	Reset time	-		1000	ns	

Microprocessor Interface (for reference only)

In Case of Interfacing with 8080-series (PS0 = “H”, PS1 = “L”)

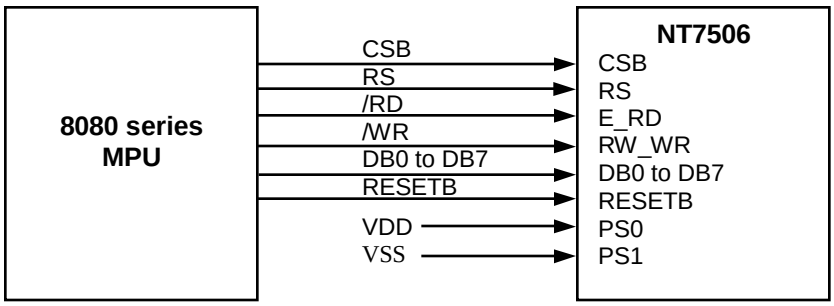


Figure 41. Interfacing with 8080-series (PS0 = “H”, PS1 = “L”)

In Case of Interfacing with 6800-series (PS0 = “H”, PS1 = “H”)

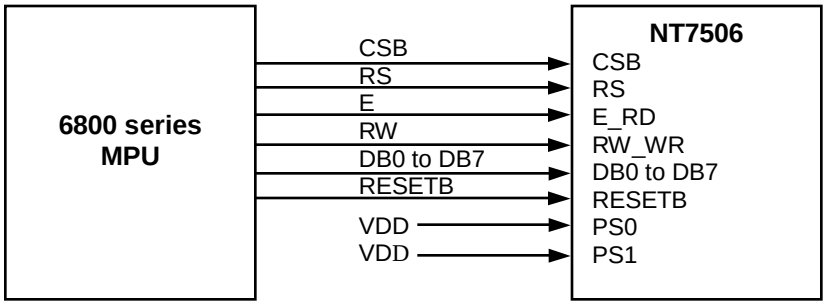


Figure 42. Interfacing with 6800-series (PS0 = “H”, PS1 = “H”)

In Case of 4-pin SPI mode (PS0 = "L" , PS1 = "H")

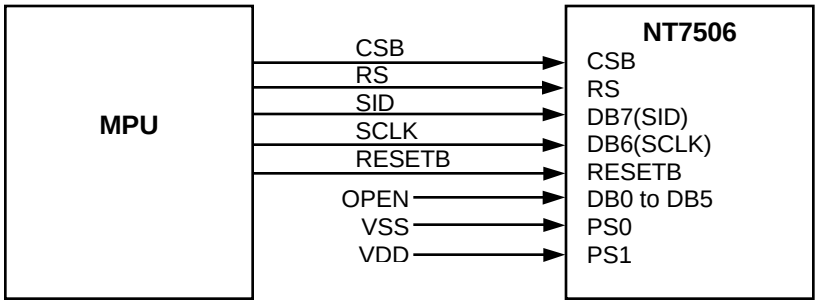


Figure 43. Serial Interface (PS0 = “L”, PS1 = “H”)

In Case of 3-pin SPI mode (PS0 = "L" , PS1 = "L")

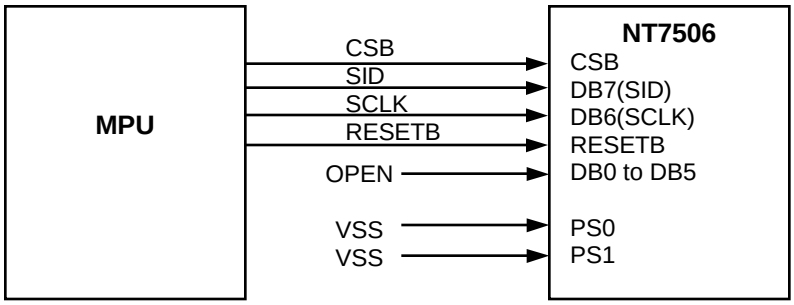


Figure 44. Serial Interface (PS0 = “L”, PS1 = “L”)

Connections Between NT7506 And LCD Panel
Single Chip Configuration (1/129 Duty Configurations)

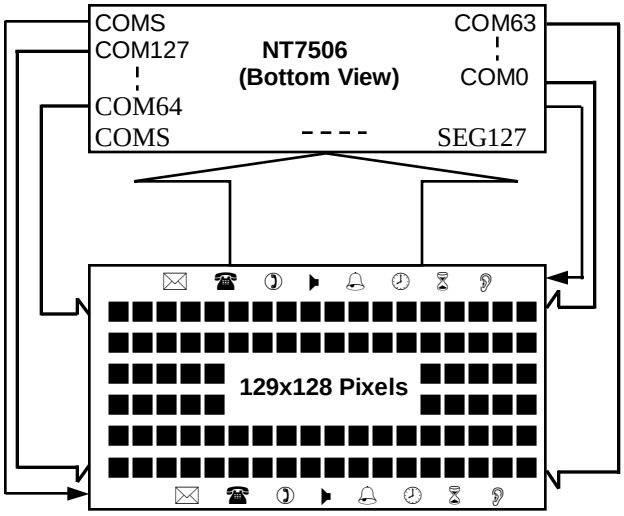


Figure 45. SHL = 0, ADC = 1

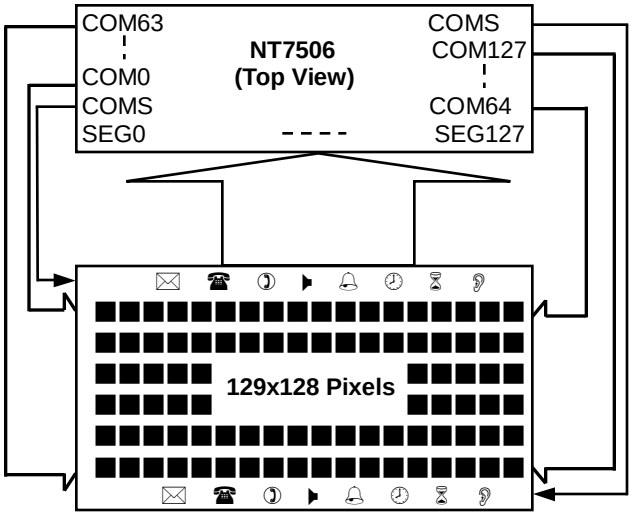


Figure 46. SHL = 0, ADC = 0

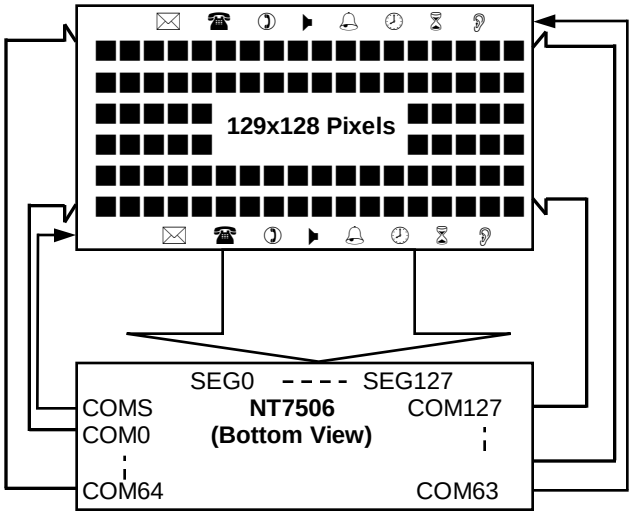


Figure 47. SHL = 1, ADC = 0

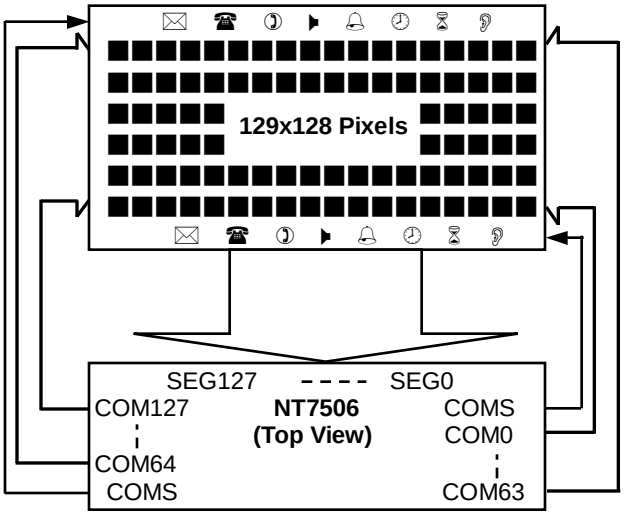
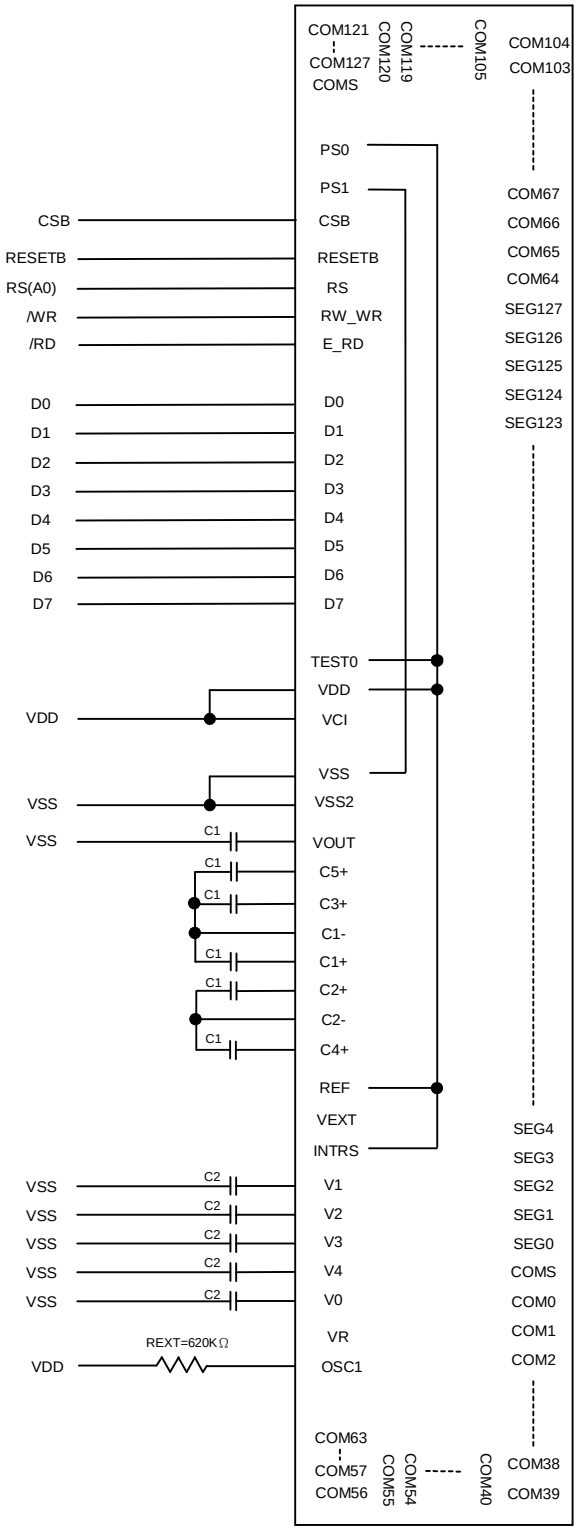


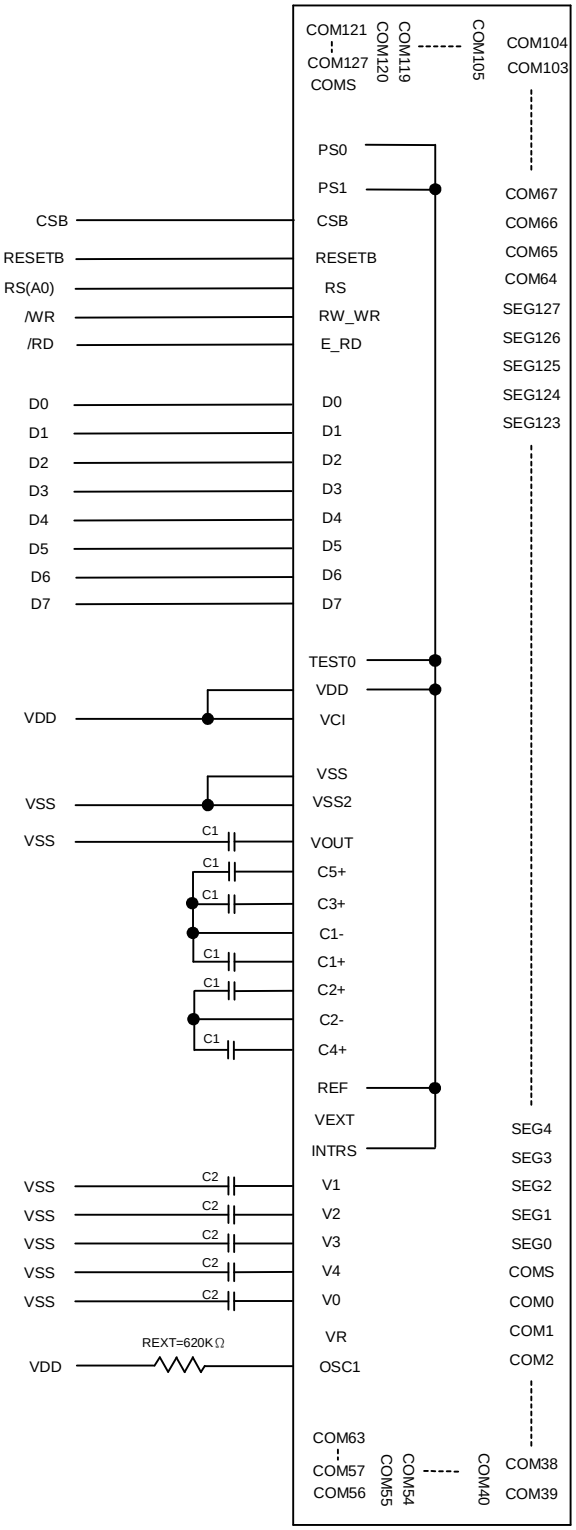
Figure 48. SHL = 1, ADC = 1

Application information for Pin Connection to MPU (for reference only)

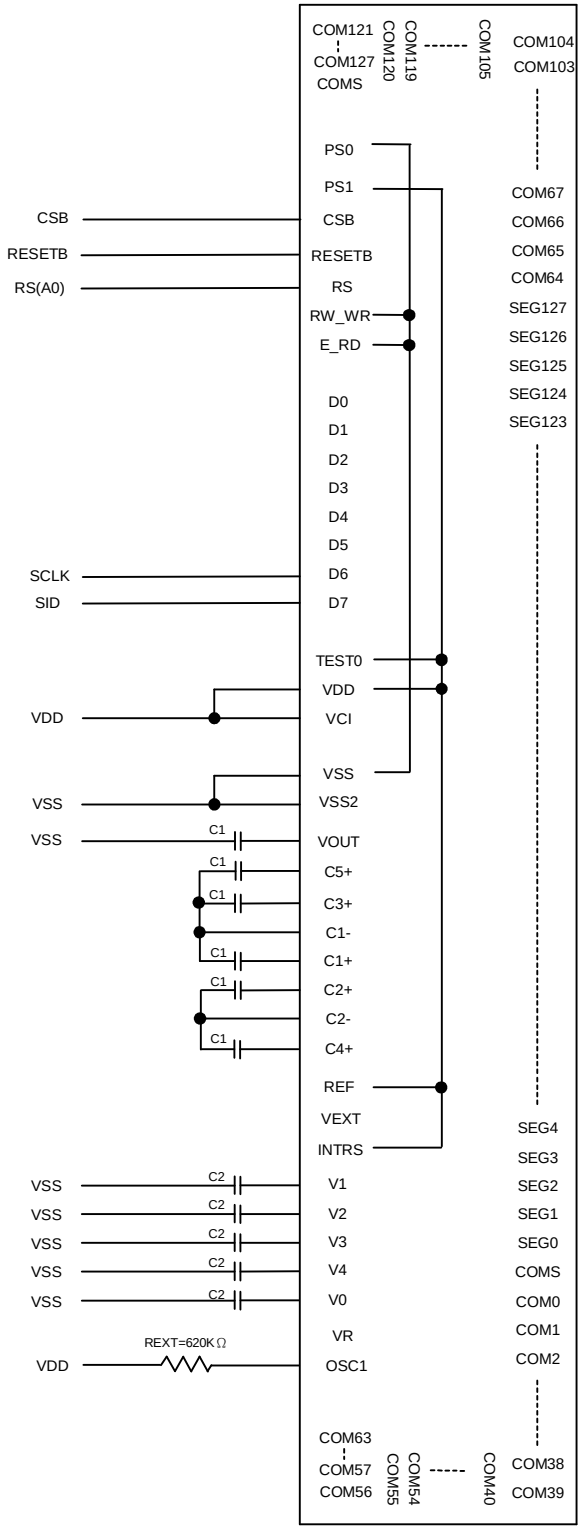
1. 8080 MPU Mode: (PS0, 1 = 10, 1/128duty, Internal OSC, REF = 1: Internal VREF, INTRS = 1 : Internal Ra/Rb, x6 pump, C1 = 1.0 ~ 4.7 µF, C2 = 0.47 ~ 2.0 µF)



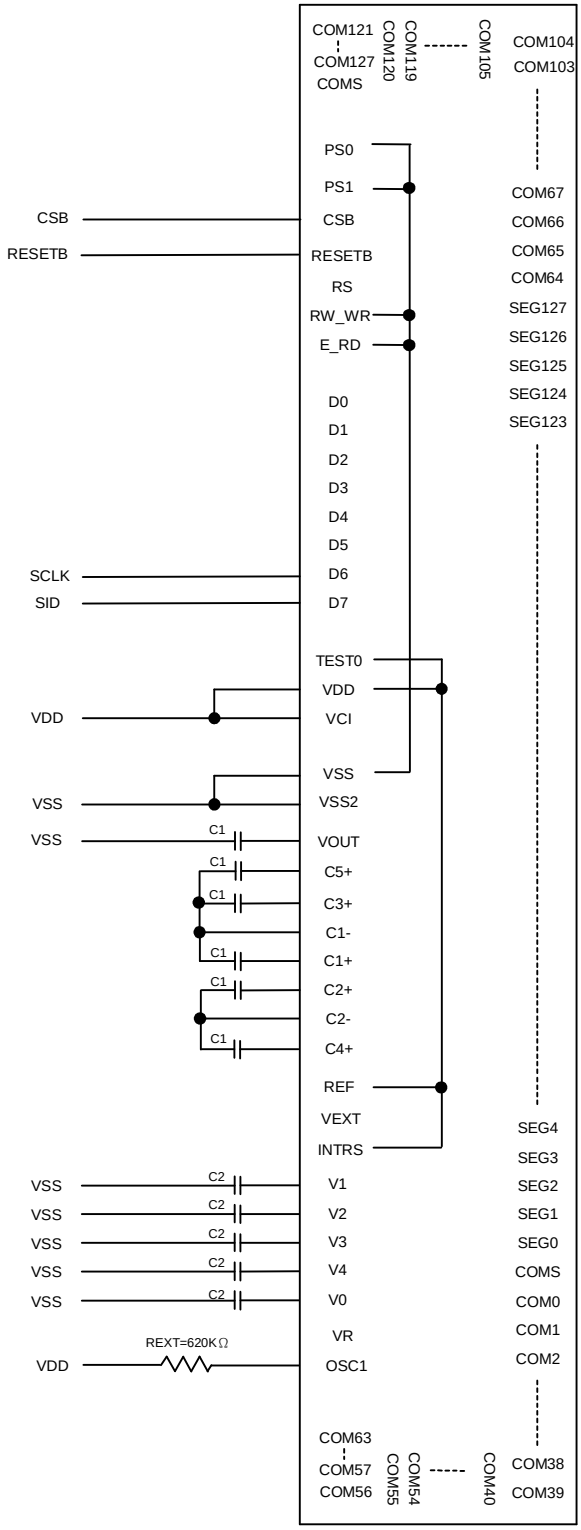
2. 6800 MPU Mode: (PS0, 1 = 11, 1/128duty, Internal OSC, REF = 1: Internal VREF, INTRS = 1 : Internal Ra/Rb, x6 pump, C1 = 1.0 ~ 4.7 µF, C2 = 0.47 ~ 2.0 µF)



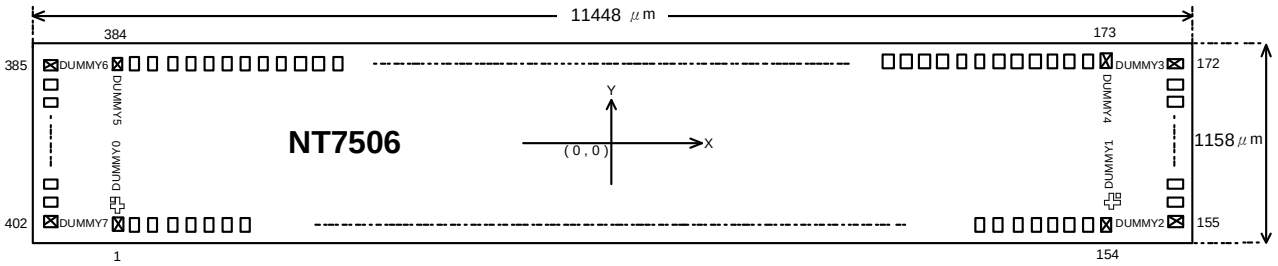
3. 4 pin Serial Mode: (PS0, 1 = 01, 1/128duty, Internal OSC, REF = 1: Internal VREF, INTRS = 1 : Internal Ra/Rb, x6 pump, C1 = 1.0 ~ 4.7 µF, C2 = 0.47 ~ 2.0 µF)



4. 3 pin Serial Mode: (PS0, 1 = 00, 1/128duty, Internal OSC, REF = 1: Internal VREF, INTRS = 1 : Internal Ra/Rb, x6 pump, C1 = 1.0 ~ 4.7 µF, C2 = 0.47 ~ 2.0 µF)



Bonding Diagram



Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	DUMMY0	-5295.00	-453.00	31	NC	-3220.00	-453.00
2	COM121	-5225.00	-453.00	32	DB1	-3150.00	-453.00
3	COM122	-5175.00	-453.00	33	DB1	-3080.00	-453.00
4	COM123	-5125.00	-453.00	34	NC	-3010.00	-453.00
5	COM124	-5075.00	-453.00	35	DB2	-2940.00	-453.00
6	COM125	-5025.00	-453.00	36	DB2	-2870.00	-453.00
7	COM126	-4975.00	-453.00	37	NC	-2800.00	-453.00
8	COM127	-4925.00	-453.00	38	DB3	-2730.00	-453.00
9	COMS1	-4875.00	-453.00	39	DB3	-2660.00	-453.00
10	VSS	-4760.00	-453.00	40	NC	-2590.00	-453.00
11	PS0	-4690.00	-453.00	41	DB4	-2520.00	-453.00
12	PS0	-4620.00	-453.00	42	DB4	-2450.00	-453.00
13	VDD	-4550.00	-453.00	43	NC	-2380.00	-453.00
14	PS1	-4480.00	-453.00	44	DB5	-2310.00	-453.00
15	PS1	-4410.00	-453.00	45	DB5	-2240.00	-453.00
16	VSS	-4340.00	-453.00	46	NC	-2170.00	-453.00
17	CSB	-4270.00	-453.00	47	DB6	-2100.00	-453.00
18	CSB	-4200.00	-453.00	48	DB6	-2030.00	-453.00
19	RESETB	-4060.00	-453.00	49	NC	-1960.00	-453.00
20	VDD	-3990.00	-453.00	50	DB7	-1890.00	-453.00
21	RS	-3920.00	-453.00	51	DB7	-1820.00	-453.00
22	RS	-3850.00	-453.00	52	NC	-1750.00	-453.00
23	RW_WR	-3780.00	-453.00	53	NC	-1680.00	-453.00
24	RW_WR	-3710.00	-453.00	54	NC	-1610.00	-453.00
25	VSS	-3640.00	-453.00	55	NC	-1540.00	-453.00
26	E_RD	-3570.00	-453.00	56	NC	-1470.00	-453.00
27	E_RD	-3500.00	-453.00	57	NC	-1400.00	-453.00
28	NC	-3430.00	-453.00	58	NC	-1330.00	-453.00
29	DB0	-3360.00	-453.00	59	NC	-1260.00	-453.00
30	DB0	-3290.00	-453.00	60	NC	-1190.00	-453.00

Bonding Diagram (continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
61	TEST0	-1120.00	-453.00	100	C1+	1610.00	-453.00
62	VDD	-1050.00	-453.00	101	C1+	1680.00	-453.00
63	VDD	-980.00	-453.00	102	C1+	1750.00	-453.00
64	VDD	-910.00	-453.00	103	C2+	1820.00	-453.00
65	VDD	-840.00	-453.00	104	C2+	1890.00	-453.00
66	VDD	-770.00	-453.00	105	C2+	1960.00	-453.00
67	VCI	-700.00	-453.00	106	C2+	2030.00	-453.00
68	VCI	-630.00	-453.00	107	C2-	2100.00	-453.00
69	VCI	-560.00	-453.00	108	C2-	2170.00	-453.00
70	VCI	-490.00	-453.00	109	C2-	2240.00	-453.00
71	VCI	-420.00	-453.00	110	C2-	2310.00	-453.00
72	VSS	-350.00	-453.00	111	C4+	2380.00	-453.00
73	VSS	-280.00	-453.00	112	C4+	2450.00	-453.00
74	VSS	-210.00	-453.00	113	C4+	2520.00	-453.00
75	VSS	-140.00	-453.00	114	C4+	2590.00	-453.00
76	VSS	-70.00	-453.00	115	NC	2660.00	-453.00
77	VSS	0.00	-453.00	116	VDD	2730.00	-453.00
78	VSS2	70.00	-453.00	117	REF	2800.00	-453.00
79	VSS2	140.00	-453.00	118	VSS	2870.00	-453.00
80	VSS2	210.00	-453.00	119	VEXT	2940.00	-453.00
81	VSS2	280.00	-453.00	120	VDD	3010.00	-453.00
82	NC	350.00	-453.00	121	INTRS	3080.00	-453.00
83	VOUT	420.00	-453.00	122	VSS	3150.00	-453.00
84	VOUT	490.00	-453.00	123	NC	3220.00	-453.00
85	VOUT	560.00	-453.00	124	V4	3290.00	-453.00
86	VOUT	630.00	-453.00	125	V4	3360.00	-453.00
87	C5+	700.00	-453.00	126	V4	3430.00	-453.00
88	C5+	770.00	-453.00	127	V3	3500.00	-453.00
89	C5+	840.00	-453.00	128	V3	3570.00	-453.00
90	C5+	910.00	-453.00	129	V3	3640.00	-453.00
91	C3+	980.00	-453.00	130	V2	3710.00	-453.00
92	C3+:	1050.00	-453.00	131	V2	3780.00	-453.00
93	C3+:	1120.00	-453.00	132	V2	3850.00	-453.00
94	C3+	1190.00	-453.00	133	V1	3920.00	-453.00
95	C1-	1260.00	-453.00	134	V1	3990.00	-453.00
96	C1-	1330.00	-453.00	135	V1	4060.00	-453.00
97	C1-	1400.00	-453.00	136	V0	4130.00	-453.00
98	C1-	1470.00	-453.00	137	V0	4200.00	-453.00
99	C1+	1540.00	-453.00	138	V0	4270.00	-453.00

Bonding Diagram (continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
139	NC	4340.00	-453.00	177	COM36	5075.00	453.00
140	VR	4410.00	-453.00	178	COM35	5025.00	453.00
141	VR	4480.00	-453.00	179	COM34	4975.00	453.00
142	VSS	4550.00	-453.00	180	COM33	4925.00	453.00
143	VDD	4620.00	-453.00	181	COM32	4875.00	453.00
144	OSC1	4690.00	-453.00	182	COM31	4825.00	453.00
145	OSC1	4760.00	-453.00	183	COM30	4775.00	453.00
146	COM63	4875.00	-453.00	184	COM29	4725.00	453.00
147	COM62	4925.00	-453.00	185	COM28	4675.00	453.00
148	COM61	4975.00	-453.00	186	COM27	4625.00	453.00
149	COM60	5025.00	-453.00	187	COM26	4575.00	453.00
150	COM59	5075.00	-453.00	188	COM25	4525.00	453.00
151	COM58	5125.00	-453.00	189	COM24	4475.00	453.00
152	COM57	5175.00	-453.00	190	COM23	4425.00	453.00
153	COM56	5225.00	-453.00	191	COM22	4375.00	453.00
154	DUMMY1	5295.00	-453.00	192	COM21	4325.00	453.00
155	DUMMY2	5598.50	-445.00	193	COM20	4275.00	453.00
156	COM55	5598.50	-375.00	194	COM19	4225.00	453.00
157	COM54	5598.50	-325.00	195	COM18	4175.00	453.00
158	COM53	5598.50	-275.00	196	COM17	4125.00	453.00
159	COM52	5598.50	-225.00	197	COM16	4075.00	453.00
160	COM51	5598.50	-175.00	198	COM15	4025.00	453.00
161	COM50	5598.50	-125.00	199	COM14	3975.00	453.00
162	COM49	5598.50	-75.00	200	COM13	3925.00	453.00
163	COM48	5598.50	-25.00	201	COM12	3875.00	453.00
164	COM47	5598.50	25.00	202	COM11	3825.00	453.00
165	COM46	5598.50	75.00	203	COM10	3775.00	453.00
166	COM45	5598.50	125.00	204	COM9	3725.00	453.00
167	COM44	5598.50	175.00	205	COM8	3675.00	453.00
168	COM43	5598.50	225.00	206	COM7	3625.00	453.00
169	COM42	5598.50	275.00	207	COM6	3575.00	453.00
170	COM41	5598.50	325.00	208	COM5	3525.00	453.00
171	COM40	5598.50	375.00	209	COM4	3475.00	453.00
172	DUMMY3	5598.50	445.00	210	COM3	3425.00	453.00
173	DUMMY4	5295.00	453.00	211	COM2	3375.00	453.00
174	COM39	5225.00	453.00	212	COM1	3325.00	453.00
175	COM38	5175.00	453.00	213	COM0	3275.00	453.00
176	COM37	5125.00	453.00	214	COMS	3225.00	453.00

Bonding Diagram (continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
215	SEG0	3175.00	453.00	254	SEG39	1225.00	453.00
216	SEG1	3125.00	453.00	255	SEG40	1175.00	453.00
217	SEG2	3075.00	453.00	256	SEG41	1125.00	453.00
218	SEG3	3025.00	453.00	257	SEG42	1075.00	453.00
219	SEG4	2975.00	453.00	258	SEG43	1025.00	453.00
220	SEG5	2925.00	453.00	259	SEG44	975.00	453.00
221	SEG6	2875.00	453.00	260	SEG45	925.00	453.00
222	SEG7	2825.00	453.00	261	SEG46	875.00	453.00
223	SEG8	2775.00	453.00	262	SEG47	825.00	453.00
224	SEG9	2725.00	453.00	263	SEG48	775.00	453.00
225	SEG10	2675.00	453.00	264	SEG49	725.00	453.00
226	SEG11	2625.00	453.00	265	SEG50	675.00	453.00
227	SEG12	2575.00	453.00	266	SEG51	625.00	453.00
228	SEG13	2525.00	453.00	267	SEG52	575.00	453.00
229	SEG14	2475.00	453.00	268	SEG53	525.00	453.00
230	SEG15	2425.00	453.00	269	SEG54	475.00	453.00
231	SEG16	2375.00	453.00	270	SEG55	425.00	453.00
232	SEG17	2325.00	453.00	271	SEG56	375.00	453.00
233	SEG18	2275.00	453.00	272	SEG57	325.00	453.00
234	SEG19	2225.00	453.00	273	SEG58	275.00	453.00
235	SEG20	2175.00	453.00	274	SEG59	225.00	453.00
236	SEG21	2125.00	453.00	275	SEG60	175.00	453.00
237	SEG22	2075.00	453.00	276	SEG61	125.00	453.00
238	SEG23	2025.00	453.00	277	SEG62	75.00	453.00
239	SEG24	1975.00	453.00	278	SEG63	25.00	453.00
240	SEG25	1925.00	453.00	279	SEG64	-25.00	453.00
241	SEG26	1875.00	453.00	280	SEG65	-75.00	453.00
242	SEG27	1825.00	453.00	281	SEG66	-125.00	453.00
243	SEG28	1775.00	453.00	282	SEG67	-175.00	453.00
244	SEG29	1725.00	453.00	283	SEG68	-225.00	453.00
245	SEG30	1675.00	453.00	284	SEG69	-275.00	453.00
246	SEG31	1625.00	453.00	285	SEG70	-325.00	453.00
247	SEG32	1575.00	453.00	286	SEG71	-375.00	453.00
248	SEG33	1525.00	453.00	287	SEG72	-425.00	453.00
249	SEG34	1475.00	453.00	288	SEG73	-475.00	453.00
250	SEG35	1425.00	453.00	289	SEG74	-525.00	453.00
251	SEG36	1375.00	453.00	290	SEG75	-575.00	453.00
252	SEG37	1325.00	453.00	291	SEG76	-625.00	453.00
253	SEG38	1275.00	453.00	292	SEG77	-675.00	453.00

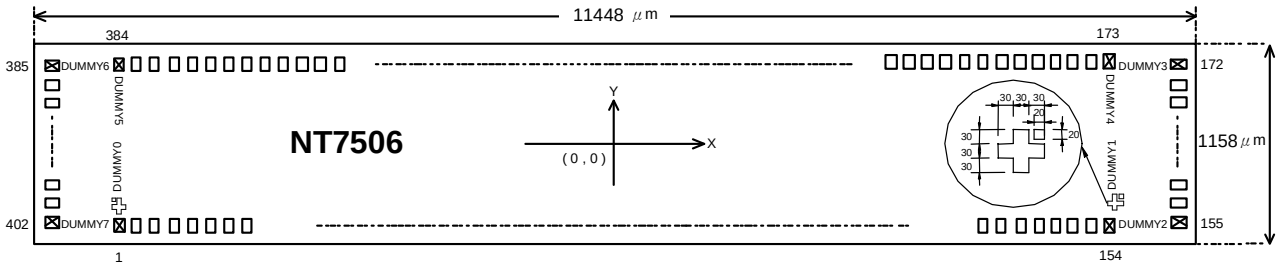
Bonding Diagram (continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
293	SEG78	-725.00	453.00	331	SEG116	-2625.00	453.00
294	SEG79	-775.00	453.00	332	SEG117	-2675.00	453.00
295	SEG80	-825.00	453.00	333	SEG118	-2725.00	453.00
296	SEG81	-875.00	453.00	334	SEG119	-2775.00	453.00
297	SEG82	-925.00	453.00	335	SEG120	-2825.00	453.00
298	SEG83	-975.00	453.00	336	SEG121	-2875.00	453.00
299	SEG84	-1025.00	453.00	337	SEG122	-2925.00	453.00
300	SEG85	-1075.00	453.00	338	SEG123	-2975.00	453.00
301	SEG86	-1125.00	453.00	339	SEG124	-3025.00	453.00
302	SEG87	-1175.00	453.00	340	SEG125	-3075.00	453.00
303	SEG88	-1225.00	453.00	341	SEG126	-3125.00	453.00
304	SEG89	-1275.00	453.00	342	SEG127	-3175.00	453.00
305	SEG90	-1325.00	453.00	343	COM64	-3225.00	453.00
306	SEG91	-1375.00	453.00	344	COM65	-3275.00	453.00
307	SEG92	-1425.00	453.00	345	COM66	-3325.00	453.00
308	SEG93	-1475.00	453.00	346	COM67	-3375.00	453.00
309	SEG94	-1525.00	453.00	347	COM68	-3425.00	453.00
310	SEG95	-1575.00	453.00	348	COM69	-3475.00	453.00
311	SEG96	-1625.00	453.00	349	COM70	-3525.00	453.00
312	SEG97	-1675.00	453.00	350	COM71	-3575.00	453.00
313	SEG98	-1725.00	453.00	351	COM72	-3625.00	453.00
314	SEG99	-1775.00	453.00	352	COM73	-3675.00	453.00
315	SEG100	-1825.00	453.00	353	COM74	-3725.00	453.00
316	SEG101	-1875.00	453.00	354	COM75	-3775.00	453.00
317	SEG102	-1925.00	453.00	355	COM76	-3825.00	453.00
318	SEG103	-1975.00	453.00	356	COM77	-3875.00	453.00
319	SEG104	-2025.00	453.00	357	COM78	-3925.00	453.00
320	SEG105	-2075.00	453.00	358	COM79	-3975.00	453.00
321	SEG106	-2125.00	453.00	359	COM80	-4025.00	453.00
322	SEG107	-2175.00	453.00	360	COM81	-4075.00	453.00
323	SEG108	-2225.00	453.00	361	COM82	-4125.00	453.00
324	SEG109	-2275.00	453.00	362	COM83	-4175.00	453.00
325	SEG110	-2325.00	453.00	363	COM84	-4225.00	453.00
326	SEG111	-2375.00	453.00	364	COM85	-4275.00	453.00
327	SEG112	-2425.00	453.00	365	COM86	-4325.00	453.00
328	SEG113	-2475.00	453.00	366	COM87	-4375.00	453.00
329	SEG114	-2525.00	453.00	367	COM88	-4425.00	453.00
330	SEG115	-2575.00	453.00	368	COM89	-4475.00	453.00

Bonding Diagram (continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
369	COM90	-4525.00	453.00	387	COM106	-5598.50	325.00
370	COM91	-4575.00	453.00	388	COM107	-5598.50	275.00
371	COM92	-4625.00	453.00	389	COM108	-5598.50	225.00
372	COM93	-4675.00	453.00	390	COM109	-5598.50	175.00
373	COM94	-4725.00	453.00	391	COM110	-5598.50	125.00
374	COM95	-4775.00	453.00	392	COM111	-5598.50	75.00
375	COM96	-4825.00	453.00	393	COM112	-5598.50	25.00
376	COM97	-4875.00	453.00	394	COM113	-5598.50	-25.00
377	COM98	-4925.00	453.00	395	COM114	-5598.50	-75.00
378	COM99	-4975.00	453.00	396	COM115	-5598.50	-125.00
379	COM100	-5025.00	453.00	397	COM116	-5598.50	-175.00
380	COM101	-5075.00	453.00	398	COM117	-5598.50	-225.00
381	COM102	-5125.00	453.00	399	COM118	-5598.50	-275.00
382	COM103	-5175.00	453.00	400	COM119	-5598.50	-325.00
383	COM104	-5225.00	453.00	401	COM120	-5598.50	-375.00
384	DUMMY5	-5295.00	453.00	402	DUMMY7	-5598.50	-445.00
385	DUMMY6	-5598.50	445.00		ALK_R	5311.00	-334.00
386	COM105	-5598.50	375.00		ALK_L	-5311.00	-334.00

Package Information



Pad Dimensions unit: μm

	Pad No.	Size	
		X	Y
Chip size	-	11448	1158
Pad pitch	1~2, 10~18, 19~145, 153~154, 155~156, 171~172, 173~174, 383~384, 385~386, 401~402	70	
	2~9, 146~153, 156~171, 174~383, 386~401	50	
	9~10	115	
	18~19, 145~146	140	
Bump size	1, 154, 173, 384	50	90
	155, 172, 385, 402	90	50
	2~9, 146~153, 174~383	32	90
	156~171, 386~401	90	32
	10~145	42	90
Bump height	All pad	15±3	

Ordering Information

Part No.	Packages
NT7506H-BDT	Gold Bump on Chip Tray
NT7506H-TAB0014	48mm Tape Automated Bonding Package

Cautions

1. The contents of this document will be subjected to change without notice.
2. Precautions against light projection:
   Light has the effect of causing the electrons of semiconductor to move; so light projection may change the characteristics of semiconductor devices. For this reason, it is necessary to take account of effective protection measures for the packages (such as COB, COG, TCP and COF, etc.) causing chip to be exposed to a light environment in order to isolate the projection of light on any part of the chip, including top, bottom and the area around the chip.
   Observe the following instructions in using this product:
   a. During the design stage, it is necessary to notice and confirm the light sensitivity and preventive measures for using IC on substrate (PCB, Glass or Film) or product.
   b. Test and inspect the product under an environment free of light source penetration.
   c. Confirm that all surfaces around the IC will not be exposed to light source.