NT66P12

OTP 4-bit Microcontroller with LCD Driver

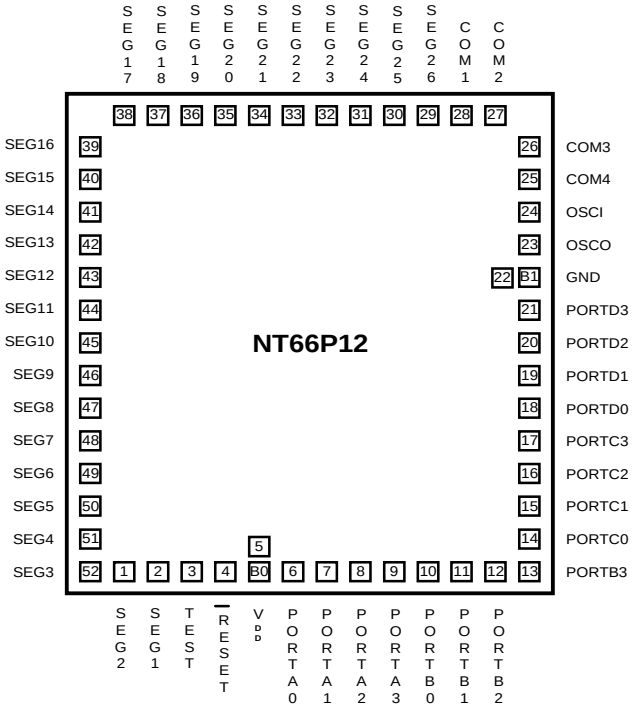
Features

- NT6610C-based single-chip 4-bit microcontroller with LCD driver
- ROM: 2048 X 16 bits
- RAM: 256 X 4 bits (Data memory)
- Operation voltage: 2.5V - 5.4V
- 16 CMOS I/O pins
  - CMOS or Open Drain (code option)
- 4 level subroutine nesting (including interrupts)
- Two 8-bit timer/counter with pre-divider circuit
- Oscillator warm-up timer
- 4 priority interrupt sources:
  - External interrupt (falling edge)
  - Timer0 interrupt
  - Timer1 interrupt
  - PortB interrupt (falling edge)
- Oscillator
  - 32.768KHz crystal or 262K RC (code option)
- Instruction cycle time:
  - 4/32.768KHz (≈ 122μs) for 32.768KHz OSC clock
  - 4/262KHz (≈ 15μs) for 262KHz OSC clock
- LCD driver:
  - 4 X 26 (1/4 duty, 1/3 bias or 1/3 duty, 1/2 bias)
- Two low power operation modes: HALT or STOP mode
- Built-in alarm generator carrier frequency:
  - 2KHz or 4KHz (code option)
- Low power consumption (Iop < 30μA, 32.768KHz, 3V)
- Bonding option for multi-code software
- Available in CHIP FORM

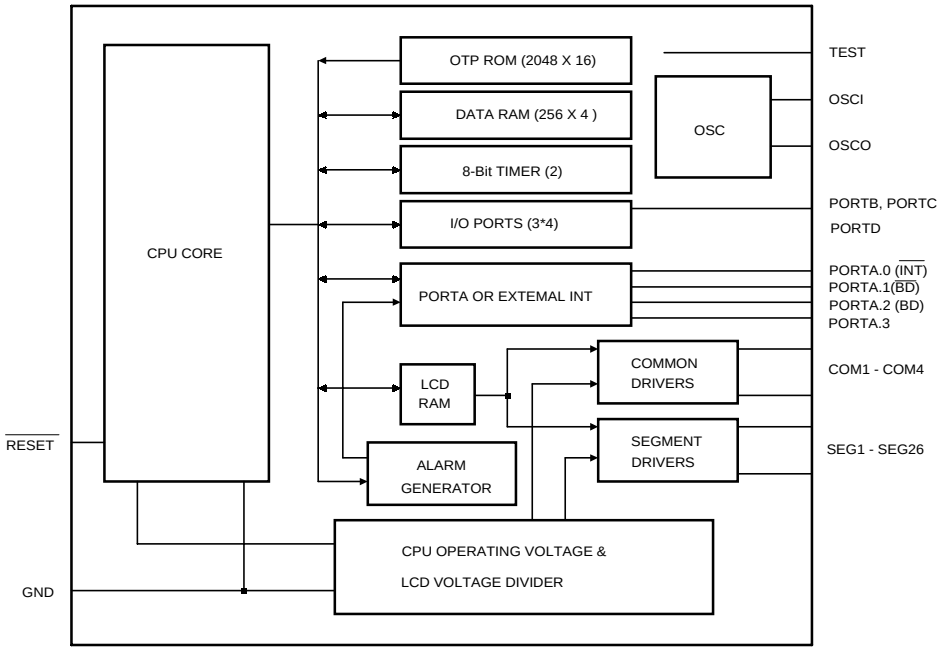
General Description

NT66P12 is a single-chip microcontroller integrated with an NT6610C 4-bit CPU core, SRAM, timer, alarm generator, LCD driver, I/O port, and program ROM.

Pad Configuration



Block Diagram



Pad Description

Pad No.	Designation	I/O	Description
2 - 1, 52 - 29	SEG1 - 26	O	Segment signal output for LCD display. Seg1 - 4 as output ports
3	TEST	I	Test pin internally pull-down.(No connect for user)
4	$\overline{\text{RESET}}$	I	Pad reset input
5	V_{DD} B0	P I	Power pin Share with Bonding option, internally pull-low
6 - 9	PORTA0 - 3	I/O	Bit programmable I/O PA.0 could be external interrupt input ($\overline{\text{INT}}$) PA.1, PA.2 could be buzzer output PA.1 (BD), PA.2 ($\overline{\text{BD}}$) In the program mode, PA.1 shared with DATA, PA. 2 shared with PINPGMB, PA. 3 shared with PINOE
10 - 13	PORTB0 - 3	I/O	Bit programmable I/O, vector interrupts (active falling edge)
14 - 17	PORTC0 - 3	I/O	Bit programmable I/O
18 - 21	PORTD0 - 3	I/O	Bit programmable I/O
22	GND B1	P I	Ground pin Share with Bonding option, internally pull-high
23	OSCO	O	Oscillator output pin, connected to crystal oscillator
24	OSCI	I	Oscillator input pin, connected to crystal or external resistor
28 - 25	COM1 - 4	O	Common signal output for LCD display

Total 52 pads.

Functional Description

1. CPU

The CPU contains the following function blocks: Program Counter, Arithmetic Logic Unit (ALU), Carry Flag, Accumulator, Table Branch Register, Data Pointer (INX, DPH, DPM, and DPL), and Stack.

(a) PC (Program Counter)

The Program Counter is used to address the 2K program ROM. It consists of 12-bits: Page Register (PC11), and Ripple Carry Counter (PC10, PC9, PC8, PC7, PC6, PC5, PC4, PC3, PC2, PC1, PC0).

The program counter normally increases by one (+1) with every execution of an instruction except in the following cases:

(1) When executing a jump instruction (such as JMP, BA0, BAC);

(2) When executing a subroutine call instruction (CALL);

(3) When an interrupt occurs;

(4) When the chip is at the INITIAL RESET mode.

The program counter is loaded with data corresponding to each instruction.

(b) ALU and CY

ALU performs arithmetic and logic operations. The ALU provides the following functions:

Binary addition/subtraction (ADC, SBC, ADD, SUB, ADI, SBI)

Decimal adjustment for addition/subtraction (DAA, DAS)
Logic operations (AND, EOR, OR, ANDIM, EORIM, ORIM)
Decision (BA0, BA1, BA2, BA3, BAZ, BC)
Logic Shift (SHR)

The Carry Flag (CY) holds the ALU overflow, which the arithmetic operation generates. During an interrupt service or call instruction, the carry flag is pushed into the stack and restored back from the stack by the RTNI instruction. It is unaffected by the RTNW instruction.

(c) Accumulator

Accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with ALU, data is transferred between the accumulator and system register, LCD RAM, or data memory can be performed.

(d) Stack

A group of registers used to save the contents of CY & PC (10-0) sequentially with each subroutine call or interrupt. It is organized 13 bits X 4 levels. The MSB is saved for CY. 4 levels are the maximum allowed for subroutine calls and interrupts.

The contents of stack are returned sequentially to the PC with the return instructions (RTNI/RTNW). Stack is operated on a first-in, last-out basis. This 4-level nesting includes both subroutine calls and interrupts requests. Note that program execution may enter an abnormal state if the number of calls and interrupt requests exceeds 4, and the bottom of stack will be shifted out.

2. ROM

The ROM can address 2048 words X 16 bits of program area from $000 to $7FF.

(a) Vector Address Area ($000 to $004)

The program is sequentially executed. There is an area address $000 through $004 that is reserved for a special interrupt service routine such as starting vector address.

Address	Instruction	Function
$000H	JMP instruction	Jump to RESET service routine
$001H	JMP instruction	Jump to External interrupt service routine
$002H	JMP instruction	Jump to TIMER0 service routine
$003H	JMP instruction	Jump to TIMER1 service routine
$004H	JMP instruction	Jump to PB service routine (PORTB)

(b) Table Data Reference

Table Data can be stored in program memory and can be referenced by using Table Branch (TJMP) and Return Constant (RTNW) instructions. The Table Branch Register (TBR) and Accumulator (AC) is placed by an offset address in program ROM. TJMP instruction branch into address ((PC11 - PC8) X (2^8) + (TBR, AC)). The address is determined by RTNW to return look-up value into (TBR, AC). ROM code bit7-bit4 is placed into TBR and bit3-bit0 into AC.

3. RAM

Built-in RAM contains of general-purpose data memory, LCD RAM, and system register. Data memory, LCD RAM, and system register can be direct accessed by in one instruction cycle. Because of its static nature, the RAM can keep data after the CPU enters STOP or HALT.

(a) Data memory, LCD RAM, and System register

The following is the memory allocation map:
$000 - $01F: System register and I/O
$020 - $11F: Data memory (256 X 4 bits divided into 2 banks)
$300 - $319: LCD RAM space (26 X 4 bits)

(b) Data Pointer

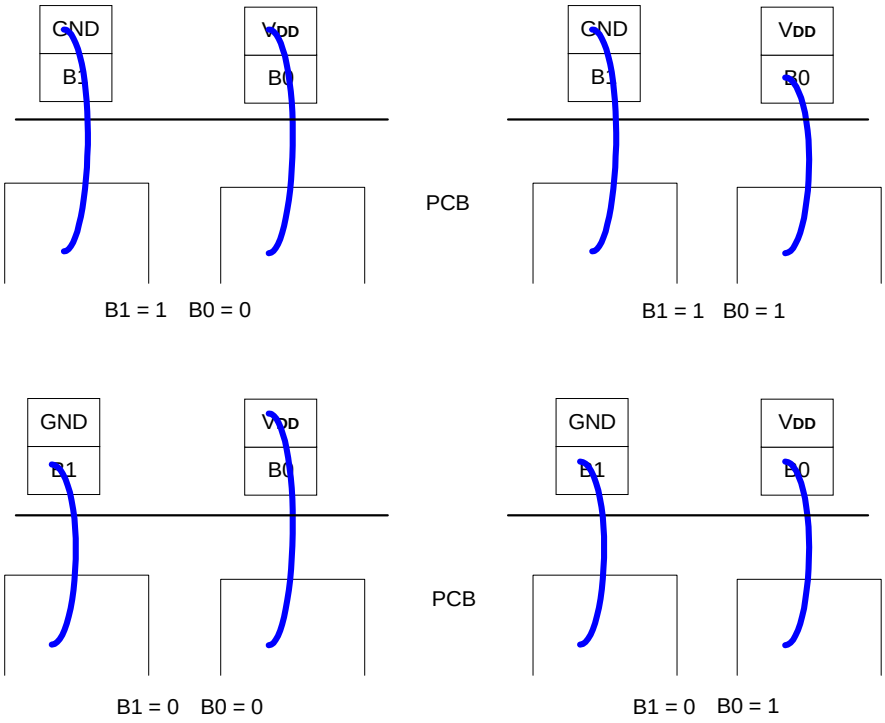
The Data Pointer can indirectly address data memory. Pointer address is located in register DPM (3-bits) and DPL (4-bits). The addressing range can have 128 locations. Pseudo index address (INX) is used to read or write Data memory, and then RAM address bit9-bit0 comes from DPH, DPM and DPL.

(c) Configuration of System Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Description
$00	IEX	IET0	IET1	IEP	R/W	Interrupt enable flags
$01	IRQX	IRQT0	IRQT1	IRQP	R/W	Interrupt request flags
$02	-	T0M.2	T0M.1	T0M.0	R/W	Bit0-2: Timer0 Mode register
$03	-	T1M.2	T1M.1	T1M.0	R/W	Bit0-2: Timer1 Mode register
$04	T0L.3	T0L.2	T0L.1	T0L.0	R/W	Timer0 load/counter register low nibble
$05	T0H.3	T0H.2	T0H.1	T0H.0	R/W	Timer0 load/counter register high nibble
$06	T1L.3	T1L.2	T1L.1	T1L.0	R/W	Timer1 load/counter register low nibble
$07	T1H.3	T1H.2	T1H.1	T1H.0	R/W	Timer1 load/counter register high nibble
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD
$0C	LPD3	LPD2	LPD1	LPD0	W	LPD Enable Control (LPD3 - 0): 0101: LPD Enable (Default); 1010: LPD Disable
$0D	-	-	B1	B0	R	Bonding option
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table Branch Register
$0F	INX.3	INX.2	INX.1	INX.0	R/W	Pseudo index register
$10	DPL.3	DPL.2	DPL.1	DPL.0	R/W	Data pointer for INX low nibble
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble
$12	-	DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble
$13	O/S	LCDOFF	HLM	PAM	R/W	Bit0: set PA.1, PA.2 as Alarm output Bit1: HEAVY LOAD Mode Bit2: LCD off or LCD on Bit3: set LCD segment as output
$14	AEC3	AEC2	AEC1	AEC0	R/W	Alarm Envelope Control
$15	-	-	-	DUTY	R/W	Bit0: change LCD duty to 1/4 duty, 1/3 bias
$16 - $1F	-	-	-	-	-	Reserved

System Register $0D:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks	Power-on
$0D	-	-	B1	B0	R	Bit0: Bonding option 0, internal weak drive Bit1: Bonding option 1, internal weak drive	Pull low Pull high
	X	X	1	0			Yes
	X	X	0	0		B1 bond to GND	
	X	X	1	1		B0 bond to V_{DD}	
	X	X	0	1		B1 bond to GND and B0 bond to V_{DD}	



NT66P12 Bonding Option

Up to 4 different bonding options is possible for the user's needs. The chip's program has 4 different program flows that will vary depending on which bonding option is used. The readable contents of B1 and B0 will differ depending on bonding.

System Register $13:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks	Power on
$13	O/S	LCDOFF	HLM	PAM	R/W	Bit0: set PA.1, PA.2 as ALARM output Bit1: HEAVY LOAD Mode Bit2: LCD Power Control Bit3: set seg1 - 4 as output ports	
	X	X	X	0		PORTA.1, PORTA.2 as I/O port	Yes
	X	X	X	1		PORTA.1, PORTA.2 as ALARM output	
	X	X	0	X		No Heavy Load	Yes
	X	X	1	X		HEAVY LOAD mode	
	X	0	X	X		LCD on	Yes
	X	1	X	X		LCD off	
	0	X	X	X		Seg1 - 4 as LCD output	Yes
	1	X	X	X		Seg1 - 4 as output ports	

HEAVY LOAD Mode (HLM): This mode is designed for the 32KHz crystal oscillator, so that the oscillation can be maintained in a noisy power environment. The power might drop suddenly when the ALARM is driving a speaker. The HLM is designed to control this power variation. The consumption of power will increase during the use of the HLM mode, but it will not affect the RC oscillator.

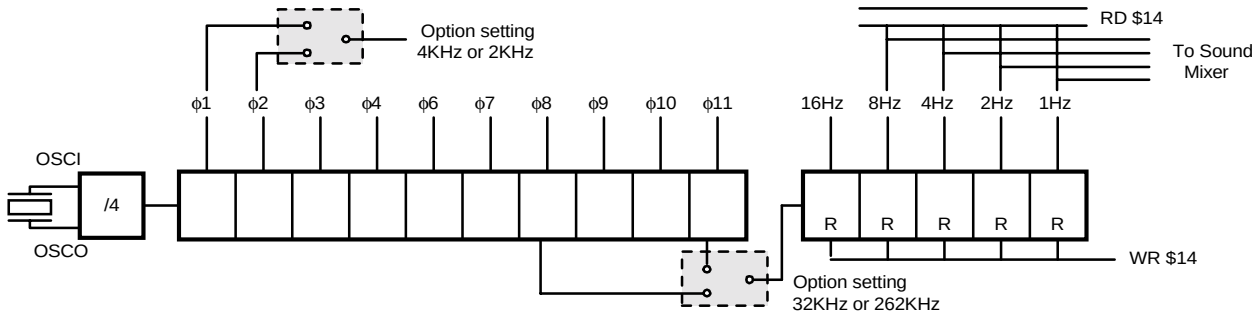
Note: The HLM needs about 5 instruction cycles to set-up the oscillation for 32.768KHz crystal oscillator.

System Register $14 (AEC):

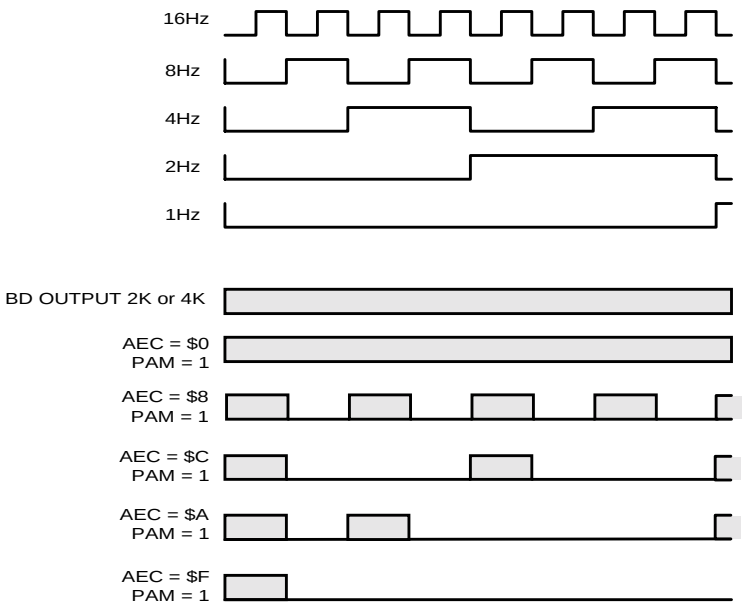
Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks	Power On
$14	AEC3	AEC2	AEC1	AEC0	R/W	ALARM envelope control	
	0	0	0	0		DC envelope	Yes
	X	X	X	1		1Hz envelope	
	X	X	1	X		2Hz envelope	
	X	1	X	X		4Hz envelope	
	1	X	X	X		8Hz envelope	

Default carrier frequency is 4KHz. Can be selected to 2KHz by code option.
WRITE mode: controls the envelope selection.
READ mode can read out current envelope waveforms.

Below is the ALARM functional block equivalent circuit diagram. To activate the ALARM function, first switch the PAM to ALARM OUTPUT mode. After setting PAM equal to 1, then set the proper envelope. When the data writes into AEC, the envelope counter will be synchronized at the same time. The programmer can read back the envelope from AEC register and make any pattern changes needed by programmer. The Read operation will not affect the alarm output waveform.



The programming alarm waveform is shown below:



System Register $15:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Description	Power on
$15	-	-	-	DUTY	R/W	Bit0: LCD duty control.	
	-	-	-	1		LCD driver = 1/4 duty, 1/3 bias	
	-	-	-	0		LCD driver = 1/3 duty, 1/2 bias	Yes

4. LCD Driver

The LCD driver contains a controller, voltage generator, 4 common signal pins, and 26 segment driver pins. There are two different driving modes that are programmable, one is 1/4 duty and 1/3 bias, and the other is 1/3 duty and 1/2 bias. Driving mode is controlled by register $15H and the power-on status is 1/3 duty, 1/2 bias. The controller consists of display data RAM and a duty generator. The LCD data RAM is a dual port RAM that transfers data to segment pins automatically without a program control.

LCD segment 1 - 4 can also be used as output ports, it is selected by the bit3 of system register $13H. When segments 1 - 4 are output ports, data can be written to bit 0 of the same address (300H - 303H). LCD RAM can be used as data memory if needed. When the "STOP" instruction is executed, the LCD will be turned off, but the data of LCD RAM is the same before executing the "STOP" instruction.

Configuration of LCD RAM area:

(a) When segments 1 - 4 are used as output ports:

Address	Bit 3	Bit 2	Bit 1	Bit 0
	COM4	**COM3**	**COM2**	**COM1**
300H	-	-	-	DATA_BIT
301H	-	-	-	DATA_BIT
302H	-	-	-	DATA_BIT
303H	-	-	-	DATA_BIT

(b) When segments 1 - 4 are used as segment outputs:

Address	Bit 3	Bit 2	Bit 1	Bit 0
	COM4	COM3	COM2	COM1
300H	SEG1	SEG1	SEG1	SEG1
301H	SEG2	SEG2	SEG2	SEG2
302H	SEG3	SEG3	SEG3	SEG3
303H	SEG4	SEG4	SEG4	SEG4

(c) Segments 5 - 26

Address	Bit 3	Bit 2	Bit 1	Bit 0
	COM4	COM3	COM2	COM1
304H	SEG5	SEG5	SEG5	SEG5
305H	SEG6	SEG6	SEG6	SEG6
306H	SEG7	SEG7	SEG7	SEG7
307H	SEG8	SEG8	SEG8	SEG8
308H	SEG9	SEG9	SEG9	SEG9
309H	SEG10	SEG10	SEG10	SEG10
30AH	SEG11	SEG11	SEG11	SEG11
30BH	SEG12	SEG12	SEG12	SEG12
30CH	SEG13	SEG13	SEG13	SEG13
30DH	SEG14	SEG14	SEG14	SEG14
30EH	SEG15	SEG15	SEG15	SEG15
30FH	SEG16	SEG16	SEG16	SEG16
310H	SEG17	SEG17	SEG17	SEG17
311H	SEG18	SEG18	SEG18	SEG18
312H	SEG19	SEG19	SEG19	SEG19
313H	SEG20	SEG20	SEG20	SEG20
314H	SEG21	SEG21	SEG21	SEG21
315H	SEG22	SEG22	SEG22	SEG22
316H	SEG23	SEG23	SEG23	SEG23
317H	SEG24	SEG24	SEG24	SEG24
318H	SEG25	SEG25	SEG25	SEG25
319H	SEG26	SEG26	SEG26	SEG26

5. I/O PORT

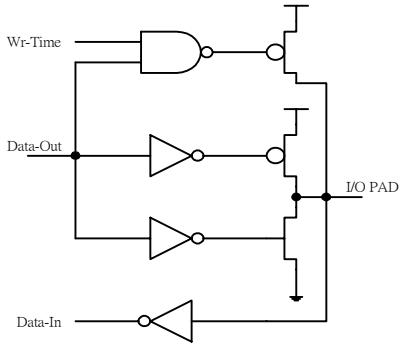
NT66P12 has 16 I/O pins. Each I/O pins are bit programmable. I/O pins are CMOS (Default) or Open Drain by code option.

(a) PORTA, PORTB, PORTC and PORTD

Each of these ports contains 4 bit I/O pins. Port I/O mapping address is shown as follows:

Address	Bit3	Bit2	Bit1	Bit0
$08	PORT A.3	PORT A.2	PORT A.1	PORT A.0
$09	PORT B.3	PORT B.2	PORT B.1	PORT B.0
$0A	PORT C.3	PORT C.2	PORT C.1	PORT C.0
$0B	PORT D.3	PORT D.2	PORT D.1	PORT D.0

If ports are pull-high internally, it is weak drive. The equivalent circuit is below:

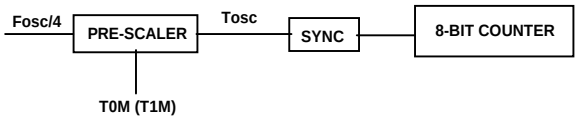


6. Timer

NT66P12 has two 8-bit timers. The timer/counter has the following features:

- 8-bit up-counting timer/counter.
- Automatic re-loads counter.
- 8-bit prescaler.
- Interrupt on overflow from $FF to $00.

The following is a simplified timer block diagram.



(a) Timer0 and Timer1 Configuration and Operation

Both the Timer0 and Timer1 consist of an 8-bit write-only timer load register (TL0L, TL0H; TL1L, TL1H) and an 8-bit read-only timer counter (TC0L, TC0H; TC1L, TC1H). Each of them has low order digits and high order digits. Writing data into the timer load register (TL0L, TL0H; TL1L, TL1H) can initialize the timer counter.

The low-order digit should be written first, and then the high-order digit. The timer counter is automatically loaded with the contents of the load register when the high order digit is written or counter counts overflow from $FF to $00.

Timer Load Register: Since the register H controls the physical READ and WRITE operations.

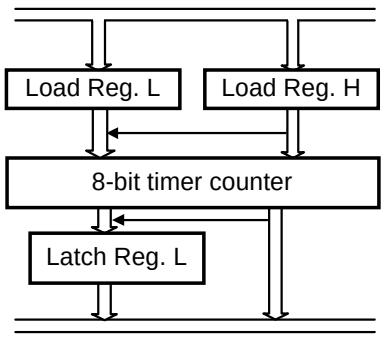
Please follow these steps:

Write Operation:

Low nibble first;
High nibble to update the counter

Read Operation:

High Nibble first;
Low nibble followed.



(b) Timer0 Interrupt

The timer overflow will generate an internal interrupt request, when the counter counts overflow from $FF to $00. If the interrupt enable flag is enabled, then a timer interrupt service routine will start. This can also be used to wake CPU from HALT mode.

(c) Timer mode register

The timer can be programmed in several different prescaler ratios by setting Timer Mode register (TM0, TM1).

The 8-bit counter prescaler output pulses. The Timer Mode registers (TM0, TM1) are 3-bit registers used for the timer control as shown in Table1 and Table 2. These mode registers select the input pulse sources into the timer.

Table 1. Timer0 Mode Register ($02)

TM0.2	TM0.1	TM0.0	Prescaler Divide Ratio	Clock Source
0	0	0	$/2^{11}$	System clock
0	0	1	$/2^{9}$	System clock
0	1	0	$/2^{7}$	System clock
0	1	1	$/2^{5}$	System clock
1	0	0	$/2^{3}$	System clock
1	0	1	$/2^{2}$	System clock
1	1	0	$/2^{1}$	System clock
1	1	1	$/2^{0}$	System clock

Table 2. Timer1 Mode Register ($03)

TM1.2	TM1.1	TM1.0	Prescaler Divide Ratio	Clock Source
0	0	0	$/2^{11}$	System clock
0	0	1	$/2^{9}$	System clock
0	1	0	$/2^{7}$	System clock
0	1	1	$/2^{5}$	System clock
1	0	0	$/2^{3}$	System clock
1	0	1	$/2^{2}$	System clock
1	1	0	$/2^{1}$	System clock
1	1	1	$/2^{0}$	System clock

7. Interrupt

Four interrupt sources are available on NT66P12:

- External interrupt ($\overline{INT}$ share with PA.0)
- Timer0 interrupt
- Timer1 interrupt
- Port's falling edge detection interrupt ($\overline{PB}$)

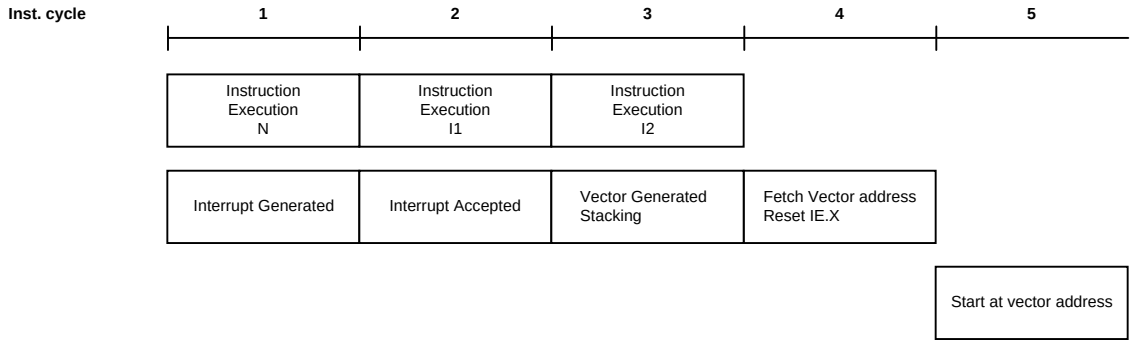
(a) Interrupt Control Bits and Interrupt Service:

The interrupt control flags are mapped on $00 and $01 of the system register. They can be accessed or tested by program. Those flags are cleared to 0 at initialization by chip reset.

Address	Bit3	Bit2	Bit1	Bit0	Remarks
$00	IEX	IET0	IET1	IEP	interrupt enable flags
$01	IRQX	IRQT0	IRQT1	IRQP	interrupt request flags

When IEx is set to 1 and the interrupt request is generated (IRQx is 1), the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources. When an interrupt occurs, the PC and CY flag will be saved into stack memory and jump to interrupt service vector address. After the interrupt occurs, all interrupt enable flags (IEx) are reset to 0 automatically, so when IRQx is 1 and IEx is set to 1 again, the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources.

(b) Interrupt Servicing Sequence Diagram:



Interrupt Nesting:

During the NT6610C CPU interrupt service, the user can enable any INTERRUPT enable flag before returning from the interrupt. The servicing sequence diagram shows the next interrupt and the next nesting interrupt occurrences. If the interrupt request is ready and the instruction of execution N is IE enable, then the interrupt will start immediately after the next two instruction executions. However, if instruction I1 or instruction I2 disables the interrupt request or enable flag, then the interrupt service will be terminated.

(c) External Interrupt ($\overline{INT}$)

External interrupt is shared with the bit0 of PORTA. When bit3 of system register 0 (IEX) is set to 1, the external interrupt will be enabled, and a falling edge signal on PA.0 will generate an external interrupt. (Note: while external interrupt is enabled, writing a "0" to bit0 of PORTA will generate an external interrupt).

8. System Clock

NT66P12 has one clock source. OSC is 32.768KHz crystal or 262KHz RC determined by code option. The OSC generates the basic clock pulses that provide the system clock to supply CPU and on-chip peripherals (TIMER0, TIMER1, LCD).

Initial State

There are 3 types of system reset.
1. Hardware reset input
2. Power on reset
3. Low Power Detection reset

Hardware	After power-on reset
Program counter	$000
CY	Undefined
Data memory	Undefined
AC	Undefined
Timer counter	0
Timer load register	0
Interrupt Enable Flags	0
Interrupt Request Flags	0
LPD [3:0]	0101

Code option

(a) Oscillator Type:

0 = Set as 32.768KHz crystal (Default)
1 = Set as 262KHz RC

(b) Alarm Carrier Frequency:

0 = Set as is 4KHz (Default)
1 = Set as is 2KHz

(c) Reset Pin Pull-up Resistor:

0 = Disable Pull-up resistance (Default)
1 = Enable Pull-up resistance

(d) NT6612/UM6410 Body Option:

0 = NT6612 Body (Default)
1 = UM6410 Body

(e) Port Type:

0 = Set I/O as CMOS (Default)
1 = Set I/O as PMOS

Instructions Set

All instructions are one cycle and one-word instructions. The characteristics are memory-oriented operation.

Arithmetic and Logical Instruction

Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X (, B)	00000 0bbb xxx xxxx	AC ← Mx + AC + CY	CY
ADCM X (, B)	00000 1bbb xxx xxxx	AC, Mx← Mx + AC + CY	CY
ADD X (, B)	00001 0bbb xxx xxxx	AC ← Mx + AC	CY
ADDM X (, B)	00001 1bbb xxx xxxx	AC, Mx← Mx + AC	CY
SBC X (, B)	00010 0bbb xxx xxxx	AC ← Mx + -AC + CY	CY
SBCM X (, B)	00010 1bbb xxx xxxx	AC, Mx← Mx + -AC + CY	CY
SUB X (, B)	00011 0bbb xxx xxxx	AC ← Mx + -AC + 1	CY
SUBM X (, B)	00011 1bbb xxx xxxx	AC, Mx← Mx + -AC + 1	CY
EOR X (, B)	00100 0bbb xxx xxxx	AC ← Mx ⊕ AC	
EORM X (, B)	00100 1bbb xxx xxxx	AC, Mx← Mx ⊕ AC	
OR X (, B)	00101 0bbb xxx xxxx	AC ← Mx | AC	
ORM X (, B)	00101 1bbb xxx xxxx	AC, Mx← Mx | AC	
AND X (, B)	00110 0bbb xxx xxxx	AC ← Mx & AC	
ANDM X (, B)	00110 1bbb xxx xxxx	AC, Mx← Mx & AC	
SHR	11110 0000 000 0000	0 → AC [3]; AC [0] → CY; AC shift right one bit	CY

Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X, I	01000 iiii xxx xxxx	AC ← Mx + I	CY
ADIM X, I	01001 iiii xxx xxxx	AC, Mx ← Mx + I	CY
SBI X, I	01010 iiii xxx xxxx	AC ← Mx + -I +1	CY
SBIM X, I	01011 iiii xxx xxxx	AC, Mx ← Mx + -I + 1	CY
EORIM X, I	01100 iiii xxx xxxx	AC, Mx ← Mx ⊕ I	
ORIM X, I	01101 iiii xxx xxxx	AC, Mx ← Mx | I	
ANDIM X, I	01110 iiii xxx xxxx	AC, Mx ← Mx & I	

* In the assembler ASM66 V1.0, EORIM mnemonic is EORI. However, EORI has the same operation identical with EORIM. It is true for the ORIM with respect to ORI, and ANDIM with respect to ANDI.

Decimal Adjust

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC; Mx ← Decimal adjust for add	CY
DAS X	11001 1010 xxx xxxx	AC; Mx ← Decimal adjust for sub	CY

Transfer Instruction

Mnemonic	Instruction Code	Function	Flag Change
LDA X (, B)	00111 0bbb xxx xxxx	AC ← Mx	
STA X (, B)	00111 1bbb xxx xxxx	Mx ← AC	
LDI X, I	01111 iiii xxx xxxx	AC, Mx ← I	

Control Instruction

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC ← X if AC = 0	
BNZ X	10000 xxxx xxx xxxx	PC ← X if AC ≠ 0	
BC X	10011 xxxx xxx xxxx	PC ← X if CY = 1	
BNC X	10001 xxxx xxx xxxx	PC ← X if CY ≠ 1	
BA0 X	10100 xxxx xxx xxxx	PC ← X if AC (0) = 1	
BA1 X	10101 xxxx xxx xxxx	PC ← X if AC (1) = 1	
BA2 X	10110 xxxx xxx xxxx	PC ← X if AC (2) = 1	
BA3 X	10111 xxxx xxx xxxx	PC ← X if AC (3) = 1	
CALL X	11000 xxxx xxx xxxx	ST ← CY; PC + 1 PC ← X (Not include p)	
RTNW H, L	11010 000h hhh llll	PC ←ST; TBR ← hhhh; A ← llll	
RTNI	11010 1000 000 0000	CY;PC ← ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC ← X (Include p)	
TJMP	11110 1111 111 1111	PC ← (PC11-PC8) (TBR) (A)	
NOP	11111 1111 111 1111	No Operation	

Where,

PC	Program counter	I	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank
p	ROM page = 0		
ST	Stack	TBR	Table Branch Register

Absolute Maximum Rating*

DC Supply Voltage . . . . . -0.3V to + 7.0V

Input Voltage . . . . . -0.3V to V_{DD}+ 0.3V

Operating Ambient Temperature . . . -10°C to + 60°C

Storage Temperature . . . . . -55°C to + 125°C

*Comments

Stresses above those listed under "**Absolute Maximum Ratings**" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} = 3.0V, GND = 0V, T_A = 25°C, F_{OSC} = 32.768KHz, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating Voltage	V_{DD}	2.5	3	3.4	V	
Operating Current	I_{OP}		20	30	μA	All output pins unload execute NOP instruction
Standby Current	I_{SB1}		15	25	μA	All output pins unload (HALT mode) exclude LCD current
Standby Current	I_{SB2}			1	μA	All output pins unload (STOP mode) exclude LCD current
Input High Voltage	V_{IH}	0.7 X V_{DD}		V_{DD} + 0.3	V	PORTA, PORTB, PORTC, PORTD
Input Low Voltage	V_{IL}	GND - 0.3		0.2 X V_{DD}	V	PORTA, PORTB, PORTC, PORTD
Output High Voltage	V_{OH1}	2.3			V	PORTA, PORTB, PORTC (I_{OH} = 15μA)
Output Low Voltage	V_{OL1}			0.2	V	PORTA, PORTB, PORTC (I_{OL} = 300μA)
Output High Voltage	V_{OH2}	2.1			V	BD/$\overline{BD}$ (set PA.1and PA.2 to be ALARM output), I_{OH} = 2mA
Output Low Voltage	V_{OL2}			0.9	V	BD/$\overline{BD}$ (set PA.1and PA.2 to be ALARM output), I_{OL} = 2mA
Output High Voltage	V_{OH3}	2.8			V	SEGx, I_{OH} = 3μA, SEG1 - 4 to be output port (for reference only)
Output Low Voltage	V_{OL3}			0.2	V	SEGx, I_{OL} = 3μA, SEG1 - 4 to be output port (for reference only)
Output High Voltage	V_{OH4}	2.8			V	COMx, I_{OH} = 8μA (for reference only)
Output Low Voltage	V_{OL4}			0.2	V	COMx, I_{OL} = 8μA (for reference only)
LCD Lighting	I_{LCD}		6.5	7.5	μA	HALT mode

DC Electrical Characteristics (V_{DD} = 5.0V, GND = 0V, T_A = 25°C, F_{OSC} = 32.768KHz, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating Voltage	V_{DD}	4.5	5.0	5.4	V	
Operating Current	I_{OP}		20	30	μA	All output pins unload execute NOP instruction
Standby Current	I_{SB1}		15	25	μA	All output pins unload (HALT mode) exclude LCD current
Standby Current	I_{SB2}			1	μA	All output pins unload (STOP mode) exclude LCD current
Input High Voltage	V_{IH}	0.7 X V_{DD}		V_{DD} + 0.3	V	PORTA, PORTB, PORTC, PORTD
Input Low Voltage	V_{IL}	GND - 0.3		0.2 X V_{DD}	V	PORTA, PORTB, PORTC, PORTD
Output High Voltage	V_{OH1}	4.3			V	PORTA, PORTB, PORTC (I_{OH} = 15μA)
Output Low Voltage	V_{OL1}			0.3	V	PORTA, PORTB, PORTC (I_{OL} = 300μA)
Output High Voltage	V_{OH2}	2.1			V	BD/$\overline{BD}$ (set PA.1and PA.2 to be ALARM output), I_{OH} = 2mA
Output Low Voltage	V_{OL2}			1.0	V	BD/$\overline{BD}$ (set PA.1and PA.2 to be ALARM output), I_{OL} = 2mA
Output High Voltage	V_{OH3}	4.8			V	SEGx, I_{OH} = 3μA, SEG1 - 4 to be output port (for reference only)
Output Low Voltage	V_{OL3}			0.3	V	SEGx, I_{OL} = 3μA, SEG1 - 4 to be output port (for reference only)
Output High Voltage	V_{OH4}	4.8			V	COMx, I_{OH} = 8μA (for reference only)
Output Low Voltage	V_{OL4}			0.3	V	COMx, I_{OL} = 8μA (for reference only)
LCD Lighting	I_{LCD}		19.5	23.0	μA	HALT mode

Note:

1. Operation frequency vs. I_{SB1}

   I_{SB1X} = (Frequency/32.768KHz) * I_{SB1} * 0.8

2. Operation frequency vs. I_{OP}

   I_{OPX} = (Frequency/32.768KHz) * I_{OP} * 0.8

3. HLM vs. I_{OP}, I_{SB1} and I_{SB2}

   If HLM = 1, I_{OPX} = I_{OP} * 2, I_{SB1X} = I_{SB1} * 2, I_{SB2X} = I_{SB1} * 2

LPD Circuitry (GND = 0V, T_A = 25°C, Fosc = 32.768KHz, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
LPD-detected Voltage	V_{LPD}	1.7	2.0	2.3	V	

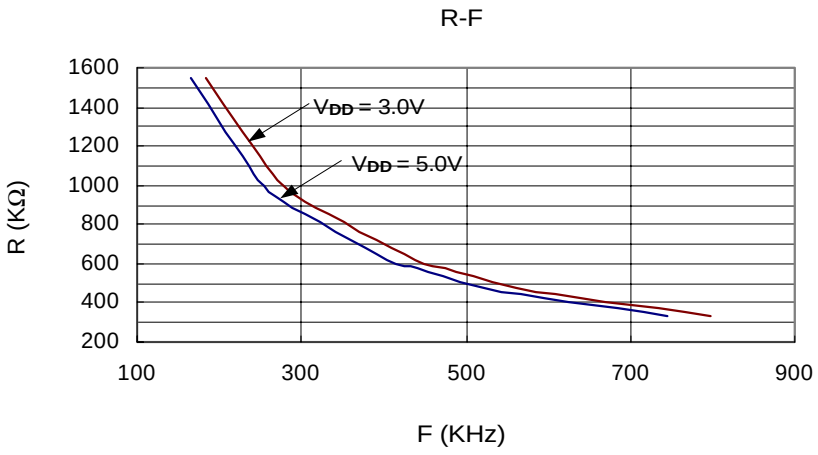
AC Characteristics (V_{DD} = 3.0V, GND = 0V, T_A = 25°C, Fosc = 32.768KHz , unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Oscillation Start Time	T_{STT}		2	5	s	
Halt Time	T_{HTT}		0		s	I_{DD} reduces to Isb1 after instruction executing
Stop Time	T_{SPT}		0		s	I_{DD} reduces to Isb2 after instruction executing
Frequency Stability	$\Delta F/F$			1	PPM	|F(3.0)-F(2.4)|/F(3.0), crystal oscillator (for reference only)
Frequency Variation	$\Delta F/F$			10	PPM	C1 = 5 - 25P (for reference only)

AC Characteristics (V_{DD} = 3.0V, GND = 0V, T_A= 25°C, Fosc= 262KHz, unless otherwise specified)

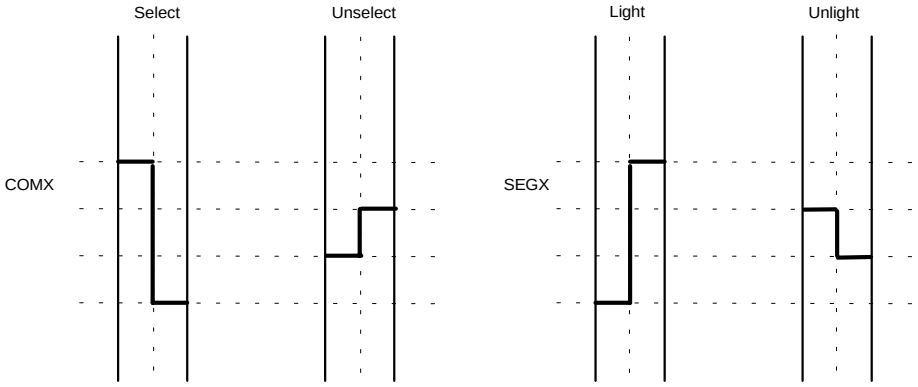
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Oscillation Start Time	T_{STT}			2	ms	
Halt Time	T_{HTT}		0		s	I_{DD} reduces to Isb1 after instruction executing
Stop Time	T_{SPT}		0		s	I_{DD} reduces to Isb3 after instruction executing
Frequency Stability	$\Delta F/F$			10	%	|F(3.0)-F(2.4)|/F(3.0), RC oscillator (for reference only)
Frequency Variation	$\Delta F/F$			15	%	variation caused by process variation (for reference only)

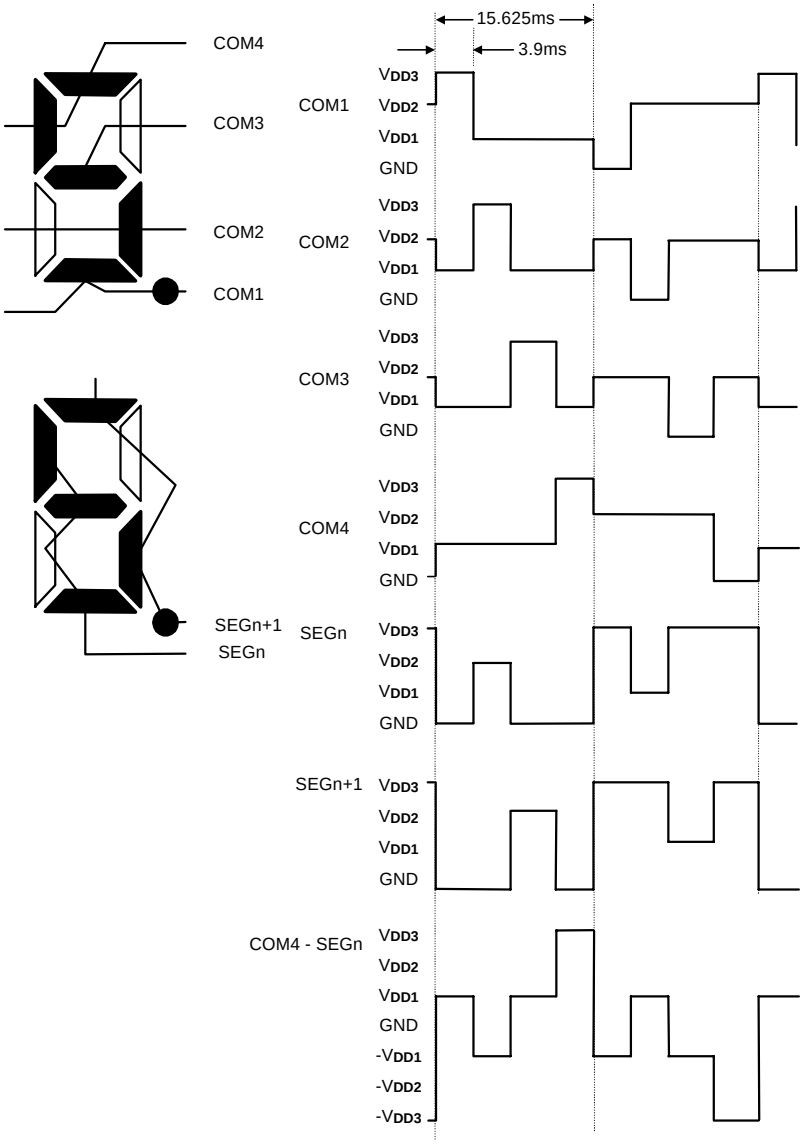
Typical RC oscillator Resistor vs. Frequency: (for reference only)



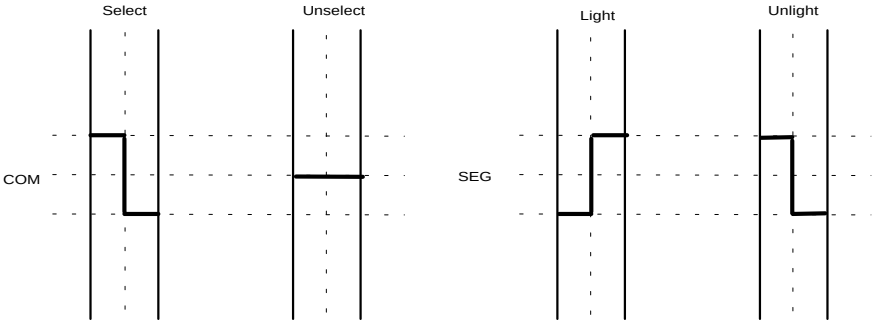
Timing Waveform

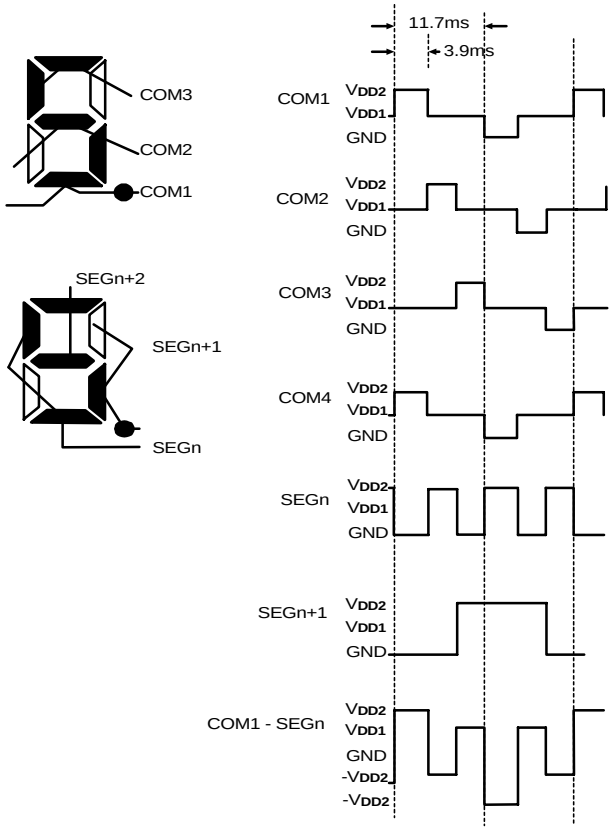
1/4 duty, 1/3 bias LCD waveform



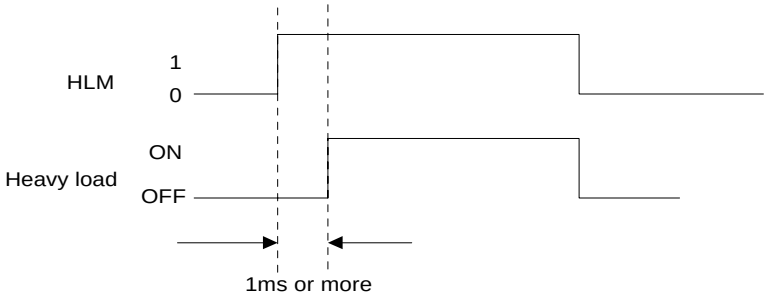


1/3 duty, 1/2 bias LCD waveform





HLM waveform

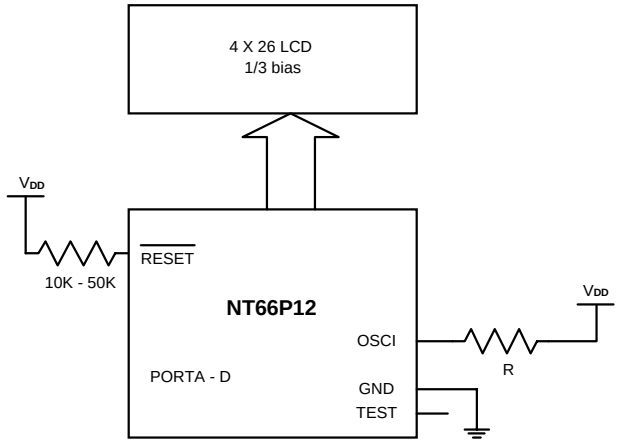


Application Circuits (for reference only)

NT66P12 chip substrate connects to system ground.

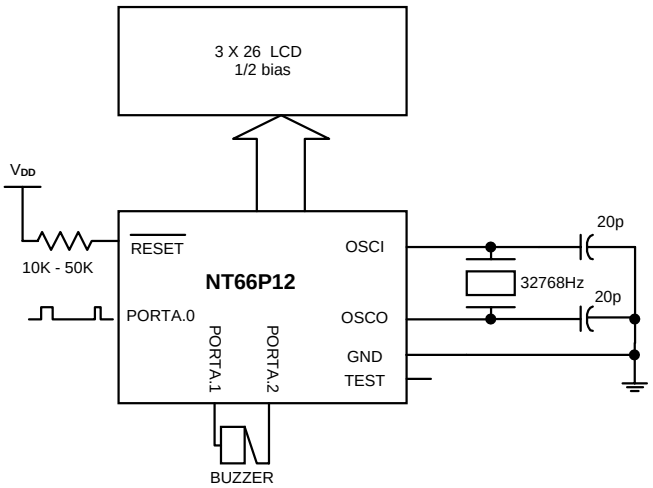
AP1

OSC: 262K RC (code option)
LCD: 1/4 duty, 1/3 bias
PORTA - D: I/O



AP2

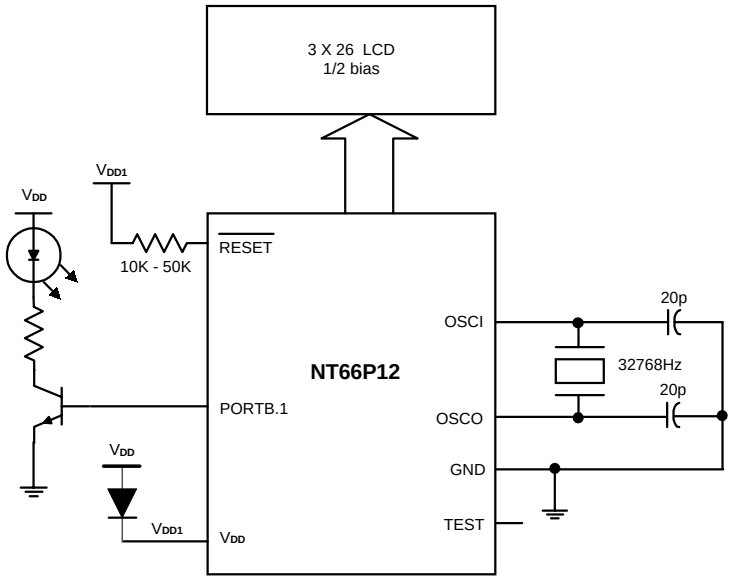
OSC: 32.768KHz crystal (code option)
LCD: 1/3 duty, 1/2 bias
PORTB - D: I/O
PORTA.0: external interrupt
PORTA.1, PORTA.2: ALARM output (carrier frequency: 2KHz or 4KHz code option)



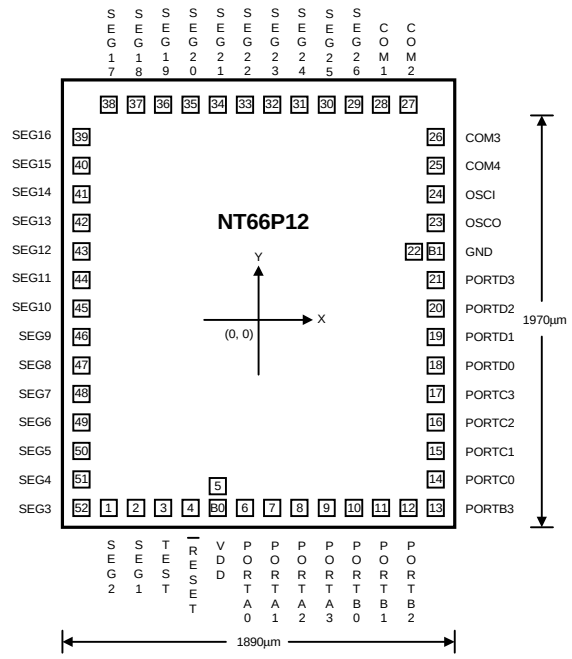
Application Circuits (continued)

AP3

OSC: 32.768KHz crystal (code option)
LCD: 1/3 duty, 1/2 bias
PORTB.1 = Output
When V_{DD} is higher than V_{LCD}, reducing V_{DD} to V_{DD1} can regulate the voltage.



Bonding Diagram



* Substrate connects to GND.
The bonding wire with diameter of 1.0mil is recommended.

Unit: µm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	SEG2	-679.50	-852.50	26	COM3	818.75	759.05
2	SEG1	-563.75	-852.50	27	COM2	688.75	857.50
3	TEST	-425.25	-852.50	28	COM1	563.75	857.50
4	$\overline{\text{RESET}}$	-286.75	-852.50	29	SEG26	438.75	857.50
5	V_{DD}	-164.05	-747.50	30	SEG25	313.75	857.50
	B0	-164.05	-852.50	31	SEG24	188.75	857.50
6	PORTA0	-27.00	-852.50	32	SEG23	63.75	857.50
7	PORTA1	93.00	-852.50	33	SEG22	-61.25	857.50
8	PORTA2	213.00	-852.50	34	SEG21	-186.25	857.50
9	PORTA3	333.00	-852.50	35	SEG20	-311.25	857.50
10	PORTB0	453.00	-852.50	36	SEG19	-436.25	857.50
11	PORTB1	573.00	-852.50	37	SEG18	-561.25	857.50
12	PORTB2	693.00	-852.50	38	SEG17	-686.25	857.50
13	PORTB3	818.75	-852.50	39	SEG16	-818.75	747.50
14	PORTC0	818.75	-722.50	40	SEG15	-818.75	617.50
15	PORTC1	818.75	-597.50	41	SEG14	-818.75	492.50
16	PORTC2	818.75	-477.55	42	SEG13	-818.75	370.00
17	PORTC3	818.75	-357.55	43	SEG12	-818.75	250.00
18	PORTD0	818.75	-237.55	44	SEG11	-818.75	130.00
19	PORTD1	818.75	-117.55	45	SEG10	-818.75	10.00
20	PORTD2	818.75	2.45	46	SEG9	-818.75	-110.00
21	PORTD3	818.75	122.45	47	SEG8	-818.75	-230.00
22	GND	713.75	259.90	48	SEG7	-818.75	-350.00
	B1	818.75	259.90	19	SEG6	-818.75	-470.00
23	OSCO	818.75	379.90	50	SEG5	-818.75	-592.50
24	OSCI	818.75	499.90	51	SEG4	-818.75	-722.50
25	COM4	818.75	629.90	52	SEG3	-818.75	-854.10

Ordering Information

Part No.	Package
NT66P12H	CHIP FORM