

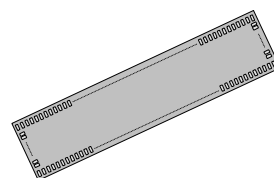
80COMMON x 104RGB LCD DRIVER FOR 4,096-COLOR STN DISPLAY

■ GENERAL DESCRIPTION

The **NJU6818** is an 80COMMON x 104RGB LCD driver for 4,096-color STN display. It contains common drivers, RGB drivers, a serial and a parallel MPU interface circuit, an internal LCD power supply, grayscale palettes and 99,840-bit display data RAM. The segment drivers for RGB (Red, Green, Blue) independently produce optimum 16 grayscales from a built-in 32-grayscale palette, and the LSI achieves 4,096 colors (16x16x16).

In addition, the **NJU6818** operates with a low voltage of 1.7V and a low operating current, therefore it is ideally suited for battery-powered handheld applications.

■ PACKAGE



BUMP CHIP

■ FEATURES

- 4,096-color STN LCD driver
- Built-in LCD Drivers : 80-common Drivers x 104RGB Drivers (312-segment Drivers in B&W)
- Built-in Display Data RAM (DDRAM) : 99,840 bits for Graphic Display
- Programmable Display Mode
 - Variable 16-grayscale Mode : 4,096 Colors
 - Variable 8-grayscale Mode : 256 Colors
 - Fixed 8-grayscale Mode : 256 Colors
 - B&W Mode : Black & White
- 8-/16-bit Parallel Interface Selectable
- 8-/16-bit Bus Length for Display Data Selectable
- 3-/4-line Serial Interface Selectable
- Programmable Duty Ratio and Bias Ratio
- Programmable Internal Voltage Booster : Maximum 6 times
- Programmable Contrast Control : 128-step Electrical Variable Resistor (EVR)
- Various Useful Instructions
- Chip Identification (ID) Function
- Low Operating Current : 450uA Typical at $V_{DD}=3V$, 4-time Boost, Checker Flag Display
- Low Logic Voltage : 1.7V to 3.3V
- Wide LCD Voltage Range : 5.0V to 18.0V
- C-MOS Technology
- Slim Chip for COG
- Package : Bump Chip / TCP

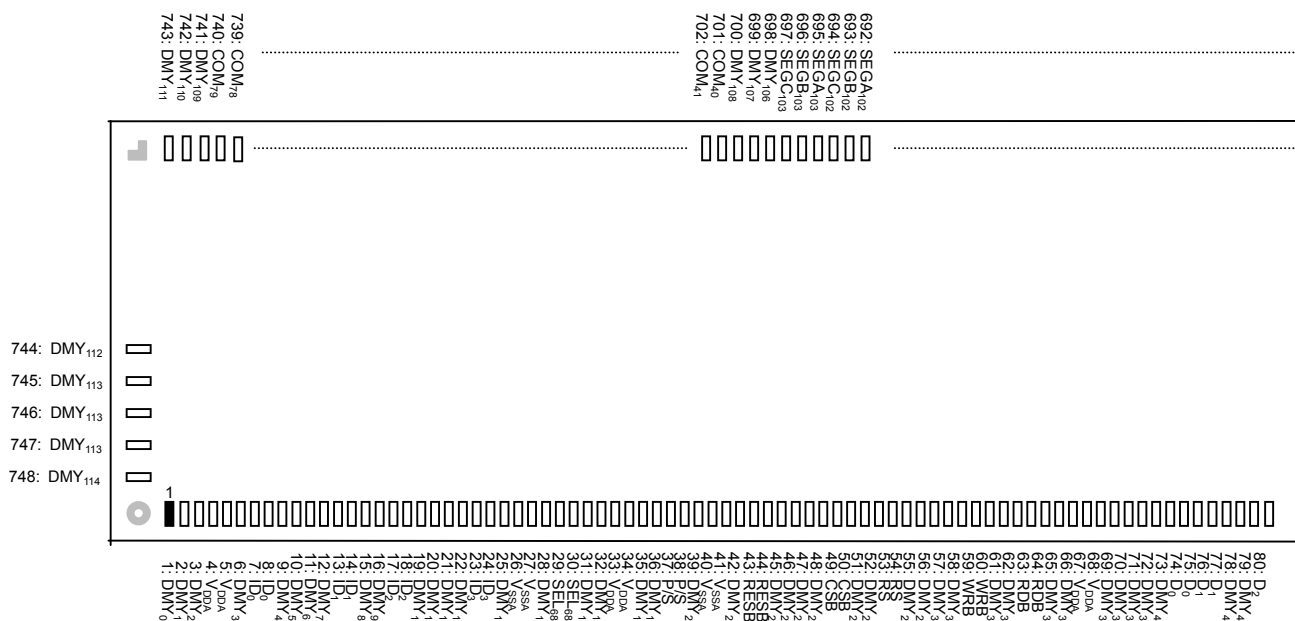
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■ PAD LOCATION

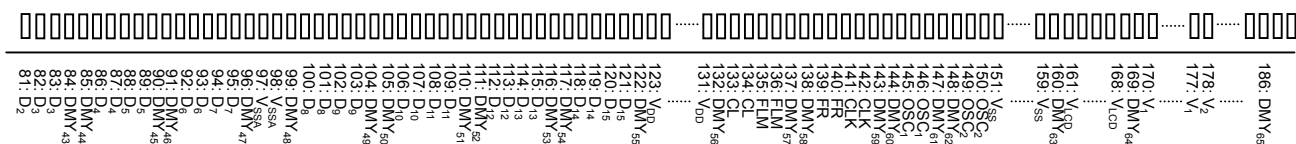


Chip Center :X=0um, Y=0um
 Chip Size :X=19.25mm, Y= 2.50mm
 Chip Thickness :625um ± 25um
 Bump Pitch :45um(Min)
 Bump Space : 19um
 Bump Size : 26um x 120um
 Bump Height :17.5um(Typical)
 Bump Material :Au

NOTE1) Multiple PADs with successive numbers are internally connected.

NOTE2) Dummy PADs, symbolized with DUMMY, are electrically open.

NOTE3) The purpose of this drawing is to show the order of PADs. Use "PAD CORDINATE TABLE 1 to 5" for design.



The diagram shows an L-shaped polygon (a right-angled concave hexagon) with a light gray fill. The dimensions are labeled as follows:

- The top horizontal segment has a width of a .
- The right vertical segment has a height of b .
- The bottom horizontal segment has a width of b .
- The left vertical segment has a height of a .

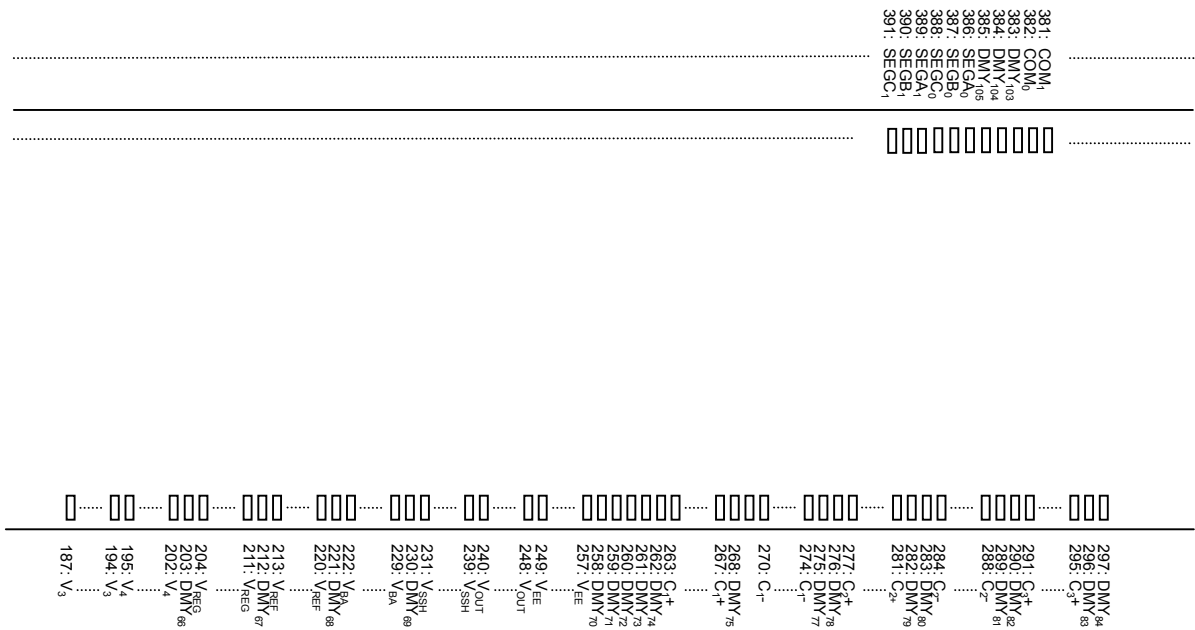
 Dotted lines extend from the corners of the shape to form a bounding box. An arrow points to the top-left corner of the shape, labeled "Alignment Mark Coordinates".

Alignment Mark Coordinates

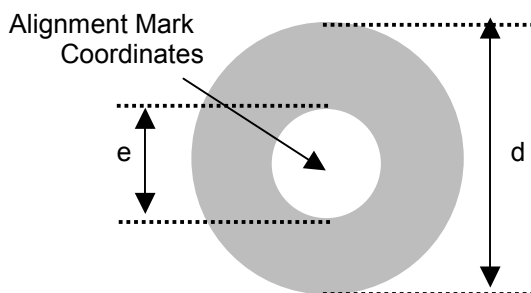
(-9445, 1070)
(9445, -1070)

A diagram showing a gray circular alignment mark. A horizontal dashed line is tangent to the top of the circle. A vertical double-headed arrow labeled c indicates the radius from the center of the circle to the dashed line. An arrow points from the text "Alignment Mark Coordinates" to the center of the circle.

Alignment Mark Coordinates
(9257, -1068)

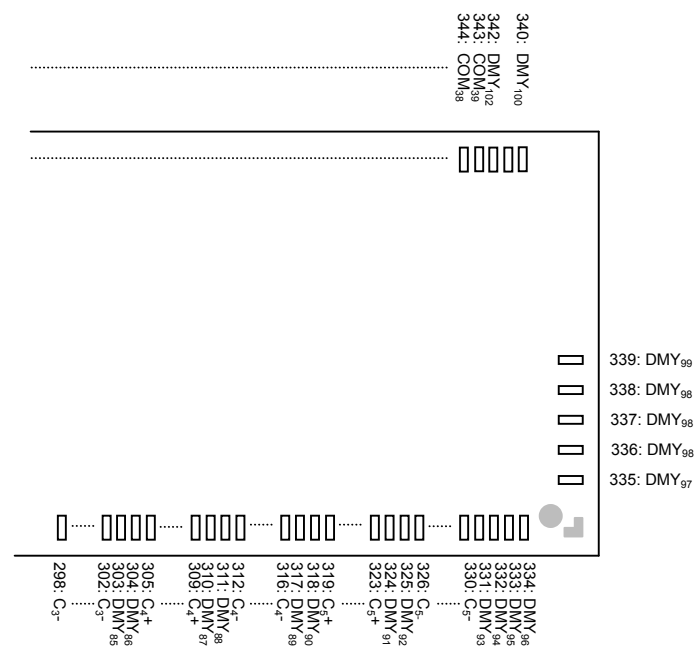


Alignment Mark 3



d : 50 μ m
e : 20 μ m

Alignment Mark Coordinates
(-9257, -1068)



■ PAD COORDINATES 1

Chip Size 19,250μm x 2,500μm (Chip Center 0μm x 0μm)

No.	PAD	X(μm)	Y(μm)	No.	PAD	X(μm)	Y(μm)	No.	PAD	X(μm)	Y(μm)
1	DMY ₀	-9067.5	-1055	52	DMY ₂₇	-6772.5	-1055	103	D ₉	-3487.5	-1055
2	DMY ₁	-9022.5	-1055	53	RS	-6727.5	-1055	104	DMY ₄₉	-3442.5	-1055
3	DMY ₂	-8977.5	-1055	54	RS	-6682.5	-1055	105	DMY ₅₀	-3307.5	-1055
4	V _{DDA}	-8932.5	-1055	55	DMY ₂₈	-6637.5	-1055	106	D ₁₀	-3262.5	-1055
5	V _{DDA}	-8887.5	-1055	56	DMY ₂₉	-6592.5	-1055	107	D ₁₀	-3217.5	-1055
6	DMY ₃	-8842.5	-1055	57	DMY ₃₀	-6547.5	-1055	108	D ₁₁	-3082.5	-1055
7	ID ₀	-8797.5	-1055	58	DMY ₃₁	-6502.5	-1055	109	D ₁₁	-3037.5	-1055
8	ID ₀	-8752.5	-1055	59	WRB	-6457.5	-1055	110	DMY ₅₁	-2992.5	-1055
9	DMY ₄	-8707.5	-1055	60	WRB	-6412.5	-1055	111	DMY ₅₂	-2857.5	-1055
10	DMY ₅	-8662.5	-1055	61	DMY ₃₂	-6367.5	-1055	112	D ₁₂	-2812.5	-1055
11	DMY ₆	-8617.5	-1055	62	DMY ₃₃	-6322.5	-1055	113	D ₁₂	-2767.5	-1055
12	DMY ₇	-8572.5	-1055	63	RDB	-6277.5	-1055	114	D ₁₃	-2632.5	-1055
13	ID ₁	-8527.5	-1055	64	RDB	-6232.5	-1055	115	D ₁₃	-2587.5	-1055
14	ID ₁	-8482.5	-1055	65	DMY ₃₄	-6187.5	-1055	116	DMY ₅₃	-2542.5	-1055
15	DMY ₈	-8437.5	-1055	66	DMY ₃₅	-6142.5	-1055	117	DMY ₅₄	-2407.5	-1055
16	DMY ₉	-8392.5	-1055	67	V _{DDA}	-6097.5	-1055	118	D ₁₄	-2362.5	-1055
17	ID ₂	-8347.5	-1055	68	V _{DDA}	-6052.5	-1055	119	D ₁₄	-2317.5	-1055
18	ID ₂	-8302.5	-1055	69	DMY ₃₆	-6007.5	-1055	120	D ₁₅	-2182.5	-1055
19	DMY ₁₀	-8257.5	-1055	70	DMY ₃₇	-5962.5	-1055	121	D ₁₅	-2137.5	-1055
20	DMY ₁₁	-8212.5	-1055	71	DMY ₃₈	-5917.5	-1055	122	DMY ₅₅	-2092.5	-1055
21	DMY ₁₂	-8167.5	-1055	72	DMY ₃₉	-5872.5	-1055	123	V _{DD}	-1957.5	-1055
22	DMY ₁₃	-8122.5	-1055	73	DMY ₄₀	-5737.5	-1055	124	V _{DD}	-1912.5	-1055
23	ID ₃	-8077.5	-1055	74	D ₀ /SCL	-5692.5	-1055	125	V _{DD}	-1867.5	-1055
24	ID ₃	-8032.5	-1055	75	D ₀ /SCL	-5647.5	-1055	126	V _{DD}	-1822.5	-1055
25	DMY ₁₄	-7987.5	-1055	76	D ₁ /SDA	-5512.5	-1055	127	V _{DD}	-1777.5	-1055
26	V _{SSA}	-7942.5	-1055	77	D ₁ /SDA	-5467.5	-1055	128	V _{DD}	-1732.5	-1055
27	V _{SSA}	-7897.5	-1055	78	DMY ₄₁	-5422.5	-1055	129	V _{DD}	-1687.5	-1055
28	DMY ₁₅	-7852.5	-1055	79	DMY ₄₂	-5287.5	-1055	130	V _{DD}	-1642.5	-1055
29	SEL ₆₈	-7807.5	-1055	80	D ₂	-5242.5	-1055	131	V _{DD}	-1597.5	-1055
30	SEL ₆₈	-7762.5	-1055	81	D ₂	-5197.5	-1055	132	DMY ₅₆	-1372.5	-1055
31	DMY ₁₆	-7717.5	-1055	82	D ₃ /SMODE	-5062.5	-1055	133	CL	-1327.5	-1055
32	DMY ₁₇	-7672.5	-1055	83	D ₃ /SMODE	-5017.5	-1055	134	CL	-1282.5	-1055
33	V _{DDA}	-7627.5	-1055	84	DMY ₄₃	-4972.5	-1055	135	FLM	-1147.5	-1055
34	V _{DDA}	-7582.5	-1055	85	DMY ₄₄	-4837.5	-1055	136	FLM	-1102.5	-1055
35	DMY ₁₈	-7537.5	-1055	86	D ₄ /SPOL	-4792.5	-1055	137	DMY ₅₇	-1057.5	-1055
36	DMY ₁₉	-7492.5	-1055	87	D ₄ /SPOL	-4747.5	-1055	138	DMY ₅₈	-922.5	-1055
37	P/S	-7447.5	-1055	88	D ₅	-4612.5	-1055	139	FR	-877.5	-1055
38	P/S	-7402.5	-1055	89	D ₅	-4567.5	-1055	140	FR	-832.5	-1055
39	DMY ₂₀	-7357.5	-1055	90	DMY ₄₅	-4522.5	-1055	141	CLK	-697.5	-1055
40	V _{SSA}	-7312.5	-1055	91	DMY ₄₆	-4387.5	-1055	142	CLK	-652.5	-1055
41	V _{SSA}	-7267.5	-1055	92	D ₆	-4342.5	-1055	143	DMY ₅₉	-607.5	-1055
42	DMY ₂₁	-7222.5	-1055	93	D ₆	-4297.5	-1055	144	DMY ₆₀	-472.5	-1055
43	RESB	-7177.5	-1055	94	D ₇	-4162.5	-1055	145	OSC ₁	-427.5	-1055
44	RESB	-7132.5	-1055	95	D ₇	-4117.5	-1055	146	OSC ₁	-382.5	-1055
45	DMY ₂₂	-7087.5	-1055	96	DMY ₄₇	-4072.5	-1055	147	DMY ₆₁	-337.5	-1055
46	DMY ₂₃	-7042.5	-1055	97	V _{SSA}	-3937.5	-1055	148	DMY ₆₂	-292.5	-1055
47	DMY ₂₄	-6997.5	-1055	98	V _{SSA}	-3892.5	-1055	149	OSC ₂	-157.5	-1055
48	DMY ₂₅	-6952.5	-1055	99	DMY ₄₈	-3757.5	-1055	150	OSC ₂	-112.5	-1055
49	CSB	-6907.5	-1055	100	D ₈	-3712.5	-1055	151	V _{SS}	22.5	-1055
50	CSB	-6862.5	-1055	101	D ₈	-3667.5	-1055	152	V _{SS}	67.5	-1055
51	DMY ₂₆	-6817.5	-1055	102	D ₉	-3532.5	-1055	153	V _{SS}	112.5	-1055

■ PAD COORDINATES 2

Chip Size 19,250μm x 2,500μm (Chip Center 0μm x 0μm)

No.	PAD	X(μm)	Y(μm)	No.	PAD	X(μm)	Y(μm)	No.	PAD	X(μm)	Y(μm)
154	V _{SS}	157.5	-1055	205	V _{REG}	2812.5	-1055	256	V _{EE}	5467.5	-1055
155	V _{SS}	202.5	-1055	206	V _{REG}	2857.5	-1055	257	V _{EE}	5512.5	-1055
156	V _{SS}	247.5	-1055	207	V _{REG}	2902.5	-1055	258	DMY ₇₀	5647.5	-1055
157	V _{SS}	292.5	-1055	208	V _{REG}	2947.5	-1055	259	DMY ₇₁	5692.5	-1055
158	V _{SS}	337.5	-1055	209	V _{REG}	2992.5	-1055	260	DMY ₇₂	5737.5	-1055
159	V _{SS}	382.5	-1055	210	V _{REG}	3037.5	-1055	261	DMY ₇₃	5782.5	-1055
160	DMY ₆₃	517.5	-1055	211	V _{REG}	3082.5	-1055	262	DMY ₇₄	5827.5	-1055
161	V _{LCD}	652.5	-1055	212	DMY ₆₇	3127.5	-1055	263	C1+	5872.5	-1055
162	V _{LCD}	697.5	-1055	213	V _{REF}	3172.5	-1055	264	C1+	5917.5	-1055
163	V _{LCD}	742.5	-1055	214	V _{REF}	3217.5	-1055	265	C1+	5962.5	-1055
164	V _{LCD}	787.5	-1055	215	V _{REF}	3262.5	-1055	266	C1+	6007.5	-1055
165	V _{LCD}	832.5	-1055	216	V _{REF}	3307.5	-1055	267	C1+	6052.5	-1055
166	V _{LCD}	877.5	-1055	217	V _{REF}	3352.5	-1055	268	DMY ₇₅	6097.5	-1055
167	V _{LCD}	922.5	-1055	218	V _{REF}	3397.5	-1055	269	DMY ₇₆	6142.5	-1055
168	V _{LCD}	967.5	-1055	219	V _{REF}	3442.5	-1055	270	C1-	6187.5	-1055
169	DMY ₆₄	1012.5	-1055	220	V _{REF}	3487.5	-1055	271	C1-	6232.5	-1055
170	V ₁	1057.5	-1055	221	DMY ₆₈	3532.5	-1055	272	C1-	6277.5	-1055
171	V ₁	1102.5	-1055	222	V _{BA}	3577.5	-1055	273	C1-	6322.5	-1055
172	V ₁	1147.5	-1055	223	V _{BA}	3622.5	-1055	274	C1-	6367.5	-1055
173	V ₁	1192.5	-1055	224	V _{BA}	3667.5	-1055	275	DMY ₇₇	6412.5	-1055
174	V ₁	1237.5	-1055	225	V _{BA}	3712.5	-1055	276	DMY ₇₈	6457.5	-1055
175	V ₁	1282.5	-1055	226	V _{BA}	3757.5	-1055	277	C2+	6502.5	-1055
176	V ₁	1327.5	-1055	227	V _{BA}	3802.5	-1055	278	C2+	6547.5	-1055
177	V ₁	1372.5	-1055	228	V _{BA}	3847.5	-1055	279	C2+	6592.5	-1055
178	V ₂	1507.5	-1055	229	V _{BA}	3892.5	-1055	280	C2+	6637.5	-1055
179	V ₂	1552.5	-1055	230	DMY ₆₉	3937.5	-1055	281	C2+	6682.5	-1055
180	V ₂	1597.5	-1055	231	V _{SSH}	3982.5	-1055	282	DMY ₇₉	6727.5	-1055
181	V ₂	1642.5	-1055	232	V _{SSH}	4027.5	-1055	283	DMY ₈₀	6772.5	-1055
182	V ₂	1687.5	-1055	233	V _{SSH}	4072.5	-1055	284	C2-	6817.5	-1055
183	V ₂	1732.5	-1055	234	V _{SSH}	4117.5	-1055	285	C2-	6862.5	-1055
184	V ₂	1777.5	-1055	235	V _{SSH}	4162.5	-1055	286	C2-	6907.5	-1055
185	V ₂	1822.5	-1055	236	V _{SSH}	4207.5	-1055	287	C2-	6952.5	-1055
186	DMY ₆₅	1867.5	-1055	237	V _{SSH}	4252.5	-1055	288	C2-	6997.5	-1055
187	V ₃	1912.5	-1055	238	V _{SSH}	4297.5	-1055	289	DMY ₈₁	7042.5	-1055
188	V ₃	1957.5	-1055	239	V _{SSH}	4342.5	-1055	290	DMY ₈₂	7087.5	-1055
189	V ₃	2002.5	-1055	240	V _{OUT}	4567.5	-1055	291	C3+	7132.5	-1055
190	V ₃	2047.5	-1055	241	V _{OUT}	4612.5	-1055	292	C3+	7177.5	-1055
191	V ₃	2092.5	-1055	242	V _{OUT}	4657.5	-1055	293	C3+	7222.5	-1055
192	V ₃	2137.5	-1055	243	V _{OUT}	4702.5	-1055	294	C3+	7267.5	-1055
193	V ₃	2182.5	-1055	244	V _{OUT}	4747.5	-1055	295	C3+	7312.5	-1055
194	V ₃	2227.5	-1055	245	V _{OUT}	4792.5	-1055	296	DMY ₈₃	7357.5	-1055
195	V ₄	2362.5	-1055	246	V _{OUT}	4837.5	-1055	297	DMY ₈₄	7402.5	-1055
196	V ₄	2407.5	-1055	247	V _{OUT}	4882.5	-1055	298	C3-	7447.5	-1055
197	V ₄	2452.5	-1055	248	V _{OUT}	4927.5	-1055	299	C3-	7492.5	-1055
198	V ₄	2497.5	-1055	249	V _{EE}	5152.5	-1055	300	C3-	7537.5	-1055
199	V ₄	2542.5	-1055	250	V _{EE}	5197.5	-1055	301	C3-	7582.5	-1055
200	V ₄	2587.5	-1055	251	V _{EE}	5242.5	-1055	302	C3-	7627.5	-1055
201	V ₄	2632.5	-1055	252	V _{EE}	5287.5	-1055	303	DMY ₈₅	7672.5	-1055
202	V ₄	2677.5	-1055	253	V _{EE}	5332.5	-1055	304	DMY ₈₆	7717.5	-1055
203	DMY ₆₆	2722.5	-1055	254	V _{EE}	5377.5	-1055	305	C4+	7762.5	-1055
204	V _{REG}	2767.5	-1055	255	V _{EE}	5422.5	-1055	306	C4+	7807.5	-1055

■ PAD COORDINATES 3

Chip Size 19,250μm x 2,500μm (Chip Center 0μm x 0μm)

No.	PAD	X(μm)	Y(μm)	No.	PAD	X(μm)	Y(μm)	No.	PAD	X(μm)	Y(μm)
307	C ₄ +	7852.5	-1055	358	COM ₂₄	8257.5	1055	409	SEGC ₇	5962.5	1055
308	C ₄ +	7897.5	-1055	359	COM ₂₃	8212.5	1055	410	SEGA ₈	5917.5	1055
309	C ₄ +	7942.5	-1055	360	COM ₂₂	8167.5	1055	411	SEGB ₈	5872.5	1055
310	DMY ₈₇	7987.5	-1055	361	COM ₂₁	8122.5	1055	412	SEGC ₈	5827.5	1055
311	DMY ₈₈	8032.5	-1055	362	COM ₂₀	8077.5	1055	413	SEGA ₉	5782.5	1055
312	C ₄ -	8077.5	-1055	363	COM ₁₉	8032.5	1055	414	SEGB ₉	5737.5	1055
313	C ₄ -	8122.5	-1055	364	COM ₁₈	7987.5	1055	415	SEGC ₉	5692.5	1055
314	C ₄ -	8167.5	-1055	365	COM ₁₇	7942.5	1055	416	SEGA ₁₀	5647.5	1055
315	C ₄ -	8212.5	-1055	366	COM ₁₆	7897.5	1055	417	SEGB ₁₀	5602.5	1055
316	C ₄ -	8257.5	-1055	367	COM ₁₅	7852.5	1055	418	SEGC ₁₀	5557.5	1055
317	DMY ₈₉	8302.5	-1055	368	COM ₁₄	7807.5	1055	419	SEGA ₁₁	5512.5	1055
318	DMY ₉₀	8347.5	-1055	369	COM ₁₃	7762.5	1055	420	SEGB ₁₁	5467.5	1055
319	C ₅ +	8392.5	-1055	370	COM ₁₂	7717.5	1055	421	SEGC ₁₁	5422.5	1055
320	C ₅ +	8437.5	-1055	371	COM ₁₁	7672.5	1055	422	SEGA ₁₂	5377.5	1055
321	C ₅ +	8482.5	-1055	372	COM ₁₀	7627.5	1055	423	SEGB ₁₂	5332.5	1055
322	C ₅ +	8527.5	-1055	373	COM ₉	7582.5	1055	424	SEGC ₁₂	5287.5	1055
323	C ₅ +	8572.5	-1055	374	COM ₈	7537.5	1055	425	SEGA ₁₃	5242.5	1055
324	DMY ₉₁	8617.5	-1055	375	COM ₇	7492.5	1055	426	SEGB ₁₃	5197.5	1055
325	DMY ₉₂	8662.5	-1055	376	COM ₆	7447.5	1055	427	SEGC ₁₃	5152.5	1055
326	C ₅ -	8707.5	-1055	377	COM ₅	7402.5	1055	428	SEGA ₁₄	5107.5	1055
327	C ₅ -	8752.5	-1055	378	COM ₄	7357.5	1055	429	SEGB ₁₄	5062.5	1055
328	C ₅ -	8797.5	-1055	379	COM ₃	7312.5	1055	430	SEGC ₁₄	5017.5	1055
329	C ₅ -	8842.5	-1055	380	COM ₂	7267.5	1055	431	SEGA ₁₅	4972.5	1055
330	C ₅ -	8887.5	-1055	381	COM ₁	7222.5	1055	432	SEGB ₁₅	4927.5	1055
331	DMY ₉₃	8932.5	-1055	382	COM ₀	7177.5	1055	433	SEGC ₁₅	4882.5	1055
332	DMY ₉₄	8977.5	-1055	383	DMY ₁₀₃	7132.5	1055	434	SEGA ₁₆	4837.5	1055
333	DMY ₉₅	9022.5	-1055	384	DMY ₁₀₄	7087.5	1055	435	SEGB ₁₆	4792.5	1055
334	DMY ₉₆	9067.5	-1055	385	DMY ₁₀₅	7042.5	1055	436	SEGC ₁₆	4747.5	1055
335	DMY ₉₇	9430	-964	386	SEGA ₀	6997.5	1055	437	SEGA ₁₇	4702.5	1055
336	DMY ₉₈	9430	-919	387	SEGB ₀	6952.5	1055	438	SEGB ₁₇	4657.5	1055
337	DMY ₉₈	9430	-874	388	SEGC ₀	6907.5	1055	439	SEGC ₁₇	4612.5	1055
338	DMY ₉₈	9430	-829	389	SEGA ₁	6862.5	1055	440	SEGA ₁₈	4567.5	1055
339	DMY ₉₉	9430	-784	390	SEGB ₁	6817.5	1055	441	SEGB ₁₈	4522.5	1055
340	DMY ₁₀₀	9067.5	1055	391	SEGC ₁	6772.5	1055	442	SEGC ₁₈	4477.5	1055
341	DMY ₁₀₁	9022.5	1055	392	SEGA ₂	6727.5	1055	443	SEGA ₁₉	4432.5	1055
342	DMY ₁₀₂	8977.5	1055	393	SEGB ₂	6682.5	1055	444	SEGB ₁₉	4387.5	1055
343	COM ₃₉	8932.5	1055	394	SEGC ₂	6637.5	1055	445	SEGC ₁₉	4342.5	1055
344	COM ₃₈	8887.5	1055	395	SEGA ₃	6592.5	1055	446	SEGA ₂₀	4297.5	1055
345	COM ₃₇	8842.5	1055	396	SEGB ₃	6547.5	1055	447	SEGB ₂₀	4252.5	1055
346	COM ₃₆	8797.5	1055	397	SEGC ₃	6502.5	1055	448	SEGC ₂₀	4207.5	1055
347	COM ₃₅	8752.5	1055	398	SEGA ₄	6457.5	1055	449	SEGA ₂₁	4162.5	1055
348	COM ₃₄	8707.5	1055	399	SEGB ₄	6412.5	1055	450	SEGB ₂₁	4117.5	1055
349	COM ₃₃	8662.5	1055	400	SEGC ₄	6367.5	1055	451	SEGC ₂₁	4072.5	1055
350	COM ₃₂	8617.5	1055	401	SEGA ₅	6322.5	1055	452	SEGA ₂₂	4027.5	1055
351	COM ₃₁	8572.5	1055	402	SEGB ₅	6277.5	1055	453	SEGB ₂₂	3982.5	1055
352	COM ₃₀	8527.5	1055	403	SEGC ₅	6232.5	1055	454	SEGC ₂₂	3937.5	1055
353	COM ₂₉	8482.5	1055	404	SEGA ₆	6187.5	1055	455	SEGA ₂₃	3892.5	1055
354	COM ₂₈	8437.5	1055	405	SEGB ₆	6142.5	1055	456	SEGB ₂₃	3847.5	1055
355	COM ₂₇	8392.5	1055	406	SEGC ₆	6097.5	1055	457	SEGC ₂₃	3802.5	1055
356	COM ₂₆	8347.5	1055	407	SEGA ₇	6052.5	1055	458	SEGA ₂₄	3757.5	1055
357	COM ₂₅	8302.5	1055	408	SEGB ₇	6007.5	1055	459	SEGB ₂₄	3712.5	1055

■ PAD COORDINATES 4

Chip Size 19,250μm x 2,500μm (Chip Center 0μm x 0μm)

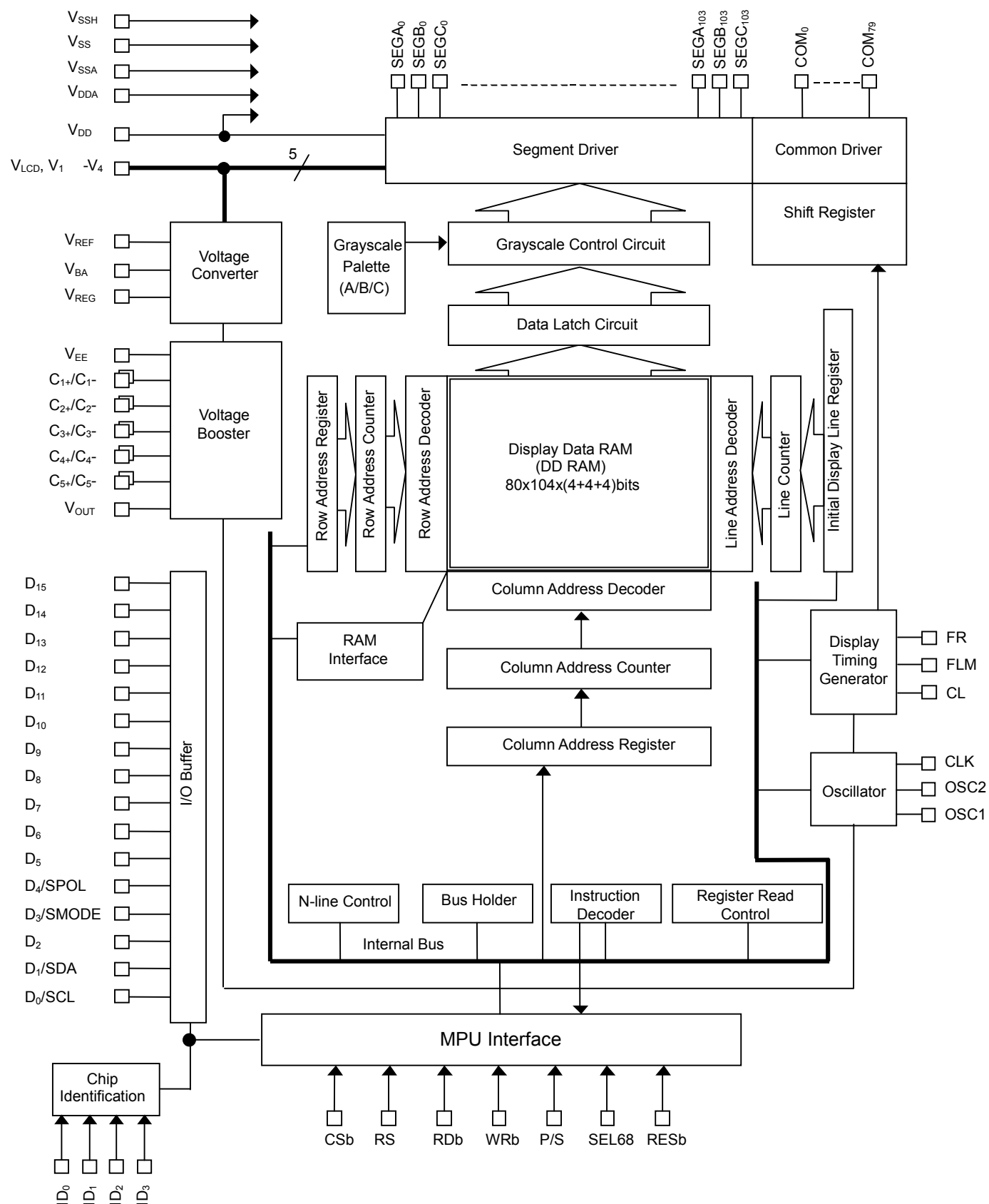
No.	PAD	X(μm)	Y(μm)	No.	PAD	X(μm)	Y(μm)	No.	PAD	X(μm)	Y(μm)
460	SEGC ₂₄	3667.5	1055	511	SEGC ₄₁	1372.5	1055	562	SEGC ₅₈	-922.5	1055
461	SEGA ₂₅	3622.5	1055	512	SEGA ₄₂	1327.5	1055	563	SEGA ₅₉	-967.5	1055
462	SEGB ₂₅	3577.5	1055	513	SEGB ₄₂	1282.5	1055	564	SEGB ₅₉	-1012.5	1055
463	SEGC ₂₅	3532.5	1055	514	SEGC ₄₂	1237.5	1055	565	SEGC ₅₉	-1057.5	1055
464	SEGA ₂₆	3487.5	1055	515	SEGA ₄₃	1192.5	1055	566	SEGA ₆₀	-1102.5	1055
465	SEGB ₂₆	3442.5	1055	516	SEGB ₄₃	1147.5	1055	567	SEGB ₆₀	-1147.5	1055
466	SEGC ₂₆	3397.5	1055	517	SEGC ₄₃	1102.5	1055	568	SEGC ₆₀	-1192.5	1055
467	SEGA ₂₇	3352.5	1055	518	SEGA ₄₄	1057.5	1055	569	SEGA ₆₁	-1237.5	1055
468	SEGB ₂₇	3307.5	1055	519	SEGB ₄₄	1012.5	1055	570	SEGB ₆₁	-1282.5	1055
469	SEGC ₂₇	3262.5	1055	520	SEGC ₄₄	967.5	1055	571	SEGC ₆₁	-1327.5	1055
470	SEGA ₂₈	3217.5	1055	521	SEGA ₄₅	922.5	1055	572	SEGA ₆₂	-1372.5	1055
471	SEGB ₂₈	3172.5	1055	522	SEGB ₄₅	877.5	1055	573	SEGB ₆₂	-1417.5	1055
472	SEGC ₂₈	3127.5	1055	523	SEGC ₄₅	832.5	1055	574	SEGC ₆₂	-1462.5	1055
473	SEGA ₂₉	3082.5	1055	524	SEGA ₄₆	787.5	1055	575	SEGA ₆₃	-1507.5	1055
474	SEGB ₂₉	3037.5	1055	525	SEGB ₄₆	742.5	1055	576	SEGB ₆₃	-1552.5	1055
475	SEGC ₂₉	2992.5	1055	526	SEGC ₄₆	697.5	1055	577	SEGC ₆₃	-1597.5	1055
476	SEGA ₃₀	2947.5	1055	527	SEGA ₄₇	652.5	1055	578	SEGA ₆₄	-1642.5	1055
477	SEGB ₃₀	2902.5	1055	528	SEGB ₄₇	607.5	1055	579	SEGB ₆₄	-1687.5	1055
478	SEGC ₃₀	2857.5	1055	529	SEGC ₄₇	562.5	1055	580	SEGC ₆₄	-1732.5	1055
479	SEGA ₃₁	2812.5	1055	530	SEGA ₄₈	517.5	1055	581	SEGA ₆₅	-1777.5	1055
480	SEGB ₃₁	2767.5	1055	531	SEGB ₄₈	472.5	1055	582	SEGB ₆₅	-1822.5	1055
481	SEGC ₃₁	2722.5	1055	532	SEGC ₄₈	427.5	1055	583	SEGC ₆₅	-1867.5	1055
482	SEGA ₃₂	2677.5	1055	533	SEGA ₄₉	382.5	1055	584	SEGA ₆₆	-1912.5	1055
483	SEGB ₃₂	2632.5	1055	534	SEGB ₄₉	337.5	1055	585	SEGB ₆₆	-1957.5	1055
484	SEGC ₃₂	2587.5	1055	535	SEGC ₄₉	292.5	1055	586	SEGC ₆₆	-2002.5	1055
485	SEGA ₃₃	2542.5	1055	536	SEGA ₅₀	247.5	1055	587	SEGA ₆₇	-2047.5	1055
486	SEGB ₃₃	2497.5	1055	537	SEGB ₅₀	202.5	1055	588	SEGB ₆₇	-2092.5	1055
487	SEGC ₃₃	2452.5	1055	538	SEGC ₅₀	157.5	1055	589	SEGC ₆₇	-2137.5	1055
488	SEGA ₃₄	2407.5	1055	539	SEGA ₅₁	112.5	1055	590	SEGA ₆₈	-2182.5	1055
489	SEGB ₃₄	2362.5	1055	540	SEGB ₅₁	67.5	1055	591	SEGB ₆₈	-2227.5	1055
490	SEGC ₃₄	2317.5	1055	541	SEGC ₅₁	22.5	1055	592	SEGC ₆₈	-2272.5	1055
491	SEGA ₃₅	2272.5	1055	542	SEGA ₅₂	-22.5	1055	593	SEGA ₆₉	-2317.5	1055
492	SEGB ₃₅	2227.5	1055	543	SEGB ₅₂	-67.5	1055	594	SEGB ₆₉	-2362.5	1055
493	SEGC ₃₅	2182.5	1055	544	SEGC ₅₂	-112.5	1055	595	SEGC ₆₉	-2407.5	1055
494	SEGA ₃₆	2137.5	1055	545	SEGA ₅₃	-157.5	1055	596	SEGA ₇₀	-2452.5	1055
495	SEGB ₃₆	2092.5	1055	546	SEGB ₅₃	-202.5	1055	597	SEGB ₇₀	-2497.5	1055
496	SEGC ₃₆	2047.5	1055	547	SEGC ₅₃	-247.5	1055	598	SEGC ₇₀	-2542.5	1055
497	SEGA ₃₇	2002.5	1055	548	SEGA ₅₄	-292.5	1055	599	SEGA ₇₁	-2587.5	1055
498	SEGB ₃₇	1957.5	1055	549	SEGB ₅₄	-337.5	1055	600	SEGB ₇₁	-2632.5	1055
499	SEGC ₃₇	1912.5	1055	550	SEGC ₅₄	-382.5	1055	601	SEGC ₇₁	-2677.5	1055
500	SEGA ₃₈	1867.5	1055	551	SEGA ₅₅	-427.5	1055	602	SEGA ₇₂	-2722.5	1055
501	SEGB ₃₈	1822.5	1055	552	SEGB ₅₅	-472.5	1055	603	SEGB ₇₂	-2767.5	1055
502	SEGC ₃₈	1777.5	1055	553	SEGC ₅₅	-517.5	1055	604	SEGC ₇₂	-2812.5	1055
503	SEGA ₃₉	1732.5	1055	554	SEGA ₅₆	-562.5	1055	605	SEGA ₇₃	-2857.5	1055
504	SEGB ₃₉	1687.5	1055	555	SEGB ₅₆	-607.5	1055	606	SEGB ₇₃	-2902.5	1055
505	SEGC ₃₉	1642.5	1055	556	SEGC ₅₆	-652.5	1055	607	SEGC ₇₃	-2947.5	1055
506	SEGA ₄₀	1597.5	1055	557	SEGA ₅₇	-697.5	1055	608	SEGA ₇₄	-2992.5	1055
507	SEGB ₄₀	1552.5	1055	558	SEGB ₅₇	-742.5	1055	609	SEGB ₇₄	-3037.5	1055
508	SEGC ₄₀	1507.5	1055	559	SEGC ₅₇	-787.5	1055	610	SEGC ₇₄	-3082.5	1055
509	SEGA ₄₁	1462.5	1055	560	SEGA ₅₈	-832.5	1055	611	SEGA ₇₅	-3127.5	1055
510	SEGB ₄₁	1417.5	1055	561	SEGB ₅₈	-877.5	1055	612	SEGB ₇₅	-3172.5	1055

■ PAD COORDINATES 5

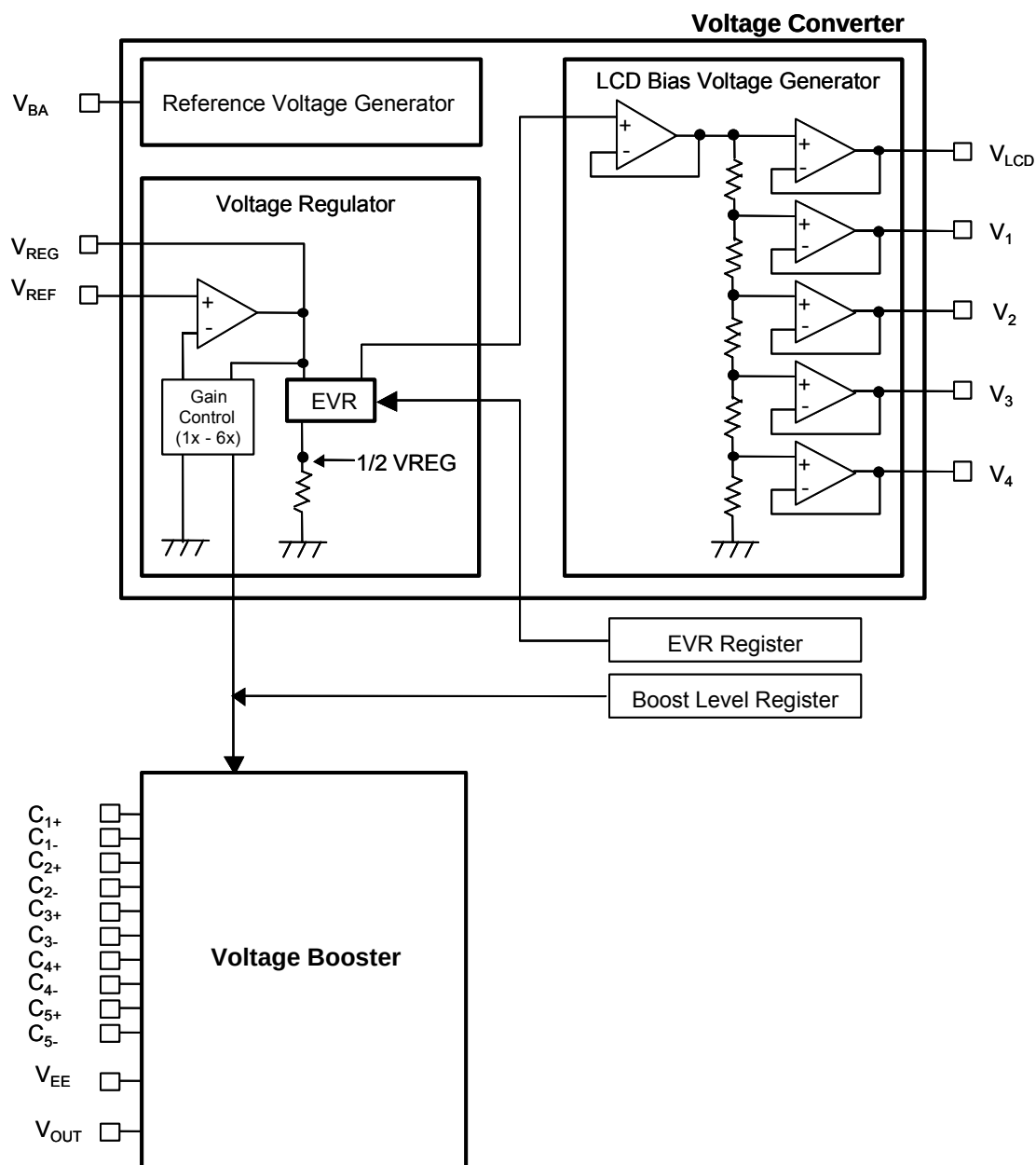
Chip Size 19,250μm x 2,500μm (Chip Center 0μm x 0μm)

No.	PAD	X(μm)	Y(μm)	No.	PAD	X(μm)	Y(μm)	No.	PAD	X(μm)	Y(μm)
613	SEGC ₇₅	-3217.5	1055	664	SEGC ₉₂	-5512.5	1055	715	COM ₅₄	-7807.5	1055
614	SEGA ₇₆	-3262.5	1055	665	SEGA ₉₃	-5557.5	1055	716	COM ₅₅	-7852.5	1055
615	SEGB ₇₆	-3307.5	1055	666	SEGB ₉₃	-5602.5	1055	717	COM ₅₆	-7897.5	1055
616	SEGC ₇₆	-3352.5	1055	667	SEGC ₉₃	-5647.5	1055	718	COM ₅₇	-7942.5	1055
617	SEGA ₇₇	-3397.5	1055	668	SEGA ₉₄	-5692.5	1055	719	COM ₅₈	-7987.5	1055
618	SEGB ₇₇	-3442.5	1055	669	SEGB ₉₄	-5737.5	1055	720	COM ₅₉	-8032.5	1055
619	SEGC ₇₇	-3487.5	1055	670	SEGC ₉₄	-5782.5	1055	721	COM ₆₀	-8077.5	1055
620	SEGA ₇₈	-3532.5	1055	671	SEGA ₉₅	-5827.5	1055	722	COM ₆₁	-8122.5	1055
621	SEGB ₇₈	-3577.5	1055	672	SEGB ₉₅	-5872.5	1055	723	COM ₆₂	-8167.5	1055
622	SEGC ₇₈	-3622.5	1055	673	SEGC ₉₅	-5917.5	1055	724	COM ₆₃	-8212.5	1055
623	SEGA ₇₉	-3667.5	1055	674	SEGA ₉₆	-5962.5	1055	725	COM ₆₄	-8257.5	1055
624	SEGB ₇₉	-3712.5	1055	675	SEGB ₉₆	-6007.5	1055	726	COM ₆₅	-8302.5	1055
625	SEGC ₇₉	-3757.5	1055	676	SEGC ₉₆	-6052.5	1055	727	COM ₆₆	-8347.5	1055
626	SEGA ₈₀	-3802.5	1055	677	SEGA ₉₇	-6097.5	1055	728	COM ₆₇	-8392.5	1055
627	SEGB ₈₀	-3847.5	1055	678	SEGB ₉₇	-6142.5	1055	729	COM ₆₈	-8437.5	1055
628	SEGC ₈₀	-3892.5	1055	679	SEGC ₉₇	-6187.5	1055	730	COM ₆₉	-8482.5	1055
629	SEGA ₈₁	-3937.5	1055	680	SEGA ₉₈	-6232.5	1055	731	COM ₇₀	-8527.5	1055
630	SEGB ₈₁	-3982.5	1055	681	SEGB ₉₈	-6277.5	1055	732	COM ₇₁	-8572.5	1055
631	SEGC ₈₁	-4027.5	1055	682	SEGC ₉₈	-6322.5	1055	733	COM ₇₂	-8617.5	1055
632	SEGA ₈₂	-4072.5	1055	683	SEGA ₉₉	-6367.5	1055	734	COM ₇₃	-8662.5	1055
633	SEGB ₈₂	-4117.5	1055	684	SEGB ₉₉	-6412.5	1055	735	COM ₇₄	-8707.5	1055
634	SEGC ₈₂	-4162.5	1055	685	SEGC ₉₉	-6457.5	1055	736	COM ₇₅	-8752.5	1055
635	SEGA ₈₃	-4207.5	1055	686	SEGA ₁₀₀	-6502.5	1055	737	COM ₇₆	-8797.5	1055
636	SEGB ₈₃	-4252.5	1055	687	SEGB ₁₀₀	-6547.5	1055	738	COM ₇₇	-8842.5	1055
637	SEGC ₈₃	-4297.5	1055	688	SEGC ₁₀₀	-6592.5	1055	739	COM ₇₈	-8887.5	1055
638	SEGA ₈₄	-4342.5	1055	689	SEGA ₁₀₁	-6637.5	1055	740	COM ₇₉	-8932.5	1055
639	SEGB ₈₄	-4387.5	1055	690	SEGB ₁₀₁	-6682.5	1055	741	DMY ₁₀₉	-8977.5	1055
640	SEGC ₈₄	-4432.5	1055	691	SEGC ₁₀₁	-6727.5	1055	742	DMY ₁₁₀	-9022.5	1055
641	SEGA ₈₅	-4477.5	1055	692	SEGA ₁₀₂	-6772.5	1055	743	DMY ₁₁₁	-9067.5	1055
642	SEGB ₈₅	-4522.5	1055	693	SEGB ₁₀₂	-6817.5	1055	744	DMY ₁₁₂	-9430	-784
643	SEGC ₈₅	-4567.5	1055	694	SEGC ₁₀₂	-6862.5	1055	745	DMY ₁₁₃	-9430	-829
644	SEGA ₈₆	-4612.5	1055	695	SEGA ₁₀₃	-6907.5	1055	746	DMY ₁₁₃	-9430	-874
645	SEGB ₈₆	-4657.5	1055	696	SEGB ₁₀₃	-6952.5	1055	747	DMY ₁₁₃	-9430	-919
646	SEGC ₈₆	-4702.5	1055	697	SEGC ₁₀₃	-6997.5	1055	748	DMY ₁₁₄	-9430	-964
647	SEGA ₈₇	-4747.5	1055	698	DMY ₁₀₆	-7042.5	1055	749			
648	SEGB ₈₇	-4792.5	1055	699	DMY ₁₀₇	-7087.5	1055	750			
649	SEGC ₈₇	-4837.5	1055	700	DMY ₁₀₈	-7132.5	1055	751			
650	SEGA ₈₈	-4882.5	1055	701	COM ₄₀	-7177.5	1055	752			
651	SEGB ₈₈	-4927.5	1055	702	COM ₄₁	-7222.5	1055	753			
652	SEGC ₈₈	-4972.5	1055	703	COM ₄₂	-7267.5	1055	754			
653	SEGA ₈₉	-5017.5	1055	704	COM ₄₃	-7312.5	1055	755			
654	SEGB ₈₉	-5062.5	1055	705	COM ₄₄	-7357.5	1055	756			
655	SEGC ₈₉	-5107.5	1055	706	COM ₄₅	-7402.5	1055	757			
656	SEGA ₉₀	-5152.5	1055	707	COM ₄₆	-7447.5	1055	758			
657	SEGB ₉₀	-5197.5	1055	708	COM ₄₇	-7492.5	1055	759			
658	SEGC ₉₀	-5242.5	1055	709	COM ₄₈	-7537.5	1055	760			
659	SEGA ₉₁	-5287.5	1055	710	COM ₄₉	-7582.5	1055	761			
660	SEGB ₉₁	-5332.5	1055	711	COM ₅₀	-7627.5	1055	762			
661	SEGC ₉₁	-5377.5	1055	712	COM ₅₁	-7672.5	1055	763			
662	SEGA ₉₂	-5422.5	1055	713	COM ₅₂	-7717.5	1055	764			
663	SEGB ₉₂	-5467.5	1055	714	COM ₅₃	-7762.5	1055	765			

■ BLOCK DIAGRAM



■ LCD POWER SUPPLY BLOCK DIAGRAM



■ TERMINAL DESCRIPTION 1

No.	Terminal	I/O	Function						
123~131	V _{DD}	Power	Power Supply for Logic Circuits						
151~159	V _{SS}	Power	GND for Logic Circuits						
231~239	V _{SSH}	Power	GND for High Voltage Circuits						
4,5 33,34 67,68	V _{DDA}	Power	V _{DDA} is internally connected to V _{DD} to fix SEL68 or P/S to “H” if necessary, and cannot be used as main power supply. • V _{DDA} should be open if not used.						
26,27 40,41 97,98	V _{SSA}	Power	V _{SSA} is internally connected to V _{SS} to fix SEL68 or P/S to “L” if necessary, and cannot be used as main GND. • V _{SSA} should be open if not used.						
161~168 170~177 178~185 187~194 195~202	V _{LCD} V ₁ V ₂ V ₃ V ₄	Power	LCD Bias Voltages • When the internal LCD power supply is used, internal LCD bias voltages (V _{LCD} and V ₁ -V ₄) are activated by the “Power Control” instruction. Stabilizing capacitors are required between each bias voltage and V _{SS} . • When the external LCD power supply is used, LCD bias voltages are externally supplied on V _{LCD} , V ₁ , V ₂ , V ₃ and V ₄ individually, with the following relation maintained: V _{SSH} <V ₄ <V ₃ <V ₂ <V ₁ <V _{LCD}						
263~267 270~274	C ₁₊ C ₁₋	Power	Capacitor Connection for Voltage Booster						
277~281 284~288	C ₂₊ C ₂₋	Power	Capacitor Connection for Voltage Booster						
291~295 298~302	C ₃₊ C ₃₋	Power	Capacitor Connection for Voltage Booster						
305~309 312~216	C ₄₊ C ₄₋	Power	Capacitor Connection for Voltage Booster						
319~323 326~330	C ₅₊ C ₅₋	Power	Capacitor Connection for Voltage Booster						
222~229	V _{BA}	Power	Reference-Voltage Generator Output						
213~220	V _{REF}	Power	Voltage Regulator Input						
249~257	V _{EE}	Power	Voltage Booster Input • V _{EE} is normally connected to V _{DD} .						
240~248	V _{OUT}	Power	Voltage Booster Output • Input if an external LCD power supply is used.						
204~211	V _{REG}	Power	Voltage Regulator Output						
43,44	RESb	I	Reset • Active “L”						
29,30	SEL68	I	MPU Mode Select <table><tr><td>SEL68</td><td>H</td><td>L</td></tr><tr><td>MPU</td><td>68 series</td><td>80 series</td></tr></table>	SEL68	H	L	MPU	68 series	80 series
SEL68	H	L							
MPU	68 series	80 series							
7,8 13,14 17,18 23,24	ID ₀ ID ₁ ID ₂ ID ₃	I	ID Code • These terminals are fixed at “H” or “L” for ID code.						

■ TERMINAL DESCRIPTION 2

No.	Terminal	I/O	Function						
74,75	D ₀ /SCL	I/O	<u>Parallel Interface</u> D ₇ to D ₀ : 8-bit Bi-directional Bus • In the parallel interface mode (P/S="H"), D ₇ -D ₀ are connected to 8-bit bi-directional MPU bus. <u>Serial Interface</u> SDA : Serial Data SCL : Serial Clock SMODE : 3-/4-line Serial Mode Select SPOL : RS Polarity Select (3-line Serial Interface Mode) • In the 3 or 4-line serial interface mode (P/S="L"), D ₀ is assigned to SCL, and D ₁ to SDA. • In the 3-line serial interface mode, D ₄ is assigned to SPOL. • Serial data on SDA is latched at the rising edge of SCL signal in order of D ₇ , D ₆ ,... and D ₀ , and then converted into 8-bit parallel data at the timing of the internal signal produced from the 8 th SCL. • SCL should be set to "L" right after data transmission or during non-access.						
76,77	D ₁ /SDA	I/O							
82,83	D ₃ /SMODE	I/O							
86,87	D ₄ /SPOL	I/O							
80,81 88,89 92,93 94,95	D ₂ D ₅ D ₆ D ₇	I/O							
100,101 102,103 106,107 108,109 112,113 114,115 118,119 120,121	D ₈ D ₉ D ₁₀ D ₁₁ D ₁₂ D ₁₃ D ₁₄ D ₁₅	I/O	8-bit Bi-directional Bus • In the 16-bit bus length mode, D ₁₅ -D ₈ are assigned to upper 8-bit data bus. • In the serial interface mode or the 8-bit parallel interface mode, D ₁₅ -D ₈ should be fixed to "H" or "L".						
49,50	CSb	I	Chip Select • Active "L"						
53,54	RS	I	Register Select • This signal interprets transferred data as display data or instruction. <table><tr><td>RS</td><td>H</td><td>L</td></tr><tr><td>Data</td><td>Instruction</td><td>Display Data</td></tr></table>	RS	H	L	Data	Instruction	Display Data
RS	H	L							
Data	Instruction	Display Data							
63,64	RDb (E)	I	<u>80-series MPU Interface (P/S="H", SEL68="L")</u> Data Read (RDb) Signal • Active "L" <u>68-series MPU Interface (P/S="H", SEL68="H")</u> Enable Signal • Active "H"						
59,60	WRb (R/W)	I	<u>80-series MPU Interface (P/S="H", SEL68="L")</u> Data Write (WRb) Signal • Active "L" <u>68-series MPU Interface (P/S="H", SEL68="H")</u> Data Read or Write (R/W) Signal <table><tr><td>R/W</td><td>H</td><td>L</td></tr><tr><td>Status</td><td>Read</td><td>Write</td></tr></table>	R/W	H	L	Status	Read	Write
R/W	H	L							
Status	Read	Write							

■ TERMINAL DESCRIPTION 3

No.	Terminal	I/O	Function																		
37,38	P/S	I	Parallel/Serial Interface Mode Select <table><tr><th>P/S</th><th>Chip Select</th><th>Display / Instruction</th><th>Data</th><th>Read /Write</th><th>Serial Clock</th></tr><tr><td>H</td><td>CSb</td><td>RS</td><td>D₀ ~ D₇</td><td>RDb, WRb</td><td>-</td></tr><tr><td>L</td><td>CSb</td><td>RS</td><td>SDA (D₁)</td><td>Write Only</td><td>SCL (D₀)</td></tr></table> • In the serial interface mode (P/S="L"), RDb, WRb, D₂ and D₅-D₁₅ should be fixed to "H" or "L",.	P/S	Chip Select	Display / Instruction	Data	Read /Write	Serial Clock	H	CSb	RS	D ₀ ~ D ₇	RDb, WRb	-	L	CSb	RS	SDA (D ₁)	Write Only	SCL (D ₀)
P/S	Chip Select	Display / Instruction	Data	Read /Write	Serial Clock																
H	CSb	RS	D ₀ ~ D ₇	RDb, WRb	-																
L	CSb	RS	SDA (D ₁)	Write Only	SCL (D ₀)																
133,134	CL	O	Line Clock • CL is normally open.																		
135,136	FLM	O	First Line Maker • FLM is normally open.																		
139,140	FR	O	Frame Rate • FR is normally open.																		
141,142	CLK	O	Clock Output • CLK is normally open.																		
145,146 149,150	OSC1 OSC2	I O	OSC • When the internal oscillator is used, fix OSC1 to "H" or "L" and leave OSC2 open. To attain more accurate frequency, connect OSC1 and OSC2 with an external resistor. • When the internal oscillator is not used, input external clock to OSC1 and leave OSC2 open.																		
386~697	SEGA ₀ ~SEGA ₁₀₃ SEGB ₀ ~SEGB ₁₀₃ SEGC ₀ ~SEGC ₁₀₃	O	Segment Drivers <table><tr><th>REV Register</th><th>OFF</th><th>ON</th></tr><tr><td>Normal</td><td>0</td><td>1</td></tr><tr><td>Reverse</td><td>1</td><td>0</td></tr></table> • Segment drivers output the following voltage levels. B/W Mode (Example) FR Signal Display Data Reverse Display OFF (Normal) Reverse Display ON V₂ V_{LCD} V₃ V_{SSH} V_{LCD} V₂ V_{SSH} V₃	REV Register	OFF	ON	Normal	0	1	Reverse	1	0									
REV Register	OFF	ON																			
Normal	0	1																			
Reverse	1	0																			
343~382 701~740	COM ₀ ~ COM ₇₉	O	Common Drivers • Common drivers output the following voltage levels. <table><tr><th>Data</th><th>FR</th><th>Output Levels</th></tr><tr><td>H</td><td>H</td><td>V_{SSH}</td></tr><tr><td>L</td><td>H</td><td>V₁</td></tr><tr><td>H</td><td>L</td><td>V_{LCD}</td></tr><tr><td>L</td><td>L</td><td>V₄</td></tr></table>	Data	FR	Output Levels	H	H	V _{SSH}	L	H	V ₁	H	L	V _{LCD}	L	L	V ₄			
Data	FR	Output Levels																			
H	H	V _{SSH}																			
L	H	V ₁																			
H	L	V _{LCD}																			
L	L	V ₄																			

NOTE) DUMMY PADs: No. 1~3,6, 9~12, 15, 16, 19~22, 25, 28, 31, 32, 35, 36, 39, 42, 45~48, 51, 52, 55~58, 61, 62, 65, 66, 69~73, 78, 79, 84, 85, 90, 91, 96, 99, 104, 105, 110, 111, 116, 117, 122, 132, 137, 138, 143, 144, 147, 148, 160, 169, 186, 203, 212, 221, 230, 258~262, 268, 269, 275, 276, 282, 283, 289, 290, 296, 297, 303, 304, 310, 311, 317, 318, 324, 325, 331~342, 383~385, 698~700, 741~748

■ FUNCTIONAL DESCRIPTION

(1) MPU INTERFACE

(1-1) Selection of Parallel/Serial Interface Mode

The P/S selects a parallel or a serial interface mode, as shown in Table 1. In the serial interface mode, Except “Boost Level / ID Code Read” instruction data, neither display data in the DDRAM nor instruction data in the registers can be read out.

Table 1 Selection of Parallel/Serial Interface Mode

P/S	I/F Mode	CSb	RS	RDb	WRb	SEL68	SDA	SCL	Data
H	Parallel I/F	CSb	RS	RDb	WRb	SEL68			D ₇ -D ₀ (D ₁₅ -D ₀)
L	Serial I/F	CSb	RS	-	-	-	SDA	SCL	-

NOTE) “-” : Fix to “H” or “L”.

(1-2) Selection of MPU Mode

In the parallel interface mode, the SEL68 selects 68 or 80-series MPU mode, as shown in Table 2.

Table 2 Selection of MPU Mode

SEL68	MPU Mode	CSb	RS	RDb	WRb	Data
H	68-series MPU	CSb	RS	E	R/W	D ₇ -D ₀ (D ₁₅ -D ₀)
L	80-series MPU	CSb	RS	RDb	WRb	D ₇ -D ₀ (D ₁₅ -D ₀)

(1-3) Data Recognition

In the parallel interface mode, the data from MPU is interpreted as display data or instruction according to the combination of the RS, RDb and WRb (R/W) signals, as shown in Table 3.

Table 3 Data Recognition (Parallel Interface Mode)

RS	68-series	80-series		Function
	R/W	RDb	WRb	
H	H	L	H	Read Instruction
H	L	H	L	Write Instruction
L	H	L	H	Read Display Data
L	L	H	L	Write Display Data

(1-4) Selection of 3-/4-line Serial Interface Mode

In the serial interface mode, the SMODE selects 3- or 4-line serial interface mode, as shown in Table 4.

Table 4 Selection of 3-/4-line Serial Interface Mode

SMODE	Serial Interface Mode
H	3-line
L	4-line

(1-5) 4-line Serial Interface Mode

While the chip select is active (CSb=“L”), the SDA and SCL are enabled. While the chip select is inactive (CSb=“H”), the SDA and SCL are disabled, and the internal shift register and the internal counter are being initialized. 8-bit serial data on the SDA is latched at the rising edge of the SCL signal in order of D₇, D₆,..., and D₀, and converted into 8-bit parallel data at the timing of the internal signal produced from the 8th SCL signal. The data on the SDA is interpreted as display data or instruction according to the RS.

Table 5 Data Recognition (4-line Serial Interface)

RS	Data Recognition
H	Instruction
L	Display Data

Note that the SCL should be set to “L” right after data transmission or during non-access because the serial interface is susceptible to external noises which may cause malfunctions. For added safety, inactivate the chip-select (CSb=“H”) temporary whenever 8-bit data transmission is completed. Fig 1 illustrates the interface timing of the 4-line serial interface mode.

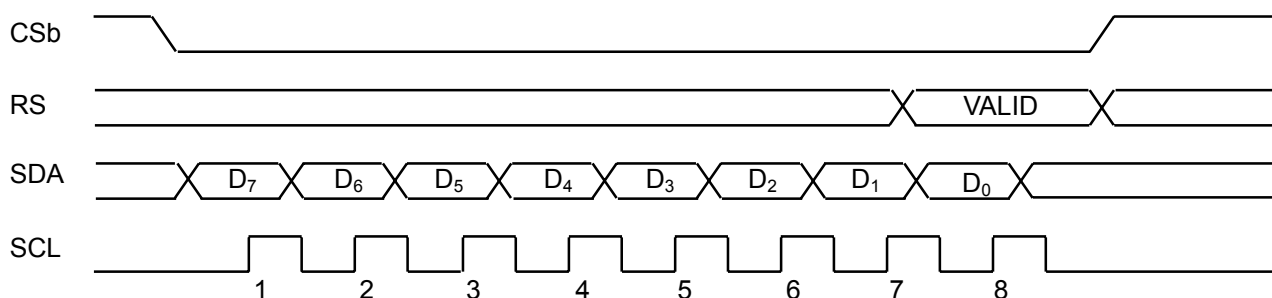


Fig 1 4-line Serial Interface Timing

(1-6) 3-line Serial Interface Mode

While the chip select is active (CSb=“L”), the SDA and SCL are enabled. While the chip select is not active (CSb=“H”), the SDA and SCL are disabled, and the internal shift register and the internal counter are being initialized. 9-bit serial data on the SDA is latched at the rising edge of the SCL signal in order of RS, D7, D6,..., and D0, and then converted into 9-bit parallel data at the timing of the internal signal produced from the 9th SCL signal. The data on the SDA is interpreted as display data or instruction according to the combination of the RS bit and the SPOL status, as follows.

Table 6 Data Recognition (3-line Serial Interface)

SPOL=L		SPOL=H	
RS	Data Recognition	RS	Data Recognition
0	Display Data	0	Instruction
1	Instruction	1	Display Data

Note that the SCL should be set to “L” right after data transmission or during non-access because the serial interface is susceptible to external noises which may cause malfunctions. For added safety, inactivate the chip-select (CSb=“H”) temporary whenever 9-bit data transmission is completed. Fig 2 illustrates the interface timing of the 3-line serial interface mode.

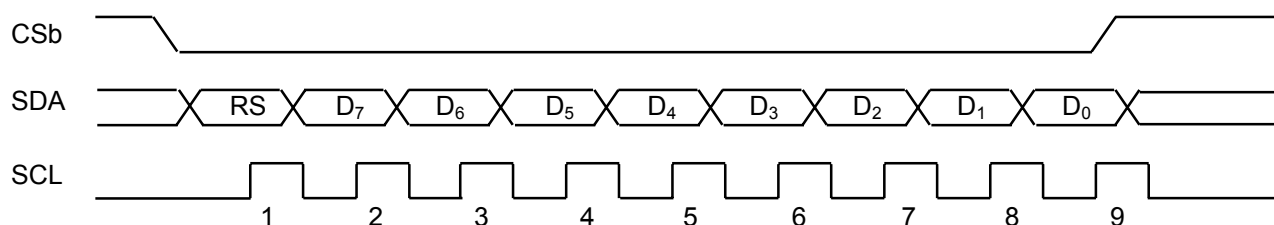


Fig 2 3-line Serial Interface Timing

(1-7) Accessing DDRAM

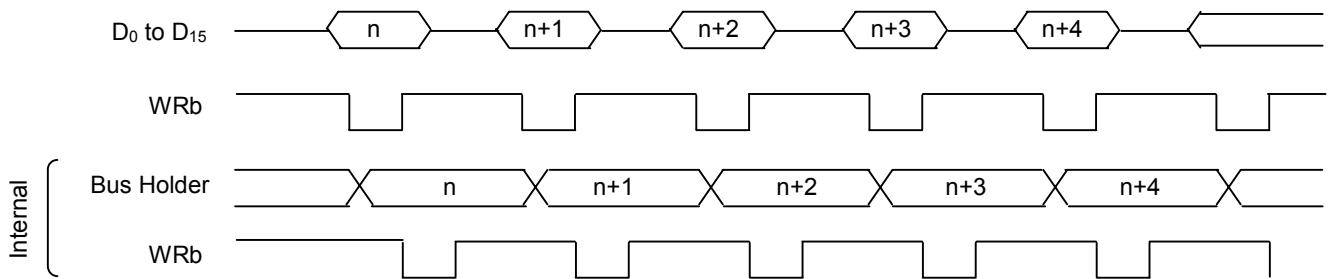
While the chip select is active (CSb="L"), the data from MPU can be written into the DDRAM or the instruction register. When the RS is "L", the data is interpreted as display data which is stored in the DDRAM. The display data is latched at the rising edge of the WRb signal in the 80-series MPU mode, or at the falling edge of the E signal in the 68-series MPU mode.

Table 7 Data Recognition

RS	Data Recognition
L	Display Data
H	Instruction

In the DDRAM read sequence, be sure to execute a dummy read right after setting an address or right after writing display data or instruction. The data from MPU is temporarily held in the internal bus-holder, then released on the internal data-bus, therefore a dummy data is read out by the 1st "Display Data Read" instruction. After that, the display data is read out from a specified address by the 2nd instruction. Note that the "Display Data Read" instruction cannot be used in the serial interface mode.

Display Data Write Operation



Display Data Read Operation

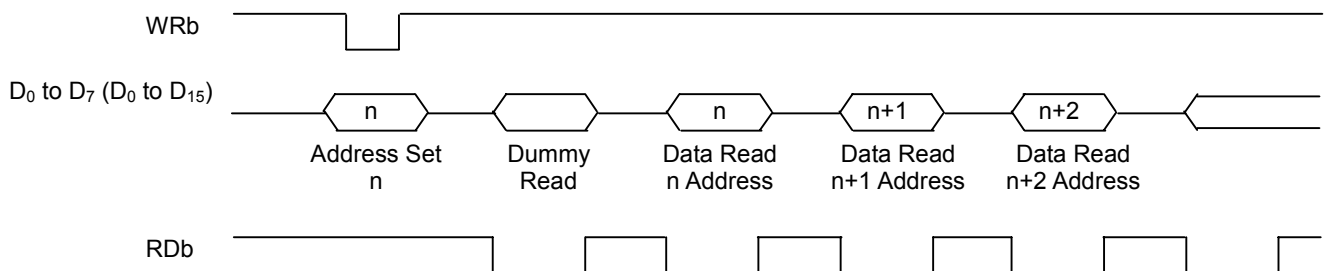


Fig 3 Internal-signal Timing of Display Data Read/Write Operations

NOTE) In 16-bit bus length mode, instruction is transmitted to/from instruction register in 16 bits, as well as display data.

(1-8) Accessing Instruction Register

Each instruction register has a specific address in between (0H) and (FH), and instruction data is read out from the register by the “Register Address” and “Register Read” instructions. For more information, refer to “(14-23) Register Address” and “(14-24) Register Read /ID Code Read”.

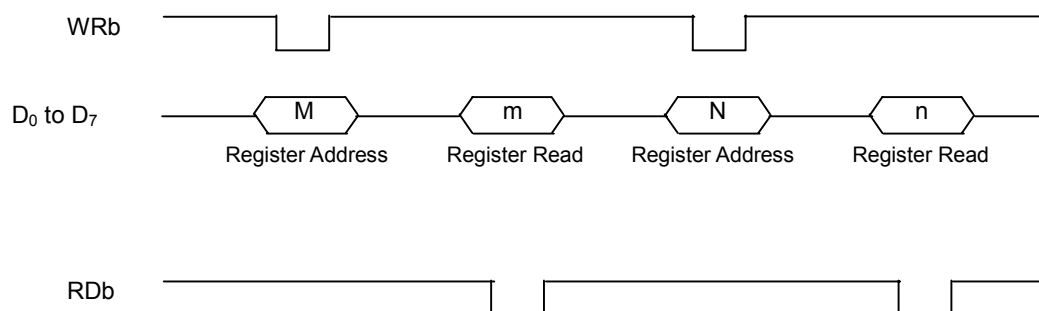


Fig 4 Access Timing of Instruction Register

(1-9) Selection of 8-/16-bit Bus Length (Parallel Interface Mode)

Either 8- or 16-bit bus length is selected by the D_0 (WLS) bit of the “Bus Length” instruction. In the 16-bit bus length mode, instruction as well as display data is transmitted to/from the instruction registers in 16 bits (D_{15} to D_0). However, only lower 8 bits (D_7 to D_0) are valid for instruction register access. And only 12 bits are actually stored in the DDRAM, even though entire 16 bits (D_{15} to D_0) are transmitted for DDRAM access. For more information, refer to “(4-4) Bit Assignment of Display Data”.

Table 8 Selection of 8-/16-bit Bus Length Mode

WLS	Bus Length Mode
L	8-bit Bus Length
H	16-bit Bus Length

(2) INITIAL DISPLAY LINE REGISTER

The address data in the initial display line register specifies the row address, which corresponds to an initial COM and is normally positioned on top of a screen in full display. The initial COM is the start position of common scanning, which is specified by the “Initial COM” instruction.

The row address, which is established in the initial display line register, is preset into the line counter whenever the FLM becomes “H”. At the rising edge of the CL signal, the line counter is counted-up, then 312-bit display data is latched into the data latch circuit. At the falling edge of the CL signal, the latch data is released to the grayscale control circuit to decide a grayscale level, then the segment drivers A_i , B_i and C_i ($i=0$ to 103) generate LCD waveforms.

(3) COLUMN AND ROW ADDRESS COUNTERS

The column and row address counters designate a column address and a row address respectively for DDRAM access, but they are completely independent from the line counter. The line counter provides a line address which is synchronized with display control timings such as the FLM and the CL.

(4) DDRAM

(4-1) DDRAM Address Range

The DDRAM is capable of 80 bits for row address and 1,248 bits (12-bit x 104-segment) for column address. The range of the column address is varied depending on the settings as follows, and the row address is from (00H) to (4FH). Setting outside these ranges is not allowed, otherwise it may cause malfunctions. For DDRAM access, two data transmissions are needed for 1 RGB-pixel in the 8-bit bus length mode, and one transmission in the 16-bit bus length mode.

8-bit Bus Length

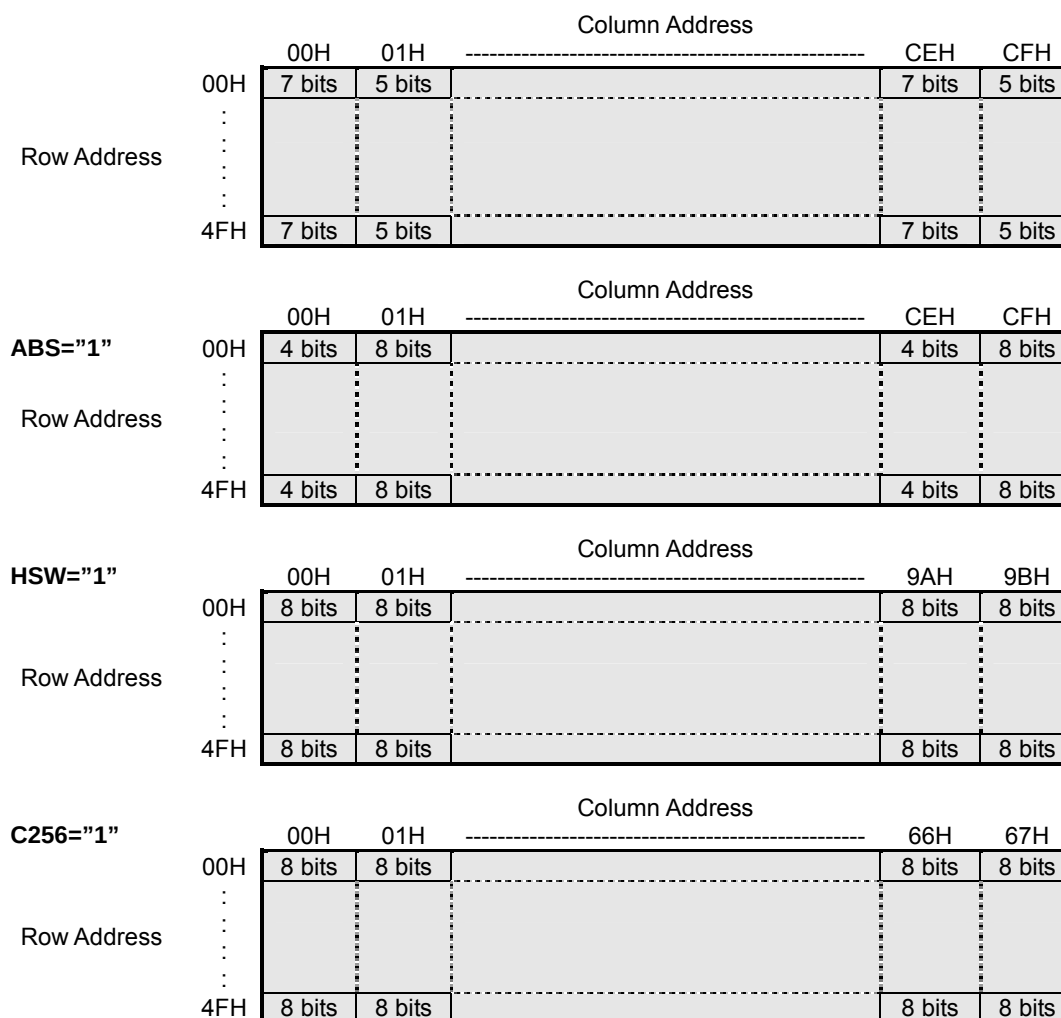


Fig 5 Range of Column Address in 8-bit Bus Length

16-bit Bus Length

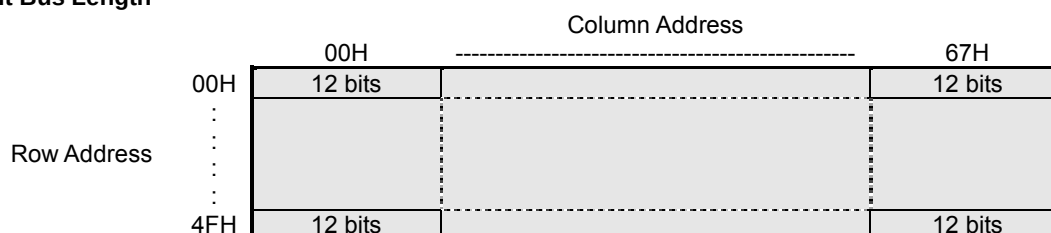


Fig 6 Range of Column Address in 16-bit Bus Length

(4-2) Window Area for DDRAM Access

In addition to the normal DDRAM access discussed previously, the window area access can be used. This area is set by the “Increment Control” instruction and the designation of the start point and the end point.

By the “Increment Control”, an auto-increment is set for column address and row address individually. Once this mode is set up, the column address, row address or both are automatically counted up, whenever the DDRAM is accessed. And, the start point is specified by the “Column Address” and “Row Address” instructions, and the end point by the “Window End Column Address” and “Window End Row Address” instructions. For more information, refer to “(14-9) Increment Control”, “(14-25) Window End Column Address” and “(14-26) Window End Row Address”. The typical sequence of the window area setting is listed below.

1. Set “1” at D₃ (WIN), D₁ (AYI) and D₀ (AXI) of “Increment Control” instruction.
2. Set start point by “Column Address” and “Row Address” instructions.
3. Set end point by “Window End Column Address” and “Window End Row Address” instructions.
4. Window area is set up, and DDRAM can be accessed.

NOTE) The order of address setting is column address first, then row address.

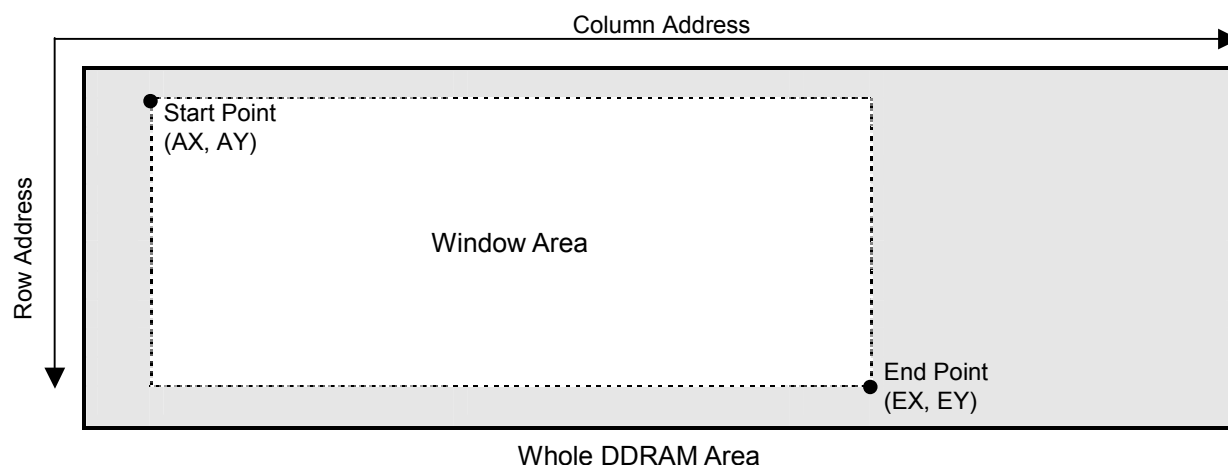
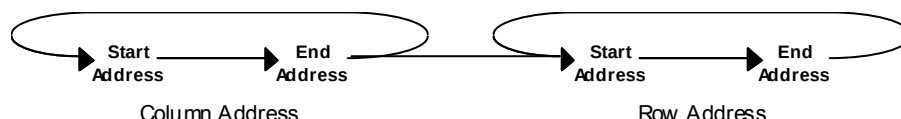


Fig 7 Window Area

NOTE1) The following relation should be maintained to avoid malfunctions.

- AX (Window Start Column Address) < EX (Window End Column Address) < Maximum Column Address
- AY (Window Start Row Address) < EY (Window End Row Address) < Maximum Row Address

NOTE3) Auto-increment in the window area



NOTE2) A read-modify-write operation is enabled by setting “1” at the D₂ (AIM) of the “Increment Control” instruction. Refer to the description about “AIM” bit in “(14-9) Increment Control”.

(4-3) Segment Direction

The DDRAM access direction is controlled by the D₀ (REF) bit of the “Display Control (2)” instruction. This function is used to reverse the segment direction for reducing the restrictions on the IC position of an LCD module.

(4-4) Bit Assignment of Display Data

(4-4-1) Bit Assignment Overview

These maps are used for grasping general outlines of the variations in the bit assignment of display data.

Table 9-1 RAM MAP 1 (Variable 16-grayscale Mode, Fixed 8-grayscale Mode or B&W Mode)

Mode	WLS	ABS	HSW	RF	C256	SEG ₀												SEG ₁												SEG ₁₀₂												SEG ₁₀₃																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																							
						Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																															
						A ₃	A ₂	A ₁	A ₀	B ₃	B ₂	B ₁	B ₀	C ₃	C ₂	C ₁	C ₀	A ₃	A ₂	A ₁	A ₀	B ₃	B ₂	B ₁	B ₀	C ₃	C ₂	C ₁	C ₀	A ₃	A ₂	A ₁	A ₀	B ₃	B ₂	B ₁	B ₀	C ₃	C ₂	C ₁	C ₀	A ₃	A ₂	A ₁	A ₀	B ₃	B ₂	B ₁	B ₀	C ₃	C ₂	C ₁	C ₀																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																												
	1	0	x	0	0	X=00H				X=67H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=01H				X=66H				X=0			

(4-4-2) Bit Assignment in Variable 16-grayscale Mode

16-bit Bus Length (MON=0, PWM=0, C256=0, WLS=1)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																												
*	0	0	0	X=00H														↔	X=67H													
*	0	1	1	X=67H														↔	X=00H													
Display Data in DDRAM				D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁	↕	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁				
				Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C							
				SEGA ₀				SEGB ₀				SEGC ₀				↔	SEGA ₁₀₃				SEGB ₁₀₃				SEGC ₁₀₃							

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																												
*	0	0	1	X=00H														↔	X=67H													
*	0	1	0	X=67H														↔	X=00H													
Display Data in DDRAM				D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁	↕	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁				
				Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C							
				SEGC ₀				SEGB ₀				SEGA ₀				↔	SEGC ₁₀₃				SEGB ₁₀₃				SEGA ₁₀₃							

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																												
*	1	0	0	X=00H														↔	X=67H													
*	1	1	1	X=67H														↔	X=00H													
Display Data in DDRAM				D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀				
				Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C							
				SEGA ₀				SEGB ₀				SEGC ₀				↔	SEGA ₁₀₃				SEGB ₁₀₃				SEGC ₁₀₃							

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																											
*	1	0	1	X=00H												↔	X=67H														
*	1	1	0	X=67H												↔	X=00H														
Display Data in DDRAM				D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀			
				Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C						
				SEGC ₀				SEGB ₀				SEGA ₀				↔	SEGC ₁₀₃				SEGB ₁₀₃				SEGA ₁₀₃						

8-bit Bus Length (MON=0, PWM=0, C256=0, WLS=0)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																														
0	0	0	0	X=00H					X=01H					↔	X=CEH					X=CFH														
0	0	1	1	X=CEH					X=CFH					↔	X=00H					X=01H														
Display Data in DDRAM				D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁	↔	D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁						
				Palette A					Palette B					Palette C					↔	Palette A					Palette B					Palette C				
				SEGA ₀					SEGB ₀					SEGC ₀					↔	SEGA ₁₀₃					SEGB ₁₀₃					SEGC ₁₀₃				

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																														
0	0	0	1	X=00H					X=01H					↔	X=CEH					X=CFH														
0	0	1	0	X=CEH					X=CFH					↔	X=00H					X=01H														
Display Data in DDRAM				D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁	↔	D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁						
				Palette A					Palette B					Palette C					↔	Palette A					Palette B					Palette C				
				SEGC ₀					SEGB ₀					SEGA ₀					↔	SEGC ₁₀₃					SEGB ₁₀₃					SEGA ₁₀₃				

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																								
0	1	0	0	X=00H				X=01H				↔		X=CEH				X=CFH										
0	1	1	1	X=CEH				X=CFH				↔		X=00H				X=01H										
Display Data in DDRAM				D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
				SEGA ₀				SEGB ₀				SEGC ₀				↔	SEGA ₁₀₃				SEGB ₁₀₃				SEGC ₁₀₃			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																								
0	1	0	1	X=00H				X=01H				↔		X=CEH				X=CFH										
0	1	1	0	X=CEH				X=CFH				↔		X=00H				X=01H										
Display Data in DDRAM				D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
				SEGC ₀				SEGB ₀				SEGA ₀				↔	SEGC ₁₀₃				SEGB ₁₀₃				SEGA ₁₀₃			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																									
1	*	0	0	X=00H								X=01H								X=02H								..	
Display Data in DDRAM Grayscale Palette Segment Driver				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	..	
				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				...	
				SEGA ₀				SEGB ₀				SEGC ₀				SEGA ₁				SEGB ₁				SEGC ₁				...	

Column Address / Display Data / Segment Driver																												
...	X=99H								X=9AH								X=9BH											
..	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀				
...	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C							
...	SEGA ₁₀₂				SEGB ₁₀₂				SEGC ₁₀₂				SEGA ₁₀₃				SEGB ₁₀₃				SEGC ₁₀₃							

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																											
1	*	0	1	X=00H								X=01H								X=02H								..			
Display Data in DDRAM Grayscale Palette Segment Driver				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	..			
				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				...			
				SEGC ₀				SEGB ₀				SEGA ₀				SEGC ₁				SEGB ₁				SEGA ₁				...			

Column Address / Display Data / Segment Driver																												
...	X=99H								X=9AH								X=9BH											
..	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀				
...	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C							
...	SEGC ₁₀₂				SEGB ₁₀₂				SEGA ₁₀₂				SEGC ₁₀₃				SEGB ₁₀₃				SEGA ₁₀₃							

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																								
1	*	1	0	X=9AH				X=9BH								X=99H								X=9AH				..
Display Data in DDRAM Grayscale Palette Segment Driver				D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	..
				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				...
				SEGC ₀				SEGB ₀				SEGA ₀				SEGC ₁				SEGB ₁				SEGA ₁				...

Column Address / Display Data / Segment Driver																												
...	X=01H				X=02H								X=00H								X=01H							
..	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄				
...	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C							
...	SEGC ₁₀₂				SEGB ₁₀₂				SEGA ₁₀₂				SEGC ₁₀₃				SEGB ₁₀₃				SEGA ₁₀₃							

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																								
1	*	1	1	X=9AH				X=9BH								X=99H								X=9AH				..
Display Data in DDRAM Grayscale Palette Segment Driver				D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	..
				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				...
				SEGA ₀				SEGB ₀				SEGC ₀				SEGA ₁				SEGB ₁				SEGC ₁				...

Column Address / Display Data / Segment Driver																												
...	X=01H				X=02H								X=00H								X=01H							
..	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄				
...	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C							
...	SEGA ₁₀₂				SEGB ₁₀₂				SEGC ₁₀₂				SEGA ₁₀₃				SEGB ₁₀₃				SEGC ₁₀₃							

(4-4-3) Bit Assignment in Variable 8-level Gradation Mode

8-bit Bus Length (MON=0, PWM=0, C256=1, WLS=0)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																	
*	*	0	0	X=00H								↔	X=67H								
*	*	1	1	X=67H								↔	X=00H								
Display Data in DDRAM				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↕	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
				Palette A			Palette B			Palette C		↔	Palette A			Palette B			Palette C		
				SEGA ₀			SEGB ₀			SEGC ₀		↔	SEGA ₁₀₃			SEGB ₁₀₃			SEGC ₁₀₃		

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																
*	*	0	1	X=00H								↔	X=67H							
*	*	1	0	X=67H								↔	X=00H							
Display Data in DDRAM				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				Palette A			Palette B			Palette C		↔	Palette A			Palette B			Palette C	
				SEGC ₀			SEGB ₀			SEGA ₀		↔	SEGC ₁₀₃			SEGB ₁₀₃			SEGA ₁₀₃	

(4-4-4) Bit Assignment in Fixed 8-level Gradation Mode

16-bit Bus Length (MON=0, PWM=1, C256=0, WLS=1)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																								
*	0	0	0	X=00H												↔	X=67H											
*	0	1	1	X=67H												↔	X=00H											
Display Data in DDRAM				D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁	↕	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁
				Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
				SEGA ₀				SEGB ₀				SEGC ₀				↔	SEGA ₁₀₃				SEGB ₁₀₃				SEGC ₁₀₃			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																								
*	0	0	1	X=00H												↔	X=67H											
*	0	1	0	X=67H												↔	X=00H											
Display Data in DDRAM				D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁	↕	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁
				Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
				SEGC ₀				SEGB ₀				SEGA ₀				↔	SEGC ₁₀₃				SEGB ₁₀₃				SEGA ₁₀₃			

NOTE) The data indicated with a slash mark (/) is invalid.

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																								
*	1	0	0	X=00H										↔	X=67H													
*	1	1	1	X=67H										↔	X=00H													
Display Data in DDRAM				D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
				SEGA ₀				SEGB ₀				SEGC ₀				↔	SEGA ₁₀₃				SEGB ₁₀₃				SEGC ₁₀₃			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																								
*	1	0	1	X=00H										↔	X=67H													
*	1	1	0	X=67H										↔	X=00H													
Display Data in DDRAM				D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
				SEGC ₀				SEGB ₀				SEGA ₀				↔	SEGC ₁₀₃				SEGB ₁₀₃				SEGA ₁₀₃			

NOTE) The data indicated with a slash mark (/) is invalid.

8-bit Bus Length (MON=0, PWM=1, C256=0, WLS=0)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver							
0	0	0	0	X=00H		X=01H		↔	X=CEH		X=CFH
0	0	1	1	X=CEH		X=CFH		↔	X=00H		X=01H
Display Data in DDRAM				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Grayscale Palette				Palette A		Palette B		↔	Palette A		Palette B
Segment Driver				SEGA ₀		SEGB ₀		↔	SEGA ₁₀₃		SEGB ₁₀₃

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver							
0	0	0	1	X=00H		X=01H		↔	X=CEH		X=CFH
0	0	1	0	X=CEH		X=CFH		↔	X=00H		X=01H
Display Data in DDRAM				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Grayscale Palette				Palette A		Palette B		↔	Palette A		Palette B
Segment Driver				SEGC ₀		SEGB ₀		↔	SEGC ₁₀₃		SEGB ₁₀₃

NOTE) The data indicated with a slash mark (/) is invalid.

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver							
0	1	0	0	X=00H		X=01H		↔	X=CEH		X=CFH
0	1	1	1	X=CEH		X=CFH		↔	X=00H		X=01H
Display Data in DDRAM				D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄
Grayscale Palette				Palette A		Palette B		↔	Palette A		Palette B
Segment Driver				SEGA ₀		SEGB ₀		↔	SEGA ₁₀₃		SEGB ₁₀₃

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver							
0	1	0	1	X=00H		X=01H		↔	X=CEH		X=CFH
0	1	1	0	X=CEH		X=CFH		↔	X=00H		X=01H
Display Data in DDRAM				D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄
Grayscale Palette				Palette A		Palette B		↔	Palette A		Palette B
Segment Driver				SEGC ₀		SEGB ₀		↔	SEGC ₁₀₃		SEGB ₁₀₃

NOTE) The data indicated with a slash mark (/) is invalid.

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																											
1	*	0	0	X=00H								X=01H								X=02H								..			
Display Data in DDRAM Grayscale Palette Segment Driver				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	..			
				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				...			
				SEGA ₀				SEGB ₀				SEGC ₀				SEGA ₁				SEGB ₁				SEGC ₁				...			

Column Address / Display Data / Segment Driver																									
...	X=99H								X=9AH								X=9BH								
...	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
...	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				
...	SEGA ₁₀₂				SEGB ₁₀₂				SEGC ₁₀₂				SEGA ₁₀₃				SEGB ₁₀₃				SEGC ₁₀₃				

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																											
1	*	0	1	X=00H								X=01H								X=02H								..			
Display Data in DDRAM Grayscale Palette Segment Driver				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	..			
				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				...			
				SEGC ₀				SEGB ₀				SEGA ₀				SEGC ₁				SEGB ₁				SEGA ₁				...			

Column Address / Display Data / Segment Driver																								
...	X=99H								X=9AH								X=9BH							
...	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
...	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
...	SEGC ₁₀₂				SEGB ₁₀₂				SEGA ₁₀₂				SEGC ₁₀₃				SEGB ₁₀₃				SEGA ₁₀₃			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																											
1	*	1	0	X=9AH				X=9BH								X=99H								X=9AH				..			
Display Data in DDRAM Grayscale Palette Segment Driver				D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	...			
				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				...			
				SEGC ₀				SEGB ₀				SEGA ₀				SEGC ₁				SEGB ₁				SEGA ₁				...			

Column Address / Display Data / Segment Driver																									
...	X=01H				X=02H								X=00H								X=01H				...
...	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	...
...	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				...
...	SEGC ₁₀₂				SEGB ₁₀₂				SEGA ₁₀₂				SEGC ₁₀₃				SEGB ₁₀₃				SEGA ₁₀₃				...

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																												
1	*	1	1	X=9AH				X=9BH								X=99H								X=9AH				..				
Display Data in DDRAM Grayscale Palette Segment Driver				D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	...
				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				...				
				SEGA ₀				SEGB ₀				SEGC ₀				SEGA ₁				SEGB ₁				SEGC ₁				...				

Column Address / Display Data / Segment Driver																									
...	X=01H				X=02H								X=00H								X=01H				...
...	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	...
...	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				...
...	SEGA ₁₀₂				SEGB ₁₀₂				SEGC ₁₀₂				SEGA ₁₀₃				SEGB ₁₀₃				SEGC ₁₀₃				...

8-bit Bus Length (MON=0, PWM=1, C256=1, WLS=0)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																	
*	*	0	0	X=00H								↔	X=67H								
*	*	1	1	X=67H								↔	X=00H								
Display Data in DDRAM				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
				Palette A			Palette B			Palette C		↔	Palette A			Palette B			Palette C		
				SEGA ₀			SEGB ₀			SEGC ₀		↔	SEGA ₁₀₃			SEGB ₁₀₃			SEGC ₁₀₃		

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																	
*	*	0	1	X=00H								↔	X=67H								
*	*	1	0	X=67H								↔	X=00H								
Display Data in DDRAM				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
				Palette A			Palette B			Palette C		↔	Palette A			Palette B			Palette C		
				SEGC ₀			SEGB ₀			SEGA ₀		↔	SEGC ₁₀₃			SEGB ₁₀₃			SEGA ₁₀₃		

(4-4-5) Bit Assignment in B&W Mode

16-bit Bus Length (MON=1, PWM=*, C256=0, WLS=1)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																								
*	0	0	0	X=00H										↔	X=67H													
*	0	1	1	X=67H										↔	X=00H													
Display Data in DDRAM				D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁	↕	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁
				Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
				SEGA ₀				SEGB ₀				SEGC ₀				↔	SEGA ₁₀₃				SEGB ₁₀₃				SEGC ₁₀₃			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																								
*	0	0	1	X=00H												↔	X=67H											
*	0	1	0	X=67H												↔	X=00H											
Display Data in DDRAM				D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁	↕	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁
				Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
				SEGC ₀				SEGB ₀				SEGA ₀				↔	SEGC ₁₀₃				SEGB ₁₀₃				SEGA ₁₀₃			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																								
*	1	0	0	X=00H								↔	X=67H															
*	1	1	1	X=67H								↔	X=00H															
Display Data in DDRAM				D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
				SEGA ₀				SEGB ₀				SEGC ₀				↔	SEGA ₁₀₃				SEGB ₁₀₃				SEGC ₁₀₃			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																								
*	1	0	1	X=00H										↔	X=67H													
*	1	1	0	X=67H										↔	X=00H													
Display Data in DDRAM				D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
				SEGC ₀				SEGB ₀				SEGA ₀				↔	SEGC ₁₀₃				SEGB ₁₀₃				SEGA ₁₀₃			

NOTE) The data indicated with a slash mark (/) is invalid, and only MSB bits are effective.

8-bit Bus Length (MON=1, PWM=*, C256=0, WLS=0)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																								
0	0	0	0	X=00H				X=01H		↔	X=CEH				X=CFH													
0	0	1	1	X=CEH				X=CFH		↔	X=00H				X=01H													
Display Data in DDRAM				D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁	↔	D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁
				Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
				SEGA ₀				SEGB ₀				SEGC ₀				↔	SEGA ₁₀₃				SEGB ₁₀₃				SEGC ₁₀₃			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																								
0	0	0	1	X=00H				X=01H		↔	X=CEH				X=CFH													
0	0	1	0	X=CEH				X=CFH		↔	X=00H				X=01H													
Display Data in DDRAM				D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁	↔	D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁
				Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
				SEGC ₀				SEGB ₀				SEGA ₀				↔	SEGC ₁₀₃				SEGB ₁₀₃				SEGA ₁₀₃			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																
0	1	0	0	X=00H				X=01H				↔	X=CEH				X=CFH			
0	1	1	1	X=CEH				X=CFH				↔	X=00H				X=01H			
Display Data in DDRAM																				
				Palette A				Palette B				Palette C				↔				
				SEGA ₀				SEGB ₀				SEGC ₀				↔				
Grayscale Palette				Palette A				Palette B				Palette C				↔				
Segment Driver				SEGA ₀				SEGB ₀				SEGC ₀				↔				

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																	
0	1	0	1	X=00H		X=01H		↔	X=CEH		X=CFH										
0	1	1	0	X=CEH		X=CFH		↔	X=00H		X=01H										
Display Data in DDRAM												↔									
				Palette A		Palette B		Palette C		↔		Palette A		Palette B		Palette C					
				SEGC ₀		SEGB ₀		SEGA ₀		↔		SEGC ₁₀₃		SEGB ₁₀₃		SEGA ₁₀₃					

NOTE) The data indicated with a slash mark (/) is invalid, and only MSB bits are effective.

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver											
1	*	0	0	X=00H				X=01H				X=02H			
Display Data in DDRAM				D ₇	D ₆	D ₅	D ₄	D ₇	D ₆	D ₅	D ₄	D ₇	D ₆	D ₅	D ₄
Grayscale Palette Segment Driver				Palette A	Palette B	Palette C	Palette A	Palette B	Palette C	Palette A	Palette B	Palette C	Palette A	Palette B	Palette C
				SEGA ₀	SEGB ₀	SEGC ₀	SEGA ₁	SEGB ₁	SEGC ₁	SEGA ₁	SEGB ₁	SEGC ₁	SEGA ₁	SEGB ₁	SEGC ₁

Column Address / Display Data / Segment Driver											
...	X=99H				X=9AH				X=9BH		
...	D ₇	D ₆	D ₅	D ₄	D ₇	D ₆	D ₅	D ₄	D ₇	D ₆	D ₅
...	Palette A	Palette B	Palette C	Palette A	Palette B	Palette C	Palette A	Palette B	Palette C	Palette A	Palette B
...	SEGA ₁₀₂	SEGB ₁₀₂	SEGC ₁₀₂	SEGA ₁₀₃	SEGB ₁₀₃	SEGC ₁₀₃	SEGA ₁₀₃	SEGB ₁₀₃	SEGC ₁₀₃	SEGA ₁₀₃	SEGB ₁₀₃

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver											
1	*	0	1	X=00H				X=01H				X=02H			
Display Data in DDRAM				D ₇	D ₆	D ₅	D ₄	D ₇	D ₆	D ₅	D ₄	D ₇	D ₆	D ₅	D ₄
Grayscale Palette Segment Driver				Palette A	Palette B	Palette C	Palette A	Palette B	Palette C	Palette A	Palette B	Palette C	Palette A	Palette B	Palette C
				SEGC ₀	SEGB ₀	SEGA ₀	SEGC ₁	SEGB ₁	SEGA ₁	SEGC ₁	SEGB ₁	SEGA ₁	SEGC ₁	SEGB ₁	SEGA ₁

Column Address / Display Data / Segment Driver											
...	X=99H				X=9AH				X=9BH		
...	D ₇	D ₆	D ₅	D ₄	D ₇	D ₆	D ₅	D ₄	D ₇	D ₆	D ₅
...	Palette A	Palette B	Palette C	Palette A	Palette B	Palette C	Palette A	Palette B	Palette C	Palette A	Palette B
...	SEGC ₁₀₂	SEGB ₁₀₂	SEGA ₁₀₂	SEGC ₁₀₃	SEGB ₁₀₃	SEGA ₁₀₃	SEGC ₁₀₃	SEGB ₁₀₃	SEGA ₁₀₃	SEGC ₁₀₃	SEGB ₁₀₃

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver											
1	*	1	0	X=9AH			X=9BH			X=99H			X=9AH		
Display Data in DDRAM				D ₃	D ₂	D ₁	D ₃	D ₂	D ₁	D ₃	D ₂	D ₁	D ₃	D ₂	D ₁
Grayscale Palette Segment Driver				Palette A	Palette B	Palette C	Palette A	Palette B	Palette C	Palette A	Palette B	Palette C	Palette A	Palette B	Palette C
				SEGC ₀	SEGB ₀	SEGA ₀	SEGC ₁	SEGB ₁	SEGA ₁	SEGC ₁	SEGB ₁	SEGA ₁	SEGC ₁	SEGB ₁	SEGA ₁

Column Address / Display Data / Segment Driver																								
...	X=01H				X=02H				X=00H				X=01H											
...	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄								
...	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
...	SEGC ₁₀₂				SEGB ₁₀₂				SEGA ₁₀₂				SEGC ₁₀₃				SEGB ₁₀₃				SEGA ₁₀₃			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver											
1	*	1	1	X=9AH			X=9BH			X=99H			X=9AH		
Display Data in DDRAM				D ₃	D ₂	D ₁	D ₃	D ₂	D ₁	D ₃	D ₂	D ₁	D ₃	D ₂	D ₁
Grayscale Palette Segment Driver				Palette A	Palette B	Palette C	Palette A	Palette B	Palette C	Palette A	Palette B	Palette C	Palette A	Palette B	Palette C
				SEGA ₀	SEGB ₀	SEGC ₀	SEGA ₁	SEGB ₁	SEGC ₁	SEGA ₁	SEGB ₁	SEGC ₁	SEGA ₁	SEGB ₁	SEGC ₁

Column Address / Display Data / Segment Driver												
...	X=01H			X=02H			X=00H			X=01H		
...	D ₃	D ₂	D ₁	D ₇	D ₆	D ₅	D ₃	D ₂	D ₁	D ₇	D ₆	D ₅
...	Palette A			Palette B			Palette C			Palette A		
...	SEGA ₁₀₂			SEGB ₁₀₂			SEGC ₁₀₂			SEGA ₁₀₃		

NOTE) The data indicated with a slash mark (/) is invalid, and only MSB bits are effective.

8-bit Bus Length (MON=1, PWM=*, C256=1, WLS=0)

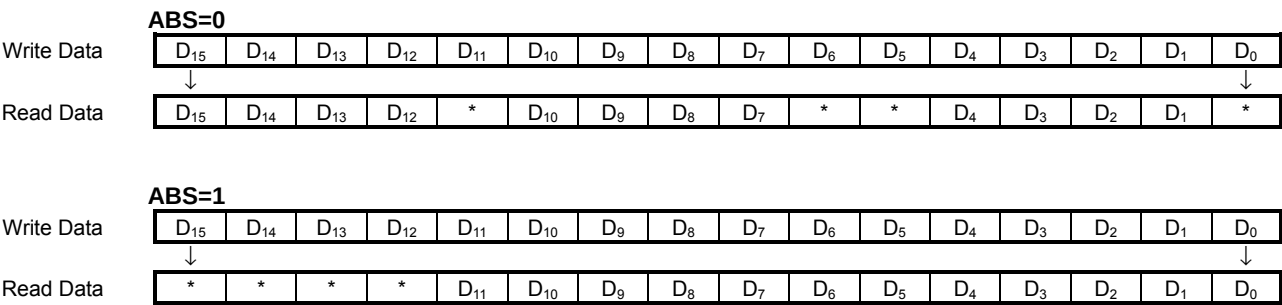
HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																																												
*	*	0	0	X=00H								↔	X=67H																																			
*	*	1	1	X=67H								↔	X=00H																																			
Display Data in DDRAM				D ₇			D ₆			D ₅			D ₄			D ₃			D ₂			D ₁			D ₀	↔	D ₇			D ₆			D ₅			D ₄			D ₃			D ₂			D ₁			D ₀
				Palette A			Palette B			Palette C			↔	Palette A			Palette B			Palette C																												
				SEGA ₀			SEGB ₀			SEGC ₀			↔	SEGA ₁₀₃			SEGB ₁₀₃			SEGC ₁₀₃																												

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																
*	*	0	1	X=00H								↔	X=67H							
*	*	1	0	X=67H								↔	X=00H							
Display Data in DDRAM				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				Palette A			Palette B			Palette C		↔	Palette A			Palette B			Palette C	
				SEGC ₀			SEGB ₀			SEGA ₀		↔	SEGC ₁₀₃			SEGB ₁₀₃			SEGA ₁₀₃	

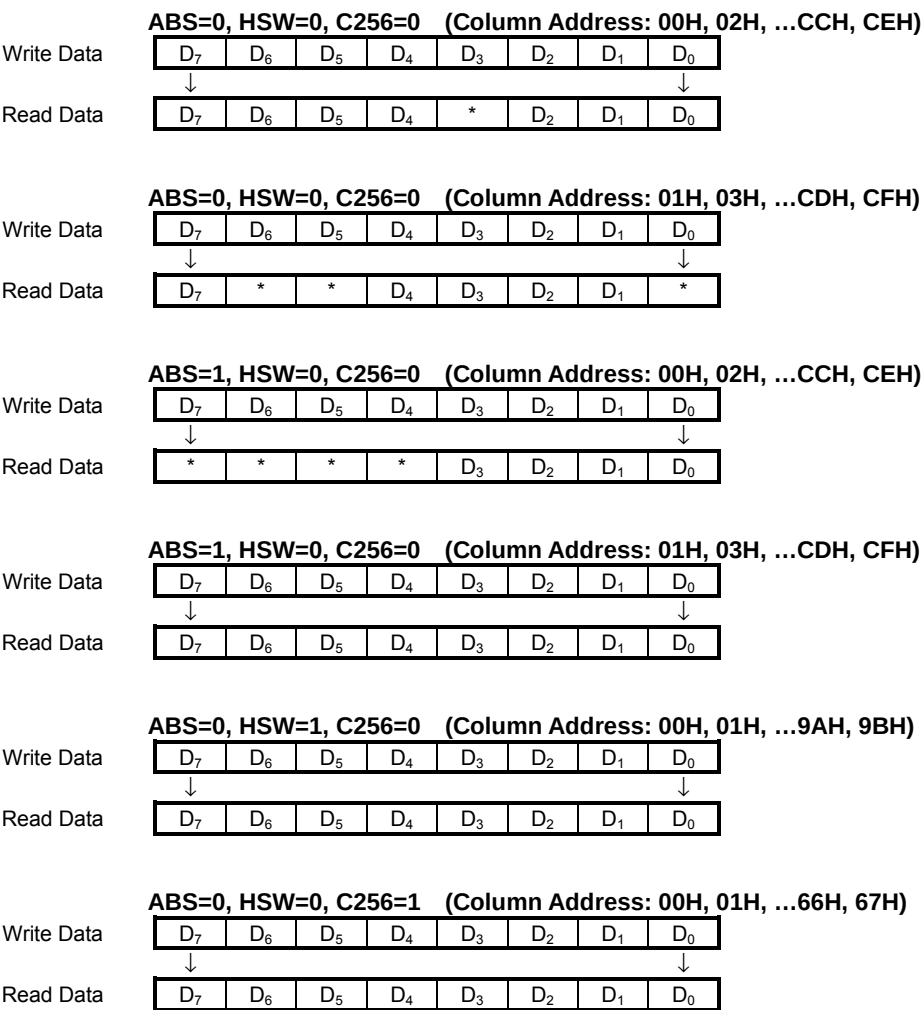
NOTE) The data indicated with a slash mark (/) is invalid, and only MSB bits are effective.

(4-5) Write Data and Read Data

16-bit Bus Length



8-bit Bus Length



NOTE) * : Invalid Data

(5) GRAYSCALE CONTROL CIRCUIT

(5-1) Display Mode Selection

A display mode is selected by the combination of the D₂ (MON) bit of the “Display Control (1)” instruction and the D₃ (PWM) and D₂ (C256) bits of the “Display Mode Control” instruction, as shown below.

Table 11 Display Mode Selection

MON	PWM	C256 (NOTE1)	Display Mode		Bus Length		Oscillation (NOTE2)
0	0	0	Variable 16-grayscale Mode	4096 Colors	8-/16-bit	(WLS=0/1)	f _{OSC1}
		1	Variable 8-grayscale Mode	256 Colors	8-bit	(WLS=0)	
	1	0	Fixed 8-grayscale Mode	256 Colors	8-/16-bit	(WLS=0/1)	f _{OSC2}
		1			8-bit	(WLS=0)	
1	*	0	B&W Mode	Black & White	8-/16-bit	(WLS=0/1)	f _{OSC3}
		1			8-bit	(WLS=0)	

NOTE1) In the variable grayscale mode, “C256” bit selects either 16-grayscale (4K colors) or 8-grayscale (256 colors). When C256=“0” (16-grayscale), all 12 bits are assigned to 1 RGB-pixel. When C256=“1” (8-grayscale), only 8 bits are assigned and the 8-bit bus length should be used. In the fixed 8-grayscale mode or the B&W mode, the “C256” bit is usually “1”. For more information how the display data is assigned, refer to “(4-4) Bit Assignment of Display Data”.

NOTE2) Oscillation frequency is decided according to the display mode, and is fine-tuned by the “Frequency Control” Instruction. Refer to “(10) OSCILLATOR” and “OSCILLATION FREQUENCY AND FRAME FREQUENCY”.

(5-1-1) Variable 16-grayscale Mode

In this mode, each of the palettes A_j, B_j and C_j (j=0-15) is capable of selecting 16 from 32 grayscales (0/31-31/31) by setting palette data in the grayscale palette. Then, each of the segment drivers SEG_{Ai}, SEG_{Bi} and SEG_{Ci} (i=0 to 103) generates 16 grayscales to achieve 4,096 colors. Refer to Table 12-1 and Table 12-2.

(5-1-2) Variable 8-grayscale Mode

Each of the palettes A_j, B_j and C_j (j=0-15) is capable of selecting 8 from 32 grayscales (0/31-31/31). 2 segment drivers of 1 RGB-group (SEG_{Ai}, SEG_{Bi} and SEG_{Ci} (i=0 to 103)) generate 8 grayscales, and the other driver does 4 grayscales to achieve 256 colors. Refer to Table 13-1 through Table 13-4. The 8-bit bus length is usually used in this mode.

(5-1-3) Fixed 8-grayscale Mode

The palette setting is not necessary, because the palettes A_j, B_j and C_j (j=0-15) are always fixed at 4 or 8 grayscales between 0/7 and 7/7. 2 segment drivers of 1 RGB-group (SEG_{Ai}, SEG_{Bi} and SEG_{Ci} (i=0 to 103)) are fixed at 8 grayscales, and the other driver is 4 grayscales, then results in 256 colors. Refer to Table 14-1 and Table 14-2.

(5-1-4) B&W Mode

The palette setting is not necessary, where the only MSB bits of display data are valid. Refer to Table 15.

(6) GRAYSCALE PALETTE

(6-1) Grayscale Selection in Variable 16-grayscale Mode

Table 12-1 Grayscale selection

(Palette Aj, Bj, and Cj)

Display Data MSB----LSB	Palette Name
0 0 0 0	Palette A0/B0/C0
0 0 0 1	Palette A1/B1/C1
0 0 1 0	Palette A2/B2/C2
0 0 1 1	Palette A3/B3/C3
0 1 0 0	Palette A4/B4/C4
0 1 0 1	Palette A5/B5/C5
0 1 1 0	Palette A6/B6/C6
0 1 1 1	Palette A7/B7/C7
1 0 0 0	Palette A8/B8/C8
1 0 0 1	Palette A9/B9/C9
1 0 1 0	Palette A10/B10/C10
1 0 1 1	Palette A11/B11/C11
1 1 0 0	Palette A12/B12/C12
1 1 0 1	Palette A13/B13/C13
1 1 1 0	Palette A14/B14/C14
1 1 1 1	Palette A15/B15/C15

Table 12-2 Grayscale Palette

(Palette Aj, Bj, and Cj)

Palette Data MSB---LSB	Grayscale	Default Setting	Palette Data MSB---LSB	Grayscale	Default Setting
0 0 0 0 0	0	Palette A0/B0/C0	1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	Palette A8/B8/C8
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31	Palette A1/B1/C1	1 0 0 1 1	19/31	Palette A9/B9/C9
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31	Palette A2/B2/C2	1 0 1 0 1	21/31	Palette A10/B10/C10
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31	Palette A3/B3/C3	1 0 1 1 1	23/31	Palette A11/B11/C11
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31	Palette A4/B4/C4	1 1 0 0 1	25/31	Palette A12/B12/C12
0 1 0 1 0	10/31		1 1 0 1 0	26/31	
0 1 0 1 1	11/31	Palette A5/B5/C5	1 1 0 1 1	27/31	Palette A13/B13/C13
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31	Palette A6/B6/C6	1 1 1 0 1	29/31	Palette A14/B14/C14
0 1 1 1 0	14/31		1 1 1 1 0	30/31	
0 1 1 1 1	15/31	Palette A7/B7/C7	1 1 1 1 1	31/31	Palette A15/B15/C15

NOTE1) "MON=0", "PWM=0", "C256=0"

NOTE2) Applied to palette Aj, Bj and Cj (j=0 to 15)

(6-2) Grayscale Selection in Variable 8-grayscale Mode

Table 13-1 Grayscale selection

(Palette Aj and Bj)

Display Data MSB---LSB	Palette Name
0 0 0 *	Palette A1/B1/C1
0 0 1 *	Palette A3/B3/C3
0 1 0 *	Palette A5/B5/C5
0 1 1 *	Palette A7/B7/C7
1 0 0 *	Palette A9/B9/C9
1 0 1 *	Palette A11/B11/C11
1 1 0 *	Palette A13/B13/C13
1 1 1 *	Palette A15/B15/C15

Table 13-2 Grayscale Palette

(Palette Aj and Bj)

Palette Data MSB---LSB	Grayscale	Default Setting	Palette Data MSB---LSB	Grayscale	Default Setting
0 0 0 0 0	0		1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31	Palette A1/B1/C1	1 0 0 1 1	19/31	Palette A9/B9/C9
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31		1 0 1 0 1	21/31	
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31	Palette A3/B3/C3	1 0 1 1 1	23/31	Palette A11/B11/C11
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31		1 1 0 0 1	25/31	
0 1 0 1 0	10/31		1 1 0 1 0	26/31	
0 1 0 1 1	11/31	Palette A5/B5/C5	1 1 0 1 1	27/31	Palette A13/B13/C13
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31		1 1 1 0 1	29/31	
0 1 1 1 0	14/31		1 1 1 1 0	30/31	
0 1 1 1 1	15/31	Palette A7/B7/C7	1 1 1 1 1	31/31	Palette A15/B15/C15

NOTE1) "MON=0", "PWM=0", "C256=1".

NOTE2) Applied to palette Aj and Bj (j=0 to 15)

NOTE3) Palette 0, 2, 4, 6, 8, 10, 12 and 14 are disabled.

Table 13-3 Grayscale selection

(Palette Cj)

Display Data MSB---LSB	Palette Name
0 0 **	Palette A3/B3/C3
0 1 **	Palette A7/B7/C7
1 0 **	Palette A11/B11/C11
1 1 **	Palette A15/B15/C15

Table 13-4 Grayscale Palette

(Palette Cj)

Palette Data MSB---LSB	Grayscale	Default Setting	Palette Data MSB---LSB	Grayscale	Default Setting
0 0 0 0 0	0		1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31		1 0 0 1 1	19/31	
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31		1 0 1 0 1	21/31	
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31	Palette A3/B3/C3	1 0 1 1 1	23/31	Palette A11/B11/C11
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31		1 1 0 0 1	25/31	
0 1 0 1 0	10/31		1 1 0 1 0	26/31	
0 1 0 1 1	11/31		1 1 0 1 1	27/31	
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31		1 1 1 0 1	29/31	
0 1 1 1 0	14/31		1 1 1 1 0	30/31	
0 1 1 1 1	15/31	Palette A7/B7/C7	1 1 1 1 1	31/31	Palette A15/B15/C15

NOTE1) "MON=0", "PWM=0", "C256=1"

NOTE2) Applied to palette Cj (j=0 to 15)

NOTE3) Palette 0, 1, 2, 4, 5, 6, 8, 9, 10, 12, 13 and 14 are disabled.

(6-3) Grayscale Selection in Fixed 8-grayscale Mode

Table 14-1 Grayscale Selection

(Palette Aj and Bj)

Display Data MSB- - - -LSB	Grayscale
0 0 0 *	0/7
0 0 1 *	1/7
0 1 0 *	2/7
0 1 1 *	3/7
1 0 0 *	4/7
1 0 1 *	5/7
1 1 0 *	6/7
1 1 1 *	7/7

Table 14-2 Grayscale Palette

(Palette Cj)

Display Data MSB- - - -LSB	Grayscale
0 0 **	0/7
0 1 **	3/7
1 0 **	5/7
1 1 **	7/7

NOTE1) "MON=0", "PWM=1", "C256=0 or 1"

(6-4) Grayscale Selection in B&W Mode

Table 15 Grayscale Selection

Display Data MSB- - - -LSB	Grayscale
0 ***	0
1 ***	1

NOTE1) "MON=1", "PWM=0 or 1" and "C256=0 or 1"

(7) DISPLAY TIMING GENERATOR

The display timing generator generates timing clocks such as the CL (Line Clock), FR (Frame Rate) and FLM (First Line Maker) by dividing an oscillation frequency. These clocks are used inside the LSI, and are activated by setting "1" at the D₀ (SON) bit of the "Duty-1 /Display Clock ON/OFF" instruction.

The CL is used for the line counter and the data latch circuit. At the rising edge of the CL signal, the line counter is counted up, then 312-bit display data is latched into the data latch circuit. At the falling edge of the CL signal, the latch data is released to the grayscale control circuit, then segment drivers A_i, B_i and C_i (i=0 to 103) produce LCD driving waveforms. The internal data-transmission timing between the DDRAM and segment drivers is completely independent of external data-transmission timing, so that MPU makes access to the LSI without concern for the LSI's internal operation.

The FR and FLM are generated by the CL. The FR toggles once every frame in the default status, and is programmed to toggle once every N lines. And the FLM is used to specify an initial display line, which is preset whenever the FLM becomes "H".

(8) DATA LATCH CIRCUIT

The data latch circuit is used to temporarily store display data which is released to the grayscale control circuit. The display data in this circuit is updated in synchronization with the CL. The "All Pixels ON/OFF", "Display ON/OFF" and "Reverse Display ON/OFF" instructions control the data in this circuit, but does not change the data in the DDRAM.

(9) COMMON DRIVERS AND SEGMENT DRIVERS

The LSI includes 80-common drivers and 312-segment drivers. The common drivers generate LCD driving waveforms formed on the V_{LCD}, V₁, V₄ and V_{SSH} levels. The segment drivers generate waveforms formed on the V_{LCD}, V₂, V₃ and V_{SSH} levels.

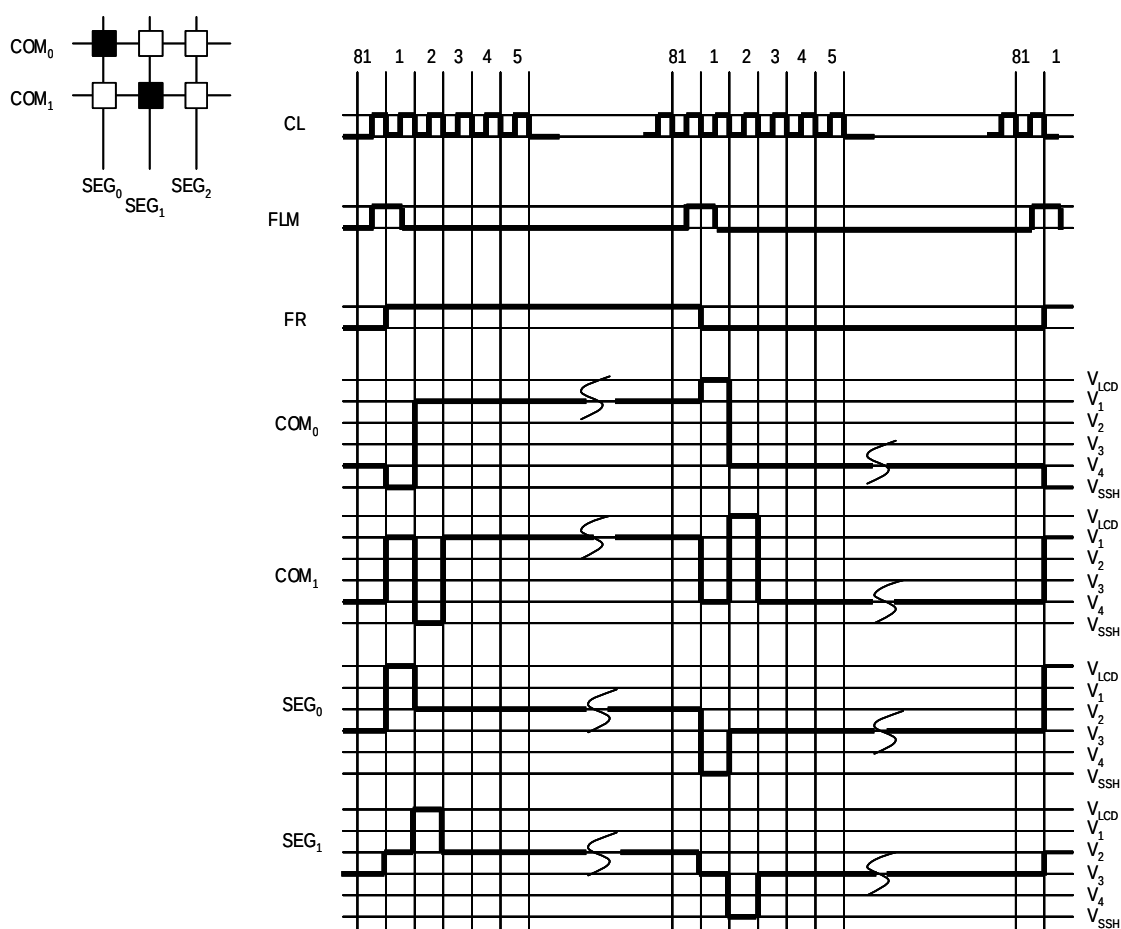


Fig 8 LCD Driving Waveforms (B&W Mode, Color Reverse OFF, 1/81 Duty)

(10) OSCILLATOR

The oscillator is equipped with a resistor and a capacitor, and generates internal clocks used for the display timing generator and the voltage booster. The internal resistor is enabled by setting “0” at the D₁ (CKS) bit of the “Bus Length” instruction. For more accurate frequency, using an external resistor or external clock is recommended.

When using the internal resistor, the resistance is controlled to optimize frame frequency for different LCD panels, by setting the D₂-D₀ (RF2-RF0) bits of the “Frequency Control” instruction. For more safety, make sure what is the best frequency in the particular application.

(10-1) Using Internal Resistor (CKS=0)

In this case, the OSC1 should be fixed at “H” or “L” and the OSC2 is open. The oscillation frequency is varied according to the display mode, as follows.

Table 16 Oscillation Frequency vs. Display Mode

Symbol	MON	PWM	Display Mode
f _{OSC1}	0	0	Variable 8-/16-grayscale Mode
f _{OSC2}	0	1	Fixed 8-grayscale Mode
f _{OSC3}	1	*	B&W Mode

*: Don't care

(10-2) Using External Resistor (CKS=1)

Be sure to connect the OSC1 and OSC2 with an external resistor. The frequency of the oscillator should be adjusted to the same value generated by the internal resistor.

(10-3) Using External Clock (CKS=1)

Input external clock to the OSC1 and leave the OSC2 open. The external clock with 50% duty is recommended. The frequency of the external clock should be the same value generated by the internal resistor.

(11) LCD POWER SUPPLY

The internal LCD power supply is organized into the voltage converter and the voltage booster. The voltage converter consists of the reference voltage generator, the voltage regulator with EVR and the LCD bias voltage generator. The configuration of the LCD power supply is arranged by setting the D₃ (AMPON) and D₁ (DCON) bits of the “Power Control” instruction. For this configuration, the internal LCD power supply can be partially used in combination with an external supply voltage, as shown in Table 17.

Table 17 Configuration of LCD Power Supply

DCON	AMPON	Voltage Booster	Voltage Converter	External Supply Voltage	NOTE
0	0	Inactive	Inactive	V _{OUT} , V _{LCD} , V ₁ , V ₂ , V ₃ , V ₄	1, 3, 4
0	1	Inactive	Active	V _{OUT}	2, 3, 4
1	1	Active	Active	—	-

NOTE1) No internal LCD power supply is used. The LCD bias voltages are externally supplied, and the C₁₊, C₁₋, C₂₊, C₂₋, C₃₊, C₃₋, C₄₊, C₄₋, C₅₊, C₅₋, V_{REF}, V_{REG} and V_{EE} are open.

NOTE2) Only the voltage converter is used. The V_{OUT} is externally supplied, and the C₁₊, C₁₋, C₂₊, C₂₋, C₃₊, C₃₋, C₄₊, C₄₋, C₅₊, C₅₋ and V_{EE} are open. The reference voltage is supplied on the V_{REF}.

NOTE3) The following relation among each LCD bias voltages must be maintained.

$$V_{OUT} \geq V_{LCD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SSH}$$

NOTE4) If the internal LCD power supply doesn't have enough capability to drive the particular LCD panel, use the external LCD power supply. Otherwise, it may affect display quality.

(11-1) Voltage Booster

The internal voltage booster generates up to $6 \times V_{EE}$ voltage. The boost level is selected from 2x, 3x, 4x, 5x or 6x by setting the D_2 - D_0 ($VU2$ - $VU0$) bits of the “Boost Level” instruction. The boost voltage V_{OUT} must not exceed 18.0V, otherwise the voltage stress may cause a permanent damage to the LSI.

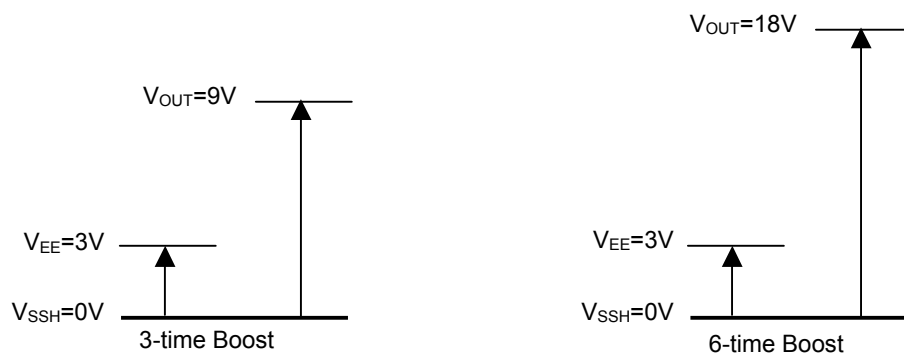


Fig 9 Boost Voltage

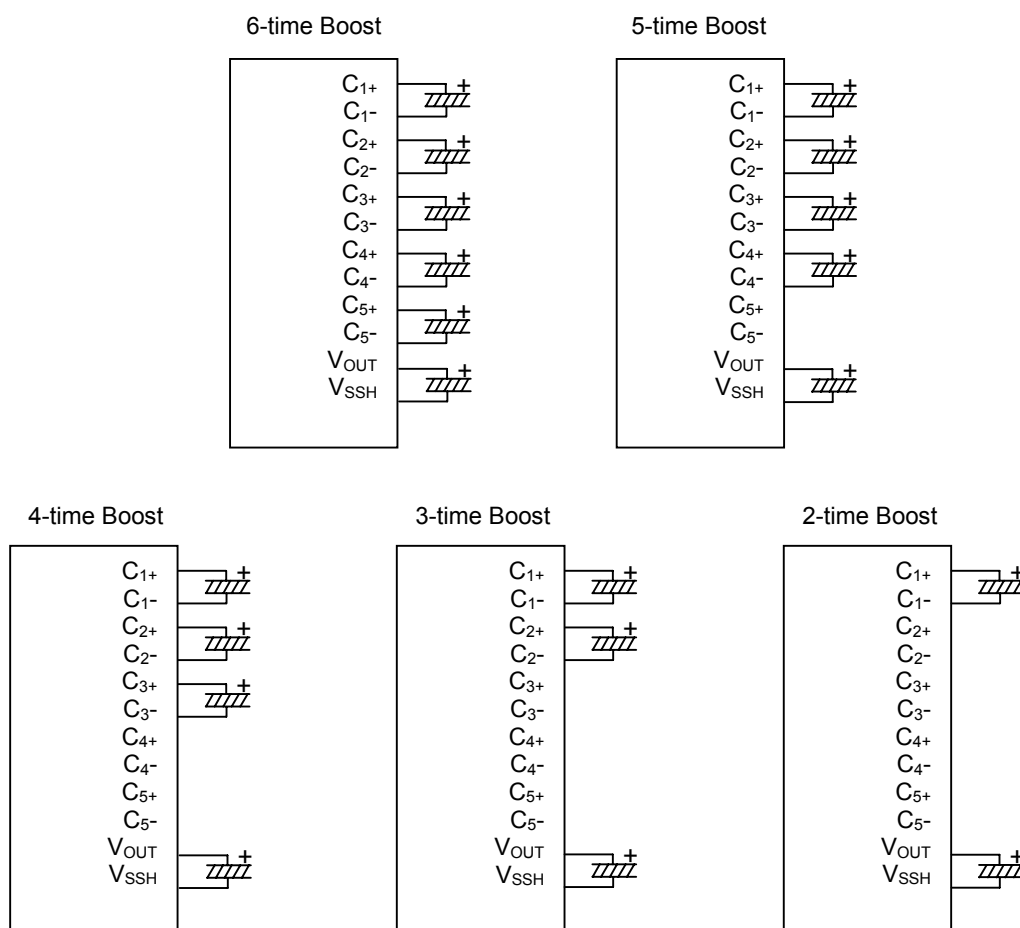


Fig 10 External Capacitor Connection of Voltage Booster

(11-2) Voltage Converter

(11-2-1) Reference Voltage Generator

The reference voltage generator produces the reference voltage ($V_{BA}=0.9 \times V_{EE}$). When using the internal LCD power supply, connect the V_{BA} and the V_{REF} , or supply $0.9 \times V_{EE}$ or lower voltage on the V_{REF} . When using an external LCD power supply, the V_{BA} should be open.

(11-2-2) Voltage Regulator

The voltage regulator consists of an operational amplifier with gain control and EVR. The V_{REF} voltage is multiplied to obtain the V_{REG} voltage, and its multiple (boost level) is set by the D_2 - D_0 ($VU2$ - $VU0$) bits of the “Boost Level” instruction. The formula is shown below.

$$V_{REG} = V_{REF} \times N \quad (N: \text{Boost Level})$$

(11-2-3) Electrical Variable Resistor (EVR)

The EVR is used to fine-tune the V_{LCD} voltage to optimize display contrast. The EVR value is controlled in 128 steps by setting the D_3 - D_0 (DV_6 - DV_0) bits of the “EVR Control” instruction. The formula is shown below.

$$V_{LCD} = 0.5 \times V_{REG} + M (V_{REG} - 0.5 \times V_{REG}) / 127 \quad (M: \text{EVR Value})$$

(11-2-4) LCD Bias Voltage Generator

The LCD bias voltage generator consists of buffer amplifiers and bleeder resistors to generate the LCD bias voltages such as the V_{LCD} , V_1 , V_2 , V_3 and V_4 , and its bias ratio is selected from 1/4, 1/5, 1/6, 1/7, 1/8, 1/9 and 1/10.

As shown in Fig 11, when using only the internal LCD power supply, the capacitors CA2 are connected to the V_{LCD} , V_1 , V_2 , V_3 and V_4 respectively.

As shown in Fig 12, when using no internal LCD power supply, the LCD bias voltages are externally supplied on the V_{LCD} , V_1 , V_2 , V_3 and V_4 , and the internal LCD power supply should be turned off by setting “0” at the “DCON” and “AMPON” bits. And the C_{1+} , C_{1-} , C_{2+} , C_{2-} , C_{3+} , C_{3-} , C_{4+} , C_{4-} , C_{5+} , C_{5-} , V_{EE} , V_{REF} and V_{REG} are open.

Fig 13 and 14 show typical peripheral circuits when partially using the LCD power supply without the reference voltage generator.

Fig 15 shows the circuit when partially using the LCD power supply without the voltage booster.

(11-3) External Components for LCD Power Supply

Using Only Internal LCD Power Supply (6x boost)

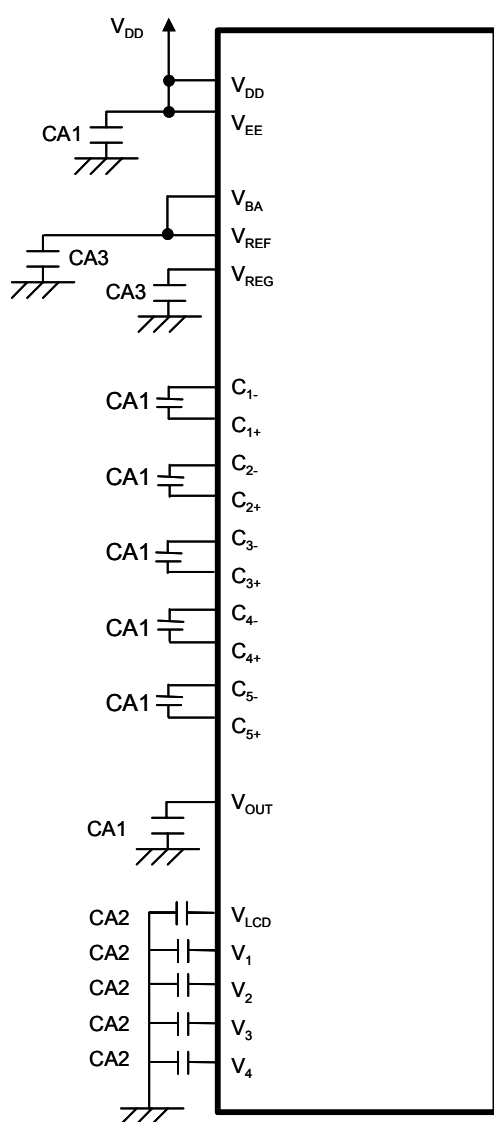


Fig 11

Using Only External LCD Power Supply

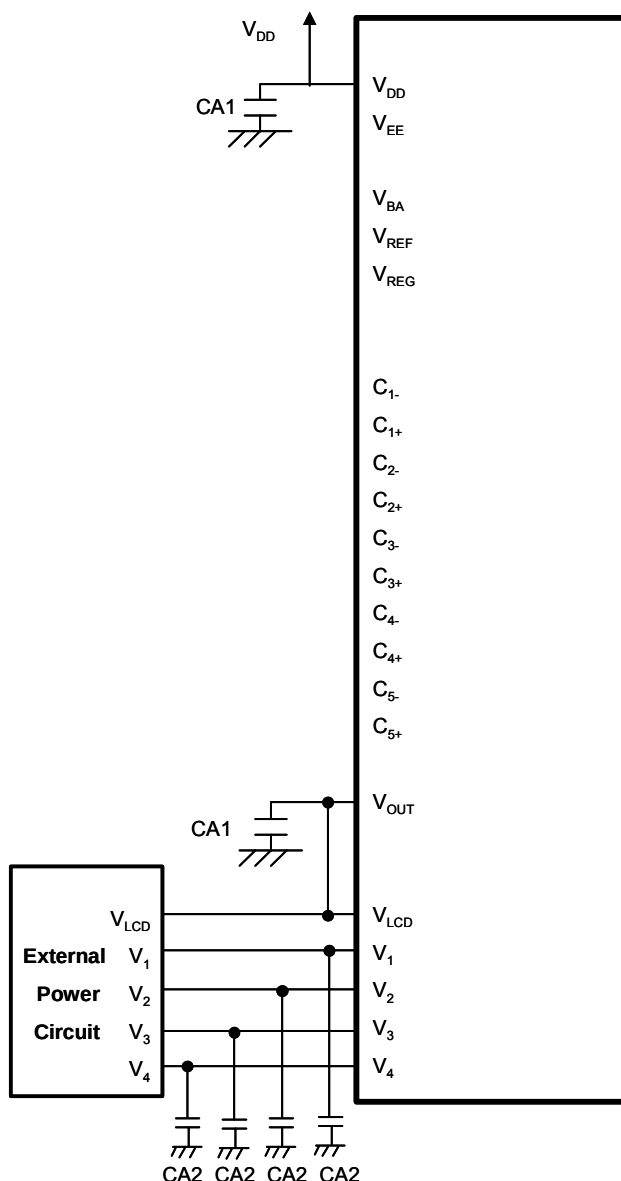


Fig 12

Reference Values

CA1	1.0 to 4.7 μ F
CA2	1.0 to 2.2 μ F
CA3	0.1 μ F

NOTE1) B grade capacitor is recommended for CA1-CA3. Make sure what is the best capacitor value in the particular application.

NOTE2) Parasitic resistance on the power supply lines (V_{DD} , V_{SS} , V_{EE} , V_{SSH} , V_{OUT} , V_{LCD} , V_1 , V_2 , V_3 and V_4) reduces step-up efficiency of the voltage booster, and may have an impact on the LSI's operation and display quality. To minimize this impact, be sure to lay out the shortest wires and place capacitors as close to the LSI as possible.

Using Internal LCD Power Supply Without Reference Voltage generator (1) (6x boost)

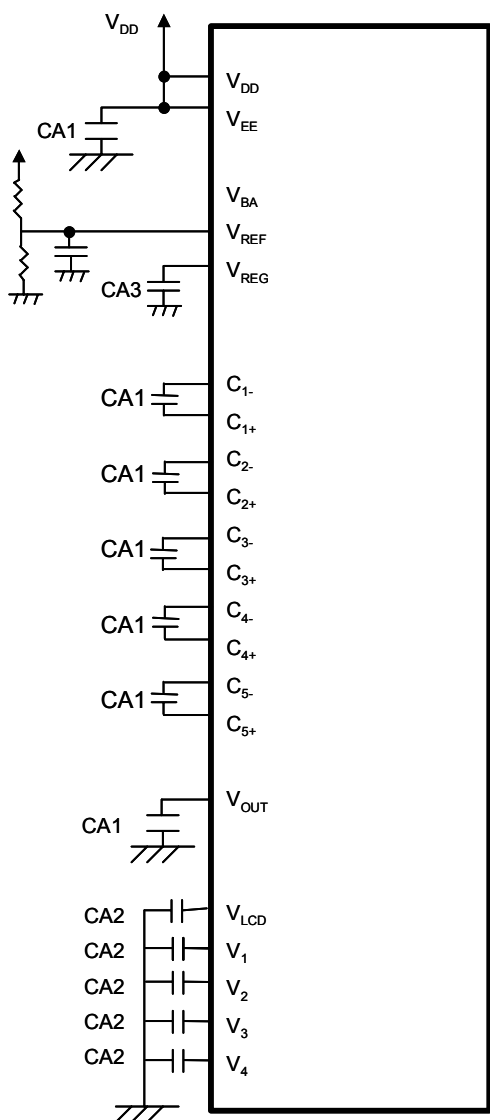


Fig 13

Using Internal LCD Power Supply Without Reference Voltage generator (2) (6x boost)

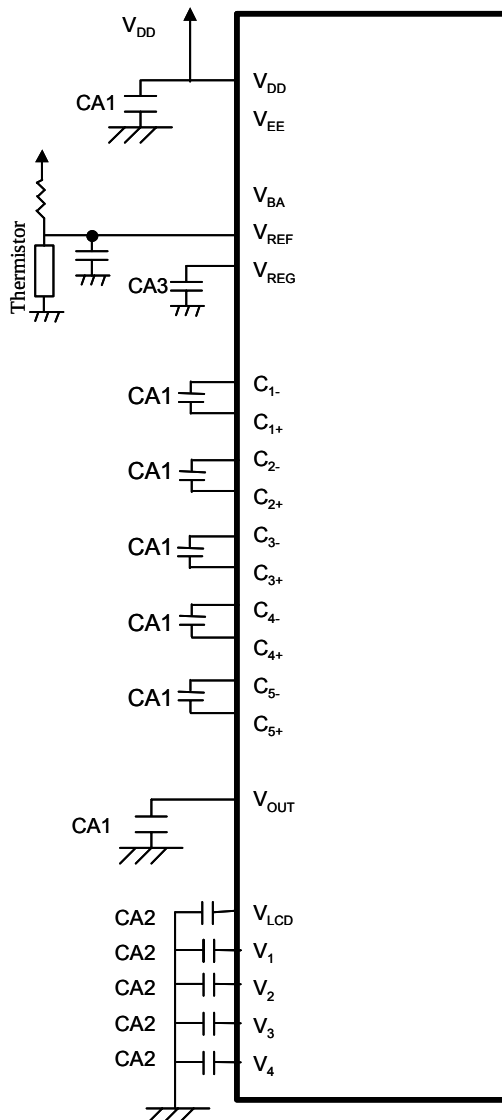


Fig 14

Reference Values

Reference values	
CA1	1.0 to 4.7 μ F
CA2	1.0 to 2.2 μ F
CA3	0.1 μ F

NOTE1) B grade capacitor is recommended for CA1-CA3. Make sure what is the best capacitor value in the particular application.

NOTE2) Parasitic resistance on the power supply lines (V_{DD} , V_{SS} , V_{EE} , V_{SSH} , V_{OUT} , V_{LCD} , V_1 , V_2 , V_3 and V_4) reduces step-up efficiency of the voltage booster, and may have an impact on the LSI's operation and display quality. To minimize this impact, be sure to lay out the shortest wires and place capacitors as close to the LSI as possible.

Using Internal LCD Power Supply Without Voltage Booster

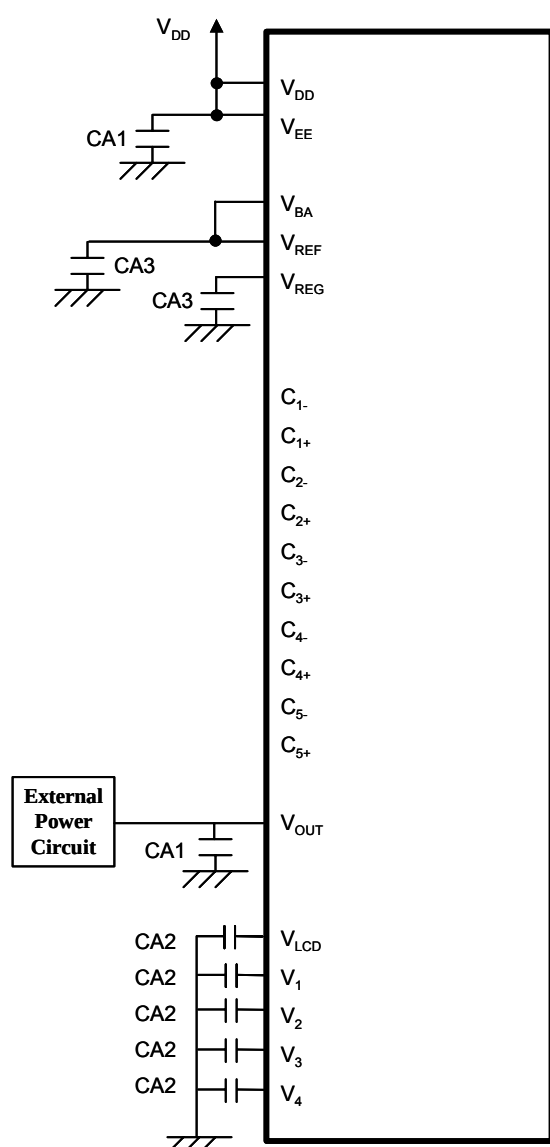


Fig 15

Reference Values

CA1	1.0 to 4.7 μ F
CA2	1.0 to 2.2 μ F
CA3	0.1 μ F

NOTE1) B grade capacitor is recommended for CA1-CA3. Make sure what is the best capacitor value in the particular application.

NOTE2) Parasitic resistance on the power supply lines (V_{DD} , V_{SS} , V_{EE} , V_{SSH} , V_{OUT} , V_{LCD} , V_1 , V_2 , V_3 and V_4) reduces step-up efficiency of the voltage booster, and may have an impact on the LSI's operation and display quality. To minimize this impact, be sure to lay out the shortest wires and place capacitors as close to the LSI as possible.

(11-4) Discharge Circuit

The LSI incorporates two discharge circuits which are independently controlled for the V_{LCD} and V_1 - V_4 and for the V_{OUT} . The V_{LCD} and V_1 - V_4 are discharged by setting "1" at the D_0 (DIS) bit of the "Discharge ON/OFF" instruction or the reset by the RESb. And the V_{OUT} (100K Ω internal resistor between V_{OUT} and V_{EE}) is discharged by setting "1" at the D_1 (DIS2) bit of this instruction. Be sure to turned off the internal or external LCD power supply when this instruction is executed, otherwise it may function as a current load and affect an operating current. Refer to "(14-22) Discharge ON/OFF".

(11-5) Power ON/OFF

To protect the LSI from overcurrent, the following sequences must be maintained to turn on and off the power supply. In addition to the following discussions, refer to "(19) TYPICAL INSTRUCTION SEQUENCES".

(11-5-1) Power ON/OFF in Using Internal LCD Power Supply

Power ON

First " V_{DD} and V_{EE} ON", next "Reset by RESb", then "Internal LCD power supply ON". Be sure to execute the "Display ON" instruction later than the completion of this power ON sequence. Otherwise, unexpected pixels may be turned on instantly.

Power OFF

First "Reset by RESb or "HALT" instruction", next " V_{DD} and V_{EE} OFF". If using different power sources for the V_{DD} and the V_{EE} individually, the V_{EE} must be turned off after the reset or the "HALT". After that, the V_{DD} can be turned off, waiting until the LCD bias voltages (V_{LCD} , V_1 , V_2 , V_3 and V_4) drop below the threshold level of LCD pixels.

(11-5-2) Power ON/OFF in Using External LCD Power Supply

Power ON

First " V_{DD} and V_{EE} ON", next "Reset by RESb", then "External LCD power supply ON". When using only external V_{OUT} , first " V_{DD} ON", next "Reset by RESb", then "External V_{OUT} ON", as well.

Power OFF

First "Reset by RESb or "HALT" instruction" to isolate external LCD bias voltages, next " V_{DD} OFF". For more safety, placing a resistor in series on the V_{LCD} line (or the V_{OUT} line in using only the external V_{OUT}) is recommended. That resistance is usually between 50 Ω and 100 Ω .

(12) RESET FUNCTION

The reset function initializes the LSI to the following default status by setting the RESb to “L”. Connecting the RESb with MPU’s reset is recommended so that the LSI and MPU is initialized at a time.

Default Status

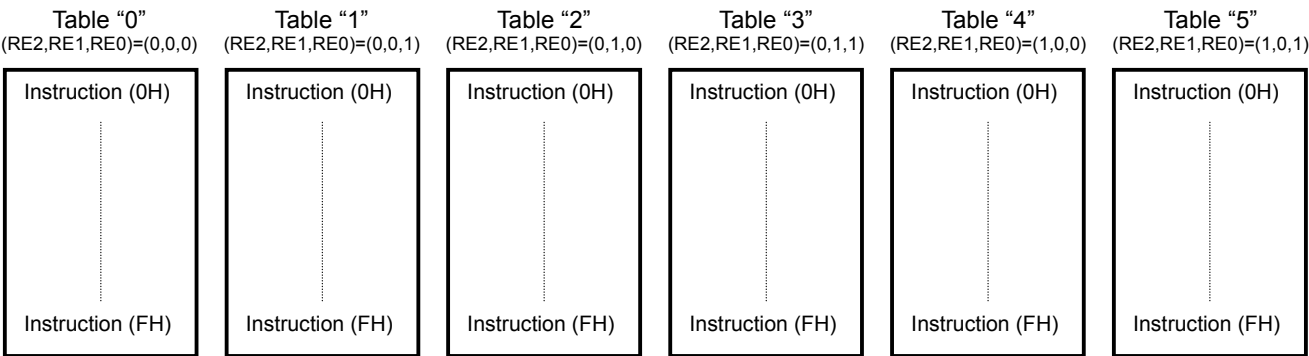
1. Display Data in DDRAM	:Undefined
2. Column Address	:(00)H
3. Row Address	:(00)H
4. Initial Display Line	:(0)H (1st line)
5. Display ON/OFF	:OFF
6. Reverse Display ON/OFF	:OFF (Normal)
7. Duty Cycle Ratio	:1/81 Duty (DSE=0)
8. N-line Inversion ON/OFF	:OFF
9. COM Scan Direction	:COM ₀ → COM ₇₉
10. Increment Control	:Auto-increment OFF (AIM, AXI, AYI)=(0, 0, 0)
11. REF	:REF=0 (Normal)
12. Swap	:OFF (Normal)
13. EVR Value	:(0, 0, 0, 0, 0, 0, 0)
14. Internal LCD Power Supply	:OFF
15. Display Mode	:Grayscale Mode
16. LCD Bias Ratio	:1/9 Bias
17. Palette 0	:(0, 0, 0, 0, 0)
18. Palette 1	:(0, 0, 0, 1, 1)
19. Palette 2	:(0, 0, 1, 0, 1)
20. Palette 3	:(0, 0, 1, 1, 1)
21. Palette 4	:(0, 1, 0, 0, 1)
22. Palette 5	:(0, 1, 0, 1, 1)
23. Palette 6	:(0, 1, 1, 0, 1)
24. Palette 7	:(0, 1, 1, 1, 1)
25. Palette 8	:(1, 0, 0, 0, 1)
26. Palette 9	:(1, 0, 0, 1, 1)
27. Palette 10	:(1, 0, 1, 0, 1)
28. Palette 11	:(1, 0, 1, 1, 1)
29. Palette 12	:(1, 1, 0, 0, 1)
30. Palette 13	:(1, 1, 0, 1, 1)
31. Palette 14	:(1, 1, 1, 0, 1)
32. Palette 15	:(1, 1, 1, 1, 1)
33. Display Mode Control	:Variable 16-grayscale Mode (4,096 Colors)
34. Bus Length	:8-bit Bus Length
35. Discharge ON/OFF	:OFF (DIS,DIS2)=(0,0)

(13) INSTRUCTION TABLES

(13-1) Instruction Table and Register Address

The LSI incorporates 6 instruction tables as shown in Fig 16, and each instruction table has a specific address in between “0” and “5”. And each instruction register has a specific address in between (0H) and (FH), and instruction is read out from the register by the “Register Address” and “Register Read” instructions.

Fig 17 shows part of the instruction sequence, where the instruction table should be specified prior to other instructions. However, when some instructions of the same table are sequentially executed, the table selection may be omitted. In addition, the “Display Data Write”, “Display Data Read” and “Register Read” instructions can be performed in any table.



NOTE) Address (FH) is assigned to “Instruction Table Select” in any table.

Fig 16 Instruction Table Overview

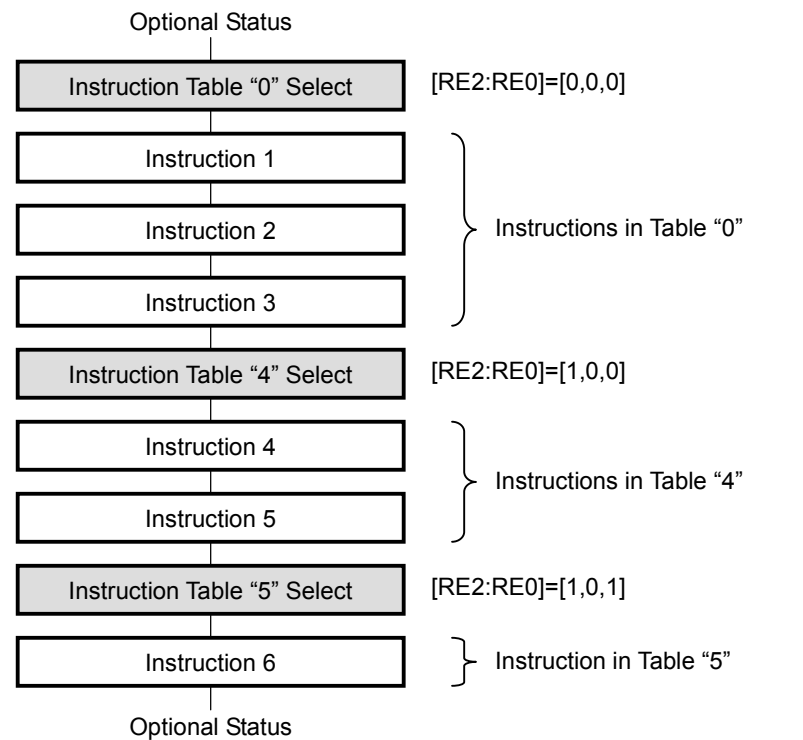


Fig 17 Outline of Instruction Sequence

(13-2) Instruction Table 0 (RE2, RE1, RE0)=(0, 0, 0)

Instructions/ Register Address [NH]		Code (80 Series MPU I/F)							Code								Functions
		CSb	RS	RDb	WRb	RE2	RE1	RE0	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
1	Display Data Write	0	0	1	0	0/1	0/1	0/1	Write Data								Writing Display Data
2	Display Data Read	0	0	0	1	0/1	0/1	0/1	Read Data								Reading Display Data
3	Column Address (Lower) [0H]	0	1	1	0	0	0	0	0	0	0	0	AX3	AX2	AX1	AX0	Setting Column Address for start point
	Column Address (Upper) [1H]	0	1	1	0	0	0	0	0	0	0	1	AX7	AX6	AX5	AX4	Setting Column Address for start point
4	Row Address (Lower) [2H]	0	1	1	0	0	0	0	0	0	1	0	AY3	AY2	AY1	AY0	Setting Row Address for start point
	Row Address (Upper) [3H]	0	1	1	0	0	0	0	0	0	1	1	*	AY6	AY5	AY4	Setting Row Address for start point
5	Initial Display Line (Lower) [4H]	0	1	1	0	0	0	0	0	1	0	0	LA3	LA2	LA1	LA0	Setting Row Address for Initial COM
	Initial Display Line (Upper) [5H]	0	1	1	0	0	0	0	0	1	0	1	*	LA6	LA5	LA4	Setting Row Address for Initial COM
6	N-line Inversion (Lower) [6H]	0	1	1	0	0	0	0	0	1	1	0	N3	N2	N1	N0	Setting the Number of N-line Inversion
	N-line Inversion (Upper) [7H]	0	1	1	0	0	0	0	0	1	1	1	*	N6	N5	N4	Setting the Number of N-line Inversion
7	Display Control (1) [8H]	0	1	1	0	0	0	0	1	0	0	0	SHIFT	MON	ALL ON	ON/ OFF	SHIFT : Common Scan Direction MON : Grayscale/B/W Mode ALLON : All Pixels ON/OFF ON/OFF : Display ON/OFF
8	Display Control (2) [9H]	0	1	1	0	0	0	0	1	0	0	1	REV	NLIN	SWAP	REF	REV : Reverse Display ON/OFF NLIN : N-line Inversion ON/OFF SWAP : SWAP ON/OFF REF : Segment Direction
9	Increment Control [AH]	0	1	1	0	0	0	0	1	0	1	0	WIN	AIM	AYI	AXI	WIN : Window Area ON/OFF AIM : Read-Modify-Write ON/OFF AYI : Row Increment AXI : Column Increment
10	Power Control [BH]	0	1	1	0	0	0	0	1	0	1	1	AMP ON	HALT	DC ON	ACL	AMPON : Voltage Converter ON/OFF HALT : Power Save ON/OFF DCON : Voltage Booster ON/OFF ACL : Reset
11	Duty Cycle Ratio [CH]	0	1	1	0	0	0	0	1	1	0	0	DS3	DS2	DS1	DS0	Setting LCD Duty Cycle Ratio
12	Boost Level /ID Code Read [DH]	0	1	1	0	0	0	0	1	1	0	1	IDR	VU2	VU1	VU0	IDR : ID Code (Serial I/F) VU2-0 : Setting Boost Level
13	LCD Bias Ratio [EH]	0	1	1	0	0	0	0	1	1	1	0	*	B2	B1	B0	Setting LCD Bias Ratio
14	Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Table

NOTE1) * : Don't care.

NOTE2) [NH] (N=0-F) : Register Address

NOTE3) Any nonexistent instruction code is prohibited.

NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.

NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

(13-3) Instruction Table 1 (RE2, RE1, RE0)=(0, 0, 1)

Instructions/ Register Address [NH]	Code (80 series MPU I/F)							Code								Functions
	CSb	RS	RDb	WRb	RE2	RE1	RE0	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
Palette A0/A8 (Lower) [0H]	0	1	1	0	0	0	1	0	0	0	0	PA03/ PA83	PA02/ PA82	PA01/ PA81	PA00/ PA80	Setting Palette Data : A0(PS=0) /A8(PS=1)
Palette A0/A8 (Upper) [1H]	0	1	1	0	0	0	1	0	0	0	1	*	*	*	PA04/ PA84	Setting Palette Data : A0(PS=0) /A8(PS=1)
Palette A1/A9 (Lower) [2H]	0	1	1	0	0	0	1	0	0	1	0	PA13/ PA93	PA12/ PA92	PA11/ PA91	PA10/ PA90	Setting Palette Data : A1(PS=0) /A9(PS=1)
Palette A1/A9 (Upper) [3H]	0	1	1	0	0	0	1	0	0	1	1	*	*	*	PA14/ PA94	Setting Palette Data : A1(PS=0) /A9(PS=1)
Palette A2/A10 (Lower) [4H]	0	1	1	0	0	0	1	0	1	0	0	PA23/ PA103	PA22/ PA102	PA21/ PA101	PA20/ PA100	Setting Palette Data : A2(PS=0) /A10(PS=1)
Palette A2/A10 (Upper) [5H]	0	1	1	0	0	0	1	0	1	0	1	*	*	*	PA24/ PA104	Setting Palette Data : A2(PS=0) /A10(PS=1)
Palette A3/A11 (Lower) [6H]	0	1	1	0	0	0	1	0	1	1	0	PA33/ PA113	PA32/P A112	PA31/ PA111	PA30/ PA110	Setting Palette Data : A3(PS=0) /A11(PS=1)
Palette A3/A11 (Upper) [7H]	0	1	1	0	0	0	1	0	1	1	1	*	*	*	PA34/ PA114	Setting Palette Data : A3(PS=0) /A11(PS=1)
Palette A4/A12 (Lower) [8H]	0	1	1	0	0	0	1	1	0	0	0	PA43/ PA123	PA42/P A122	PA41/ PA121	PA40/ PA120	Setting Palette Data : A4(PS=0) /A12(PS=1)
Palette A4/A12 (Upper) [9H]	0	1	1	0	0	0	1	1	0	0	1	*	*	*	PA44/ PA124	Setting Palette Data : A4(PS=0) /A12(PS=1)
Palette A5/A13 (Lower) [AH]	0	1	1	0	0	0	1	1	0	1	0	PA53/ PA133	PA52/P A132	PA51/ PA131	PA50/ PA130	Setting Palette Data : A5(PS=0) /A13(PS=1)
Palette A5/A13 (Upper) [BH]	0	1	1	0	0	0	1	1	0	1	1	*	*	*	PA54/ PA134	Setting Palette Data : A5(PS=0) /A13(PS=1)
Palette A6/A14 (Lower) [CH]	0	1	1	0	0	0	1	1	1	0	0	PA63/ PA143	PA62/P A142	PA61/ PA141	PA60/ PA140	Setting Palette Data : A6(PS=0) /A14(PS=1)
Palette A6/A14 (Upper) [DH]	0	1	1	0	0	0	1	1	1	0	1	*	*	*	PA64/ PA144	Setting Palette Data : A6(PS=0) /A14(PS=1)
14 Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Table

NOTE1) * : Don't care.

NOTE2) [NH] (N=0-F) : Register Address

NOTE3) Any nonexistent instruction code is prohibited.

NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.

NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

(13-4) Instruction Table 2 (RE2, RE1, RE0)=(0, 1, 0)

Instructions/ Register Address [NH]		Code (80 series MPU I/F)							Code								Functions	
		CSb	RS	RDb	WRb	RE2	RE1	RE0	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
15	Palette A7/A15 (Lower) [0H]	0	1	1	0	0	1	0	0	0	0	0	PA73/ PA153	PA72/P A152	PA71/ PA151	PA70/ PA150	Setting Palette Data : A7(PS=0) /A15(PS=1)	
	Palette A7/A15 (Upper) [1H]	0	1	1	0	0	1	0	0	0	0	1	*	*	*	PA74/ PA154	Setting Palette Data : A7(PS=0) /A15(PS=1)	
	Palette B0/B8 (Lower) [2H]	0	1	1	0	0	1	0	0	0	1	0	PB03/ PB83	PB02/ PB82	PB01/ PB81	PB00/ PB80	Setting Palette Data : B0(PS=0) /B8(PS=1)	
	Palette B0/B8 (Upper) [3H]	0	1	1	0	0	1	0	0	0	1	1	*	*	*	PB04/ PG84	Setting Palette Data : B0(PS=0) /B8(PS=1)	
	Palette B1/B9 (Lower) [4H]	0	1	1	0	0	1	0	0	1	0	0	PB13/ PB93	PB12/ PB92	PB11/ PB91	PB10/ PB90	Setting Palette Data : B1(PS=0) /B9(PS=1)	
	Palette B1/B9 (Upper) [5H]	0	1	1	0	0	1	0	0	1	0	1	*	*	*	PB14/ PB94	Setting Palette Data : B1(PS=0) /B9(PS=1)	
	Palette B2/B10 (Lower) [6H]	0	1	1	0	0	1	0	0	1	1	0	PB23/ PB103	PB22/ PB102	PB21/ PB101	PB20/ PB100	Setting Palette Data : B2(PS=0) /B10(PS=1)	
	Palette B2/B10 (Upper) [7H]	0	1	1	0	0	1	0	0	1	1	1	*	*	*	PB24/ PB104	Setting Palette Data : B2(PS=0) /B10(PS=1)	
	Palette B3/B11 (Lower) [8H]	0	1	1	0	0	1	0	1	0	0	0	0	PB33/ PB113	PB32/ PB112	PB31/ PB111	PB30/ PB110	Setting Palette Data : B3(PS=0) /B11(PS=1)
	Palette B3/B11 (Upper) [9H]	0	1	1	0	0	1	0	1	0	0	1	*	*	*	PB34/ PB114	Setting Palette Data : B3(PS=0) /B11(PS=1)	
	Palette B4/B12 (Lower) [AH]	0	1	1	0	0	1	0	1	0	1	0	0	PB43/ PB123	PB42/ PB122	PB41/ PB121	PB40/ PB120	Setting Palette Data : B4(PS=0) /B12(PS=1)
	Palette B4/B12 (Upper) [BH]	0	1	1	0	0	1	0	1	0	1	1	*	*	*	PB44/ PB124	Setting Palette Data : B4(PS=0) /B12(PS=1)	
	Palette B5/B13 (Lower) [CH]	0	1	1	0	0	1	0	1	1	0	0	0	PB53/ PB133	PB52/ PB132	PB51/ PB131	PB50/ PB130	Setting Palette Data : B5(PS=0) /B13(PS=1)
	Palette B5/B13 (Upper) [DH]	0	1	1	0	0	1	0	1	1	0	1	*	*	*	PB54/ PB134	Setting Palette Data : B5(PS=0) /B13(PS=1)	
14	Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Tablet	

NOTE1) * : Don't care.

NOTE2) [NH] (N=0-F) : Register Address

NOTE3) Any nonexistent instruction code is prohibited.

NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.

NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

(13-5) Instruction Table 3 (RE2, RE1, RE0)=(0, 1, 1)

Instructions/ Register Address [NH]		Code (80 series MPU I/F)							Code								Functions	
		CSb	RS	RDb	WRb	RE2	RE1	RE0	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
15	Palette B6/B14 (Lower) [0H]	0	1	1	0	0	1	1	0	0	0	0	PB63/ PB143	PB62/ PB142	PB61/ PB141	PB60/ PB140	Setting Palette Data : B6(PS=0) /B14(PS=1)	
	Palette B6/B14 (Upper) [1H]	0	1	1	0	0	1	1	0	0	0	1	*	*	*	PB64/ PB144	Setting Palette Data : B6(PS=0) /B14(PS=1)	
	Palette B7/B15 (Lower) [2H]	0	1	1	0	0	1	1	0	0	1	0	PB73/ PB153	PB72/ PB152	PB71/ PB151	PB70/ PB150	Setting Palette Data : B7(PS=0) /B15(PS=1)	
	Palette B7/B15 (Upper) [3H]	0	1	1	0	0	1	1	0	0	1	1	*	*	*	PB74/ PB154	Setting Palette Data : B7(PS=0) /B15(PS=1)	
	Palette C0/C8 (Lower) [4H]	0	1	1	0	0	1	1	0	1	0	0	PC03/ PC83	PC02/ PC82	PC01/ PC81	PC00/ PC80	Setting Palette Data : C0(PS=0) /C8(PS=1)	
	Palette C0/C8 (Upper) [5H]	0	1	1	0	0	1	1	0	1	0	1	*	*	*	PC04/ PC84	Setting Palette Data : C0(PS=0) /C8(PS=1)	
	Palette C1/C9 (Lower) [6H]	0	1	1	0	0	1	1	0	1	1	0	PC13/ PC93	PC12/ PC92	PC11/ PC91	PC10/ PC90	Setting Palette Data : C1(PS=0) /C9(PS=1)	
	Palette C1/C9 (Upper) [7H]	0	1	1	0	0	1	1	0	1	1	1	*	*	*	PC14/ PC94	Setting Palette Data : C1(PS=0) /C9(PS=1)	
	Palette C2/C10 (Lower) [8H]	0	1	1	0	0	1	1	1	0	0	0	PC23/ PC103	PC22/ PC102	PC21/ PC101	PC20/ PC100	Setting Palette Data : C2(PS=0) /C10(PS=1)	
	Palette C2/C10 (Upper) [9H]	0	1	1	0	0	1	1	1	0	0	1	*	*	*	PC24/ PC104	Setting Palette Data : C2(PS=0) /C10(PS=1)	
	Palette C3/C11 (Lower) [AH]	0	1	1	0	0	1	1	1	0	1	0	PC33P C113	PC32/ PC112	PC31/ PC111	PC30/ PC110	Setting Palette Data : C3(PS=0) /C11(PS=1)	
	Palette C3/C11 (Upper) [BH]	0	1	1	0	0	1	1	1	0	1	1	*	*	*	PC34/ PC114	Setting Palette Data : C3(PS=0) /C11(PS=1)	
	Palette C4/C12 (Lower) [CH]	0	1	1	0	0	1	1	1	1	1	0	0	PC43/ PC123	PC42/ PC122	PC41/ PC121	PC40/ PC120	Setting Palette Data : C4(PS=0) /C12(PS=1)
	Palette C4/C12 (Upper) [DH]	0	1	1	0	0	1	1	1	1	1	0	1	*	*	*	PC44/ PC124	Setting Palette Data : C4(PS=0) /C12(PS=1)
14	Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Table	

NOTE1) * : Don't care.

NOTE2) [NH] (N=0-F) : Register Address

NOTE3) Any nonexistent instruction code is prohibited.

NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.

NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

(13-6) Instruction Table 4 (RE2, RE1, RE0)=(1, 0, 0)

Instructions/ Register Address [NH]		Code (80 series MPU I/F)							Code								Functions
		CSb	RS	RDb	WRb	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
15	Palette C5/C13 (Lower) [0H]	0	1	1	0	1	0	0	0	0	0	0	PC53/ PC133	PC52/ PC132	PC51/ PC131	PC50/ PC130	Setting Palette Data : C5(PS=0) /C13(PS=1)
	Palette C5/C13 (Upper) [1H]	0	1	1	0	1	0	0	0	0	0	1	*	*	*	PC54/ PC134	Setting Palette Data : C5(PS=0) /C13(PS=1)
	Palette C6/C14 (Lower) [2H]	0	1	1	0	1	0	0	0	0	1	0	PC63/P C143	PC62/ PC142	PC61/ PC141	PC60/ PC140	Setting Palette Data : C6(PS=0) /C14(PS=1)
	Palette C6/C14 (Upper) [3H]	0	1	1	0	1	0	0	0	0	1	1	*	*	*	PC64/ PC144	Setting Palette Data : C6(PS=0) /C14(PS=1)
	Palette C7/C15 (Lower) [4H]	0	1	1	0	1	0	0	0	1	0	0	PC73/ PC153	PC72/ PC152	PC71/ PC151	PC70/ PC150	Setting Palette Data : C7(PS=0) /C15(PS=1)
	Palette C7/C15 (Upper) [5H]	0	1	1	0	1	0	0	0	1	0	1	*	*	*	PC74/ PC154	Setting Palette Data : C7(PS=0) /C15(PS=1)
16	Initial COM [6H]	0	1	1	0	1	0	0	0	1	1	0	SC3	SC2	SC1	SC0	Setting start COM for scanning
17	Duty-1 /Display Clock ON/OFF [7H]	0	1	1	0	1	0	0	0	1	1	1	*	*	DSE	SON	SON : Display Clock ON/OFF DSE : Duty-1 ON/OFF
18	Display Mode Control [8H]	0	1	1	0	1	0	0	1	0	0	0	PWM	C256	*	*	PWM : Variable/Fixed Grayscale Mode C256 : 256-color Mode ON/OFF
19	Bus Length [9H]	0	1	1	0	1	0	0	1	0	0	1	HSW	ABS	CKS	WLS	HSW : High Speed Writing ABS : Bit Assignment CKS : Oscillator Set WLS : 8-/16-bit Bus Length
20	EVR Control (Lower) [AH]	0	1	1	0	1	0	0	1	0	1	0	DV3	DV2	DV1	DV0	Setting EVR Value (Lower Bit)
	EVR Control (Upper) [BH]	0	1	1	0	1	0	0	1	0	1	1	*	DV6	DV5	DV4	Setting EVR Value (Upper Bit)
21	Frequency Control [DH]	0	1	1	0	1	0	0	1	1	0	1	*	RF2	RF1	RF0	Adjusting Oscillation Frequency
22	Discharge ON/OFF [EH]	0	1	1	0	1	0	0	1	1	1	0	*	*	DIS2	DIS	Discharge ON/OFF
23	Register Address [CH]	0	1	1	0	1	0	0	1	1	0	0	Register Address				Setting Register Address
24	Register Read /ID Code Read	0	1	0	1	0/1	0/1	0/1	ID3	ID2	ID1	ID0	Read Data				ID Code (Parallel I/F) Reading Instruction
14	Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Table Select

NOTE1) * : Don't care.

NOTE2) [NH] (N=0-F) : Register Address

NOTE3) Any nonexistent instruction code is prohibited.

NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.

NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

(13-7) Instruction Table 5 (RE2, RE1, RE0)=(1, 0, 1)

Instructions/ Register Address [NH]		Code (80 series MPU I/F)							Code								Functions
		CSb	RS	RDb	WRb	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
25	Window End Column Address (Lower) [0H]	0	1	1	0	1	0	1	0	0	0	0	EX3	EX2	EX1	EX0	Setting Column Address for end point
	Window End Column Address (Upper) [1H]	0	1	1	0	1	0	1	0	0	0	1	EX7	EX6	EX5	EX4	Setting Column Address for end point
26	Window End Row Address (Lower) [2H]	0	1	1	0	1	0	1	0	0	1	0	EY3	EY2	EY1	EY0	Setting Row Address for end point
	Window End Row Address (Upper) [3H]	0	1	1	0	1	0	1	0	0	1	1	*	EY6	EY5	EY4	Setting Row Address for end point
27	Initial Line-reverse Address (Lower) [4H]	0	1	1	0	1	0	1	0	1	0	0	LS3	LS2	LS1	LS0	Setting Start Line for Line-reverse Display
	Initial Line-reverse Address (Upper) [5H]	0	1	1	0	1	0	1	0	1	0	1	*	LS6	LS5	LS4	Setting Start Line for Line-reverse Display
28	Last Line-reverse Address (Lower) [6H]	0	1	1	0	1	0	1	0	1	1	0	LE3	LE2	LE1	LE0	Setting End Line for Line-reverse Display
	Last Line-reverse Address (Upper) [7H]	0	1	1	0	1	0	1	0	1	1	1	*	LE6	LE5	LE4	Setting End Line for Line-reverse Display
29	Line Reverse ON/OFF [8H]	0	1	1	0	1	0	1	1	0	0	0	*	*	BT	LREV	BT : Blink Set LREV : Line-reverse ON/OFF
30	Upper/Lower Palette Select [9H]	0	1	1	0	1	0	1	1	0	0	1	*	*	*	PS	PS : Upper/Lower Palette Register
31	PWM Control [AH]	0	1	1	0	1	0	1	1	0	1	0	PWMS	PWMA	PWMB	PWMC	Setting PWM Mode
14	Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Table

NOTE1) * : Don't care.

NOTE2) [NH] (N=0-F) : Register Address

NOTE3) Any nonexistent instruction code is prohibited.

NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.

NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

(14) INSTRUCTION DESCRIPTIONS

This chapter provides detailed descriptions about each instruction. These descriptions are written with the assumption that 80-series MPU is used. When using 68-series MPU, the polarities of the E and R/W signals differ from those of the RDb and WRb signals.

(14-1) Display Data Write

The “Display Data Write” instruction writes display data on a specified DDRAM address.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	0	1	0	0/1	0/1	0/1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Display Data							

(14-2) Display Data Read

The “Display Data Read” instruction reads out display data from a specified DDRAM address. One dummy read is necessary right after DDRAM address setting.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	0	0	1	0/1	0/1	0/1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Display Data							

(14-3) Column Address

The “Column Address” instruction specifies the column address of the start point. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	AX3	AX2	AX1	AX0

(Default: AX3-AX0=0H / Register Address: 0H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	AX7	AX6	AX5	AX4

(Default: AX7-AX4=0H / Register Address: 1H)

(14-4) Row Address

The “Row Address” instruction specifies the row address of the start point. Available setting range is from (00H) to (4FH), and outside this range is not allowed. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	AY3	AY2	AY1	AY0

(Default: AY3-AY0=0H / Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	AY6	AY5	AY4

(Default: AY6-AY4=0H / Register Address: 3H)

(14-5) Initial Display Line

This instruction sets the row address, which corresponds to an initial COM and is normally positioned on top of a screen in full display. For more information, refer to “(14-16) Initial COM”. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	LA3	LA2	LA1	LA0

(Default: LA3-LA0=0H / Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	LA6	LA5	LA4

(Default: LA6-LA4=0H / Register Address: 5H)

Table 18 Initial Display Line Address

LA6	LA5	LA4	LA3	LA2	LA1	LA0	Row Address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
⋮							⋮
1	0	0	1	1	1	1	79

(14-6) N-line Inversion

The number of N line is selected in between “2” and “80”. When the N-line inversion is enabled by setting “1” at the D₂ (NLIN) bit of the “Display Control (2)” instruction, the FR toggles once every N lines. When the N-line inversion is disabled by setting “0” at this bit, the FR toggles by the frame.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	N3	N2	N1	N0

(Default: N3-N0=0H / Register Address: 6H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	N6	N5	N4

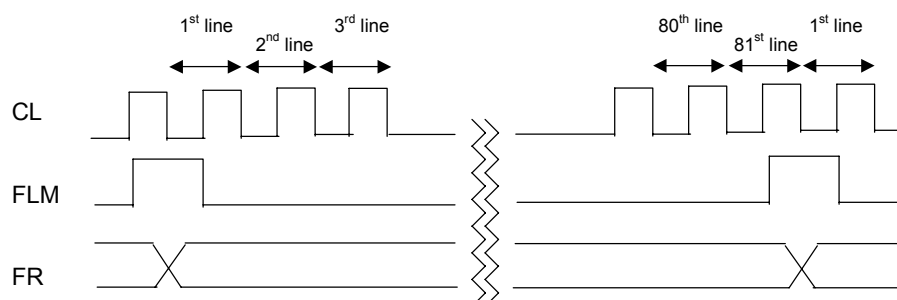
(Default: N6-N4=0H / Register Address: 7H)

Table 19 N-line Inversion

N6	N5	N4	N3	N2	N1	N0	N Line
0	0	0	0	0	0	0	Inhibited
0	0	0	0	0	0	1	2
⋮							⋮
1	0	0	1	1	1	1	80

NOTE1) N Line=(N Value)+1

N-line inversion OFF



N-line inversion ON

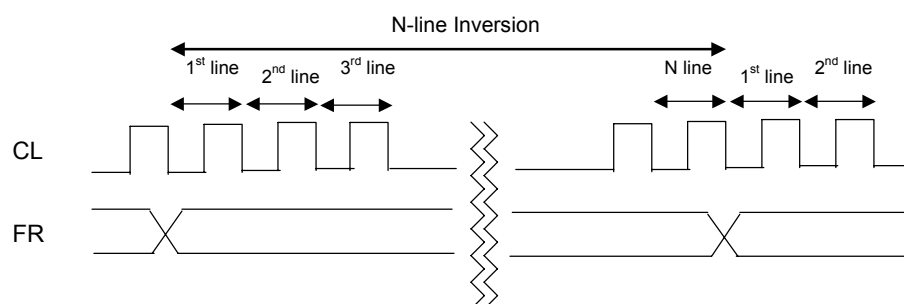


Fig 18 N-line Inversion Timing (1/81 Duty)

(14-7) Display Control (1)

The “Display Control (1)” instruction controls display conditions.

CSb	RS	RDb	WRb	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	0	0	0	1	0	0	0	SHIFT	MON	ALL ON	ON /OFF

(Default: [SHIFT,MON,ALLON,ON/OFF]=0H / Register Address: 8H)

D₀ (ON/OFF)

ON/OFF=0 : Display OFF (All COM/SEG fixed at V_{SSH} level)

ON/OFF=1 : Display ON

D₁ (ALLON)

This bit forcibly turns on all pixels regardless of display data. This bit has a priority over the “REV” bit of the “Display Control (2)” instruction.

ALLON=0 : Normal

ALLON=1 : All pixels ON

D₂ (MON)

MON=0 : Grayscale Mode (Variable 16-grayscale, Variable 8-grayscale or Fixed 8-grayscale Mode)

MON=1 : B&W Mode

D₃ (SHIFT)

SHIFT=0 : COM₀ → COM₇₉

SHIFT=1 : COM₀ ← COM₇₉

(14-8) Display Control (2)

The “Display Control (2)” instruction controls display conditions.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	REV	NLIN	SWAP	REF

(Default: [REV,NLIN,SWAP,REF]=0H / Register Address: 9H)

D₀ (REF)

This bit controls the DDRAM access direction which reverses the segment direction for reducing the restrictions on the IC position of an LCD module. For more information, refer to “(17) SWAP FUNCTION”.

D₁ (SWAP)

This bit swaps palettes A_j and palettes C_j (j=0-15). This function reduces the restrictions on the IC position of an LCD module. Refer to “(16) SWAP FUNCTION”.

SWAP=0 : SWAP OFF
SWAP=1 : SWAP ON

D₂ (NLIN)

This bit enables the N-line inversion.

NLIN=0 : N-line Inversion OFF (FR toggles by the frame.)
NLIN=1 : N-line Inversion ON (FR toggles once every N lines.)

D₃ (REV)

This bit enables the reverse display function that reverses the polarities of all display data without changing the DDRAM.

REV=0 : Reverse Display OFF (Normal)
REV=1 : Reverse Display ON

Table 20 Reverse Display ON/OFF

REV	Display	DDRAM Data → Display Data	
0	Normal	0	0
		1	1
1	Reverse	0	1
		1	0

(14-9) Increment Control

The “AIM”, “AYI” and “AXI” bits set an auto-increment operation to the column address and row address individually. Once this mode is set up, the column address, row address or both are automatically counted up, whenever the DDRAM is accessed. The “WIN” bits enables/disables the window area access.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	WIN	AIM	AYI	AXI

(Default: [WIN,AIM,AYI,AXI]=0H / Register Address: AH)

D₂ (AIM)

Table 21 Read-modify-write ON/OFF

AIM	Increment Mode	NOTE
0	Read-modify-write OFF	1
1	Read-modify-write ON	2

NOTE1) Increment in writing and reading display data

NOTE2) Increment in writing display data only

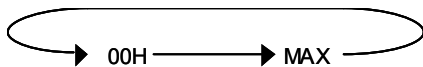
D₁, D₀ (AYI, AXI)

Table 22 Column/Row Increment

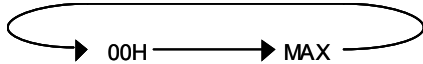
AYI	AXI	Column/Row Increment	NOTE
0	0	Non Increment	1
0	1	Column Address Increment	2
1	0	Row Address Increment	3
1	1	Column & Row Addresses Increment	4

NOTE1) Non increment. The “AIM” bit is disabled.

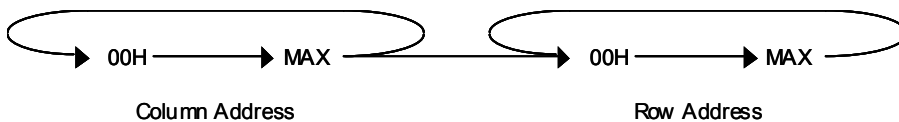
NOTE2) Column address increment. The “AIM” bit is enabled.



NOTE3) Row address increment. The “AIM” bit is enabled.



NOTE4) Column & row addresses increment. The “AIM” bit is enabled.

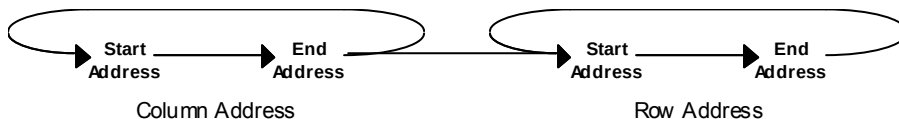


D₃ (WIN)

The window access should be enabled (WIN=1) in combination with the auto-increment operation (AXI=1, AYI=1). The typical sequence of the window area setting is discussed in “(4-2) Window Area for DDRAM Access”.

WIN=0 : Window Area Access OFF (Normal DDRAM Access)

WIN=1 : Window Area Access ON



(14-10) Power Control

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	1	AMPON	HALT	DCON	ACL

(Default: [AMPON,HALT,DCON,ACL]=0H / Register Address: BH)

D₀ (ACL)

This bit initializes the internal LCD power supply.

ACL=0 : Initialization OFF (Normal)
 ACL=1 : Initialization ON

NOTE) During the initialization, "1" is read out as the status of the "ACL" bit by the "Register Read" instruction. After the initialization, it is "0". As the CLK triggers the initialization, the "wait time" at least equivalent to 2 cycles of the CLK is required for the next instruction.

D₁ (DCON)

The "DCON" bit activates the voltage booster.

DCON=0 : Voltage Booster OFF
 DCON=1 : Voltage Booster ON

D₂ (HALT)

The "HALT" bit enables the power save mode. During the power save, operating current is down to the stand-by level. The internal state of the LSI in the power save mode is listed below.

HALT=0 : Power Save OFF (Normal)
 HALT=1 : Power Save ON

Internal State in Power Save Mode (HALT="1")

- Internal oscillator and internal LCD power supply are halted.
- All segment and common drivers are fixed at V_{SSH} level.
- External clock to the OSC1 cannot be accepted.
- Display data in the DDRAM is being maintained.
- Data in the instruction registers are being maintained.
- V_{LCD}, V₁, V₂, V₃ and V₄ are in high impedance.

NOTE) In the power save ON sequence, execute the "Display OFF" prior to the "Power Save ON". In the power save OFF sequence, execute the "Power save OFF" prior to the "Display ON". If the "Power Save ON/OFF" instruction is executed during the "Display ON", unexpected pixels may be turned on instantly.

D₃ (AMPON)

The "AMPON" bit activates the voltage converter which includes the reference voltage generator, the voltage regulator and the LCD bias generator.

AMPON=0 : Voltage Converter OFF
 AMPON=1 : Voltage Converter ON

(14-11) Duty Cycle Ratio

The “Duty Cycle Ratio” instruction selects LCD duty cycle ratio, and is used to carry out the partial display in combination with other instructions such as the “Boost Level”, the “LCD Bias Ratio” and the “EVR Control”.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	0	DS3	DS2	DS1	DS0

(Default: DS3-DS0=0H / Register Address: CH)

Table 23 Duty Cycle Ratio

DS3	DS2	DS1	DS0	Duty Cycle Ratio		# of Commons
				DSE=0	DES=1	
0	0	0	0	1/81	1/80	80 commons
0	0	0	1	1/77	1/76	76 commons
0	0	1	0	1/69	1/68	68 commons
0	0	1	1	1/57	1/56	56 commons
0	1	0	0	1/47	1/46	46 commons
0	1	0	1	1/39	1/38	38 commons
0	1	1	0	1/33	1/32	32 commons
0	1	1	1	1/27	1/26	26 commons
1	0	0	0	1/17	1/16	16 commons
1	0	0	1	1/13	1/12	12 commons
1	0	1	0	Inhibited		
1	0	1	1	Inhibited		
1	1	0	0	Inhibited		
1	1	0	1	Inhibited		
1	1	1	0	Inhibited		
1	1	1	1	Inhibited		

NOTE) Duty cycle ratio is subtracted by 1 (Duty-1) from the original duty cycle ratio by setting “1” at the D₁ (DSE) bit of the “Duty-1 ON/OFF” instruction. Refer to “(14-17) Duty-1 /Display Clock ON/OFF”.

(14-12) Boost Level /ID Code Read

The “Boost Level” selects the multiple of the voltage booster, the “ID Code Read” enables reading out the ID code.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	1	IDR	VU2	VU1	VU0

(Default: IDR,VU2-VU0=0H / Register Address: DH)

D₂, D₁, D₀ (VU2, VU1, VU0)

Table 24 Boost Level

VU2	VU1	VU0	Boost Level
0	0	0	1 time (No boost)
0	0	1	2 times
0	1	0	3 times
0	1	1	4 times
1	0	0	5 times
1	0	1	6 times
1	1	0	Inhibited
1	1	1	Inhibited

D₃ (IDR)

This bit is used only in the serial interface mode, and the ID code is read out by setting “1” at this bit. Refer to “(15) CHIP IDENTIFICATION (ID) CODE” for more information.

(14-13) LCD Bias Ratio

The “LCD bias ratio” selects LCD bias ratio.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	1	0	*	B2	B1	B0

(Default: B2-B0=0H / Register Address: EH)

Table 25 LCD Bias Ratio

B2	B1	B0	LCD Bias Ratio
0	0	0	1/9
0	0	1	1/8
0	1	0	1/7
0	1	1	1/6
1	0	0	1/5
1	0	1	1/4
1	1	0	1/10
1	1	1	Inhibited

(14-14) Instruction Table Select

This instruction specifies an instruction table, and should be executed prior to other instructions.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0/1	0/1	0/1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	1	1	TST0	RE2	RE1	RE0

(Default: TST0, RE2-RE0=0H / Register Address: FH)

Table 26 Instruction Table Select

RE2	RE1	RE0	Instructions
0	0	0	Instruction Table (0)
0	0	1	Instruction Table (1)
0	1	0	Instruction Table (2)
0	1	1	Instruction Table (3)
1	0	0	Instruction Table (4)
1	0	1	Instruction Table (5)

NOTE) “TST0” bit must be “0”. This is used for maker tests only.

(14-15) Palette A / B / C

Palette A0 (PS=0) / Palette A8 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

(Register Address: 0H)

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	PA03/ PA83	PA02/ PA82	PA01/ PA81	PA00/ PA80

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	*	*	*	PA04/ PA84

(Register Address: 1H)

Palette A1 (PS=0) / Palette A9 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	PA13/ PA93	PA12/ PA92	PA11/ PA91	PA10/ PA90

(Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	*	*	PA14/ PA94

(Register Address: 3H)

Palette A2 (PS=0) / Palette A10 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	PA23/ PA103	PA22/ PA102	PA21/ PA101	PA20/ PA100

(Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	*	*	PA24/ PA104

(Register Address: 5H)

Palette A3 (PS=0) / Palette A11 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	PA33/ PA113	PA32/ PA112	PA31/ PA111	PA30/ PA110

(Register Address: 6H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	*	*	PA34/ PA114

(Register Address: 7H)

Palette A4 (PS=0) / Palette A12 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	PA43/ PA123	PA42/ PA122	PA41/ PA121	PA40/ PA120

(Register Address: 8H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	*	*	*	PA44/ PA124

(Register Address: 9H)

NOTE) Refer to the tables in “(6) GRAYSCALE PALETTE” for default setting.

Palette A5 (PS=0) / Palette A13 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	PA53/ PA133	PA52/ PA132	PA51/ PA131	PA50/ PA130

(Register Address: AH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	1	*	*	*	PA54/ PA134

(Register Address: BH)

Palette A6 (PS=0) / Palette A14 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	0	PA63/ PA143	PA62/ PA142	PA61/ PA141	PA60/ PA140

(Register Address: CH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	1	*	*	*	PA64/ PA144

(Register Address: DH)

Palette A7 (PS=0) / Palette A15 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	PA73/ PA153	PA72/ PA152	PA71/ PA151	PA70/ PA150

(Register Address: 0H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	*	*	*	PA74/ PA154

(Register Address: 1H)

NOTE) Refer to the tables in “(6) GRAYSCALE PALETTE” for default setting.

Palette B0 (PS=0) / Palette B8 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	PB03/ PB83	PB02/ PB82	PB01/ PB81	PB00/ PB80

(Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	*	*	PB04/ PB84

(Register Address: 3H)

Palette B1 (PS=0) / Palette B9 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	PB13/ PB93	PB12/ PB92	PB11/ PB91	PB10/ PB90

(Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	*	*	PB14/ PB94

(Register Address: 5H)

Palette B2 (PS=0) / Palette B10 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	PB23/ PB103	PB22/ PB102	PB21/ PB101	PB20/ PB100

(Register Address: 6H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	*	*	PB24/ PB104

(Register Address: 7H)

Palette B3 (PS=0) / Palette B11 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	PB33/ PB113	PB32/ PB112	PB31/ PB111	PB30/ PB110

(Register Address: 8H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	*	*	*	PB34/ PB114

(Register Address: 9H)

Palette B4 (PS=0) / Palette B12 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	PB43/ PB123	PB42/ PB122	PB41/ PB121	PB40/ PB120

(Register Address: AH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	1	*	*	*	PB44/ PB124

(Register Address: BH)

NOTE) Refer to the tables in “(6) GRAYSCALE PALETTE” for default setting.

Palette B5 (PS=0) / Palette B13 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	0	PB53/ PB133	PB52/ PB132	PB51/ PB131	PB50/ PB130

(Register Address: CH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	1	*	*	*	PB54/ PB134

(Register Address: DH)

Palette B6 (PS=0) / Palette B14 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	PB63/ PB143	PB62/ PB142	PB61/ PB141	PB60/ PB140

(Register Address: 0H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	*	*	*	PB64/ PB144

(Register Address: 1H)

Palette B7 (PS=0) / Palette B15 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	PB73/ PB153	PB72/ PB152	PB71/ PB151	PB70/ PB150

(Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	*	*	PB74/ PB154

(Register Address: 3H)

NOTE) Refer to the tables in “(6) GRAYSCALE PALETTE” for default setting.

Palette C0 (PS=0) / Palette C8 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	PC03/ PC83	PC02/ PC82	PC01/ PC81	PC00/ PC80

(Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	*	*	PC04/ PC84

(Register Address: 5H)

Palette C1 (PS=0) / Palette C9 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	PC13/ PC93	PC12/ PC92	PC11/ PC91	PC10/ PC90

(Register Address: 6H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	*	*	PC14/ PC94

(Register Address: 7H)

Palette C2 (PS=0) / Palette C10 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	PC23/ PC103	PC22/ PC102	PC21/ PC101	PC20/ PC100

(Register Address: 8H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	*	*	*	PC24/ PC104

(Register Address: 9H)

Palette C3 (PS=0) / Palette C11 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	PC33/ PC113	PC32/ PC112	PC31/ PC111	PC30/ PC110

(Register Address: AH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	1	*	*	*	PC34/ PC114

(Register Address: BH)

Palette C4 (PS=0) / Palette C12 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	0	PC43/ PC123	PC42/ PC122	PC41/ PC121	PC40/ PC120

(Register Address: CH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	1	*	*	*	PC44/ PC124

(Register Address: DH)

NOTE) Refer to the tables in “(6) GRAYSCALE PALETTE” for default setting.

Palette C5 (PS=0) / Palette C13 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	PC53/ PC133	PC52/ PC132	PC51/ PC131	PC50/ PC130

(Register Address: 0H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	*	*	*	PC54/ PC134

(Register Address: 1H)

Palette C6 (PS=0) / Palette C14 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	PC63/ PC143	PC62/ PC142	PC61/ PB141	PC60/ PB140

(Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	*	*	PC64/ PC144

(Register Address: 3H)

Palette C7 (PS=0) / Palette C15 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	PC73/ PC153	PC72/ PC152	PC71/ PC151	PC70/ PC150

(Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	*	*	PC74/ PC154

(Register Address: 5H)

NOTE) Refer to the tables in “(6) GRAYSCALE PALETTE” for default setting.

(14-16) Initial COM

The “Initial COM” instruction specifies the common driver for a scan start common.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	SC3	SC2	SC1	SC0

(Default: SC3-SC0=0H / Register Address: 6H)

Table 27 Initial COM

SC3	SC2	SC1	SC0	Initial COM (SHIFT=0)	Initial COM (SHIFT=1)
0	0	0	0	COM ₀	COM ₇₉
0	0	0	1	COM ₄	COM ₇₅
0	0	1	0	COM ₈	COM ₇₁
0	0	1	1	COM ₁₆	COM ₆₃
0	1	0	0	COM ₂₄	COM ₅₅
0	1	0	1	COM ₃₂	COM ₄₇
0	1	1	0	COM ₄₀	COM ₃₉
0	1	1	1	COM ₄₈	COM ₃₁
1	0	0	0	COM ₅₆	COM ₂₃
1	0	0	1	COM ₆₄	COM ₁₅
1	0	1	0	COM ₇₂	COM ₇
1	0	1	1	Inhibited	
1	1	0	0	Inhibited	
1	1	0	1	Inhibited	
1	1	1	0	Inhibited	
1	1	1	1	Inhibited	

(14-17) Duty-1 /Display Clock ON/OFF

This instruction controls ON (Duty-1) /OFF (Duty-0) and Display Clock ON/OFF.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	*	DSE	SON

(Default: SON,DSE=0H / Register Address: 7H)

D₀ (SON)

SON=0 : CL, FLM, FR, and CLK are fixed at “L” level.

SON=1 : CL, FLM, FR, and CLK are enabled.

D₁ (DSE)

The duty cycle ratio is subtracted by 1 (Duty-1) from the original duty cycle ratio by setting “1” at the “DSE” bit.

DSE=0 : OFF (Duty-0)

DSE=1 : ON (Duty-1)

NOTE) For the last common timing at “DSE=0”, all common drivers generate non-selective waveforms, and segment drivers generate the same waveforms as for the previous common timing. For instance, in 1/81 duty cycle, the segment waveforms for 81st common timing are the same as for 80th common timing (last line).

(14-18) Display Mode Control

The “Display Mode Control” instruction sets up display modes such as the variable or fixed grayscale mode and the variable 8- or 16-grayscale mode. The D₂ (MON) bit of the “Display Control (1)” is used in combination. Refer to “(5) GRAY SCALE CONTROL CIRCUIT” and “(14-7) Display Control (1).”

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	PWM	C256	*	*

(Default: PWM,C256=0H / Register Address: 8H)

D₃ (PWM)

PWM=0 : Variable grayscale Mode (Variable 8-/16-grayscale Mode)
 PWM=1 : Fixed 8-grayscale Mode

D₂ (C256)

C256=0 : Variable 16-grayscale Mode at “PWM=0” (4096 colors)
 C256=1 : Variable 8-grayscale Mode at “PWM=0” (256 colors)

(14-19) Bus Length

This instruction selects 8- or 16-bit bus length, and sets oscillator configuration, ABS mode ON/OFF and high speed writing ON/OFF as well.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	HSW	ABS	CKS	WLS

(Default: HSW,ABS,CKS,WLS=0H / Register Address: 9H)

D₀ (WLS)

WLS=0: 8-bit Bus Length
 WLS=1: 16-bit Bus Length

D₁ (CKS)

CKS =0: Internal Oscillator using an internal resistor
 CKS =1: External Clock, or Internal Oscillator using an external resistor

NOTE) Refer to “(10) OSCILLATOR”.

D₂ (ABS)

ABS=0: ABS Mode OFF (Normal)
 ABS=1: ABS Mode ON

D₃ (HSW)

HSW=0: High Speed Writing OFF (Normal)
 HSW=1: High Speed Writing ON

(14-20) EVR Control

The “EVR Control” instruction adjusts V_{LCD} to optimize display contrast. This instruction is finally effective when both upper and lower bytes are transmitted in order to prevent high V_{LCD} . The setting order is upper byte first, then lower byte. Refer to “(11-2-3) Electrical Variable Resistor (EVR)”.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	DV ₃	DV ₂	DV ₁	DV ₀

(Default: DV₃-DV₀=0H / Register Address: AH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	1	*	DV ₆	DV ₅	DV ₄

(Default: DV₆-DV₄=0H / Register Address: BH)

Table 28 EVR Control

DV ₆	DV ₅	DV ₄	DV ₃	DV ₂	DV ₁	DV ₀	V_{LCD}
0	0	0	0	0	0	0	Low
0	0	0	0	0	0	1	:
			:				:
			:				:
1	1	1	1	1	1	1	High

Formula of VLCD

$$VLCD [V] = 0.5 \times VREG + M (VREG - 0.5 \times VREG) / 127$$

$$VBA = VEE \times 0.9$$

$$VREG = VREF \times N$$

VBA : Output of the reference voltage generator

VREF : Input of the voltage regulator

VREG : Output of the voltage regulator

N : Boost level

M : EVR Value

(14-21) Frequency Control

The “Frequency Control” instruction adjusts the frame frequency.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	1	*	Rf2	Rf1	Rf0

(Default: DV₃-DV₀=0H / Register Address: DH)

Table 29 Frequency Control

Rf 2	Rf 1	Rf 0	Feedback Resistor Value
0	0	0	Reference Value
0	0	1	0.8 x Reference Value
0	1	0	0.9 x Reference Value
0	1	1	1.1 x Reference Value
1	0	0	1.2 x Reference Value
1	0	1	0.7 x Reference Value
1	1	0	1.3 x Reference Value
1	1	1	Inhibited

(14-22) Discharge ON/OFF

Discharge circuit is used to discharge out of the stabilizing capacitors placed on the V_{LCD}, V₁, V₂, V₃, V₄ and V_{OUT}. Refer to “(11-4) Discharge Circuit”.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	1	0	*	*	DIS2	DIS

(Default: DIS2, DIS1=0H / Register Address: EH)

D₀ (DIS)

DIS=0 : Discharge OFF

DIS=1 : Discharge ON (Discharge from V_{LCD}, V₁, V₂, V₃ and V₄)

D₁ (DIS2)

DIS2=0 : Discharge OFF

DIS2=1 : Discharge ON (Discharge from V_{OUT} through the internal resistor between V_{OUT} and V_{EE})

NOTE) Resistance is 100KΩ typical.

(14-23) Register Address

The “Register Address” instruction specifies a register address.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	0	RA3	RA2	RA1	RA0

(Default: RA3-RA0=BH / Register Address: CH)

(14-24) Register Read /ID Code Read

The “Register Read /ID Code Read” instruction reads out instruction data from the register which address is specified by the “Register Address” instruction. And it reads out the ID code set by the ID₃-ID₀ terminals. Note that this instruction is used in the parallel interface mode only.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	0	1	0/1	0/1	0/1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
ID3	ID2	ID1	ID0	Internal register data			

(14-25) Window End Column Address

The “Window End Column Address” instruction specifies the column address of the end point. Refer to “(4-2) Window Area for DDRAM Access”. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	EX3	EX2	EX1	EX0

(Default: EX3-EX0=0H / Register Address: 0H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	EX7	EX6	EX5	EX4

(Default: EX7-EX4=0H / Register Address: 1H)

(14-26) Window End Row Address

The “Window End Row Address” instruction specifies the row address of the end point. Refer to “(4-2) Window Area for DDRAM Access”. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	EY3	EY2	EY1	EY0

(Default: EY3-EY0=0H / Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	EY6	EY5	EY4

(Default: EY6-EY4=0H / Register Address: 3H)

(14-27) Initial Line-reverse Address

The “Initial Line-reverse Address” instruction specifies the start line of the line-reverse display area. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	LS3	LS2	LS1	LS0

(Default: LS3-LS0=0H / Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	LS6	LS5	LS4

(Default: LS6-LS4=0H / Register Address: 5H)

(14-28) Last Line-reverse Address

The “Last Line-reverse Address” instruction specifies the end line of the line-reverse display area. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	LE3	LE2	LE1	LE0

(Default: LE3-LE0=0H / Register Address: 6H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	LE6	LE5	LE4

(Default: LE6-LE4=0H / Register Address: 7H)

(14-29) Line Reverse ON/OFF

The “Line Reverse ON/OFF” instruction enables the line-reverse display, and blink function as well. Note that the line reverse display cannot be used for entire display area. In this case, use the reverse display function by the D₃ (REV) bit of the “Display Control (2)” instruction.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	*	*	BT	LREV

(Default: BT,LREV=0H / Register Address: 8H)

D₀ (LREV)

LREV =0 : Line Reverse OFF (Normal)
LREV =1 : Line Reverse ON

D₁ (BT)

BT =0 : No Blink
BT =1 : Blink once every 32 frames

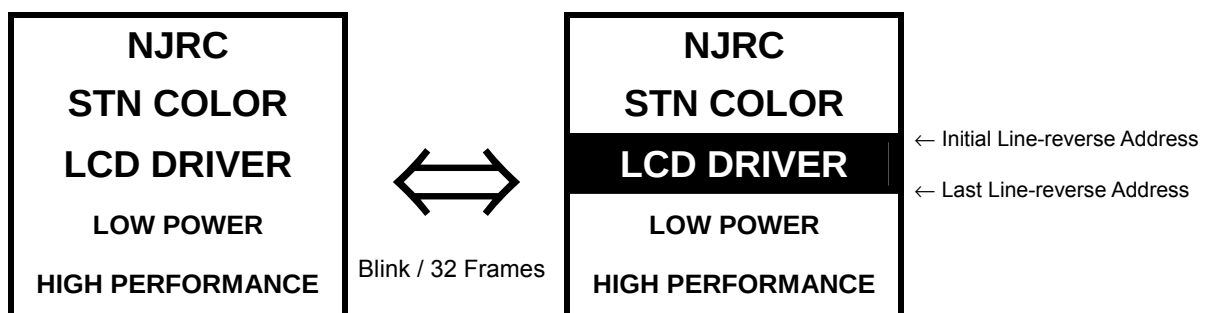
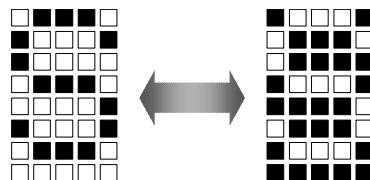


Fig 19 On-screen Image in Using Line-reverse Display and Blink Function

(14-30) Upper/Lower Palette Select

The “Upper/Lower Palette Select” instruction selects either upper or lower palette register.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	*	*	*	PS

(Default: PS=0 / Register Address: 9H)

D₀ (PS)

PS=0 : Lower Palettes (PA00, PA01, PA02, PA03, ..., PC74)
 PS=1 : Upper Palettes (PA80, PA81, PA82, PA83, ..., PC154)

(14-31) PWM Control

The “PWM control” instruction selects PWM type, as shown in Fig 20.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	PWMS	PWMA	PWMB	PWMC

(Default: PWMS,PWMA,PWMB,PWMC=0H / Register Address: AH)

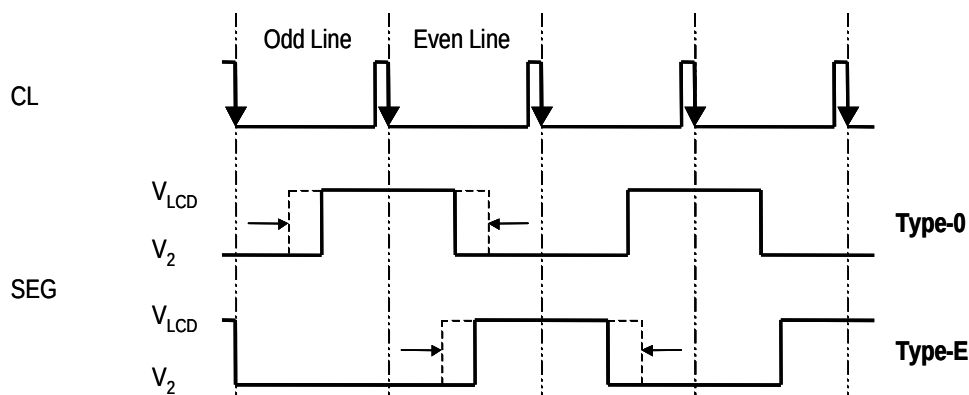
D₃ (PWMS)

PWMS=0 : Type 1
 PWMS=1 : Type 2

D₂ (PWMA), D₁ (PWMB), D₀ (PWMC)

PWMZ=0 (Z=A, B and C): Type 1-O
 PWMZ=1 (Z=A, B and C): Type 1-E

PWM Type 1 (PWMS=0)



PWM Type 2 (PWMS=1)

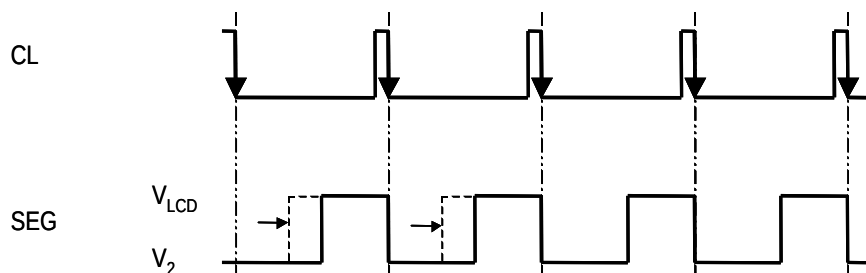


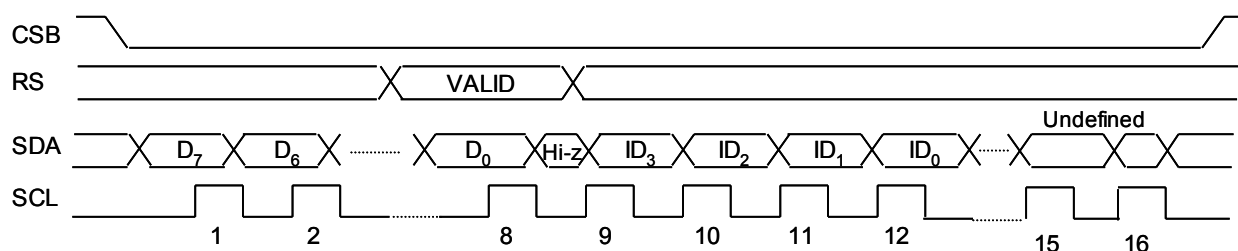
Fig 20 PWM Control

(15) CHIP IDENTIFICATION (ID) CODE

The ID code is decided by setting the ID₃, ID₂, ID₁ and ID₀ terminals. In the parallel interface mode, the ID code is read out through the data bus (D₇, D₆, D₅ and D₄) by the “Register Read /ID Code Read” instruction. In the 3 or 4-line serial interface mode, the ID code is read out by the “Boost Level /ID Code Read” instruction, as follows.

When using the 4-line serial interface mode, set “1” at the “IDR” bit of the “Boost Level /ID Code Read” instruction. Then, the SDA becomes in high-impedance (Hi-Z) at the falling edge of the 8th SCL signal, and the ID code (ID₃, ID₂, ID₁ and ID₀) is read out bit by bit at the rising edges of the 9th,...12th SCL. After that, the ID code operation continues up to the 16th SCL, then returns to the normal operation. When using the 3-line serial interface mode, the SDA becomes in high-impedance at the 9th SCL, and the ID code is read out at the 10th,...13th SCL. Then, the ID code operation continues up to the 18th SCL.

4-Line Serial Interface



3-Line Serial Interface

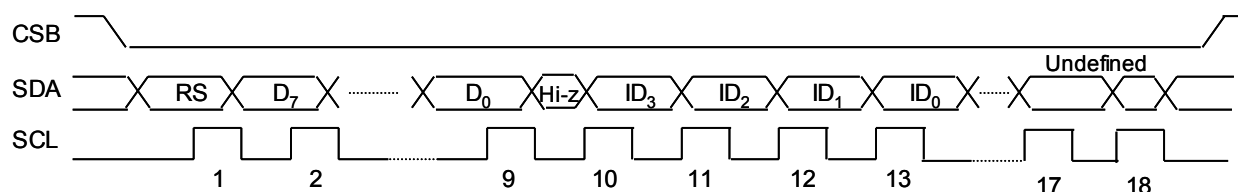


Fig 21 ID Code Reading Operation

NOTE1) The AC timing of the ID code operation is different from the timing of the normal operation. Refer to “ (6) Read Operation (Serial Interface)”.

NOTE2) After setting “1” at the “IDR” bit, the CS should remain “L” until the ID code operation is completed. Once the CS becomes “H”, the ID code operation is released.

(16) PARTIAL DISPLAY FUNCTION

The partial display function activates specified area on an LCD screen, or equivalently, common drivers are simply scanning this specified area. This function allows LCD modules to work in a minimum duty cycle ratio to minimize power consumption. The partial display function is carried out by the combination of the “Duty Cycle Ratio”, “LCD Bias Ratio”, “Boost Level” and “EVR Control” instructions. For more information, refer to “(14-11) Duty Cycle Ratio”, “(14-12) Boost Level /ID Code Read”, “(14-13) LCD Bias Ratio” and “(14-20) EVR Control”. Typical setting sequence is shown in “(19-4) Partial Display Sequence”.

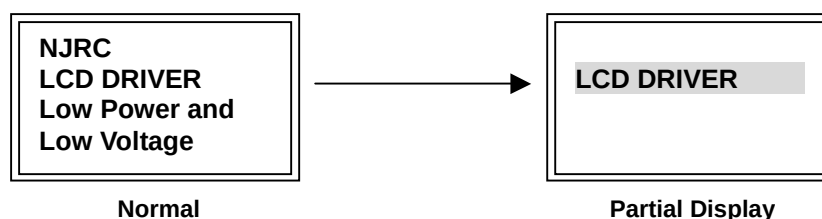


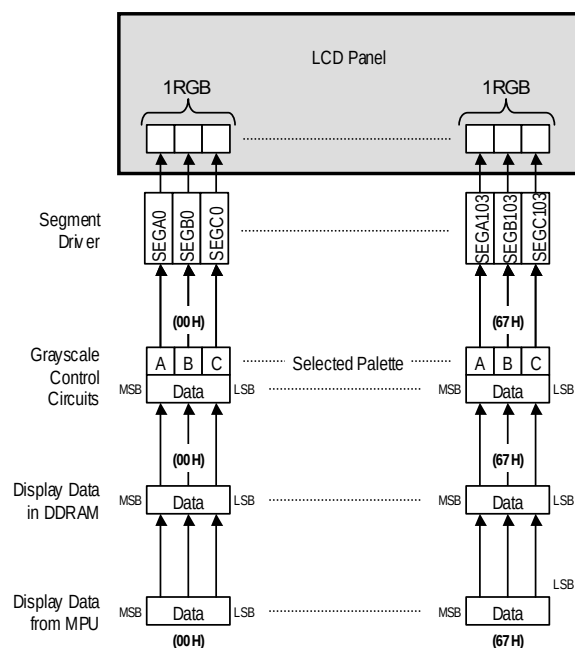
Fig 22 On-screen Image in Using Partial Display Function

(17) SWAP FUNCTION

The swap function switches the palettes Aj and the palettes Cj (j=0-15), and is controlled by the D₁ (SWAP) bit of the “Display Control (2)” instruction. This function reduces the restrictions on the IC position of an LCD module. Fig 23 “Overview of Swap Function” illustrates general outlines of internal operations, and (17-1-1) through (17-1-4) show each configuration on a mode-by-mode basis.

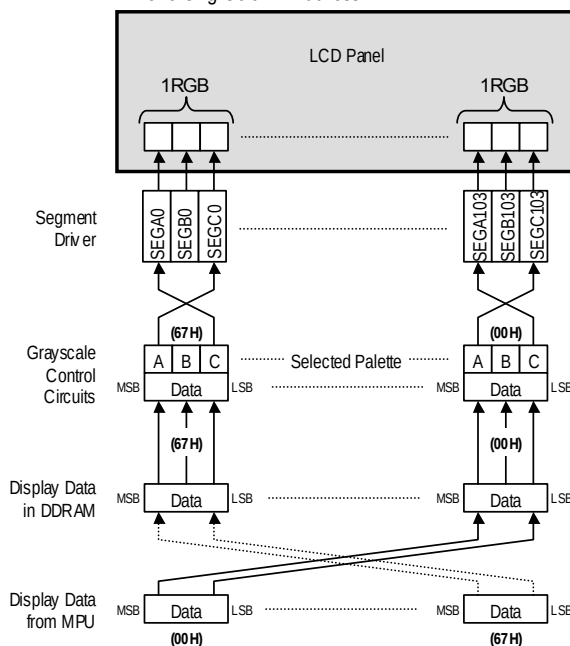
(SWAP, REF)=(0,0)

- Default state



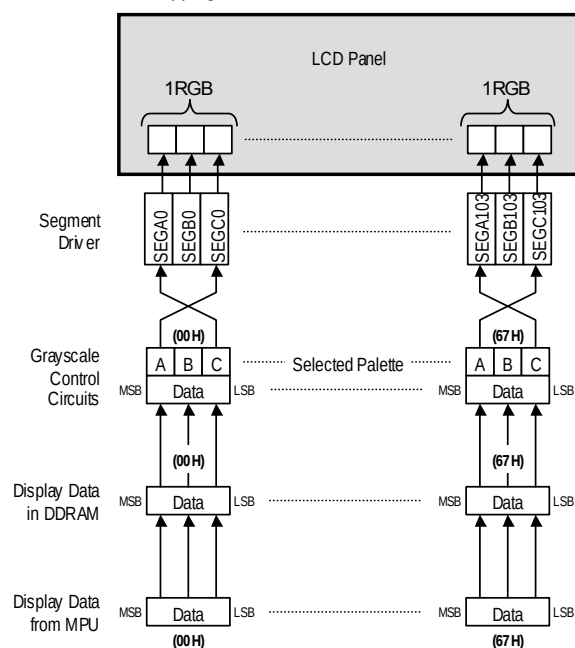
(SWAP, REF)=(0,1)

- Swapping Palette A and Palette C
- Reversing Column Address



(SWAP, REF)=(1,0)

- Swapping Palette A and Palette C



(SWAP, REF)=(1,1)

- Reversing Column Address

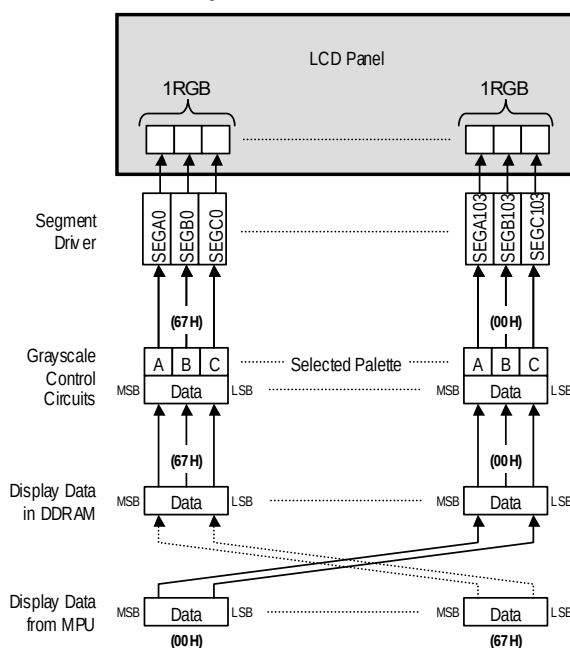
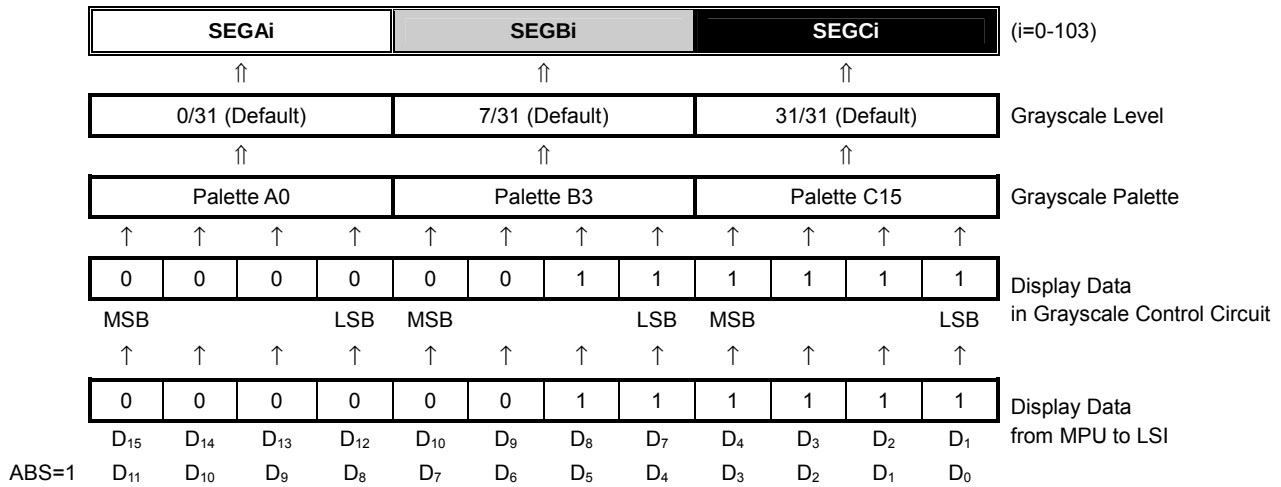


Fig 23 Overview of SWAP Function

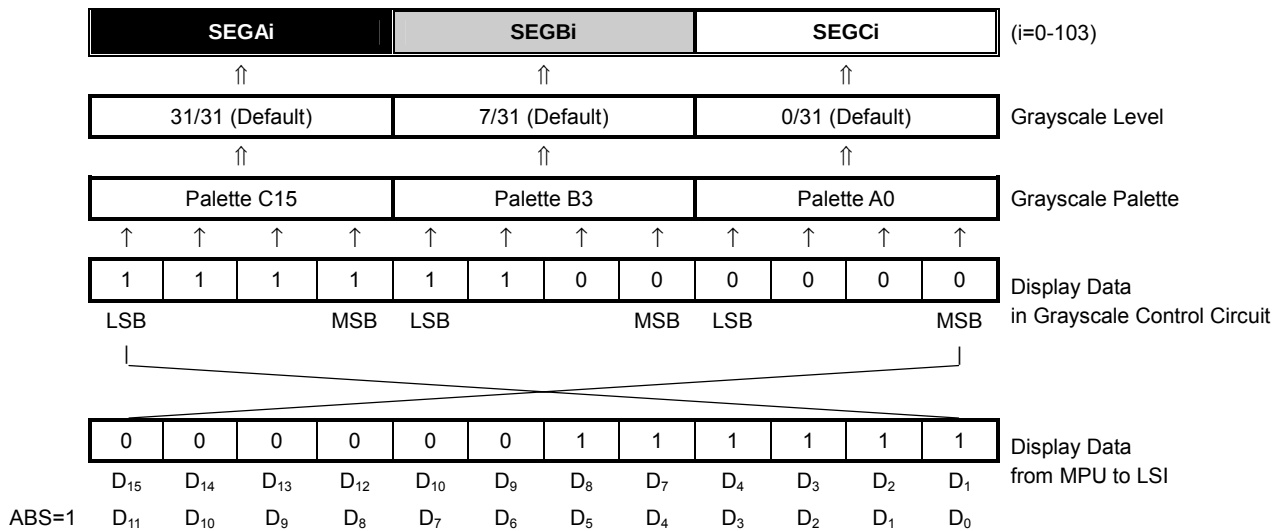
(17-1) Swap Function in Variable 16-grayscale Mode

16-bit Bus Length

(REF, SWAP)=(0,0) or (1,1)



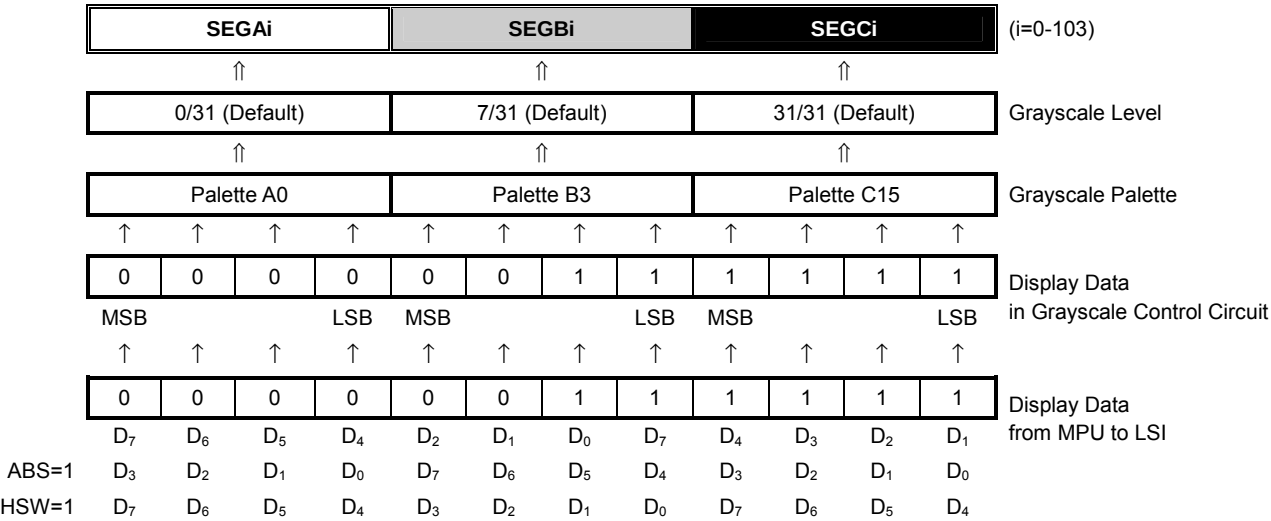
(REF, SWAP)=(0,1) or (1,0)



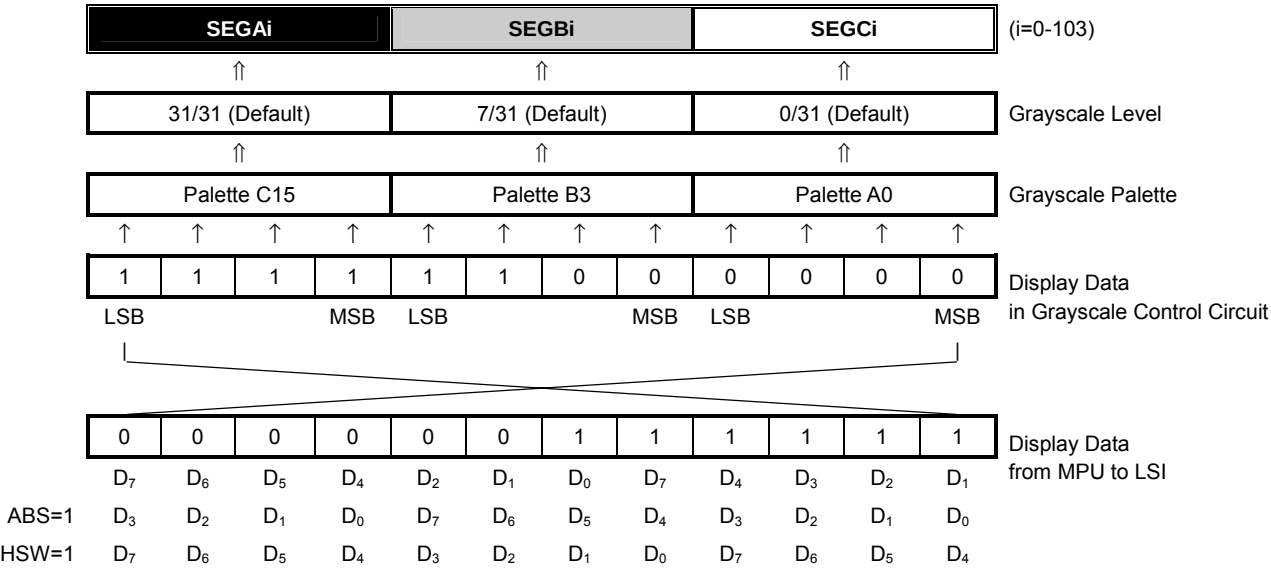
NOTE1) Without a special note on the left, the ABS, HSW and C256 bits are regarded as "0".

8-bit Bus Length

(REF, SWAP)=(0,0) or (1,1)



(REF, SWAP)=(0,1) or (1,0)

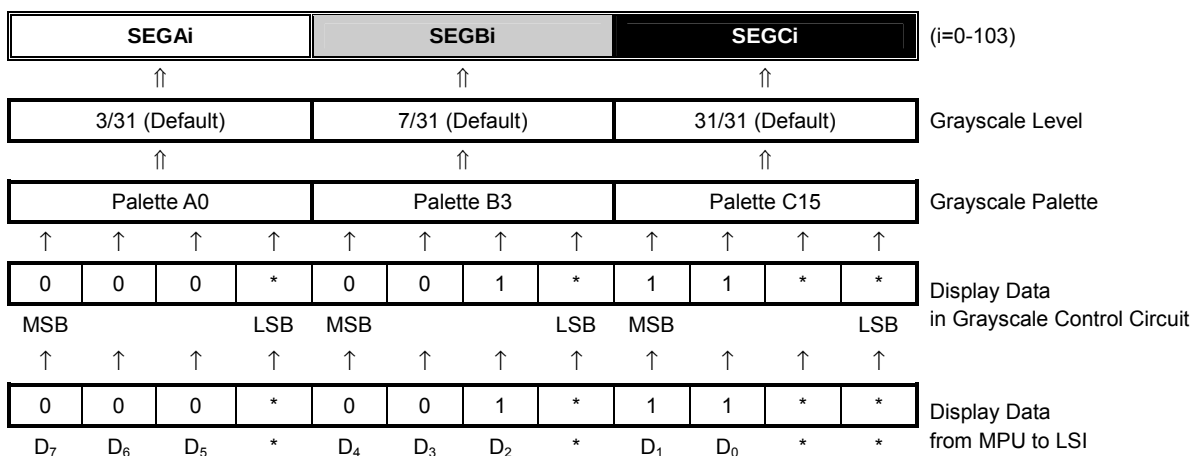


NOTE1) Without a special note on the left, the ABS, HSW and C256 bits are regarded as “0”.

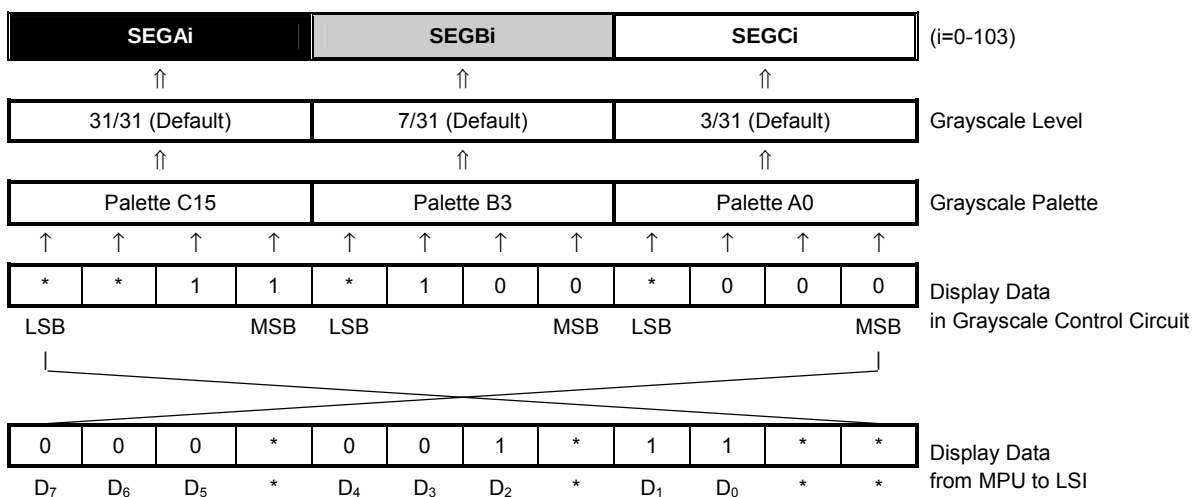
(17-2) Swap Function in Variable 8-grayscale Mode

8-bit Bus Length

(REF, SWAP)=(0,0) or (1,1)



(REF, SWAP)=(0,1) or (1,0)

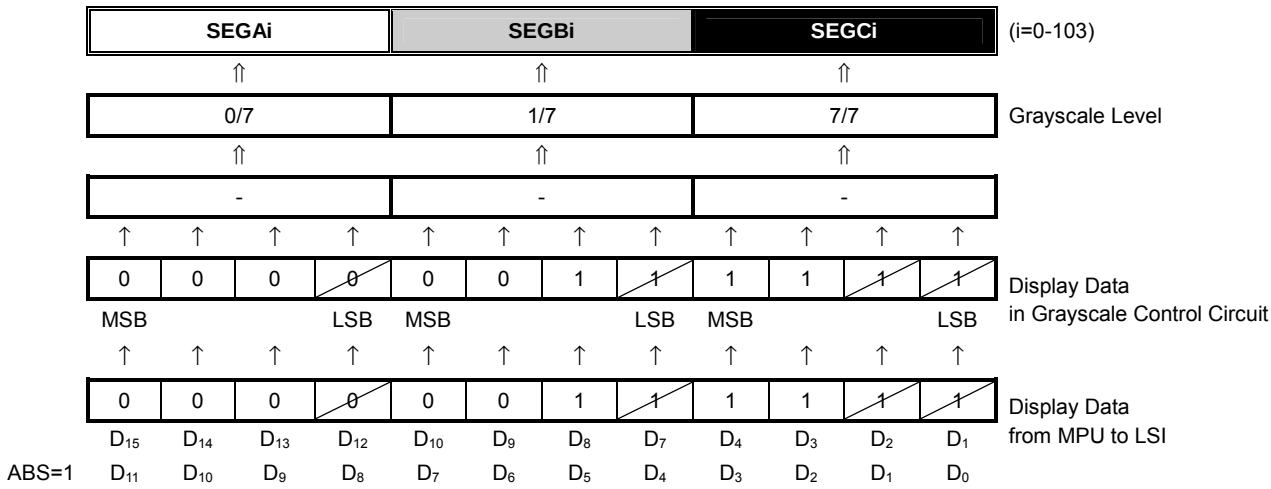


NOTE1) Without a special note on the left, the ABS, HSW and C256 bits are regarded as "0".

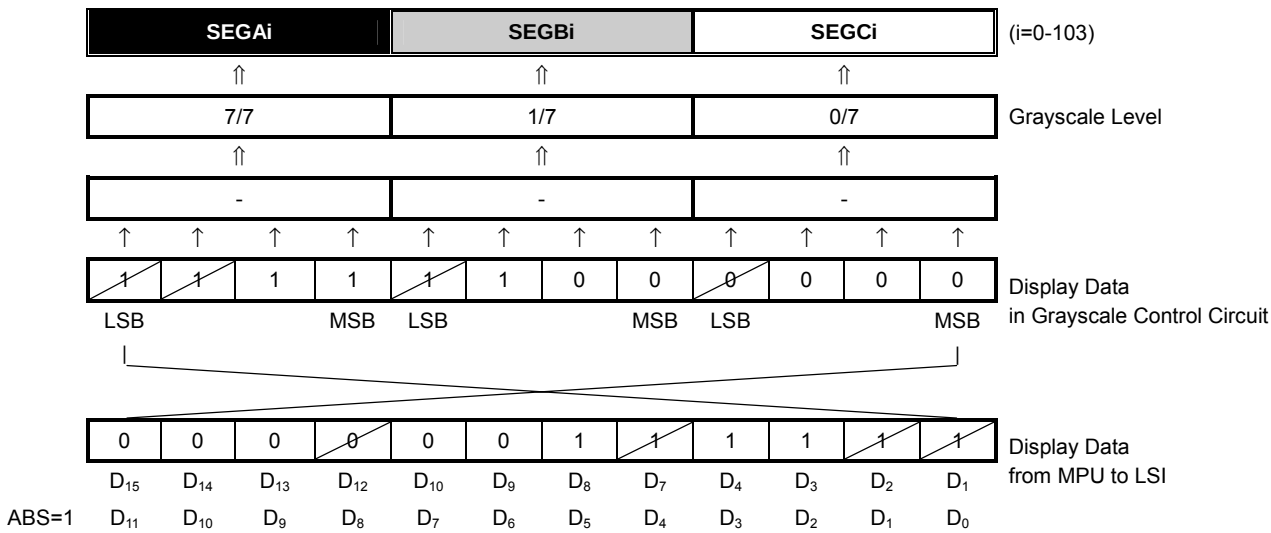
(17-3) Swap Function in Fixed 8-grayscale Mode

16-bit Bus Length

(REF, SWAP)=(0,0) or (1,1)



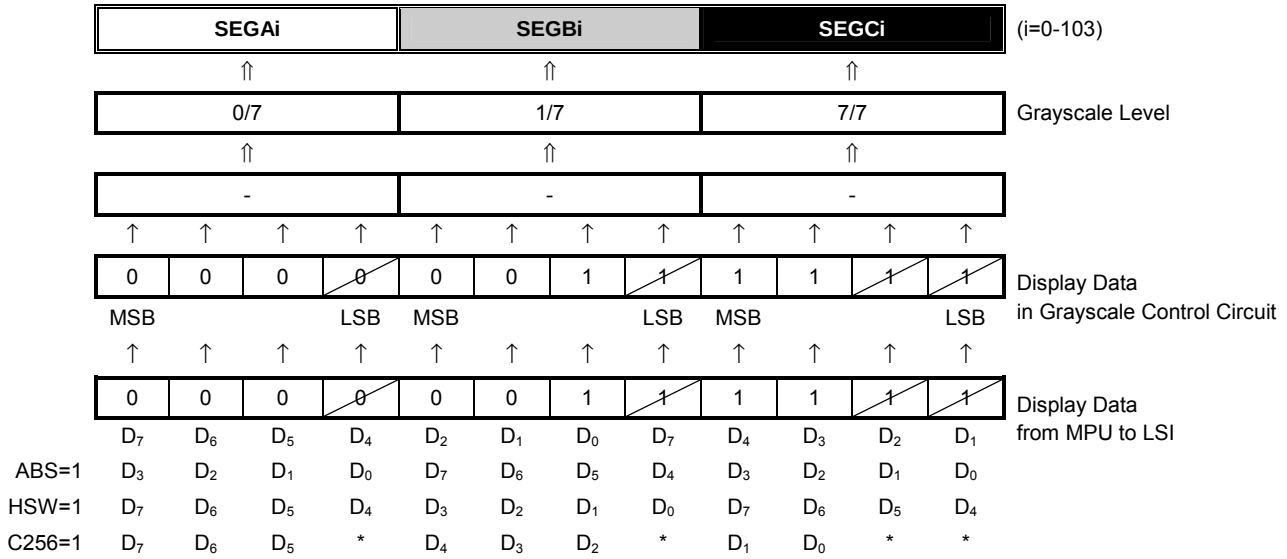
(REF, SWAP)=(0,1) or (1,0)



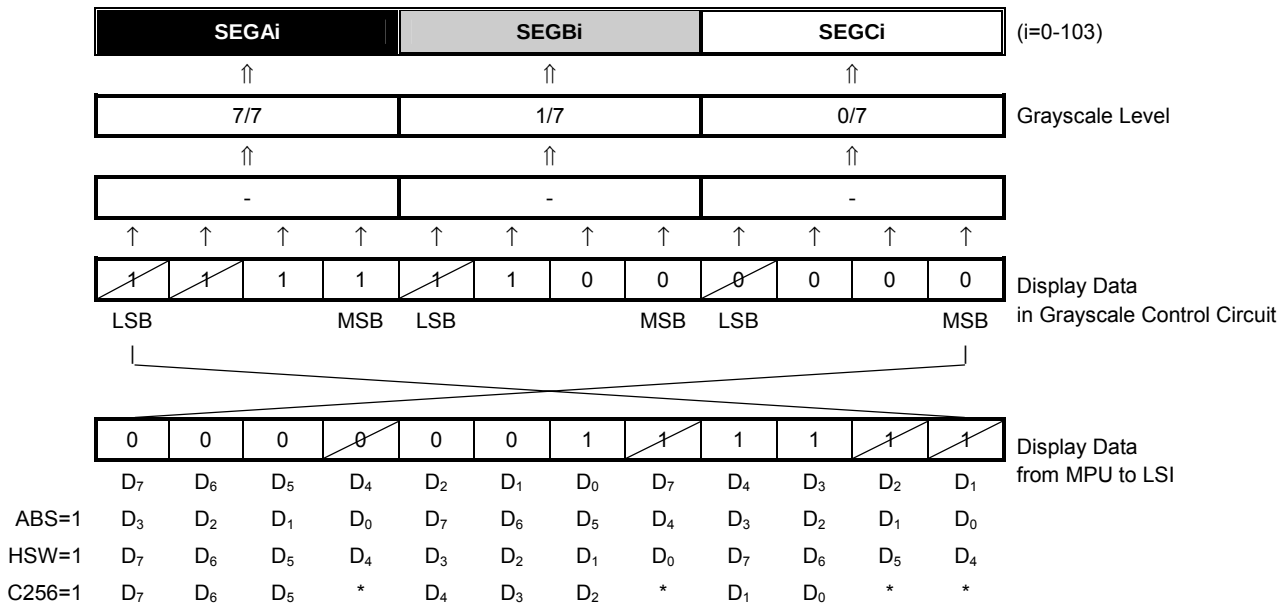
NOTE1) Without a special note on the left, the ABS, HSW and C256 bits are regarded as "0".
NOTE2) The data indicated with a slash mark (/) is invalid.

8-bit Bus Length

(REF, SWAP)=(0,0) or (1,1)



(REF, SWAP)=(0,1) or (1,0)



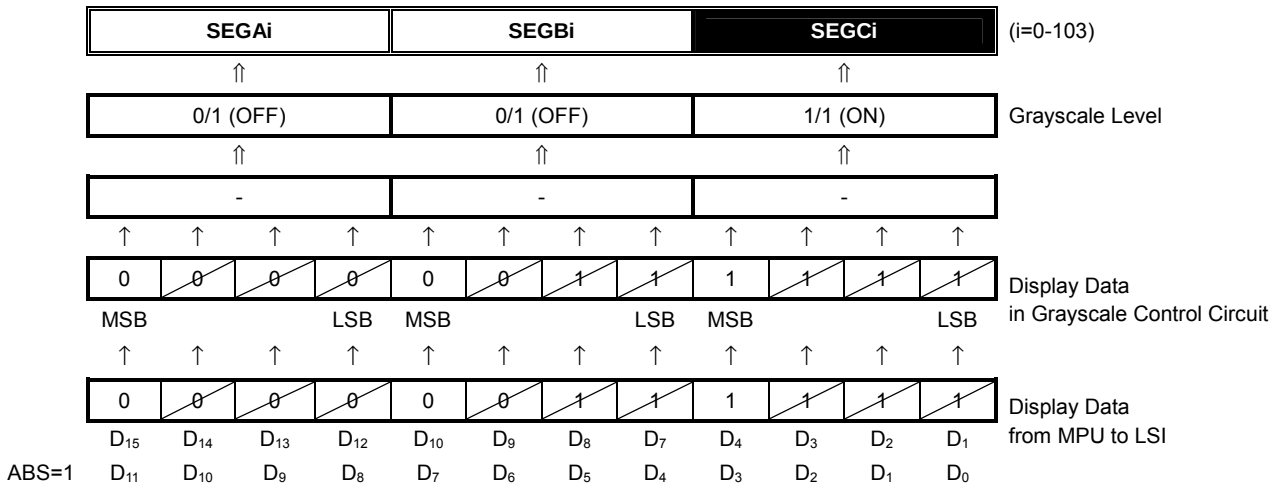
NOTE1) Without a special note on the left, the ABS, HSW and C256 bits are regarded as "0".

NOTE2) The data indicated with a slash mark (/) is invalid.

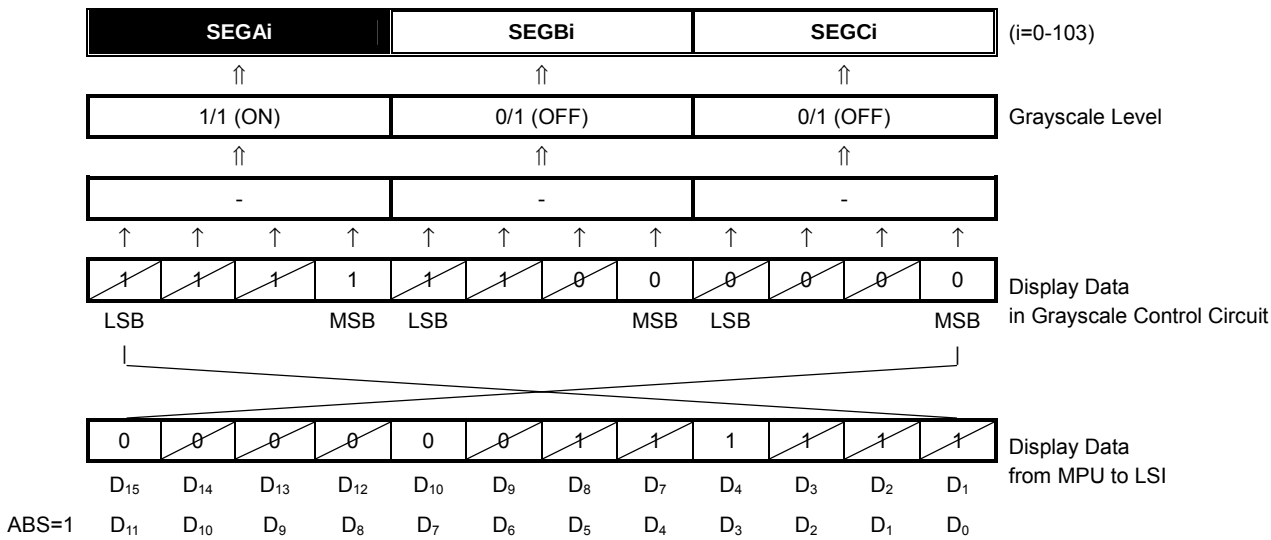
(17-4) Swap Function in B&W Mode

16-bit Bus Length

(REF, SWAP)=(0,0) or (1,1)



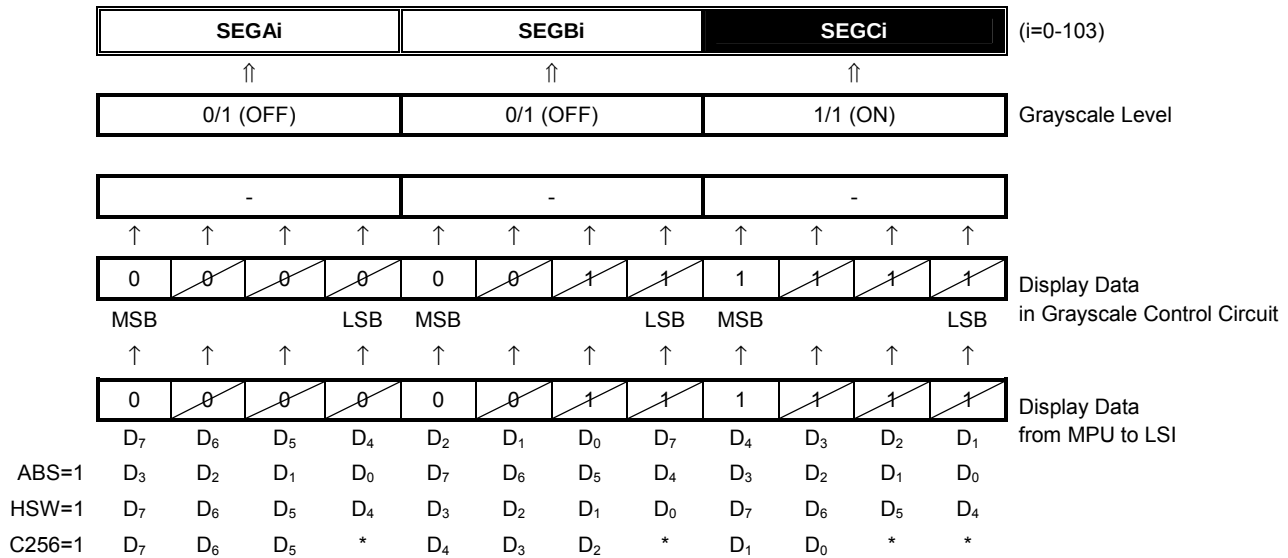
(REF, SWAP)=(0,1) or (1,0)



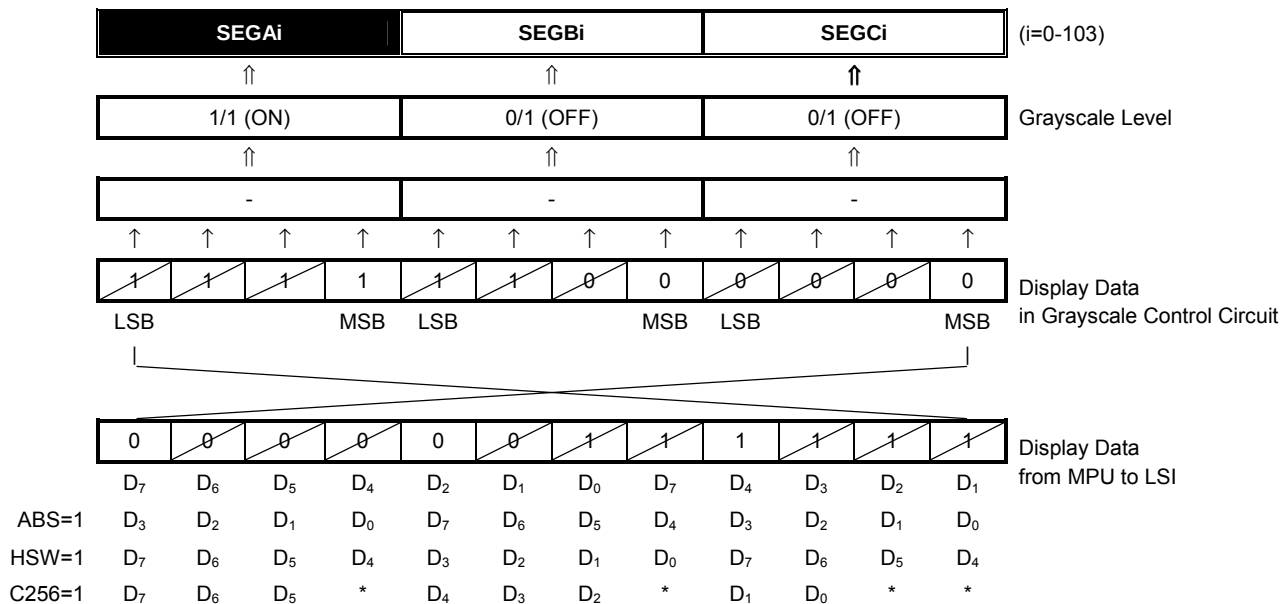
NOTE1) Without a special note on the left, the ABS, HSW and C256 bits are regarded as "0".
NOTE2) The data indicated with a slash mark (/) is invalid.

8-bit Bus Length

SWAP=0



SWAP=1



NOTE1) Without a special note on the left, the ABS, HSW and C256 bits are regarded as "0".

NOTE2) The data indicated with a slash mark (/) is invalid.

(18) RELATION BETWEEN ROW ADDRESS AND COMMON DRIVER

The relation between row address and common driver is changed by the D₃ (SHIFT) bit of the "Display Control (1)" and the "Duty Cycle Ratio", "Initial Display Line" and "Initial COM" instructions.

When the "Initial Display Line" is set to (LA6:LA0=00H: Address "0"), the row address corresponding to an initial COM is "0". However, if the "Initial Display Line" is other than "0", the row address is shifted from "0" by just that address. For instance, when the initial display line address is (LA6:LA0=05H: Address "5") and the initial COM is (SC3:SC0=1H), the row address on the initial COM is "5" and the initial COM is "COM₄".

(18-1) through (18-5) illustrate the examples of the relation between row address and common driver.

(18-1) SHIFT=0, Initial Display Line "0", Duty Cycle Ratio "1/81"

SHIFT=0, DS3-0=(0,0,0,0), LA6-LA0=(0,0,0,0,0,0), DSE=0											
SC3 - SC0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010
COM0	0	76	72	64	56	48	40	32	24	16	8
COM1	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM3	↓	79	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM4	↓	0	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM5	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM6	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM7	↓	↓	79	↓	↓	↓	↓	↓	↓	↓	↓
COM8	↓	↓	0	↓	↓	↓	↓	↓	↓	↓	↓
COM9	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM10	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM11	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM12	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM13	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM14	↓	↓	↓	79	↓	↓	↓	↓	↓	↓	↓
COM15	↓	↓	↓	0	↓	↓	↓	↓	↓	↓	↓
COM16	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM17	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM18	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM19	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM20	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM21	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM22	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM23	↓	↓	↓	↓	79	↓	↓	↓	↓	↓	↓
COM24	↓	↓	↓	↓	0	↓	↓	↓	↓	↓	↓
COM25	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM26	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM27	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM28	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM29	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM30	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM31	↓	↓	↓	↓	↓	79	↓	↓	↓	↓	↓
COM32	↓	↓	↓	↓	↓	0	↓	↓	↓	↓	↓
COM33	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM34	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM35	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM36	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM37	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM38	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM39	↓	↓	↓	↓	↓	↓	79	↓	↓	↓	↓
COM40	↓	↓	↓	↓	↓	↓	0	↓	↓	↓	↓
COM41	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM42	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM43	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM44	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM45	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM46	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM47	↓	↓	↓	↓	↓	↓	↓	79	↓	↓	↓
COM48	↓	↓	↓	↓	↓	↓	↓	0	↓	↓	↓
COM49	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM50	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM51	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM52	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM53	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM54	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM55	↓	↓	↓	↓	↓	↓	↓	↓	79	↓	↓
COM56	↓	↓	↓	↓	↓	↓	↓	↓	0	↓	↓
COM57	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM58	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM59	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM60	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM61	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM62	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM63	↓	↓	↓	↓	↓	↓	↓	↓	↓	79	↓
COM64	↓	↓	↓	↓	↓	↓	↓	↓	↓	0	↓
COM65	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM66	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM67	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM68	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM69	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM70	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM71	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	79
COM72	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0
COM73	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM74	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM75	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM76	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM77	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM78	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM79	79	75	71	63	55	47	39	31	23	15	7
81 st COM Timing	79	79	79	79	79	79	79	79	79	79	79

Fig 24 Relation between Row address and Common Driver (1)

NOTE1) DS: Duty Cycle Ratio / SC: Initial COM / LA: Initial Display Line Address

NOTE2) Segment waveforms for 81st COM timing are the same as for 80th COM timing (Row address "79").

(18-2) SHIFT=0, Initial Display Line "0", Duty Cycle Ratio "1/13"

SHIFT=0, DS3-0=(1,0,0,1), LA6-LA0=(0,0,0,0,0,0), DSE=0											
SC3 - SC0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010
COM0	0										8
COM1	↓										↓
COM2	↓										↓
COM3	↓										11
COM4	↓	0									
COM5	↓	↓									
COM6	↓	↓									
COM7	↓	↓									
COM8	↓	↓	0								
COM9	↓	↓	↓								
COM10	↓	↓	↓								
COM11	11	↓	↓								
COM12		↓	↓								
COM13		↓	↓								
COM14		↓	↓								
COM15		11	↓								
COM16			↓	0							
COM17			↓	↓							
COM18			↓	↓							
COM19			11	↓							
COM20				↓							
COM21				↓							
COM22				↓							
COM23				↓							
COM24				↓	0						
COM25				↓	↓						
COM26				↓	↓						
COM27				11	↓						
COM28					↓						
COM29					↓						
COM30					↓						
COM31					↓						
COM32					↓	0					
COM33					↓	↓					
COM34					↓	↓					
COM35					11	↓					
COM36						↓					
COM37						↓					
COM38						↓					
COM39						↓					
COM40						↓	0				
COM41						↓	↓				
COM42						↓	↓				
COM43						11	↓				
COM44							↓				
COM45							↓				
COM46							↓				
COM47							↓				
COM48							↓	0			
COM49							↓	↓			
COM50							↓	↓			
COM51							11	↓			
COM52								↓			
COM53								↓			
COM54								↓			
COM55								↓			
COM56								↓	0		
COM57								↓	↓		
COM58								↓	↓		
COM59								11	↓		
COM60									↓		
COM61									↓		
COM62									↓		
COM63									↓		
COM64									↓	0	
COM65									↓	↓	
COM66									↓	↓	
COM67									11	↓	
COM68										↓	
COM69										↓	
COM70										↓	
COM71										↓	
COM72										↓	0
COM73										↓	↓
COM74										↓	↓
COM75										11	↓
COM76											↓
COM77											↓
COM78											↓
COM79											7
13 th COM Timing	11	11	11	11	11	11	11	11	11	11	11

Fig 25 Relation between Row address and Common Driver (2)

NOTE1) DS: Duty Cycle Ratio / SC: Initial COM / LA: Initial Display Line Address

NOTE2) Segment waveforms for 13th COM timing are the same as for 12th COM timing (Row address "11").

(18-3) SHIFT=1, Initial Display Line "0", Duty Cycle Ratio "1/81"

SHIFT=1, DS3-0=(0,0,0,0), LA6-LA0=(0,0,0,0,0,0), DSE=0											
SC3 - SC0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010
COM0	79	75	71	63	55	47	39	31	23	15	7
COM1	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM2	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM3	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM4	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM5	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM6	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM7	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	0
COM8	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	79
COM9	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM10	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM11	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM12	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM13	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM14	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM15	↑	↑	↑	↑	↑	↑	↑	↑	↑	0	↑
COM16	↑	↑	↑	↑	↑	↑	↑	↑	↑	79	↑
COM17	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM18	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM19	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM20	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM21	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM22	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM23	↑	↑	↑	↑	↑	↑	↑	↑	0	↑	↑
COM24	↑	↑	↑	↑	↑	↑	↑	↑	79	↑	↑
COM25	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM26	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM27	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM28	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM29	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM30	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM31	↑	↑	↑	↑	↑	↑	↑	0	↑	↑	↑
COM32	↑	↑	↑	↑	↑	↑	↑	79	↑	↑	↑
COM33	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM34	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM35	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM36	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM37	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM38	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM39	↑	↑	↑	↑	↑	↑	0	↑	↑	↑	↑
COM40	↑	↑	↑	↑	↑	↑	79	↑	↑	↑	↑
COM41	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM42	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM43	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM44	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM45	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM46	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM47	↑	↑	↑	↑	↑	0	↑	↑	↑	↑	↑
COM48	↑	↑	↑	↑	↑	79	↑	↑	↑	↑	↑
COM49	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM50	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM51	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM52	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM53	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM54	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM55	↑	↑	↑	↑	0	↑	↑	↑	↑	↑	↑
COM56	↑	↑	↑	↑	79	↑	↑	↑	↑	↑	↑
COM57	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM58	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM59	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM60	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM61	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM62	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM63	↑	↑	↑	0	↑	↑	↑	↑	↑	↑	↑
COM64	↑	↑	↑	79	↑	↑	↑	↑	↑	↑	↑
COM65	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM66	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM67	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM68	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM69	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM70	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM71	↑	↑	0	↑	↑	↑	↑	↑	↑	↑	↑
COM72	↑	↑	79	↑	↑	↑	↑	↑	↑	↑	↑
COM73	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM74	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM75	↑	0	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM76	↑	79	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM77	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM78	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
COM79	0	76	72	64	56	48	40	32	24	16	8
81 st COM Timing	79	79	79	79	79	79	79	79	79	79	79

Fig 26 Relation between Row address and Common Driver (3)

NOTE1) DS: Duty Cycle Ratio / SC: Initial COM / LA: Initial Display Line Address

NOTE2) Segment waveforms for 81st COM timing are the same as for 80th COM timing (Row address "79").

(18-4) SHIFT=0, Initial Display Line "5", Duty Cycle Ratio "1/81"

SHIFT=0, DS3-0=(0,0,0,0), LA6-LA0=(0,0,0,0,1,0,1), DSE=0											
SC3 - SC0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010
COM0	5	1	77	69	61	53	45	37	29	21	13
COM1	↓	↓	78	↓	↓	↓	↓	↓	↓	↓	↓
COM2	↓	↓	79	↓	↓	↓	↓	↓	↓	↓	↓
COM3	↓	↓	0	↓	↓	↓	↓	↓	↓	↓	↓
COM4	↓	5	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM5	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM6	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM7	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM8	↓	↓	5	↓	↓	↓	↓	↓	↓	↓	↓
COM9	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM10	↓	↓	↓	79	↓	↓	↓	↓	↓	↓	↓
COM11	↓	↓	↓	0	↓	↓	↓	↓	↓	↓	↓
COM12	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM13	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM14	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM15	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM16	↓	↓	↓	5	↓	↓	↓	↓	↓	↓	↓
COM17	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM18	↓	↓	↓	↓	79	↓	↓	↓	↓	↓	↓
COM19	↓	↓	↓	↓	0	↓	↓	↓	↓	↓	↓
COM20	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM21	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM22	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM23	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM24	↓	↓	↓	↓	5	↓	↓	↓	↓	↓	↓
COM25	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM26	↓	↓	↓	↓	↓	79	↓	↓	↓	↓	↓
COM27	↓	↓	↓	↓	↓	0	↓	↓	↓	↓	↓
COM28	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM29	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM30	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM31	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM32	↓	↓	↓	↓	↓	5	↓	↓	↓	↓	↓
COM33	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM34	↓	↓	↓	↓	↓	↓	79	↓	↓	↓	↓
COM35	↓	↓	↓	↓	↓	↓	0	↓	↓	↓	↓
COM36	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM37	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM38	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM39	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM40	↓	↓	↓	↓	↓	↓	5	↓	↓	↓	↓
COM41	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM42	↓	↓	↓	↓	↓	↓	↓	79	↓	↓	↓
COM43	↓	↓	↓	↓	↓	↓	↓	0	↓	↓	↓
COM44	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM45	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM46	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM47	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM48	↓	↓	↓	↓	↓	↓	↓	5	↓	↓	↓
COM49	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM50	↓	↓	↓	↓	↓	↓	↓	↓	79	↓	↓
COM51	↓	↓	↓	↓	↓	↓	↓	↓	0	↓	↓
COM52	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM53	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM54	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM55	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM56	↓	↓	↓	↓	↓	↓	↓	↓	5	↓	↓
COM57	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM58	↓	↓	↓	↓	↓	↓	↓	↓	↓	79	↓
COM59	↓	↓	↓	↓	↓	↓	↓	↓	↓	0	↓
COM60	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM61	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM62	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM63	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM64	↓	↓	↓	↓	↓	↓	↓	↓	↓	5	↓
COM65	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM66	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	79
COM67	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0
COM68	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM69	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM70	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM71	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM72	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	5
COM73	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM74	79	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM75	0	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM76	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM77	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM78	↓	79	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM79	4	0	76	68	60	52	44	36	28	20	12
81 st COM Timing	4	4	4	4	4	4	4	4	4	4	4

Fig 27 Relation between Row address and Common Driver (4)

NOTE1) DS: Duty Cycle Ratio / SC: Initial COM / LA: Initial Display Line Address

NOTE2) Segment waveforms for 81st COM timing are the same as for 80th COM timing (Row address "79").

(18-5) SHIFT=0, Initial Display Line "0", Duty Cycle Ratio "1/81", Duty-1 ON

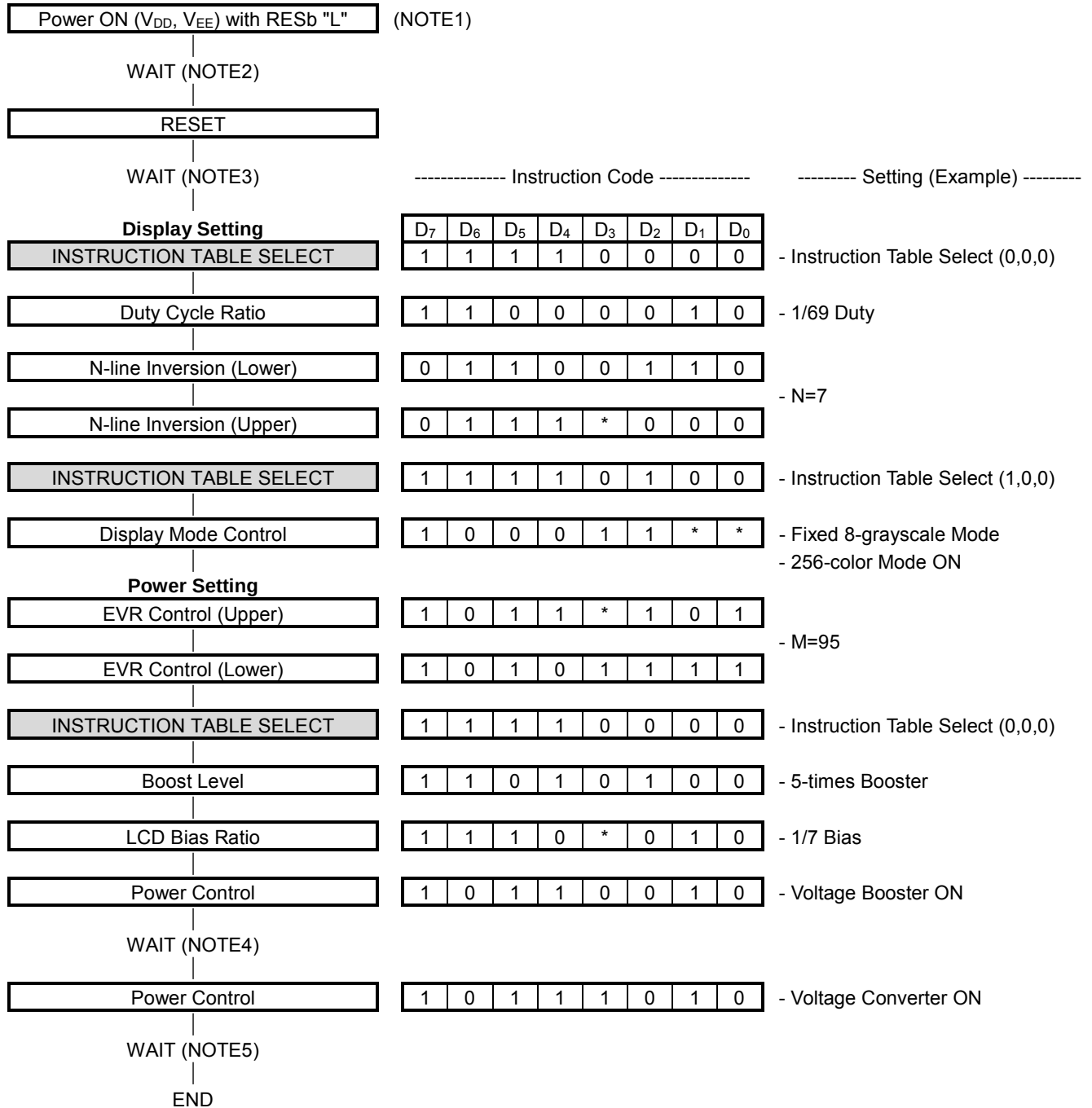
SHIFT=0, DS3-0=(0,0,0,0), LA6-LA0=(0,0,0,0,0,0), DSE=1											
SC3 - SC0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010
COM0	0	76	72	64	56	48	40	32	24	16	8
COM1	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM3	↓	79	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM4	↓	0	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM5	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM6	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM7	↓	↓	79	↓	↓	↓	↓	↓	↓	↓	↓
COM8	↓	↓	0	↓	↓	↓	↓	↓	↓	↓	↓
COM9	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM10	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM11	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM12	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM13	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM14	↓	↓	↓	79	↓	↓	↓	↓	↓	↓	↓
COM15	↓	↓	↓	0	↓	↓	↓	↓	↓	↓	↓
COM16	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM17	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM18	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM19	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM20	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM21	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM22	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM23	↓	↓	↓	↓	79	↓	↓	↓	↓	↓	↓
COM24	↓	↓	↓	↓	0	↓	↓	↓	↓	↓	↓
COM25	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM26	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM27	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM28	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM29	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM30	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM31	↓	↓	↓	↓	↓	79	↓	↓	↓	↓	↓
COM32	↓	↓	↓	↓	↓	0	↓	↓	↓	↓	↓
COM33	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM34	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM35	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM36	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM37	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM38	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM39	↓	↓	↓	↓	↓	↓	79	↓	↓	↓	↓
COM40	↓	↓	↓	↓	↓	↓	0	↓	↓	↓	↓
COM41	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM42	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM43	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM44	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM45	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM46	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM47	↓	↓	↓	↓	↓	↓	↓	79	↓	↓	↓
COM48	↓	↓	↓	↓	↓	↓	↓	0	↓	↓	↓
COM49	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM50	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM51	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM52	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM53	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM54	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM55	↓	↓	↓	↓	↓	↓	↓	↓	79	↓	↓
COM56	↓	↓	↓	↓	↓	↓	↓	↓	0	↓	↓
COM57	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM58	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM59	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM60	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM61	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM62	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM63	↓	↓	↓	↓	↓	↓	↓	↓	↓	79	↓
COM64	↓	↓	↓	↓	↓	↓	↓	↓	↓	0	↓
COM65	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM66	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM67	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM68	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM69	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM70	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM71	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	79
COM72	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0
COM73	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM74	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM75	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM76	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM77	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM78	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
COM79	79	75	71	63	55	47	39	31	23	15	7

Fig 28 Relation between Row address and Common Driver (5)

NOTE1) DS: Duty Cycle Ratio / SC: Initial COM / LA: Initial Display Line Address

(19) TYPICAL INSTRUCTION SEQUENCES

(19-1) Initialization Sequence in Using Internal LCD Power Supply



NOTE1) If different power sources are applied to the V_{DD} and the V_{EE} , turn on the V_{DD} first.

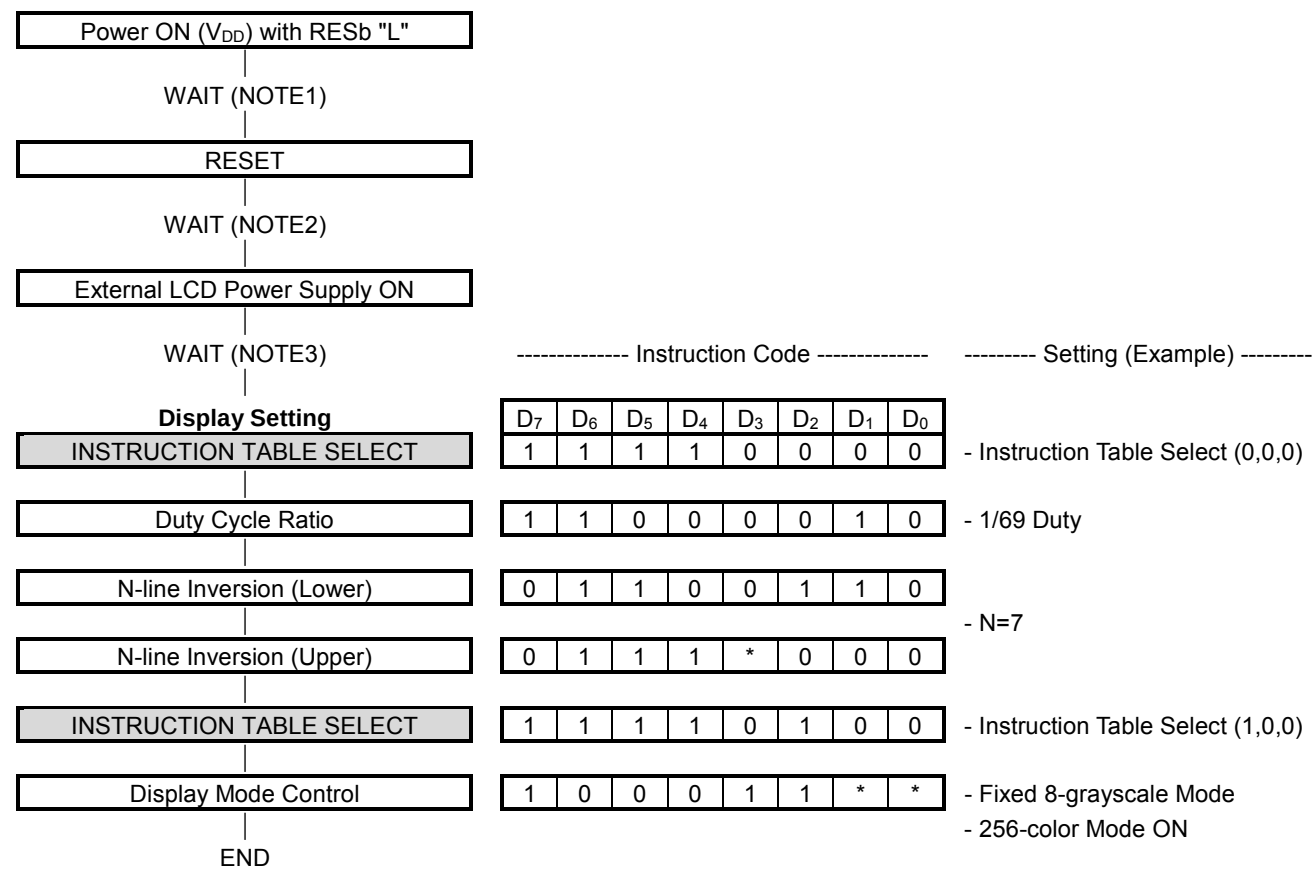
NOTE2) Wait until the V_{DD} and V_{EE} are stabilized.

NOTE3) Wait 10 [μ s] or more.

NOTE4) Wait until the V_{OUT} is stabilized.

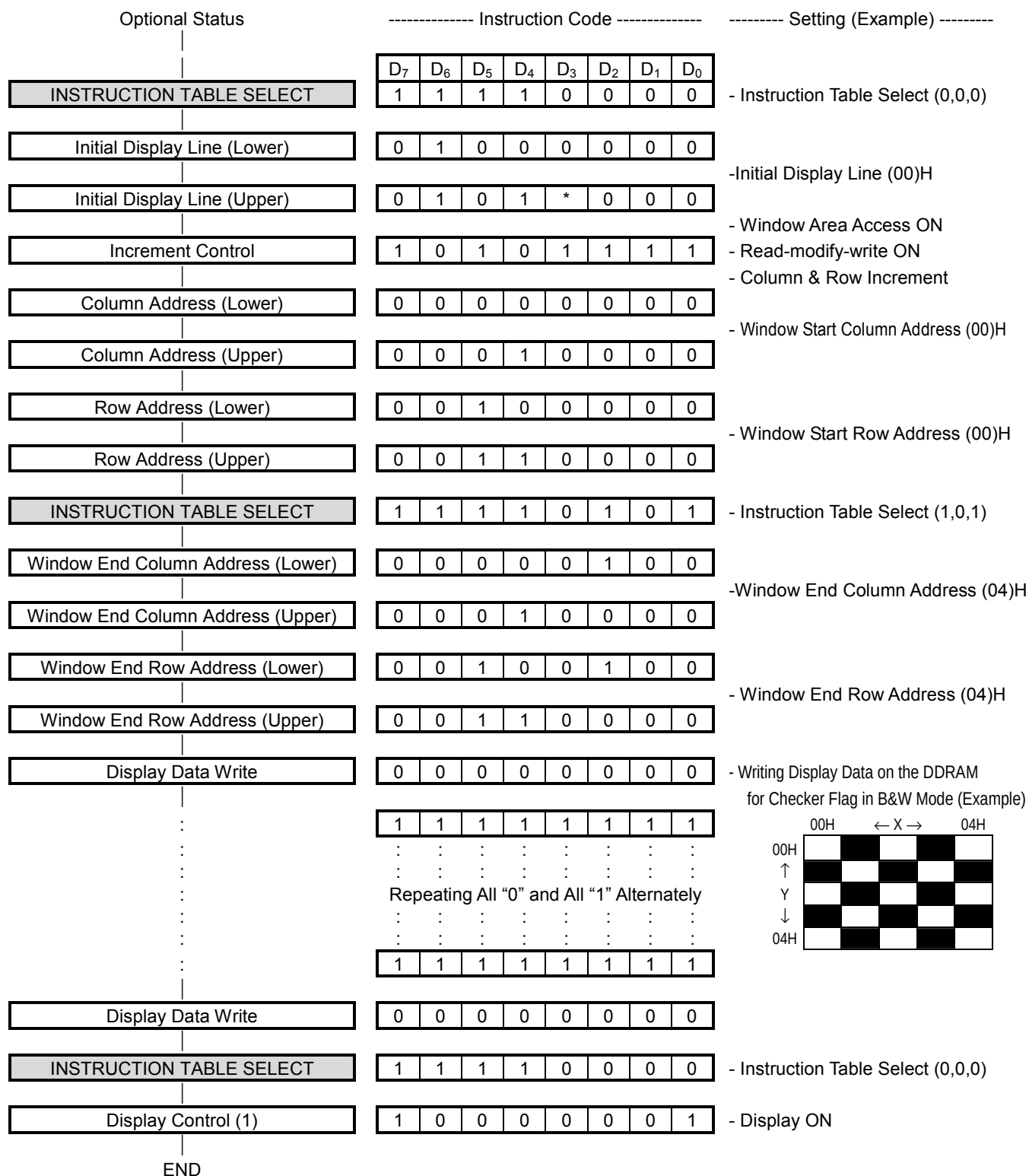
NOTE5) Wait until the V_{LCD} and V_1 - V_4 are stabilized.

(19-2) Initialization Sequence in Using External LCD Power Supply

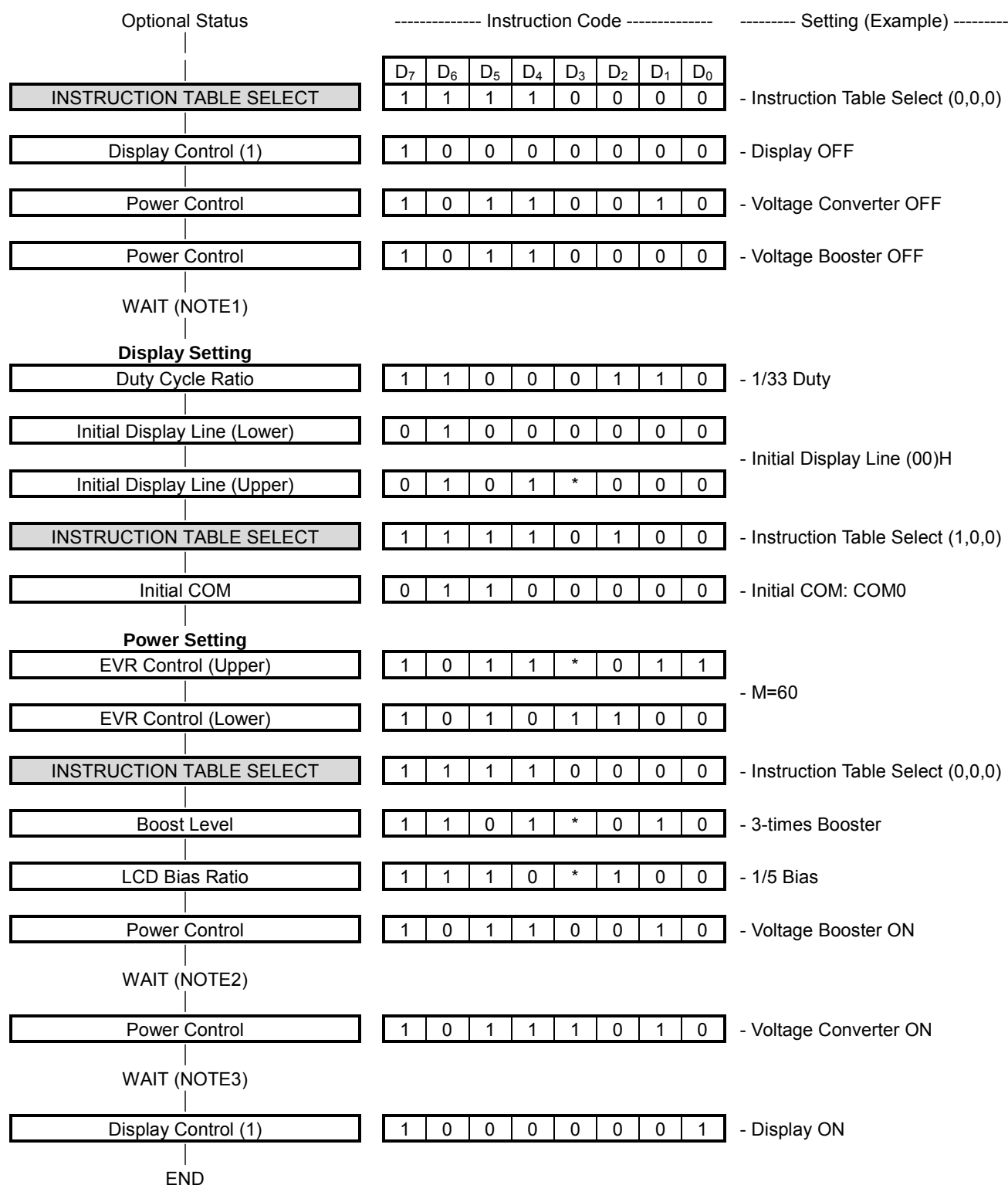


NOTE1) Wait until the V_{DD} is stabilized.
NOTE2) Wait 10 [us] or more.
NOTE3) Wait until the external LCD power supply (V_{OUT}, V_{LCD}, V₁-V₄) are stabilized.

(19-3) Display Data Write Sequence



(19-4) Partial Display Sequence

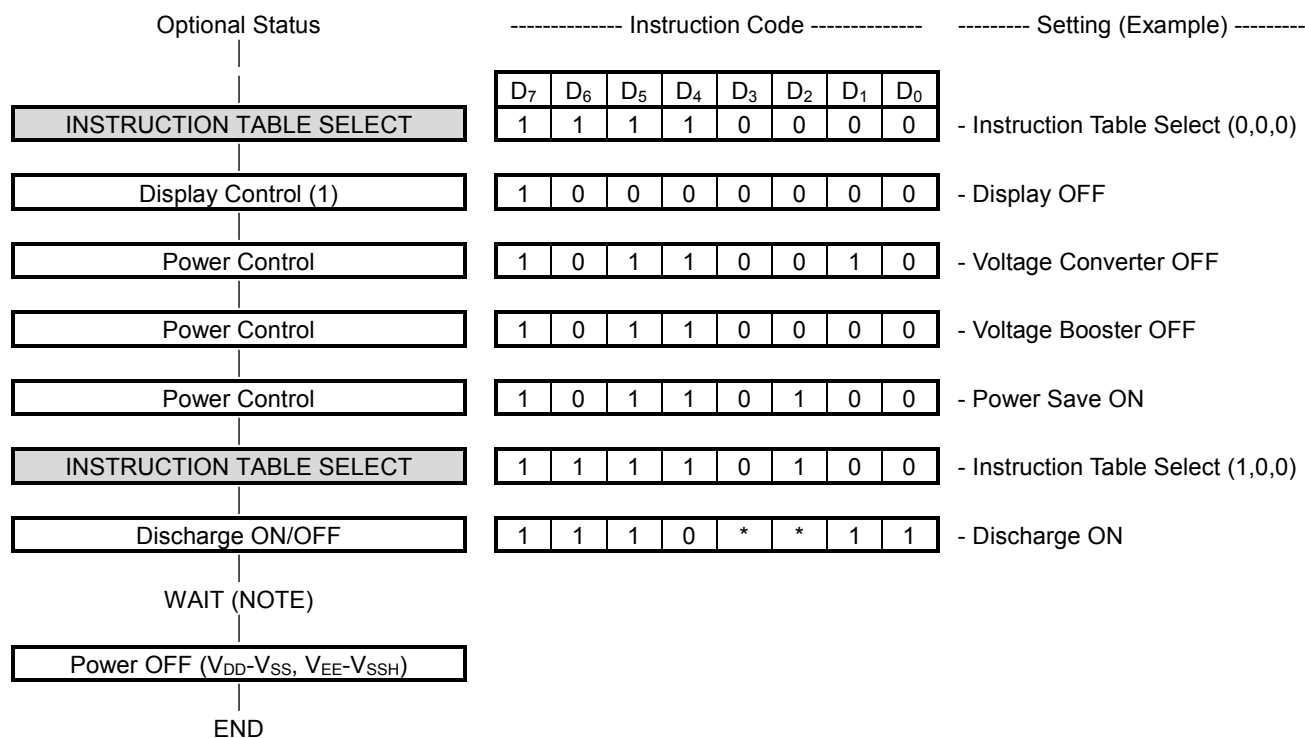


NOTE1) Wait until the voltage booster is completely turned off. Make sure what is the wait time in the particular application.

NOTE2) Wait until the V_{OUT} is stabilized.

NOTE3) Wait until the V_{LCD} and V_1 - V_4 are stabilized.

(19-5) Power OFF Sequence



NOTE) Wait until the Discharge is completed.

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITION	TERMINAL	RATING	UNIT
Supply Voltage (1)	V_{DD}	$V_{SS}=0V$ $V_{SSH}=0V$ $T_a = +25^{\circ}C$	V_{DD}	-0.3 to +4.0	V
Supply Voltage (2)	V_{EE}		V_{EE}	-0.3 to +4.0	V
Supply Voltage (3)	V_{OUT}		V_{OUT}	-0.3 to +19.0	V
Supply Voltage (4)	V_{REG}		V_{REG}	-0.3 to +19.0	V
Supply Voltage (5)	V_{LCD}		V_{LCD}	-0.3 to +19.0	V
Supply Voltage (6)	V_1, V_2, V_3, V_4		V_1, V_2, V_3, V_4	-0.3 to $V_{LCD} + 0.3$	V
Input Voltage	V_I		*1	-0.3 to $V_{DD} + 0.3$	V
Storage Temperature	T_{stg}			-45 to +125	$^{\circ}C$

NOTE1) D_0 to D_{15} , CSb, RS, RDb, WRb, OSC1, RESb, TEST1, and TEST2

NOTE2) To stabilize the LSI operation, place decoupling capacitors between V_{DD} and V_{SS} and between V_{EE} and V_{SSH} .

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TERMINAL	MIN	TYP	MAX	UNIT	NOTE
Supply Voltage	V_{DD1}	V_{DD}	1.7		3.3	V	1
	V_{DD2}		2.4		3.3	V	2
	V_{EE}	V_{EE}	2.4		3.3	V	3
Operating Voltage	V_{LCD}	V_{LCD}	5		18.0	V	4
	V_{OUT}	V_{OUT}			18.0	V	
	V_{REG}	V_{REG}			$V_{OUT} \times 0.9$	V	
	V_{REF}	V_{REF}	2.1		3.3	V	5
Operating Temperature	$Topr$		-30		85	$^{\circ}C$	

NOTE1) Applied to the condition when the reference voltage generator is not used.

NOTE2) Applied to the condition when the reference voltage generator is used.

NOTE3) Applied to the condition when the voltage booster is used.

NOTE4) The following relation among the LCD bias voltages must be maintained.

$$V_{SSH} < V_4 < V_3 < V_2 < V_1 < V_{LCD} < V_{OUT}$$

NOTE5) Relation: $V_{REF} < V_{EE}$ must be maintained.

■ DC CHARACTERISTICS

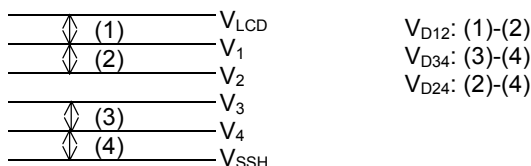
$V_{SS}=0V$, $V_{SSH}=0V$, $V_{DD}=+1.7$ to $+3.3V$, $T_a=-30$ to $+85^{\circ}C$

PARAMETER	SYM BOL	CONDITION	MIN	TYP	MAX	UNIT	NOTE
"H" Level Input Voltage	V_{IH}		$0.8 V_{DD}$		V_{DD}	V	1
"L" Level Input Voltage	V_{IL}		0		$0.2V_{DD}$	V	1
"H" Level Output Voltage	V_{OH1}	$I_{OH} = -0.4mA$	$V_{DD} - 0.4$			V	2
"L" Level Output Voltage	V_{OL1}	$I_{OL} = 0.4mA$			0.4	V	2
"H" Level Output Voltage	V_{OH2}	$I_{OH} = -0.1mA$	$V_{DD} - 0.4$			V	3
"L" Level Output Voltage	V_{OL2}	$I_{OL} = 0.1mA$			0.4	V	3
Input Leakage Current	I_{LI}	$V_I = V_{SS}$ or V_{DD}	-10		10	μA	4
Output Leakage Current	I_{LO}	$V_I = V_{SS}$ or V_{DD}	-10		10	μA	5
Driver ON-resistance	R_{ON1}	$ \Delta V_{ON} = 0.5V$					
		$V_{LCD} = 10V$		1	2	$k\Omega$	6
		$V_{LCD} = 6V$		2	4		
Stand-by Current	I_{STB}	$CSb = V_{DD}$, $T_a = 25^{\circ}C$			15	μA	7
Oscillation Frequency Using Internal Resistor	f_{OSC1}	$V_{DD} = 3V$ $T_a = 25^{\circ}C$	309	377	445	kHz	8
	f_{OSC2}		69	85	101		9
	f_{OSC3}		10	12.2	14.4		10
Oscillation Frequency Using External Resistor	f_{r1}	$R_f = 24k\Omega$		382		kHz	11
	f_{r2}	$R_f = 120k\Omega$		84			
	f_{r3}	$R_f = 820k\Omega$		12.8			
Voltage Booster Output Voltage	V_{OUT}	N-time boost (N=2 to 6) $RL = 500k\Omega$ ($V_{OUT} - V_{SSH}$)	$(N \times V_{EE}) \times 0.95$			V	12
Operating Current (1)	I_{DD1}	$V_{DD} = 3V$, 6-time boost All pixels ON		760	1140	μA	13
Operating Current (2)	I_{DD2}	$V_{DD} = 3V$, 6-time boost Checker flag display		930	1400		
Operating Current (3)	I_{DD3}	$V_{DD} = 3V$, 5-time boost All pixels ON		520	780		
Operating Current (4)	I_{DD4}	$V_{DD} = 3V$, 5-time boost Checker flag display		650	980		
Operating Current (5)	I_{DD5}	$V_{DD} = 3V$, 4-time boost All pixels ON		360	540		
Operating Current (6)	I_{DD6}	$V_{DD} = 3V$, 4-time boost Checker flag display		450	680		
V_{BA} Output Voltage	V_{BA}	$V_{EE} = 2.4$ to $3.3V$	$(0.9 V_{EE}) \times 0.98$	$0.9 V_{EE}$	$(0.9 V_{EE}) \times 1.02$	V	14
V_{REG} Output Voltage	V_{REG}	$V_{EE} = 2.4$ to $3.3V$ $V_{REF} = 0.9 \times V_{EE}$ N-time boost (N=2 to 6)	$(V_{REF} \times N) \times 0.97$	$(V_{REF} \times N)$	$(V_{REF} \times N) \times 1.03$	V	15
LCD Bias Voltages	V_2		-100	0	+100	mV	16
	V_3		-100	0	+100		
	V_{D12}		-30	0	+30		
	V_{D34}		-30	0	+30		
	V_{D24}		-30	0	+30		

■ OSCILLATION FREQUENCY AND FRAME FREQUENCY

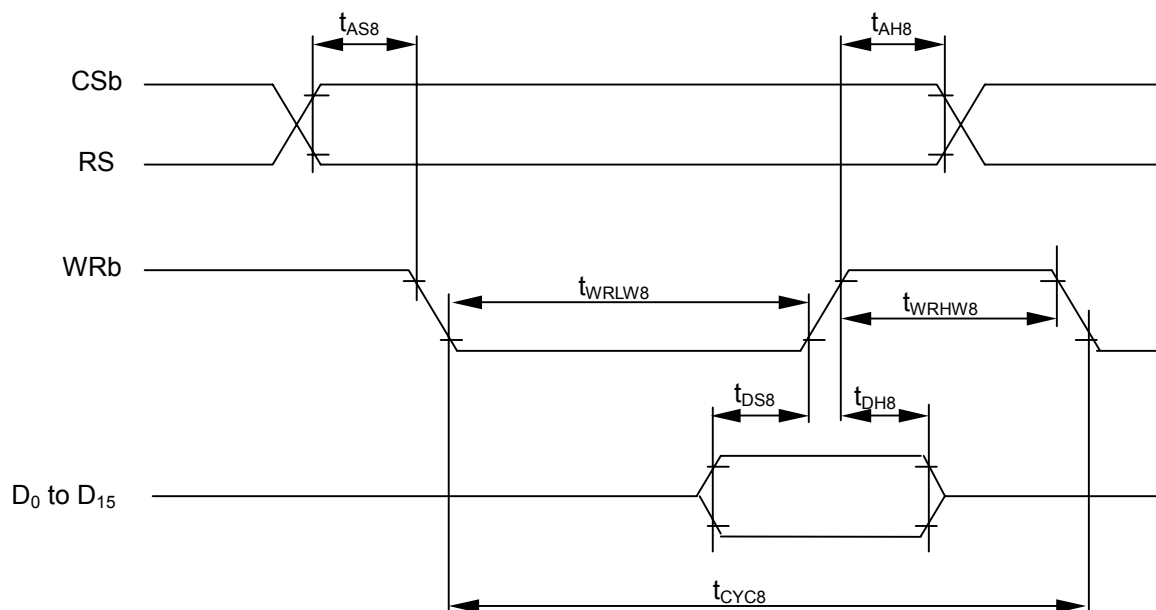
OSCILLATOR /EXTERNAL CLOCK	SYM BOL	DISPLAY MODE	FRAME FREQUENCY (FLM)		
			DUTY CYCLE RATIO (1/D) <DSE=0>		
			1/81-1/57	1/47-1/27	1/17-1/13
Using Internal Oscillator	f _{OSC1}	Variable 8-/16-level Grayscale Mode	f _{OSC} / (62xD)	f _{OSC} / (62xDx2)	f _{OSC} / (62xDx4)
	f _{OSC2}	Fixed 8-level Grayscale Mode	f _{OSC} / (14xD)	f _{OSC} / (14xDx2)	f _{OSC} / (14xDx4)
	f _{OSC3}	B&W Mode	f _{OSC} / (2xD)	f _{OSC} / (2xDx2)	f _{OSC} / (2xDx4)
Using External Clock	f _{CK1}	Variable 8-/16-level Grayscale Mode	f _{CK} / (62xD)	f _{CK} / (62xDx2)	f _{CK} / (62xDx4)
	f _{CK2}	Fixed 8-level Grayscale Mode	f _{CK} / (14xD)	f _{CK} / (14xDx2)	f _{CK} / (14xDx4)
	f _{CK3}	B&W Mode	f _{CK} / (2xD)	f _{CK} / (2xDx2)	f _{CK} / (2xDx4)

- NOTE1) D_0 - D_{15} , CSb, RS, RDb, WRb, P/S, SEL68 and RESb
- NOTE2) D_0 - D_{15}
- NOTE3) CL, FLM, FR and CLK
- NOTE4) CSb, RS, SEL68, RDb, WRb, P/S, RESb and OSC1
- NOTE5) D_0 - D_{15} in high impedance
- NOTE6) SEGA₀-SEGA₁₀₃, SEGB₀-SEGB₁₀₃, SEGC₀-SEGC₁₀₃ and COM₀-COM₇₉
This parameter defines the resistance between each COM/SEG and each LCD bias (V_{LCD} , V_1 , V_2 , V_3 and V_4).
- 0.5V Difference / 1/9 LCD Bias
- NOTE7) V_{DD}
Oscillator is halted.
- CSb=1 (Disabled) / No-load on COM/SEG
- NOTE8) CLK
This parameter defines the oscillation frequency by using the internal resistor, in the Variable grayscale mode.
- (Rf2, Rf1, Rf0)=(0,0,0)
- NOTE9) CLK
This parameter defines the oscillation frequency by using the internal resistor, in the 8-level fixed grayscale mode.
- (Rf2, Rf1, Rf0)=(0,0,0)
- NOTE10) CLK
This parameter defines the oscillation frequency by using the internal resistor, in the B&W mode.
- (Rf2, Rf1, Rf0)=(0,0,0)
- NOTE11) OSC2
- $V_{DD}=3V$ / $T_a=25^{\circ}C$
- NOTE12) V_{OUT}
This parameter is applied to the condition that the internal LCD power supply and the internal oscillator are used.
- $V_{EE}=2.4V$ to $3.3V$ / EVR= (1,1,1,1,1,1,1) / 1/4 to 1/10 LCD Bias / 1/81 Duty Cycle / No-load on COM/SEG / $RL=500k\Omega$ between V_{OUT} and V_{SSH} / CA1=CA2=1.0uF / CA3=0.1uF / DCON="1" / AMPON="1"
- NOTE13) V_{SS} , V_{SSH}
This parameter is applied to the condition that the internal LCD power supply and the internal oscillator are used.
- EVR= (1,1,1,1,1,1,1) / All Pixels ON or Checker Flag Display / No-load on COM/SEG / No-access from MPU / $V_{DD}=V_{EE}$ / $V_{REF}=0.9V_{EE}$ / CA1=CA2=1.0uF / CA3=0.1uF / DCON="1" / AMPON="1" / NLIN="0" / 1/81 Duty cycle / $T_a=25^{\circ}C$
- NOTE14) V_{BA}
- $V_{BA}=V_{REF}$ / Boost Level (N)="1", / DCON="0" / $V_{OUT}=13.5V$
- NOTE15) V_{REG}
- $V_{EE}=2.4V$ to $3.3V$ / $V_{REF}=0.9V_{EE}$ / $V_{OUT}=18V$ / 1/4 to 1/10 LCD bias ratio / 1/81 duty cycle / EVR=(1,1,1,1,1,1,1) / Checker flag display / No-load on COM/SEG / Boost Level (N)="2" to "6" / CA1=CA2=1.0uF / CA3=0.1uF / DCON="0" / AMPON="1" / NLIN="0"
- NOTE16) V_{LCD} , V_1 , V_2 , V_3 and V_4
- $V_{EE}=3.0V$ / $V_{REF}=0.9V_{EE}$ / $V_{OUT}=15V$ / 1/4 to 1/10 LCD Bias / EVR= (1,1,1,1,1,1,1) / Display OFF / No-load on COM/SEG / Boost Level (N)="5" / CA1=CA2=1.0uF / CA3=0.1uF / DCON="0" / AMPON="1"



■ AC CHARACTERISTICS

(1) Write Operation (Parallel Interface / 80-series MPU)



($V_{DD}=2.5$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	CSb
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		90		ns	
Enable "L" level pulse width	t_{WRLW8}		35		ns	WRb
Enable "H" level pulse width	t_{WRHW8}		35		ns	
Data setup time	t_{DS8}		30		ns	D ₀ to D ₁₅
Data hold time	t_{DH8}		5		ns	

($V_{DD}=2.2$ to $2.5V$, $T_a=-30$ to $+85^{\circ}C$)

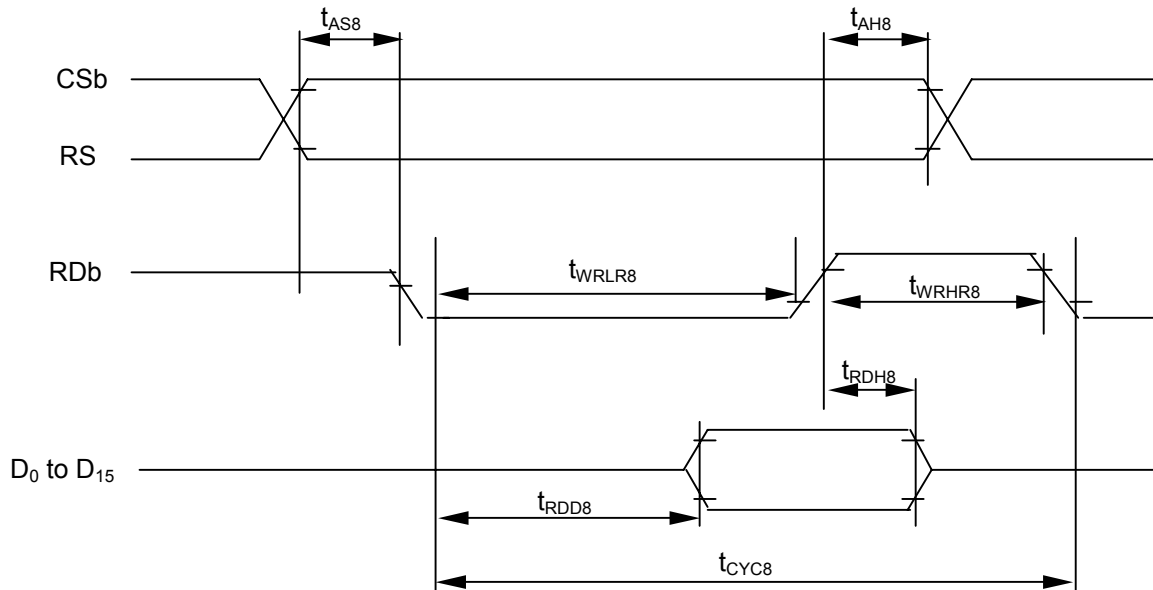
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	CSb
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		160		ns	
Enable "L" level pulse width	t_{WRLW8}		70		ns	WRb
Enable "H" level pulse width	t_{WRHW8}		70		ns	
Data setup time	t_{DS8}		40		ns	D ₀ to D ₁₅
Data hold time	t_{DH8}		5		ns	

($V_{DD}=1.7$ to $2.2V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	CSb
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		180		ns	
Enable "L" level pulse width	t_{WRLW8}		80		ns	WRb
Enable "H" level pulse width	t_{WRHW8}		80		ns	
Data setup time	t_{DS8}		70		ns	D ₀ to D ₁₅
Data hold time	t_{DH8}		10		ns	

NOTE) Each timing is specified based on 20% and 80% of V_{DD} .

(2) Read Operation (Parallel Interface / 80-series MPU)



($V_{DD}=2.5$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	CSb
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		180		ns	RDb
Enable "L" level pulse width	t_{WRLR8}		80		ns	
Enable "H" level pulse width	t_{WRHR8}		80		ns	
Read Data delay time	t_{RDD8}	CL=15pF	0	60	ns	D ₀ to D ₁₅
Read Data hold time	t_{RDH8}				ns	

($V_{DD}=2.2$ to $2.5V$, $T_a=-30$ to $+85^{\circ}C$)

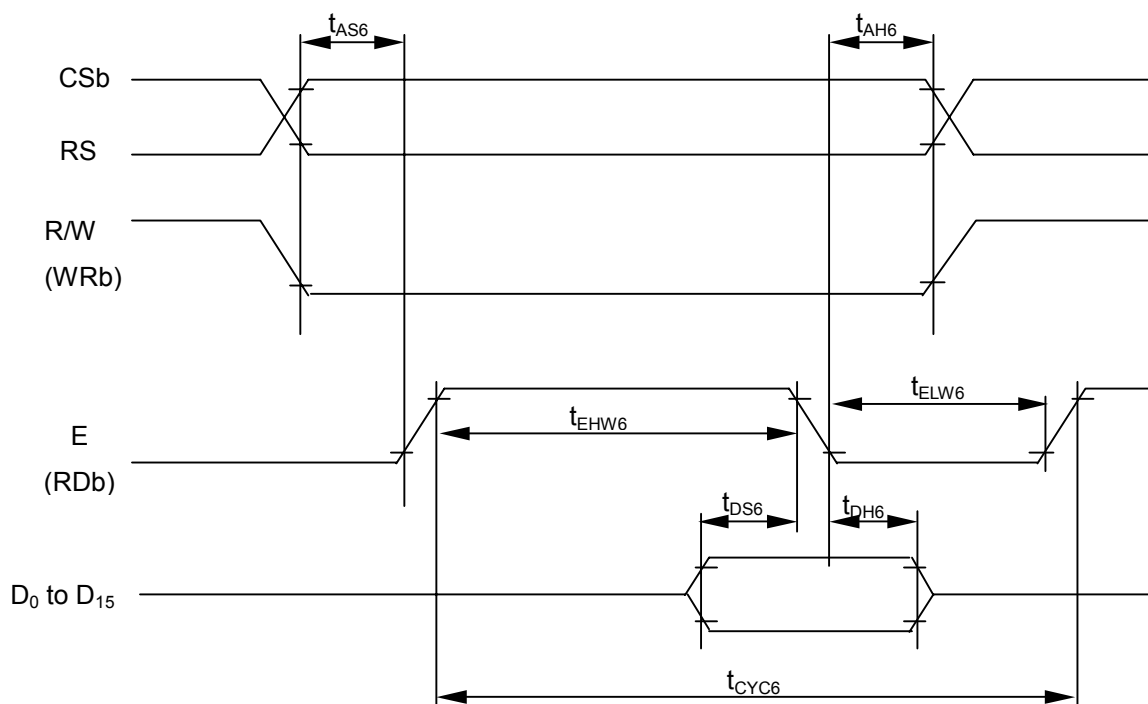
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	CSb
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		180		ns	RDb
Enable "L" level pulse width	t_{WRLR8}		80		ns	
Enable "H" level pulse width	t_{WRHR8}		80		ns	
Read Data delay time	t_{RDD8}	CL=15pF	0	60	ns	D ₀ to D ₁₅
Read Data hold time	t_{RDH8}				ns	

($V_{DD}=1.7$ to $2.2V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	CSb
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		300		ns	RDb
Enable "L" level pulse width	t_{WRLR8}		140		ns	
Enable "H" level pulse width	t_{WRHR8}		140		ns	
Read Data delay time	t_{RDD8}	CL=15pF	0	130	ns	D ₀ to D ₁₅
Read Data hold time	t_{RDH8}				ns	

NOTE) Each timing is specified based on 20% and 80% of V_{DD} .

(3) Write Operation (Parallel Interface / 68-series MPU)



($V_{DD}=2.5$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		90		ns	E
Enable "L" level pulse width	t_{ELW6}		35		ns	
Enable "H" level pulse width	t_{EHW6}		35		ns	
Data setup time	t_{DS6}		40		ns	D ₀ to D ₁₅
Data hold time	t_{DH6}		5		ns	

($V_{DD}=2.2$ to $2.5V$, $T_a=-30$ to $+85^{\circ}C$)

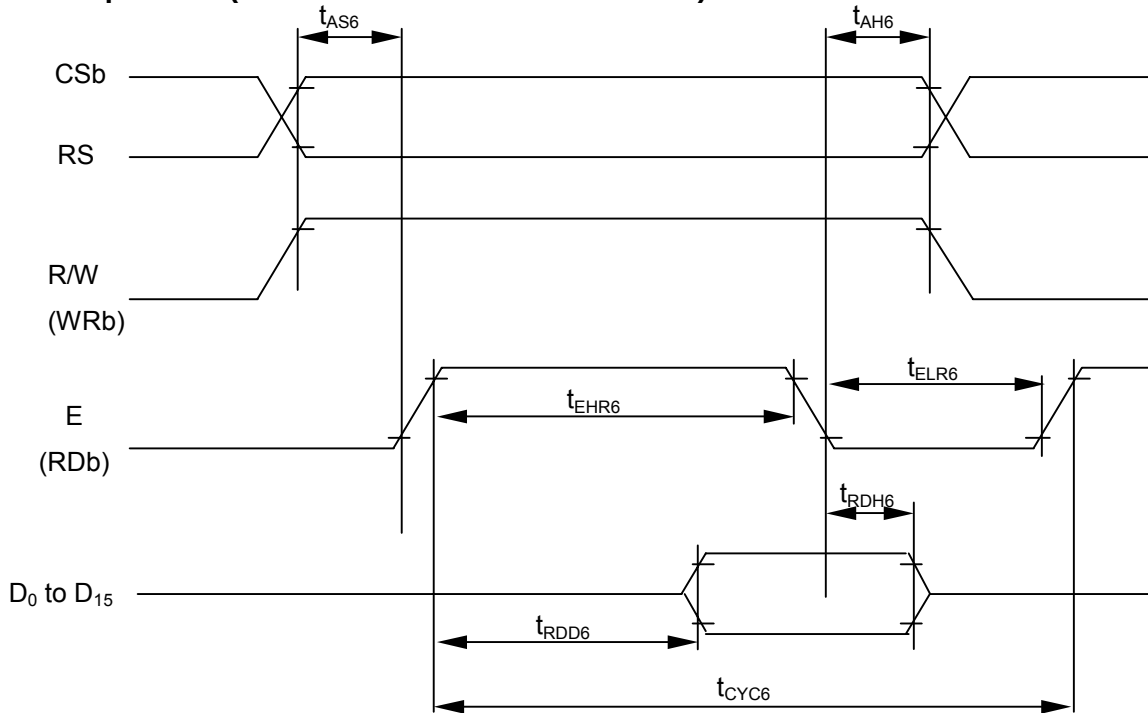
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		160		ns	E
Enable "L" level pulse width	t_{ELW6}		70		ns	
Enable "H" level pulse width	t_{EHW6}		70		ns	
Data setup time	t_{DS6}		50		ns	D ₀ to D ₁₅
Data hold time	t_{DH6}		5		ns	

($V_{DD}=1.7$ to $2.2V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		180		ns	E
Enable "L" level pulse width	t_{ELW6}		80		ns	
Enable "H" level pulse width	t_{EHW6}		80		ns	
Data setup time	t_{DS6}		70		ns	D ₀ to D ₁₅
Data hold time	t_{DH6}		10		ns	

NOTE) Each timing is specified based on 20% and 80% of V_{DD} .

(4) Read Operation (Parallel Interface / 68-series MPU)



($V_{DD}=2.5$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		180		ns	E
Enable "L" level pulse width	t_{ELR6}		80		ns	
Enable "H" level pulse width	t_{EHR6}		80		ns	
Read Data delay time	t_{RDD6}	CL=15pF	0	70	ns	D ₀ to D ₁₅
Read Data hold time	t_{RDH6}				ns	

($V_{DD}=2.2$ to $2.5V$, $T_a=-30$ to $+85^{\circ}C$)

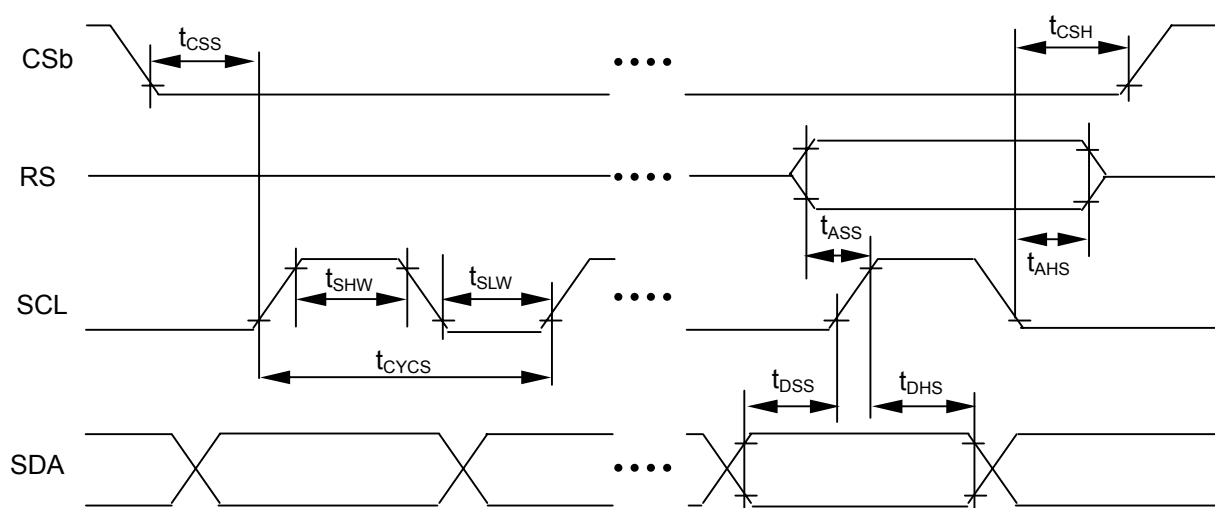
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		180		ns	E
Enable "L" level pulse width	t_{ELR6}		80		ns	
Enable "H" level pulse width	t_{EHR6}		80		ns	
Read Data delay time	t_{RDD6}	CL=15pF	0	70	ns	D ₀ to D ₁₅
Read Data hold time	t_{RDH6}				ns	

($V_{DD}=1.7$ to $2.2V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		300		ns	E
Enable "L" level pulse width	t_{ELR6}		140		ns	
Enable "H" level pulse width	t_{EHR6}		140		ns	
Read Data delay time	t_{RDD6}	CL=15pF	0	130	ns	D ₀ to D ₁₅
Read Data hold time	t_{RDH6}				ns	

NOTE) Each timing is specified based on 20% and 80% of V_{DD} .

(5) Write Operation (Serial Interface)



($V_{DD}=2.5$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		50		ns	SCL
SCL "H" level pulse width	t_{SHW}		20		ns	
SCL "L" level pulse width	t_{SLW}		20		ns	
Address setup time	t_{ASS}		20		ns	RS
Address hold time	t_{AHS}		20		ns	
Data setup time	t_{DSS}		20		ns	SDA
Data hold time	t_{DHS}		20		ns	
CSb – SCL time	t_{CSS}		20		ns	CSb
CSb hold time	t_{CSH}		20		ns	

($V_{DD}=2.2$ to $2.5V$, $T_a=-30$ to $+85^{\circ}C$)

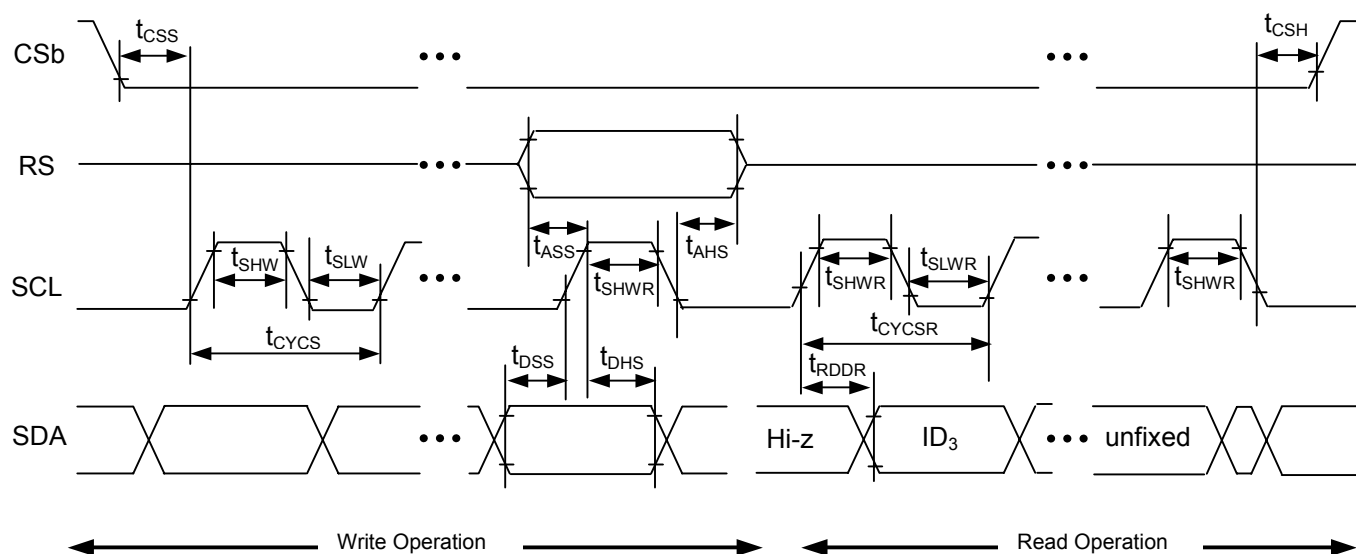
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		50		ns	SCL
SCL "H" level pulse width	t_{SHW}		20		ns	
SCL "L" level pulse width	t_{SLW}		20		ns	
Address setup time	t_{ASS}		20		ns	RS
Address hold time	t_{AHS}		20		ns	
Data setup time	t_{DSS}		20		ns	SDA
Data hold time	t_{DHS}		20		ns	
CSb – SCL time	t_{CSS}		20		ns	CSb
CSb hold time	t_{CSH}		20		ns	

($V_{DD}=1.7$ to $2.2V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		80		ns	SCL
SCL "H" level pulse width	t_{SHW}		35		ns	
SCL "L" level pulse width	t_{SLW}		35		ns	
Address setup time	t_{ASS}		35		ns	RS
Address hold time	t_{AHS}		35		ns	
Data setup time	t_{DSS}		35		ns	SDA
Data hold time	t_{DHS}		35		ns	
CSb – SCL time	t_{CSS}		35		ns	CSb
CSb hold time	t_{CSH}		35		ns	

NOTE) Each timing is specified based on 20% and 80% of V_{DD} .

(6) Read Operation (Serial Interface)



($V_{DD}=2.5$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCSR}	NOTE2)	400		ns	SCL
SCL "H" level pulse width	t_{SHWR}		300		ns	SCL
SCL "L" level pulse width	t_{SLWR}		75		ns	SCL
Read Data delay time	t_{RDDR}		80		ns	CSb

($V_{DD}=2.2$ to $2.5V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCSR}	NOTE2)	520		ns	SCL
SCL "H" level pulse width	t_{SHWR}		400		ns	SCL
SCL "L" level pulse width	t_{SLWR}		95		ns	SCL
Read Data delay time	t_{RDDR}		100		ns	CSb

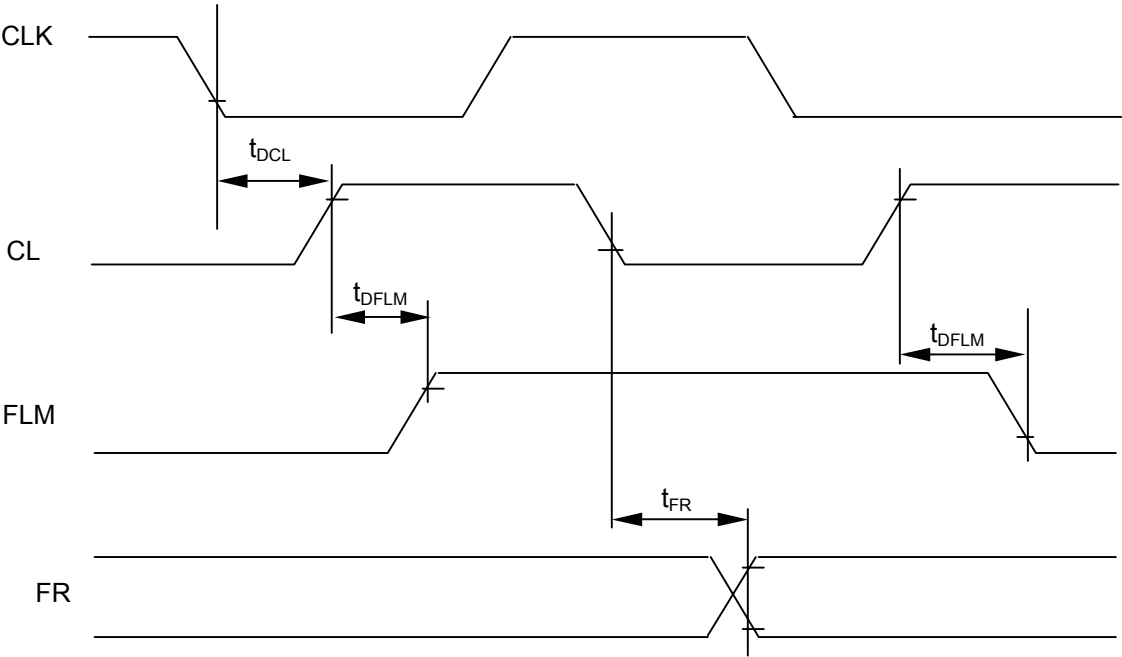
($V_{DD}=1.7$ to $2.2V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCSR}	NOTE2)	660		ns	SCL
SCL "H" level pulse width	t_{SHWR}		500		ns	SCL
SCL "L" level pulse width	t_{SLWR}		135		ns	SCL
Read Data delay time	t_{RDDR}		140		ns	CSb

NOTE1) Each timing is specified based on 20% and 80% of V_{DD} .

NOTE2) t_{CYCSR} is applied to the timing from the 8th clock and later in the 4-line serial interface, or the 9th and later in the 3-line serial interface.

(7) Display Control Timing



Output timing (V_{DD}=2.4 to 3.3V, Ta=-30 to +85°C)

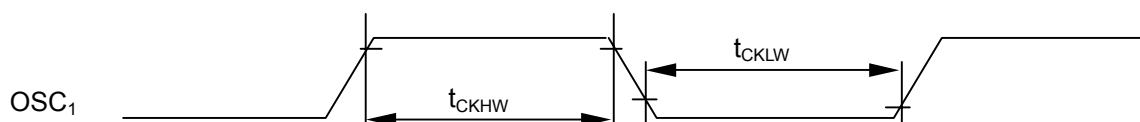
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
FLM delay time	t_{DFLM}	CL=15pF	0	500	ns	FLM
FR delay time	t_{FR}		0	500	ns	FR
CL delay time	t_{DCL}		0	200	ns	CL

Output timing (V_{DD}=1.7 to 2.4V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
FLM delay time	t_{DFLM}	CL=15pF	0	1000	ns	FLM
FR delay time	t_{FR}		0	1000	ns	FR
CL delay time	t_{DCL}		0	200	ns	CL

NOTE) Each timing is specified based on 20% and 80% of V_{DD}.

(8) Input Clock Timing



($V_{DD}=1.7$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
OSC1 "H" level pulse width (1)	t_{CKHW1}		1.12	1.62	μs	OSC1 (NOTE2)
OSC1 "L" level pulse width (1)	t_{CKLW1}		1.12	1.62	μs	
OSC1 "H" level pulse width (2)	t_{CKHW2}		4.95	7.25	μs	OSC1 (NOTE3)
OSC1 "L" level pulse width (2)	t_{CKLW2}		4.95	7.25	μs	
OSC1 "H" level pulse width (3)	t_{CKHW3}		34.7	50.0	μs	OSC1 (NOTE4)
OSC1 "L" level pulse width (3)	t_{CKLW3}		34.7	50.0	μs	

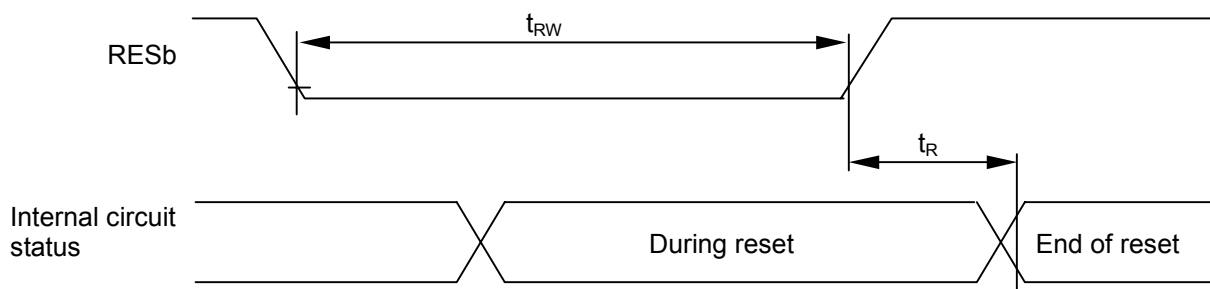
NOTE1) Each timing is specified based on 20% and 80% of V_{DD} .

NOTE2) Applied to Variable 8-/16-level grayscale mode (MON="0", PWM="0")

NOTE3) Applied to fixed 8-level grayscale mode (MON="0", PWM="1")

NOTE4) Applied to B&W mode (MON="1")

(9) Reset Input Timing



($V_{DD}=2.4$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	Terminal
Reset time	t_R			1.0	μs	
RESb "L" level pulse width	t_{RW}		10.0		μs	RESb

($V_{DD}=1.7$ to $2.4V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	Terminal
Reset time	t_R			1.5	μs	
RESb "L" level pulse width	t_{RW}		10.0		μs	RESb

NOTE) Each timing is specified based on 20% and 80% of V_{DD} .

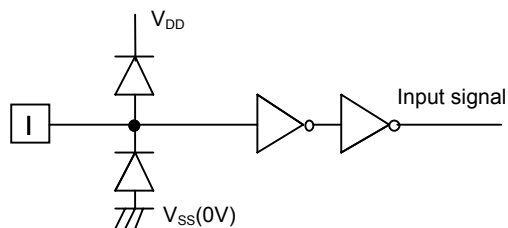
(10) Delay Time of Gate

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Delay time of gate	$T_a=+25^{\circ}C$, $V_{SS}=0V$, $V_{DD}=3.0V$		10		ns

INPUT/OUTPUT BLOCK DIAGRAMS

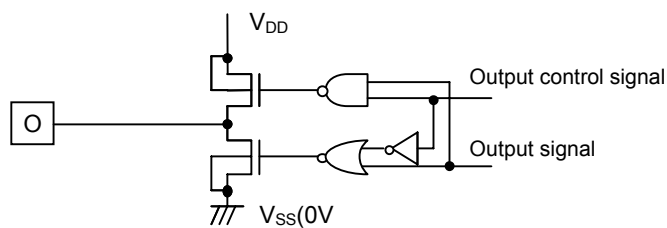
Input Block Diagram

Terminals CSb, RS, RDb, WRb, SEL68, P/S, RESb



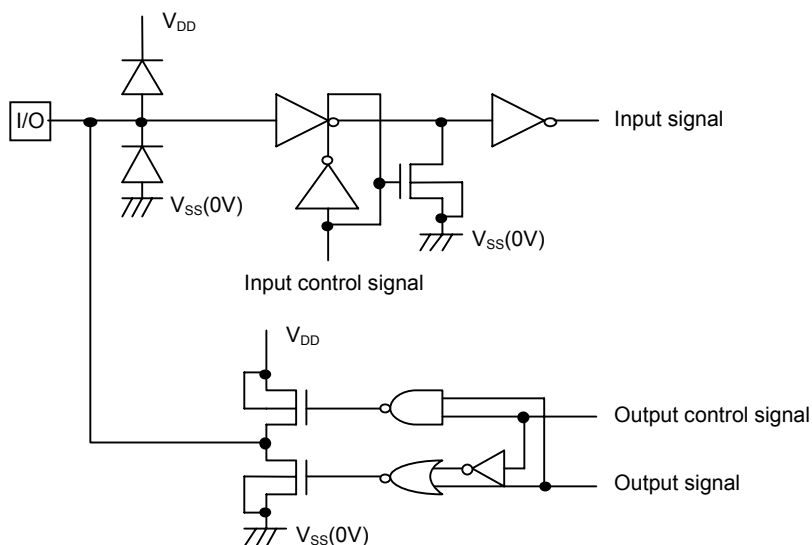
Output Block Diagram

Terminals : FLM, CL, FR, CLK



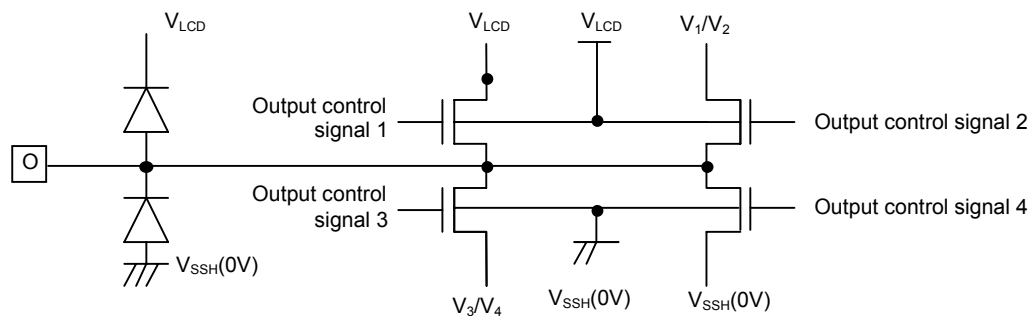
Input/Output Block Diagram

Terminals : D₀ - D₁₅



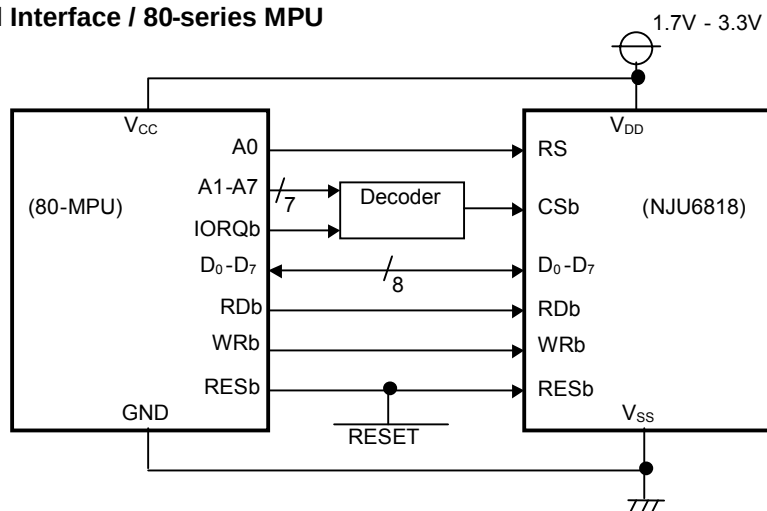
COM/SEG Driver Block Diagram

Terminals : SEGA₀/B₀/C₀ - SEGA₁₀₃/B₁₀₃/C₁₀₃, COM₀ - COM₇₉

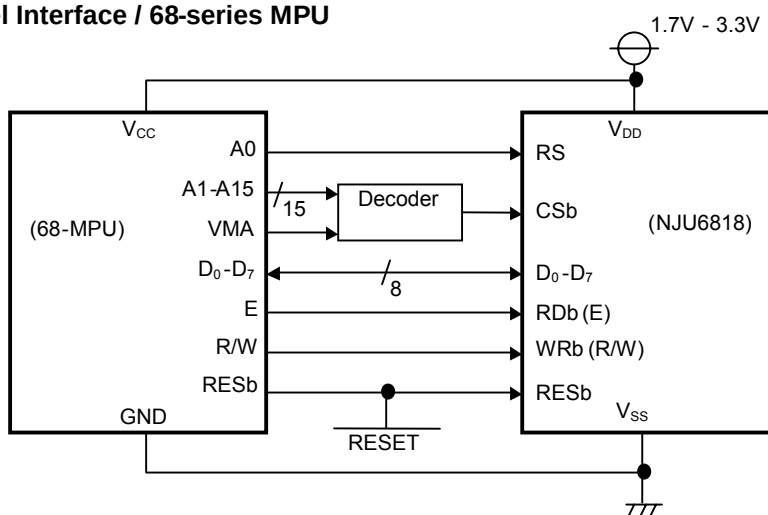


■ MPU CONNECTIONS

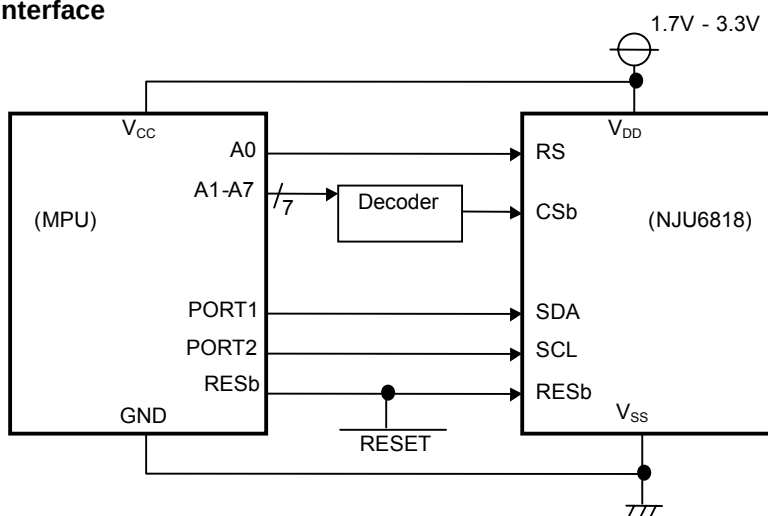
Parallel Interface / 80-series MPU



Parallel Interface / 68-series MPU



Serial Interface



[CAUTION]

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