PRELIMINARY

1/8, 1/9, 1/10 Duty
BITMAP LCD DRIVER with KEY SCAN

■ GENERAL DESCRIPTION

The **NJU6538** is a 10-common x 65-segment bitmap LCD driver to display graphics or characters.
It contains 650 bits display data RAM, microprocessor interface circuit, common and segment drivers, key scan circuit, and general output ports.

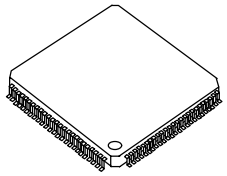
An image data from MPU through the serial interface is stored into the 650 bits internal displayed on the LCD panel through the commons and segments drivers.

The **NJU6538** displays 10 x 65 dots graphics or 11-character 1-line by 5 x 7 dots character + 3 x 65 dots icons. It contains key scan circuit transmitting the 25-keys maximum (5 x 5 = 25) to MPU.

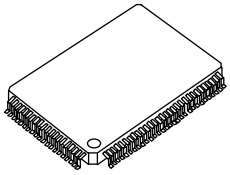
Also it provides 4 general purpose output ports with PWM output function maximum to drive LEDs or others directly.

Furthermore, the NJU6538 can select a LCD driving voltage out of 16 steps voltage by the instruction adjust the display contrast of LCD panel.

■ PACKAGE OUTLINE



NJU6538FG1

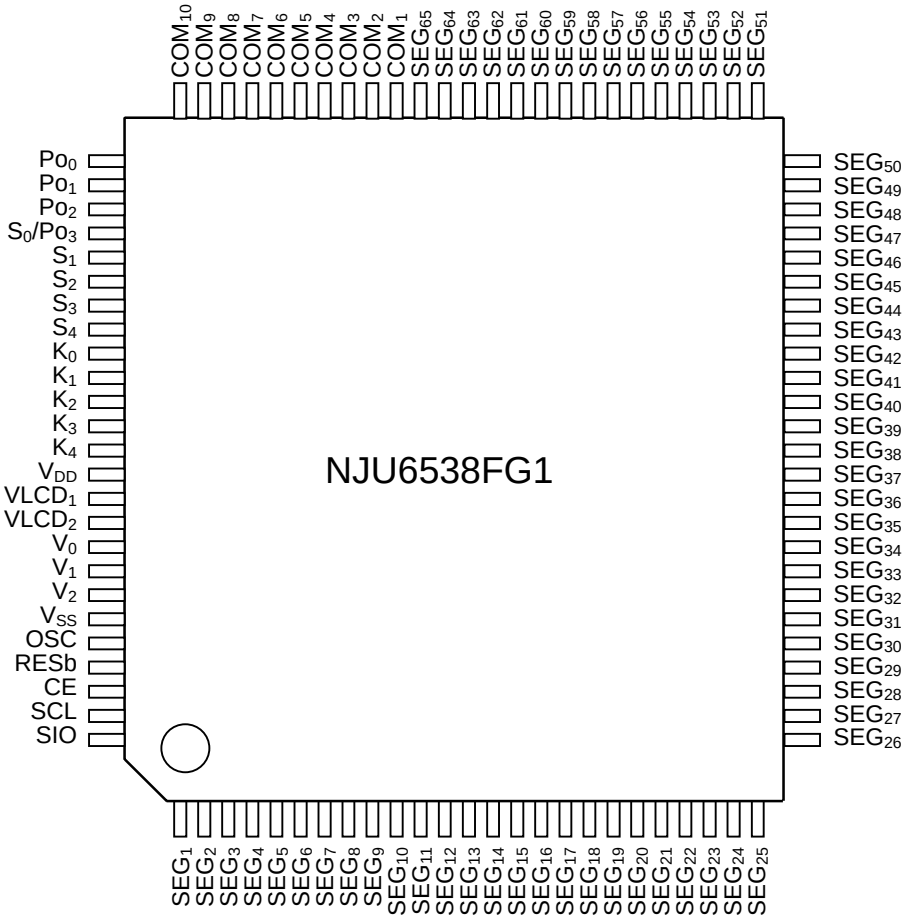


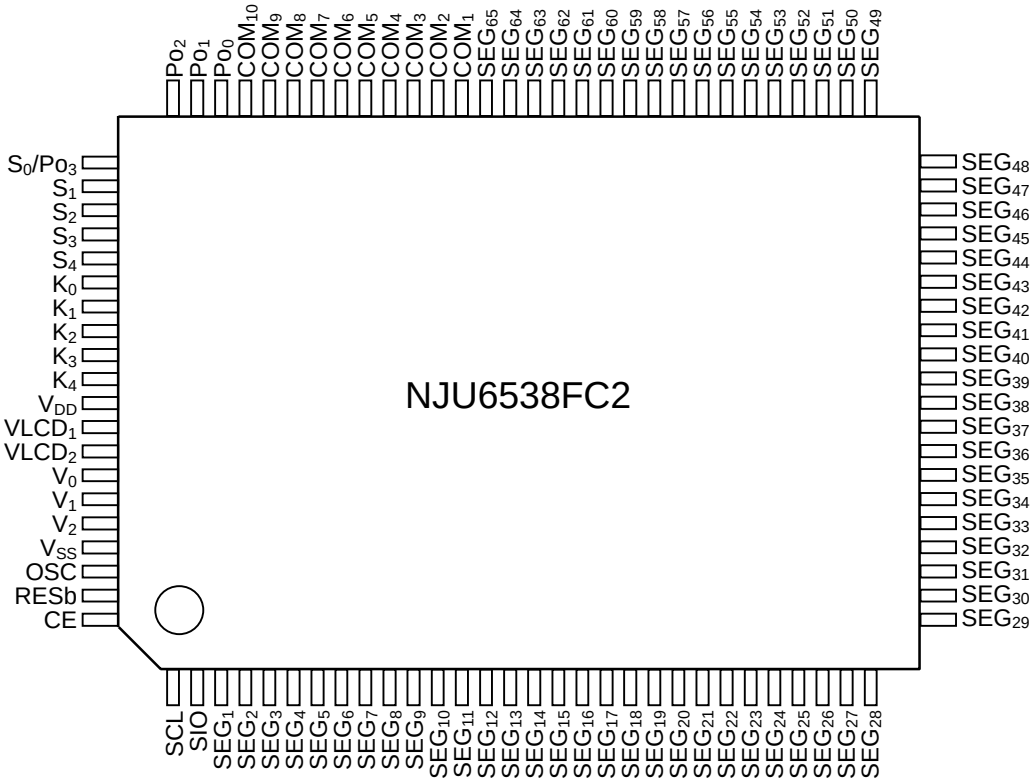
NJU6538FC2

■ FEATURES

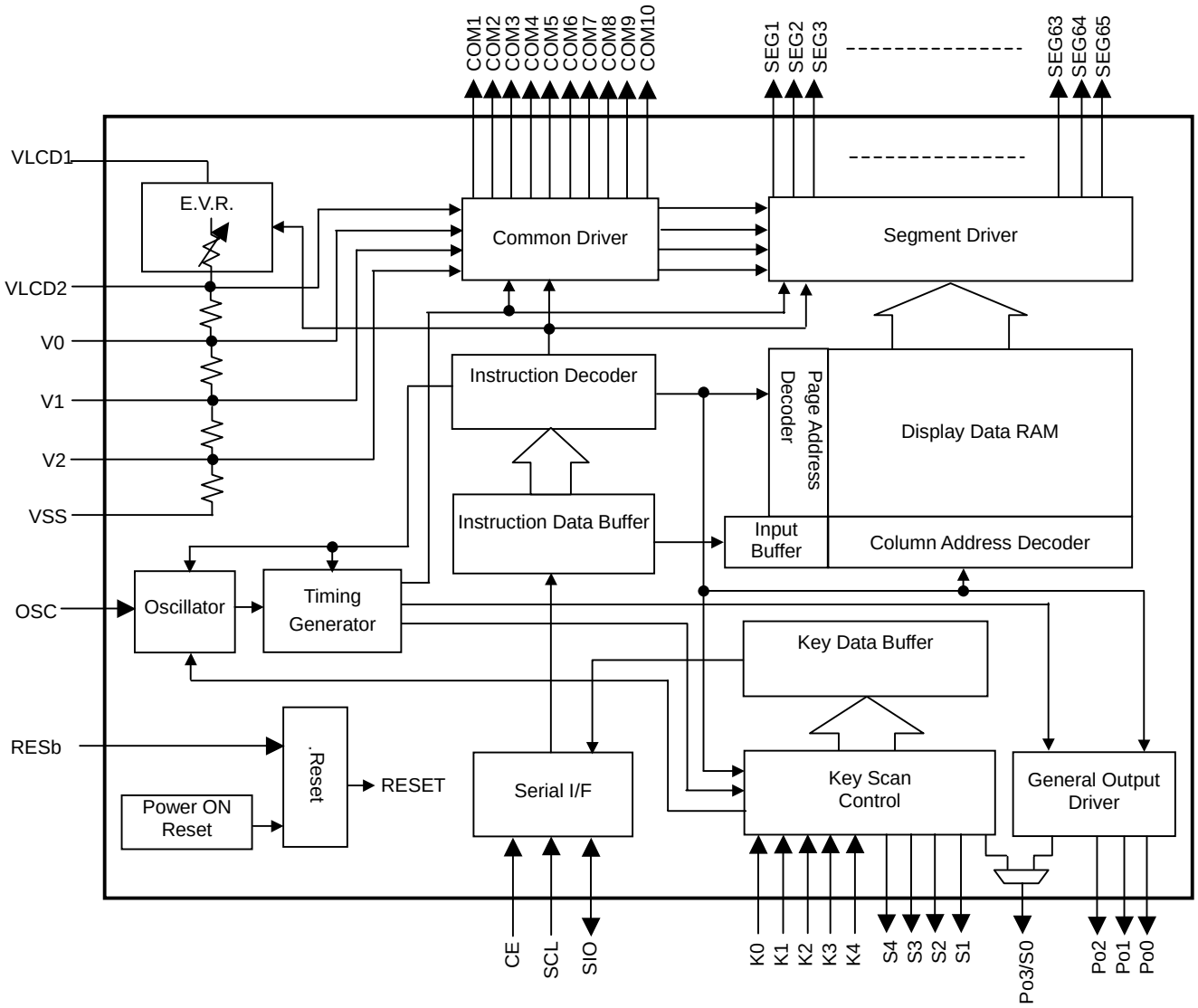
- Direct Correspondence between Display Data RAM and LCD Pixel
- Display Data RAM : 650-bits
- LCD Drivers : 65-seg, 10-com
- Serial interface (SIO, SCL, CS)
- Programmable Duty Ratio
  - 1/8 Duty 7-common x 65-segment + 1-icon common
  - 1/9 Duty 7-common x 65-segment + 2-icon common
  - 1/10Duty 7-common x 65-segment + 3-icon common
- Bias Ratio 1/4 bias
- 25-key scan Function (5 x 5 matrix)
  Needless for anti-reverse current diodes in key scan
- general Output Ports with 128-steps PWM output (possible LED driving) maximum 4-ports
- Useful Instruction Set
  Display ON/OFF, Page Address Set, Column Address Set, Display Data write, ADC Select, Inverse Display ON/OFF, whole display ON/OFF, Reset, EVR Register Set, Duty Select, Power Save mode set, General Output Port PWM phase / frequency set, General Output Port PWM data set, General Output Port / Key scan output select
- Bleeder Resistance On-chip
- Software Contrast Control (16 steps)
- Operating Voltage
  Logic Operating Voltage 2.7 to 5.5V
  LCD Driving Voltage 5.0 to 10.0V
- Package Outline QFP100-G1
  QFP100-C2
- C-MOS Technology (Substrate: P)

■ PIN CONFIGRATION





■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

No.		Symbol	I/O	Description
FG1	FC2			
1 to 65	3 to 67	SEG_1 to SEG_{65}	O	Segment output terminal.
66 to 72	68 to 74	COM_1 to COM_7	O	Common output terminal.
73 to 75	75 to 77	COM_8 to COM_{10}	O	Icon common output terminal.
76 to 78	78 to 80	Po0 to Po2	O	General output port 128-step PWM waveform output by MPU control.
79	81	Po3/S_0	O	General output port / Key scanning input terminal Select General output port or Key scanning input terminal by the instruction. A function must be selected either Po3 or S_0 General output port 128-step PWM waveform output by MPU control. Key scanning input terminals (No need for anti-reverse current diode in key scan)
80 to 83	82 to 85	S_1 to S_4	O	Key scanning input terminals. (No need for anti-reverse current diode in key scan)
84 to 88	86 to 90	K_0 to K_4	I	Key scanning input terminals. (with internal pull-down resistor)
89	91	V_{DD}	-	Power supply terminal.(2.7V to 5.5V)
90	92	VLCD1	I	LCD driving voltage input terminal.
91 92 93 94	93 94 94 96	VLCD2 V_0 V_1 V_2	I	LCD driving voltage stabilization capacitor terminals. Connect the capacitor between each terminal and Vss.
95	97	V_{SS}	-	Ground terminal.
96	98	OSC	I/O	Osclator terminal. Conect the external resistor.
97	99	RESb	I	Reset terminal. (with internal pull-up resistor) In case of only Power-on Reset should be open.
98	100	CE	I	Chip enable terminal
99	1	SCL	I	Serial clock input terminal
100	2	SIO	I/O	Serial Data input or output terminal

■ FUNCTIONAL DESCRIPTION

(1) Description for each blocks

(1-1) Serial I/F
The serial I/F controls serial data from external data.

(1-2) Instruction data buffer
The instruction data buffer stores instruction code from external.

(1-3) Instruction decoder
The instruction decoder decodes instruction code and controls each blocks.

(1-4) Display data RAM
The Display data RAM stores data for display from MPU.

(1-5) Segment driver
The Segment driver generates driving waveform to segment terminal on display data.

(1-6) General output driver
The General output driver generates output signal level to general output terminal on output data.

(1-7) Common driver
The Common driver generates driving waveform to common terminal.

(1-8) Electrical Variable Resistance (E.V.R.)
The Electrical Variable Resistance adjusts LCD driving voltage from V0 to V2.

(1-9) Key scan controller
The Key scan controller controls to input from external Key data.

(1-10) Key data buffer
The data buffer for key stores Key data until next key data is stored.

(1-11) CR Oscillator
The Oscillator is external connect resistor, which generates the master clock.

(1-12) Reset circuit
The Reset circuit is type of detectable voltage. It resets internal circuit when the power turns on or drop the voltage.

Fig.1 Display data RAM (DDRAM) Map

Page address	Data	Display Pattern
D0=”0”	D0	PAGE 0
	D1	
	D2	
	D3	
	D4	
	D5	
	D6	
D0=”1”	D0	PAGE 1
	D1	
	D2	

Common Drivers
COM1
COM2
COM3
COM4
COM5
COM6
COM7
COM8
COM9
COM10

Column Address	ADC												
		D0="0"	00	01	02	03	04	05	06	→	3F	40
		D0="1"	40	3F	3E	3D	3C	3B	3A	←	01	00
	Segment Drivers		1	2	3	4	5	6	7	- - - - - - - - - - - - - - - -	64	65

(2) Instruction

3-wired Serial I/F is clock synchronized of the SCL clock. and D_7 to D_0 signal select data or instruction by A0 signal.

The data input as MSB(D7) first serially.

Table 1. Instruction Code (*: Don't Care)

Instruction		Code									Description
		A0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
(a)	Display ON/OFF	0	1	0	1	0	1	1	1	0/1	LCD display ON / OFF D_0=0 : OFF, D_0=1 : ON
(b)	Page address set	0	1	0	1	1	0	0	0	0/1	Set the page of DDRAM to the page address registor. D_0=0 : PAGE 0, D_0=1 : PAGE 1
(c)	Culumn address set Higher order 3-bits	0	0	0	0	1	*	Higher order Column add.			Set the Higher order 3 bits column address to rhe registor.
	Culumn address set Lower order 4-bits	0	0	0	0	0	Lower order Column add.				Set the Lower order 4 bits column address to rhe registor.
(d)	Display data write	1	*	Write data							Write the data into the Display data RAM(DDRAM)
(e)	ADC select	0	1	0	1	0	0	0	0	0/1	Set the DDRAM to SEG driver D_0=0 : Nomal, D_0=1 : Inverse
(f)	Inverse display On / Off	0	1	0	1	0	0	1	1	0/1	Inverse LCD display ON / OFF D_0=0 : Nomal, D_0=1 : Inverse
(g)	Whole display ON / Normal display	0	1	0	1	0	0	1	0	0/1	Whole Display tern ON D_0=0: Normal, D_0=1: Whole Display
(h)	Reset	0	1	1	1	0	0	0	1	0	Initialize the internal circuit
(i)	E.V.R. Register Set	0	0	0	1	0	E.V.R. data				Set the Contrast control E.V.R. (16 steps)
(j)	Duty select	0	0	0	1	1	0	Duty			Duty set (1/8,1/9,1/10) (D_2,D_1,D_0)=(0,0,0) : 1/8Duty (D_2,D_1,D_0)=(0,0,1) : 1/9 Duty (D_2,D_1,D_0)=(0,1,0) : 1/10 Duty
(k)	Power save mode set	0	0	1	0	0	0	0	Power save		Set the Power save mode (D_1,D_0)=(0,0) : Nomal (D_1,D_0)=(0,1) : Power save 1 (D_1,D_0)=(1,0) : Power save 2 (D_1,D_0)=(1,1) : Power save 3
(l)	General output port PWM phase / freqency set	0	0	1	0	1	0	0	Phase	Freq.	Set the PWM phase / freqency D_1: PWM Phase set D_0: PWM Freqenccy set
(m)	General output port serect	0	0	1	1	0	0	0	Port		Select the General output port for PWM level set
	General output port PWM set High order 3-bits / PWM enable set	0	1	0	0	0	PWMEN	High order PWM data			PWMEN=0:"L" output PWMEN=1:PWM output Set the Higher order 3 bits PWM data to rhe registor.
	General output port PWM set Lower order 4-bits	0	0	1	1	1	Lower order PWM data				Set the Lower order 4 bits PWM data to rhe registor.
(n)	General output port / Key scan output select	0	1	0	0	1	0	0	0	0/1	Select General output port or Key scan output select by Po3/S_0 terminal D_0=0 : General output port D_0=1 : Key scan output
(o)	Maker test	0	1	1	1	1	Test data				Do not use this instruction.

(2-1) Instruction discription

(a) Display ON / OFF

This instruction selects display turn-on or turn-off regardless of the contents of the DDRAM.

A0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	1	1	1	D

D 0: Display OFF
1: Display ON

(b) Page address set

In order to access to the DDRAM for writing or reading display data, both “page address set” and “column address set” instructions are required before accessing.
The page address “0” should be used for icon display because the only D_0 to D_6 is valid.
The page address “1” should be used for icon display because the only D_0 to D_2 is valid.

A0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	1	0	0	0	A_0

A_0	Page
0	0
1	1

(c) Column address set

As above-mentioned, in order to access to the DDRAM for writing or reading display data, it is necessary to execute both “page address set” and “column address set” before accessing. The 8-bit column address data will be valid when both upper 3-bit and lower 4-bit data are set into the column address register.
Once the column address is set, it will automatically increment (+1) whenever the DDRAM will be accessed, so that the DDRAM will be able to be continuously accessed without “column address set” instruction.
The column address will stop increment and the page address will not be changed when the last address (40)H is addressed.

A0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	0	0	0	1	*	A_6	A_5	A_4	Upper 4-bit
0	0	0	0	0	A_3	A_2	A_1	A_0	Lower 4-bit

A_6	A_5	A_4	A_3	A_2	A_1	A_0	Column address (HEX)
0	0	0	0	0	0	0	00
0	0	0	0	0	0	1	01
:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:
1	0	0	0	0	0	0	40

(d) Display data write

This instruction writes display data into the selected column address on the DDRAM.

The column address automatically increments (+1) whenever the display data is written by this instruction, so that this instruction can be continuously issued without “column address set” instruction.

A0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	*	Write data						

*:Don’t Care

(e) ADC select

This instruction selects segment driver direction.

The correspondence between the column address and segment driver direction is shown in Fig.1.

Segment Driver Output order is inverse, when this instruction executes, therefore, the placement **NJU6538** against the LCD panel becomes easy.

A0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	0	0	0	D

D 0: Clokwise Output(Normal) S_1 $\rightarrow S_{65}$
1: Counterclockwise Output(Inverse) S_{65} $\rightarrow S_1$

(f) Inverse display ON / OFF

This instruction inverses the status of turn-on or turn-off of entire LCD pixels. It doesn’t change the contents of the DDRAM.

A0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	0	1	1	D

D 0: Normal RAM data “1” correspond to “On”
1: Inverse RAM data “0” correspond to “On”

(g) Whole display ON

This instruction turns on entire LCD pixels regardless the contents of the DDRAM. It doesn’t change the contents of DDRAM. This instruction executed prior to the “Normal or Inverse display On/Off Set” Instruction.

A0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	0	1	0	D

D 0: Normal Display (Whole display OFF)
1: Whole Display turns On (Whole display ON)

(h) Reset

This instruction reset the LSI to the following status, however it doesn't change the contents of the DDRAM. Please be careful that it can't be substituted for the reset operation by using of the RESb terminal.

Reset status by "reset" instruction:

1. Page address : (0) page
2. Column address : $(00)_H$
3. EVR register : (D_3, D_2, D_1, D_0 = "1, 1, 1, 1")
4. Duty select :1/10 Duty
5. General output port(Po0 to Po3) PWM phase / frequency (D_1,D_0 = "0,0")
6. General output port(Po0 to Po3) PWMEN=0,
   PWM value (PWM_6, PWM_5, PWM_4, PWM_3, PWM_2, PWM_1, PWM_0 = " 0,0,0,0,0,0,0")
7. Set the General output port (Po3) by Po3/S0 terminal

The DDRAM is not affected by this initialization.

A0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	0	0	0	1	0

(i)EVR register set

E.V.R. resister set instruction adjusts the contrast of the LCD, and selects.
One LCD driving voltage VLCD out of 16 voltage-stages by setting E.V.R. register.
Set the binary code "0000" when contrast adjustment is unused.

A0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	0	E.V.R. data			

D_3	D_2	D_1	D_0	V_{LCD2} terminal level (Typical)
0	0	0	0	V_{LCD1}
0	0	0	1	$0.984V_{LCD1}$
0	0	1	0	$0.968V_{LCD1}$
0	0	1	1	$0.952V_{LCD1}$
0	1	0	0	$0.938V_{LCD1}$
0	1	0	1	$0.923V_{LCD1}$
0	1	1	0	$0.909V_{LCD1}$
0	1	1	1	$0.896V_{LCD1}$
1	0	0	0	$0.882V_{LCD1}$
1	0	0	1	$0.870V_{LCD1}$
1	0	1	0	$0.857V_{LCD1}$
1	0	1	1	$0.845V_{LCD1}$
1	1	0	0	$0.833V_{LCD1}$
1	1	0	1	$0.822V_{LCD1}$
1	1	1	0	$0.811V_{LCD1}$
1	1	1	1	$0.800V_{LCD1}$

(j) Duty select

Duty select instruction is which sets LCD driving duty ratio 1/8 or 1/9 or 1/10 duty.

A0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	1	0	Duty		

D_2	D_1	D_0	Duty ratio	Scan Common
0	0	0	1/8 Duty	COM1 to COM8 (5x7 character + 1-icon)
0	0	1	1/9 Duty	COM1 to COM9 (5x7 character + 2-icon)
0	1	0	1/10 Duty	COM1 to COM10 (5x7 character + 3-icon)

(k) Power save mode set

Power save mode reduces the operating current of application using Display Off and selects a terminal condition of Key scan signal output. The terminal, which is set to "L", does not output Key scan signal as shown in following table.

A0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	0	0	0	Power save	

D_1	D_0	Function	Internal OSC.	LCD output	Key scanning output terminals states *1				
					S_0	S_1	S_2	S_3	S_4
0	0	Normal	ON	ON	H	H	H	H	H
0	1	Power save 1	Stop	Display Off	L	L	L	L	H
1	0	Power save 2	Stop	Display Off	L	L	L	H	H
1	1	Power save 3	Stop	Display Off	H	H	H	H	H

*1 No scanning states.

(l) General output port PWM phase / freqency set

General output port PWM phase / frequency set instruction setting PWM phase and PWM frequency.

A0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	1	0	0	Phase	Frequency

D_1	General Output Port PWM phase set
0	32-steps shift phase PWM output timinng by Po0 to Po1, Po1 to Po2, Po2 to Po3.
1	same phase PWM output timinng by Po0 to Po3.

D_0	General Output Port PWM frequency set
0	fsys / 128 frequency. (Default)
1	fsys / 256 frequency.

(fsys : system clock = fosc / 2)

(m) General output port set.

This instruction sets the PWM value outputted from Po0 ~ Po3 terminals. The “General output port select” instruction selects the general output port to output with PWM. The “General output port PWM set” instruction sets the PWM value.

The “General output port select instruction" and the “General output port PWM set instruction" is not necessary to continuously perform. Because these instructions are independently.

1. General output port select.

This instruction selects the general output port to output with PWM.

A0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	0	0	0	Port	

D_1	D_0	Port
0	0	Po0
0	1	Po1
1	0	Po2
1	1	Po3

2. General output port PWM set

This instruction sets the PWM value outputted from Po0 ~ Po3 terminals.

The PWM output setting is available for 128-step at each port output terminals.

A0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	PWMEN	PWM_6	PWM_5	PWM_4
0	0	1	1	1	PWM_3	PWM_2	PWM_1	PWM_0

A) PWMEN

0:Selected general output port is ”L” output.

1:Selected general output port outputs PWM depending on PWM data.

B) PWM_6 to PWM_0

PWM value:This register sets the duty value of PWM outputted from the selected general output port.

The PWM value set requires twice, which are upper 3-bit and lower 4-bit.

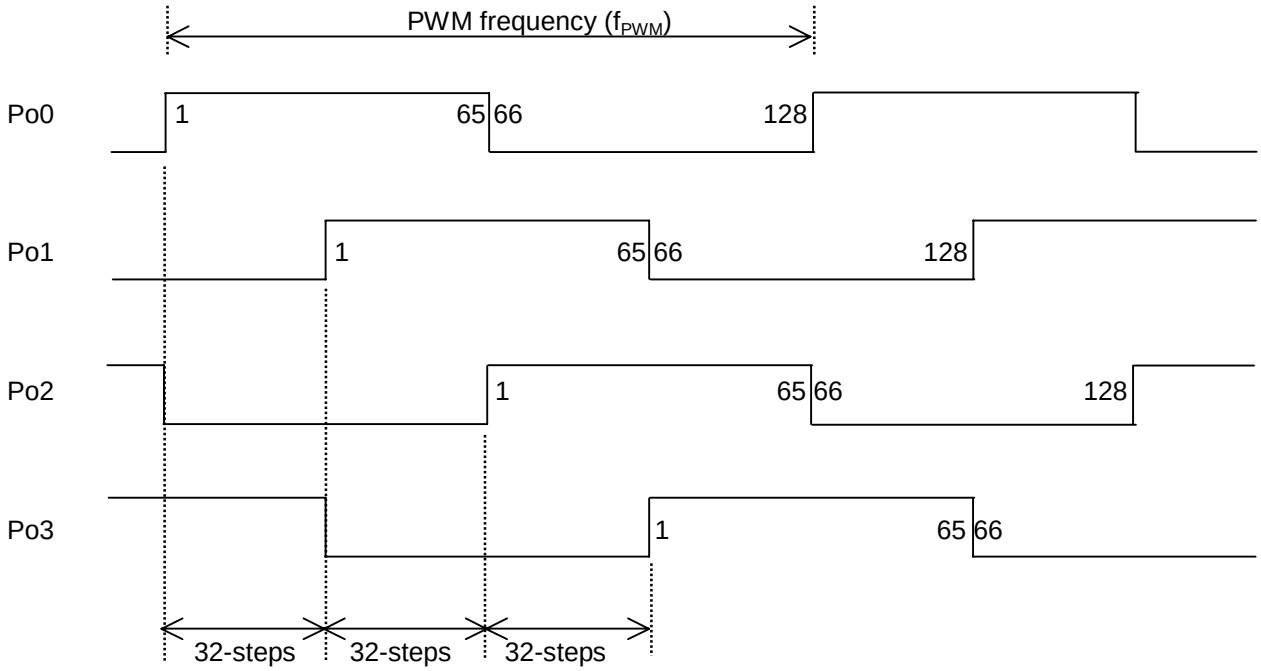
The PWM duty is (Register + 1) / 128.

(*:Don't Care)

PWMEN	PWM 6	PWM 5	PWM 4	PWM 3	PWM 2	PWM 1	PWM 0	PWM DUTY	PWMEN	PWM 6	PWM 5	PWM 4	PWM 3	PWM 2	PWM 1	PWM 0	PWM DUTY
0	*	*	*	*	*	*	*	0/128	1	1	0	0	0	0	0	0	65/128
1	0	0	0	0	0	0	0	1/128		1	0	0	0	0	0	1	66/128
	0	0	0	0	0	0	1	2/128		1	0	0	0	0	1	0	67/128
	0	0	0	0	0	1	0	3/128		1	0	0	0	0	1	1	68/128
	0	0	0	0	0	1	1	4/128		1	0	0	0	1	0	0	69/128
	0	0	0	0	1	0	0	5/128		1	0	0	0	1	0	1	70/128
	0	0	0	0	1	0	1	6/128		1	0	0	0	1	1	0	71/128
	0	0	0	0	1	1	0	7/128		1	0	0	0	1	1	1	72/128
	0	0	0	0	1	1	1	8/128		1	0	0	1	0	0	0	73/128
	0	0	0	1	0	0	0	9/128		1	0	0	1	0	0	1	74/128
	0	0	0	1	0	0	1	10/128		1	0	0	1	0	1	0	75/128
	0	0	0	1	0	1	0	11/128		1	0	0	1	0	1	1	76/128
	0	0	0	1	0	1	1	12/128		1	0	0	1	1	0	0	77/128
	0	0	0	1	1	0	0	13/128		1	0	0	1	1	0	1	78/128
	0	0	0	1	1	0	1	14/128		1	0	0	1	1	1	0	79/128
	0	0	0	1	1	1	0	15/128		1	0	0	1	1	1	1	80/128
	0	0	0	1	1	1	1	16/128		1	0	1	0	0	0	0	81/128
	0	0	1	0	0	0	0	17/128		1	0	1	0	0	0	1	82/128
	0	0	1	0	0	0	1	18/128		1	0	1	0	0	1	0	83/128
	0	0	1	0	0	1	0	19/128		1	0	1	0	0	1	1	84/128
	0	0	1	0	0	1	1	20/128		1	0	1	0	1	0	0	85/128
	0	0	1	0	1	0	0	21/128		1	0	1	0	1	0	1	86/128
	0	0	1	0	1	0	1	22/128		1	0	1	0	1	1	0	87/128
	0	0	1	0	1	1	0	23/128		1	0	1	0	1	1	1	88/128
	0	0	1	0	1	1	1	24/128		1	0	1	1	0	0	0	89/128
	0	0	1	1	0	0	0	25/128		1	0	1	1	0	0	1	90/128
	0	0	1	1	0	0	1	26/128		1	0	1	1	0	1	0	91/128
	0	0	1	1	0	1	0	27/128		1	0	1	1	0	1	1	92/128
	0	0	1	1	0	1	1	28/128		1	0	1	1	1	0	0	93/128
	0	0	1	1	1	0	0	29/128		1	0	1	1	1	0	1	94/128
	0	0	1	1	1	0	1	30/128		1	0	1	1	1	1	0	95/128
	0	0	1	1	1	1	0	31/128		1	0	1	1	1	1	1	96/128
	0	0	1	1	1	1	1	32/128	1	1	1	0	0	0	0	0	97/128
	0	1	0	0	0	0	0	33/128		1	1	0	0	0	0	1	98/128
	0	1	0	0	0	0	1	34/128		1	1	0	0	0	1	0	99/128
	0	1	0	0	0	1	0	35/128		1	1	0	0	0	1	1	100/128
	0	1	0	0	0	1	1	36/128		1	1	0	0	1	0	0	101/128
	0	1	0	0	1	0	0	37/128		1	1	0	0	1	0	1	102/128
	0	1	0	0	1	0	1	38/128		1	1	0	0	1	1	0	103/128
	0	1	0	0	1	1	0	39/128		1	1	0	0	1	1	1	104/128
	0	1	0	0	1	1	1	40/128		1	1	0	1	0	0	0	105/128
	0	1	0	1	0	0	0	41/128		1	1	0	1	0	0	1	106/128
	0	1	0	1	0	0	1	42/128		1	1	0	1	0	1	0	107/128
	0	1	0	1	0	1	0	43/128		1	1	0	1	0	1	1	108/128
	0	1	0	1	0	1	1	44/128		1	1	0	1	1	0	0	109/128
	0	1	0	1	1	0	0	45/128		1	1	0	1	1	0	1	110/128
	0	1	0	1	1	0	1	46/128		1	1	0	1	1	1	0	111/128
	0	1	0	1	1	1	0	47/128		1	1	0	1	1	1	1	112/128
	0	1	0	1	1	1	1	48/128		1	1	1	0	0	0	0	113/128
	0	1	1	0	0	0	0	49/128		1	1	1	0	0	0	1	114/128
	0	1	1	0	0	0	1	50/128		1	1	1	0	0	1	0	115/128
	0	1	1	0	0	1	0	51/128		1	1	1	0	0	1	1	116/128
	0	1	1	0	0	1	1	52/128		1	1	1	0	1	0	0	117/128
	0	1	1	0	1	0	0	53/128		1	1	1	0	1	0	1	118/128
	0	1	1	0	1	0	1	54/128		1	1	1	0	1	1	0	119/128
	0	1	1	0	1	1	0	55/128		1	1	1	0	1	1	1	120/128
	0	1	1	0	1	1	1	56/128		1	1	1	1	0	0	0	121/128
	0	1	1	1	0	0	0	57/128		1	1	1	1	0	0	1	122/128
	0	1	1	1	0	0	1	58/128		1	1	1	1	0	1	0	123/128
	0	1	1	1	0	1	0	59/128		1	1	1	1	0	1	1	124/128
	0	1	1	1	0	1	1	60/128		1	1	1	1	1	0	0	125/128
	0	1	1	1	1	0	0	61/128		1	1	1	1	1	0	1	126/128
	0	1	1	1	1	0	1	62/128		1	1	1	1	1	1	0	127/128
	0	1	1	1	1	1	0	63/128		1	1	1	1	1	1	1	128/128
	0	1	1	1	1	1	1	64/128									

Example) Set output PWM waveform of Po0 to Po3 terminal, shown below:

- PWM phase set D_1=0,
- PWMEN=1,
- (PWM_6, PWM_5, PWM_4, PWM_3, PWM_2, PWM_1, PWM_0)=(1,0,0,0,0,0,0)



(n) General output port / Key scan output select

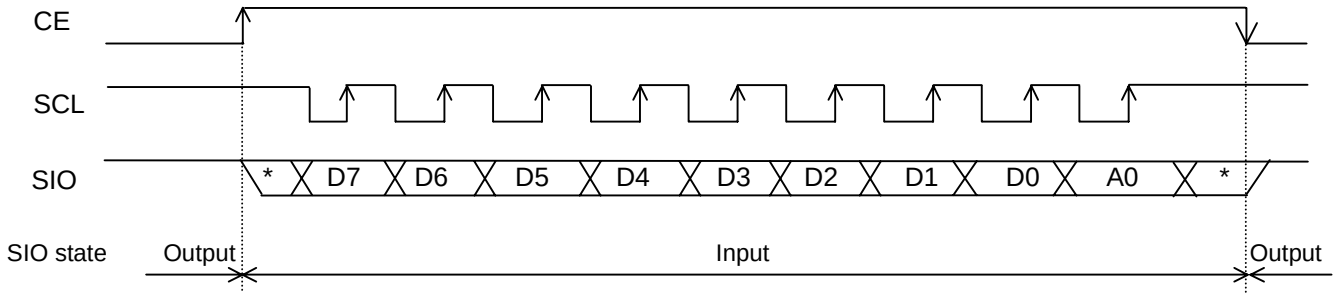
This instruction assigns function of general purpose output port or key scan output to Po3/S0 terminals.

A0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	1	0	0	0	D

D 0: General output port
1: Keyscan output

(3) Input Data Format and Timing

Data format is shown below.
When the CE terminal goes to “L”, I/F is data output.
When the CE terminal goes to “H” (rising edge) at SCL terminal “H”, I/F is data input.



NOTE1) Data fetched at SCL rising edge.
NOTE2) A contents change of the instruction and data which were written is fetched by the 9th rising edge of SCL.
NOTE3) When the instruction and data which were written are less than 9-bit, they are ignored and is not fetched.
NOTE4) When the instruction and data which were written are over 9-bit, the last 9-bit is valid.

(4) Power save mode set

Power save mode is set by “Power save mode set” instruction. The segment and common output "L" is outputted, the OSC terminal halts an oscillation (it oscillates at the time of key-on), and consumption current is decreased.

Power save mode is canceled, when normally set by "Power save mode set" instruction.

(5) Key scan circuit

Key scan circuit connects the 5 x 5 key-matrix maximum and reads the data of 25 keys maximum. It chooses the number of keys in key-matrix by “General output port / key scan output select” instruction.

It outputs a identified key data to MPU after comparison with two data read from the key-matrix in twice for reliable key operation. If those data are not identified, key data is not outputted. It outputs “L” signal through “SO” terminal as the request after 332T[s] (T=1/fsys=2/fosc,fsys : Internal system clock frequency) when any key is operated. Furthermore, the key scan circuit structures for reducing the external components like as Diodes to prevent circuit short problem.

(5-1) The relation between output data and key matrix

The relation between output data and key matrix shows bellow table and sets “1” signal for operated key.

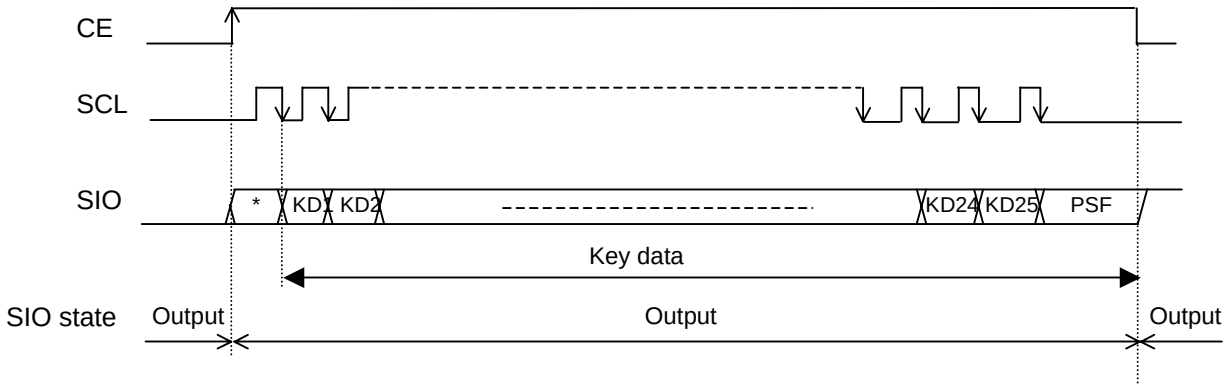
In case of 20 keys application, unassigned area for keys from KD1 to KD5 in bellow table take “0” signal.

In mode of Power save 1, area for keys from KD1 to KD20 in bellow table take “0” signal. In mode of Power save 2, area from KD1 to KD15 take “0” signal also. The terminals, which are not connected any keys, should be open.

	K_0	K_1	K_2	K_3	K_4
S_0	KD1	KD2	KD3	KD4	KD5
S_1	KD6	KD7	KD8	KD9	KD10
S_2	KD11	KD12	KD13	KD14	KD15
S_3	KD16	KD17	KD18	KD19	KD20
S_4	KD21	KD22	KD23	KD24	KD25

(5-2) Data output timing

The data output format shows bellow. The data output mode is set by “L” status of SCL terminal at the rising signal of CE terminal.

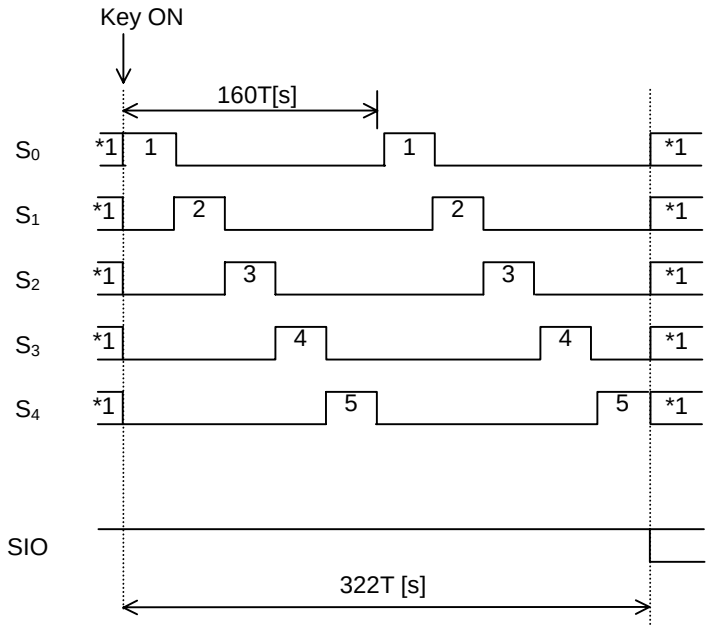


(5-3) Power save flag (PSF)

The status of Power save flag is outputted after KD25 in Key data reading. This flag sets “1” signal in mode of Power save in Key data reading and sets “0” in mode of Normal.

(5-4) Timing of Key scan

Key scan cycle is 160T[S] (T=1/fsys=2/fosc,fsys : Internal system clock frequency). The data of key scan is a result of comparison with a couple of Key scan for correct judge whether Key On or Off. When the result of comparison is correct (accord), the **NJU6538** recognizes Key On and outputs “L” level from SIO terminal after 322T[S] from start of Key scan for a request to read key data out to external MPU. When the SIO terminals outputs “L” signal, the key scan does not operate until end of key data reading by MPU, and scanned key data is kept. When the result of comparison is incorrect (not accord), Key scan operates again if any key is On. Therefore, Key scan may operate incorrectly in case of shorter period of Key on than 322T[S]



T=1/fsys =2/fosc

(fsys : Internal system clock frequency)

*1 Instruction set the General output ports or output the Key scan signals (refer (1)Instruction (n)General output port / Key scan select)

Key scan cycle and the timing of Key data read out request are constant in any Power save mode.

(5-5) Normal mode

Key scan operates with follows in normal mode.

1, Key scan signal output terminals S0 – S4 output "H" signals when key scan does not operate, and output key scan signals after start of key scan operation. The conditions of key scan signal input terminals K0 – K4 are "L" state with internal pull-down resistances, though "H" signal comes in to K0 – K4 corresponding to the turned on keys.

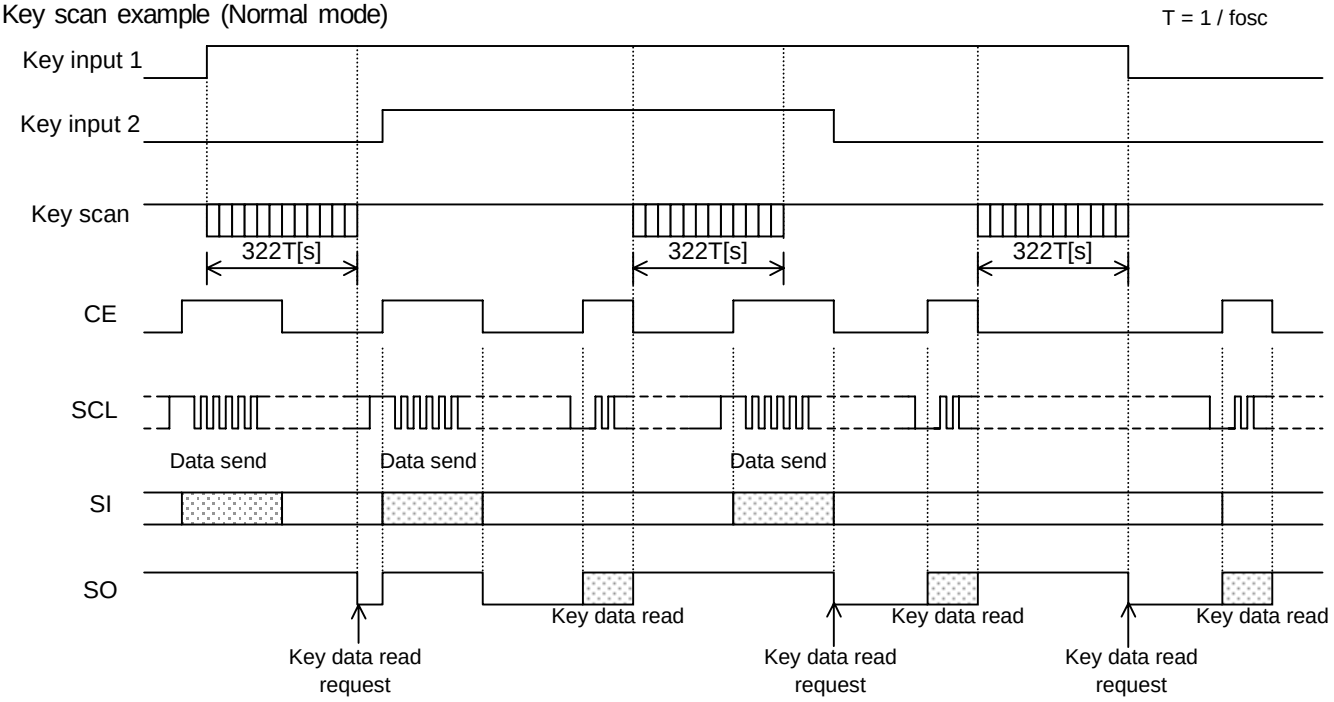
2, The function of key scan starts twice operations when any key is turned on. It stops when a couple of data by continuously twice key scan operations are accorded and fixed as a correct key status. It operates more 2 times when the key status is not fixed and any keys are still turning on. It repeats again and again until key status is fixed. The correct key status data is stored and newly key scan operation does not start until external MPU reads data out after key status is fixed.

3, When the key status is fixed, SO terminal outputs "L" signal as Key data read out request to MPU. MPU should read key data out at detection of this "L" signal.

4, The Key data read out request signal is released and SO terminal outputs "H" signal after finish of MPU key data read out for newly key scan operation.

SIO terminal requires pull up resistor because of Open drain type output. Multiple data of key are output in case of key more input so that MPU should process the data by itself.

Key scan example (Normal mode)



(5-6) Power save mode

Key scan operates with follows in Power save mode.

1, Key scan signal output terminals S0 – S4 output "H", "L" signals by the Power save mode set when key scan does not operate (refer the detail of instructions), and output key scan signals after start of key scan operation. The conditions of key scan signal input terminals K0 – K4 are "L" state with internal pull-down resistances, though "H" signal comes in to K0 – K4 corresponding to the turned on keys.

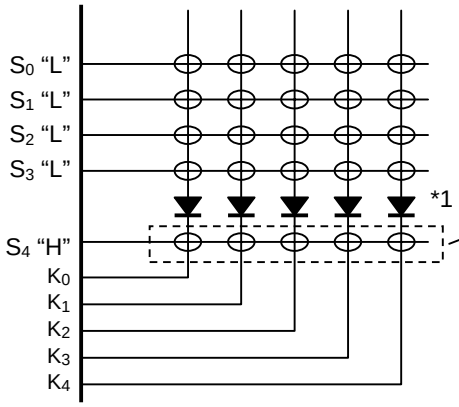
2, The oscillation circuit function of key scan starts twice operations when any keys on cross points with S0– S4 terminals line and K0 – K4 turned on. It stops when a couple of data by continuously twice key scan operations are accorded and fixed as a correct key status. It operates more 2 times when the key status is not fixed and any keys are still turning on. It repeats again and again until key status is fixed. The correct key status data is stored and newly key scan operation does not start until external MPU reads data out after key status is fixed.

3, When the key status is fixed, SIO terminal outputs "L" signal as Key data read out request to MPU. MPU should read key data out at detection of this "L" signal.

4, The Key data read out request signal is released and SIO terminal outputs "H" signal after finish of MPU key data read out for newly key scan operation. Although Power save mode is not released.

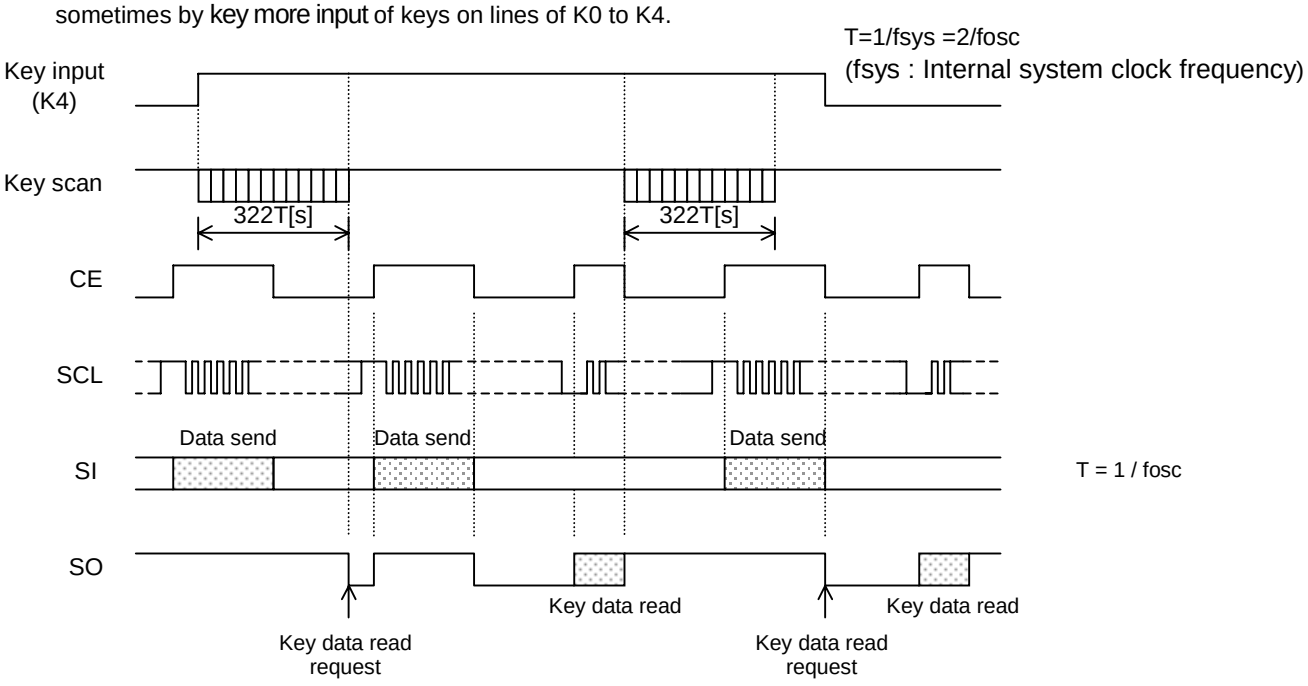
SIO terminal requires pull up resistor because of Open drain type output. Multiple data of key are output in case of key more input so that MPU should process the data by itself.

Key scan example (Power save mode)
Ex.) D0= "0", D1= "1" (K4="H" power save)



When some key on these lines are turned on, the oscillation starts and Key scan starts the operation until all of key are turned off.

*1 These diodes are required to recognize key more input of keys on the K4 line when only K4 terminal outputs "H" signal in power save mode as shown above example. In case of no diodes, incorrect key data may read out sometimes by key more input of keys on lines of K0 to K4.



(5-7) Key More Input

Key scan signal output terminal S0 to S4 output “H” level in state of Key More Input. Although Key state is detected without diodes to prevent unexpected key scan signal flow, non-pressed key data may change pressed key data in triple or more key Input as shown in Fig. 1 and incorrect key data may be output to external MPU. For prevention of miss-recognition by incorrect key data, diodes should be inserted in front of K0 – K4 terminals as shown in Fig. 3 or control program of MPU should ignore the combination of key data miss-recognition. For example, 4 keys and more ON data should be ignored.

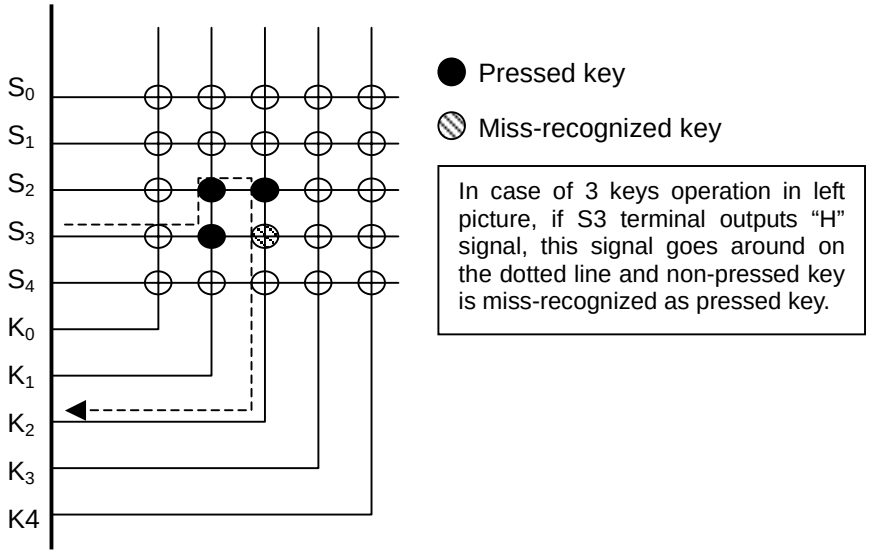


Fig. 1 Miss-recognized example by key more input

In modes of power save 1 (S0=0, S1=1 / Keys on only S5 line are valid) or power save 2 (S0=0, S1=1 / Keys on only S4 and S5 lines are valid), pay attention about the followings. When Key More Input is operated across the valid line and invalid, non-pressed key is miss-recognized as pressed key. However, Key data on the invalid line is not read out and 4 keys and more operation in the mean time are not ignored by MPU control program as shown in Fig. 2. In this case, diodes operate to prevent miss-recognition as shown in Fig. 3.

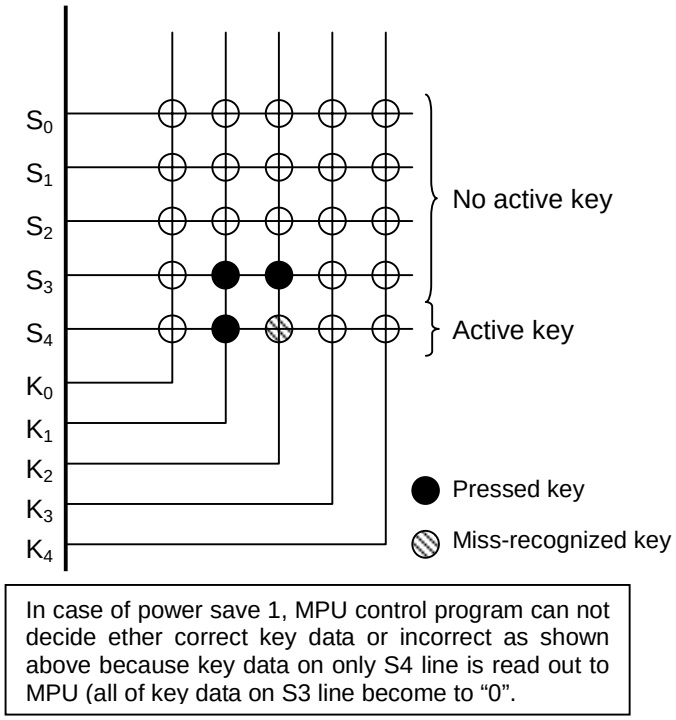


Fig. 2 Miss-recognition in power save 1

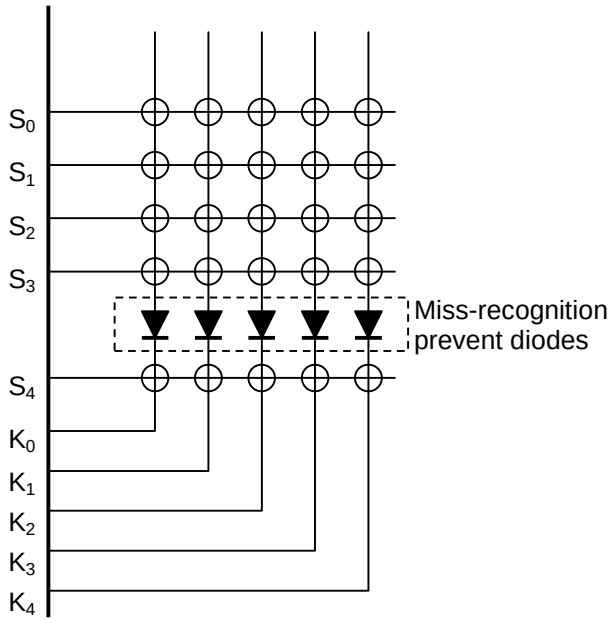


Fig. 3 Connect miss-recognition prevent diodes

(5-8) Key data reading out operation by external MPU

(a) Display data writing

Display data and an instruction change operate at the rising edge of 9-bit on SCL signal.

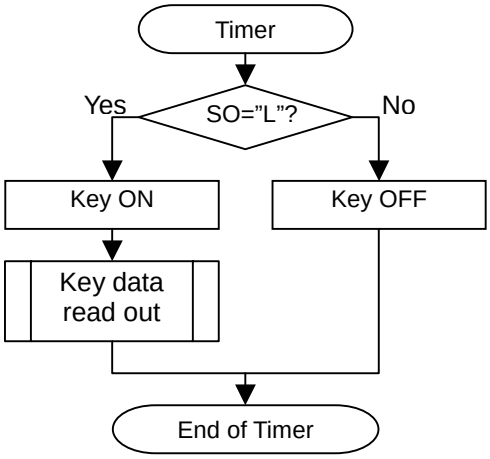
(b) Key data reading out operation

The minimum period from Key in to SIO terminal = “L” is 322T(t1) by key scan operation. When key scan operation performs again for key data fix preventing from noise or bouncing of key, the period from Key in to SIO terminal = “L” is 676T(t1). When the SIO terminal outputs “L”, the key scan operation is stopped after execution of key data reading out operation. Therefore, fixed key data is kept until end of key data reading out operation. When key data reading out operation is performed during SO terminal = “H”, both of key data from KD1 to KD25 and power save flag (PSF) are not outputted correctly.

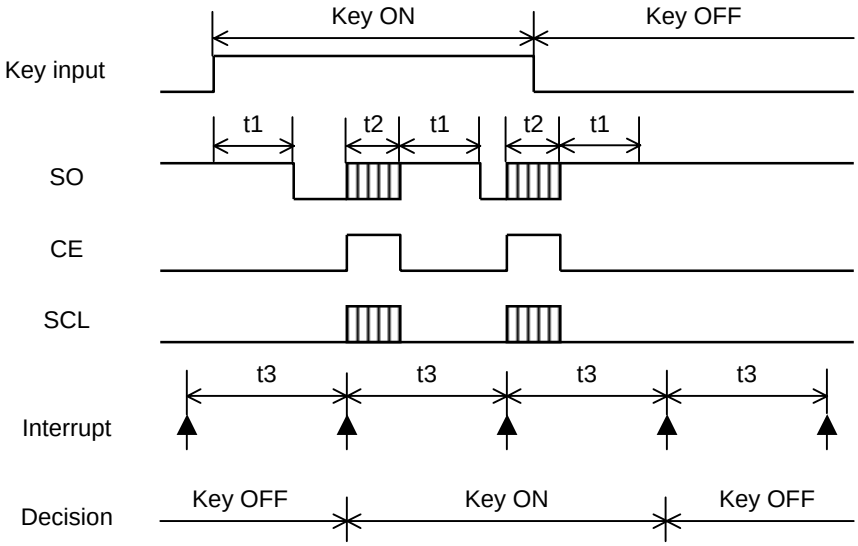
Key data reading out operation example

The flowchart below shows an example of timer interrupt application. When SIO terminal condition is “L” after check of SIO terminal condition at every timer interrupt operation, it is decided as Key In and key data reading out operation is performed. When SIO terminal condition is “H, it is decided as Key Off. For the correct decision of Key Off, the timer interrupt cycle (1/t3) should be expanded over the time added with [period of key scan (676T in case of measure against key bouncing of key) and [period of key data reading out operation (t2)]. In this time, the period of timer interrupt cycle (t3) must be set with enough margins including the range of fosc.

- Sequence of key data reading out operation



- Timing chart of key data reading out operation



t1: Key scan time
t2: Key data read time
t3: Interrupt cycle

*: t3 > t1 + t2

(6) Reset circuit initializes

Reset circuit initializes the **NJU6538** at Power ON and OFF. It generates reset signal to initialize the system at low VDD less than power down detection voltage (2.0V typical).

(6-1) Initial status in reset

1, Stop the oscillation circuit
2, Display Off (Available Serial data transmission)
3, Disable Key scan function
4, Filled "L" data in all of key data buffer

(6-2) The status of output port terminals in Reset

Output terminals	Reset status
SEG_1 to SEG_{65}	L
COM_1 to COM_{10}	L
Po0 to Po2	L
Po3/S_0	L *1
S_1 to S_4	H
SIO	H *2

*1 This terminal operates as segment driver and outputs "L".
*2 This terminal consisted of Open-drain output type circuit requires external pull-up resister connect ting to external power source for MPU. I f key data read is executed in power on reset, the read data is fixed as "H".

The reset circuit initializes the LSI to the following status by using of the input 10μs(min.) or over "L" level signal into the RESb terminal. The LSI will return to normal operation after about 1.0μs(max.) from the rising edge of the rest signal. The "Reset" instruction can't be substituted for the reset operation by using of the RESb terminal. It executes above-mentioned only 7 to 13 items.

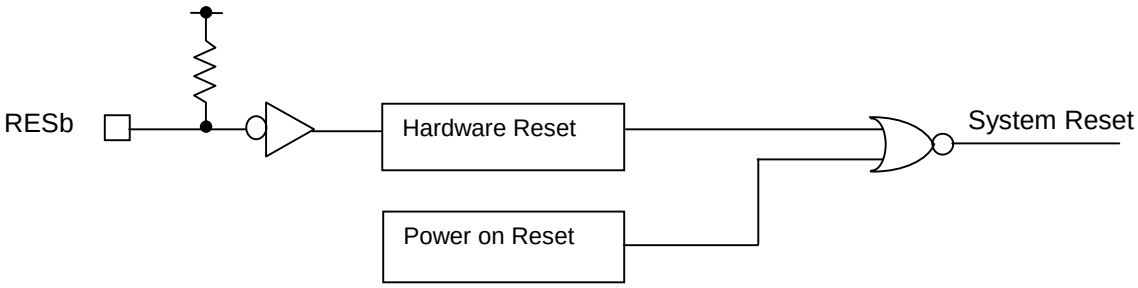
(6-3) Reset status using the RESb terminal (default)

1. Serial interface register clear
2. Display off
3. ADC select : D_0="0" (Normal mode)
4. Normal Display (Non-inverse display)
5. Whole display off : D_0="0" (Normal mode)
6. Power save mode : D_1, D_0="0, 0" (Normal mode)
7. Page address : 0 page
8. Column address : 00_H
9. EVR register : D_3, D_2, D_1, D_0="1, 1, 1, 1"
10. Duty select : 1/10 Duty
11. General output port PWM phase and frequency : D_1, D_0="0, 0"
12. General output port : PWMEN=0 ("L" output),
    PWM value : D_6, D_5, D_4, D_3, D_2, D_1, D_0="0, 0, 0, 0, 0, 0, 0"
13. Po3/S0 terminal : D_0=" 0" (Po3)

(6-4) Initialization by Hardware

The **NJU6538** incorporates reset terminal to initialize the all system. When the "L" level signal input over then 10us(min.) to the RESb terminal, reset sequence is executed. In this time, internal busy during 1us after RESb terminal goes to "H".

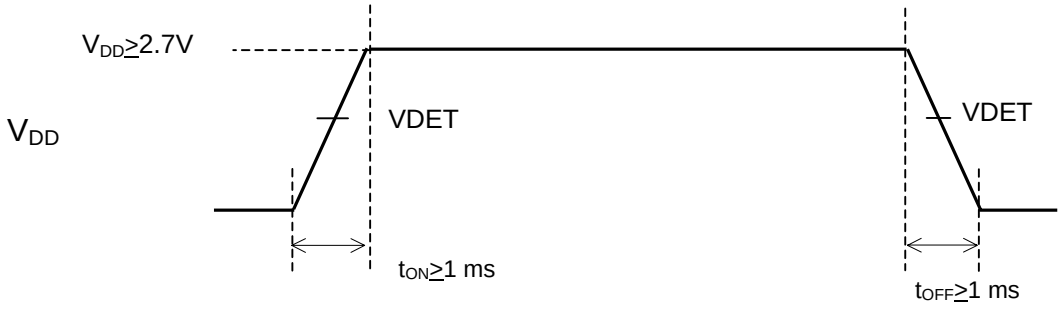
Reset circuit



(6-5) Power on reset operation

When the voltage rising time of power source is over than 1mS, the generated signal of VDET initializes the system of **NJU6538** as reset. When the voltage falling time of power source is over than 1ms, the system is also reset.

When these voltage rising or falling time of power source are not over than 1ms, the Initialization operation as reset does not operate correctly.



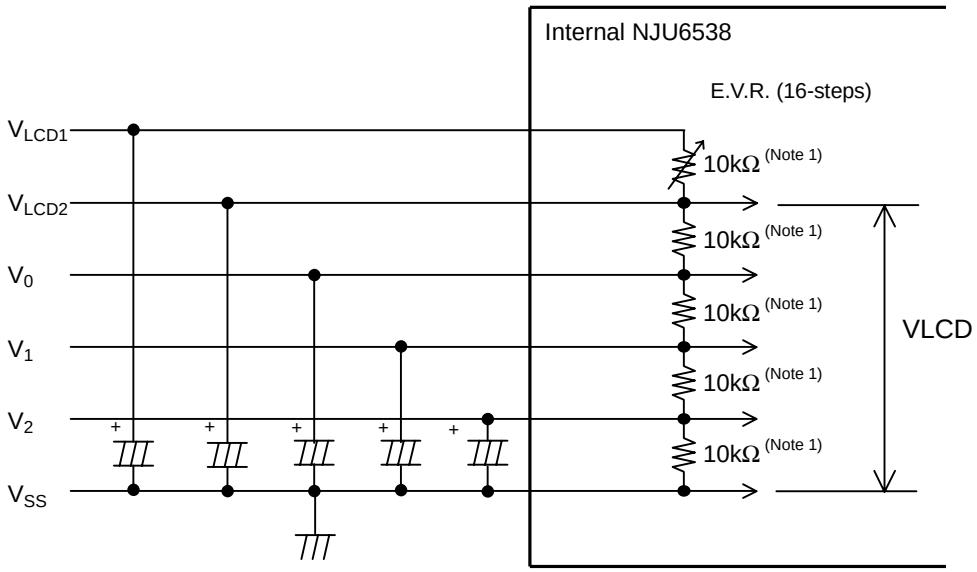
(7) LCD panel drive

(7-1) LCD driving voltage generation circuit

LCD driving voltage generation circuit generates LCD driving bias voltages V_{LCD2}, V0, V1 and V2. It adjusts the voltage by 8 steps electrical volume from V_{LCD1} and allots the voltage to V_{LCD2}, V0, V1 and V2 by resistor-voltage-dividing as shown in below.

VLCD1, VLCD2, V0, V1 and V2 terminals requires external capacitors for bias voltage stabilization for display quality. These values of capacitors should be fixed in accordance with evaluation in the application.

Power Supply	Duty ratio	1/8,1/9,1/10
	Bias	1/4
V_{LCD}		V_{LCD2}-V_{SS}



Note 1 : Resistor is typical value.

■ ABSOLUTE MAXIMUM RATINGS

Ta=25°C

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply voltage	VDD max	V_{DD} terminal	-0.3 to +7.0	V
	VLCD max	V_{LCD1} terminal	-0.3 to +11.0	
Input terminal voltage	V_{IN1}	OSC, K_0 to K_4,CE, SCL, SIO terminal	-0.3 to VDD+0.3	V
	V_{IN2}	V_{LCD2}, V_0 to V_2 terminal	-0.3 to VLCD+0.3	
Output terminal voltage	V_{OUT1}	SIO terminal	-0.3 to +6.0	V
	V_{OUT2}	OSC, SEG_1 to SEG_{65},COM_1 to COM_{10}, S_1 to S_4, Po_0 to Po_2, Po_3 /S_0 terminal	-0.3 to VDD+0.3	
Power dissipation	Pdmax	Ta=25°C QFP100-C2	1000	mW
		Ta=25°C QFP100-G1	700	
Storage temperature	Tstg	-	-55 to +125	°C
Operating temperature	Topr	-	-40 to +85	°C

Note 1) All voltage values are specified as V_{SS}=0V.

Note 2) If the LSI are used on condition beyond the absolute maximum rating, the LSI may be destroyed. Using LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the erectric characteristics conditions will cause malfunction and poor reliability.

Note 3) Decoupling capacitor should be connected between VDD and VSS due to the stabilized operation forthe voltage converter.

■ DC Electrical Characteristics

VDD=2.7 to 5.5V, Ta= - 40 to 85°C

PARAMETER	SYMBOL	CONDITION		MIN	TYP	MAX	UNIT	NOTE
Power supply (1)	VDD	VDD		2.7		5.5	V	
Power supply (2)	VLCD1	VLCD1		5.0		10.0		
Output voltage	VLCD2	VLCD2		4.0		VLCD1	V	
Input voltage	V0	V0		VSS	VLCD2x3/4	VLCD2	V	1
	V1	V1		VSS	VLCD2x2/4	VLCD2		
	V2	V2		VSS	VLCD2x1/4	VLCD2		
"H" level input voltage (1)	VIH(1)	K_0 to K_4		0.6VDD		VDD	V	
"H" level input voltage (2)	VIH(2)	SCL, SIO, CE		0.8VDD		VDD	V	
"L" level input voltage (1)	VIL(1)	K_0 to K_4, SCL, SIO, CE		0		0.2VDD	V	
Hysteresis voltage	VH	SCL, SIO, CE			0.25VDD		V	
"H" level input current	I_{IH}	SCL, SIO, CE,	V_{IN} = VDD			5.0	μA	
"L" level input current	I_{IL}	SCL, SIO, K_0 to K_4, CE,	V_{IN} = 0V	-5.0			μA	
Pull-up resistance	R_{PU}	RESb VDD=5.0V,	V_{IN} = 0V	50	150	250	kΩ	
Pull-down resistance	R_{PD}	K_0 to K_4, VDD=5.0V,	V_{IN} = VDD	50	150	250	kΩ	
Output off-leak current	IOFFH	SIO, VO=5.5V				6.0	μA	
"H" level output voltage (1)	VOH(1)	S_0 to S_4	VDD=5.0V, Io = -500uA	VDD-1.2		VDD-0.2	V	
			VDD=3.0V, Io = -250uA	VDD-1.1		VDD-0.1		
"H" level output voltage (2)	VOH(2)	Po_0 to Po_3	VDD=5.0V, Io = -10mA	VDD-1.0			V	
			VDD=3.0V, Io = -5mA	VDD-0.6				
"L" level output voltage (1)	VOL(1)	S_0 to S_4	VDD=5.0V, Io = 25μA	0.2		1.5	V	
			VDD=3.0V, Io = 5μA	0.05		0.6		
"L" level output voltage (2)	VOL(2)	Po_0 to Po_3	VDD=5.0V, Io = 10mA			1.0	V	
			VDD=3.0V, Io = 5mA			0.6		
"L" level output voltage (3)	VOL(3)	SIO	Io = 1mA			0.5	V	
Driver ON-resistance (COM)	R_{COM}	Ta=25°C, VO=V_{LCD2},VSS,V0,V2 ±Id=1μA (COM terminal)				40	kΩ	2
Driver ON-resistance (SEG)	R_{SEG}	Ta=25°C, VO=V_{LCD2},VSS,V1 ±Id=1μA (SEG terminal)				40	kΩ	2
Oscillation Frequency	f_{OSC}	Ta=25°C, VDD=5.0V R_{OSC}=150kΩ		38	50	62	kHz	
LCD Driving voltage	V0	E.V.R. value "0,0,0,0" V_{LCD1}=8.0V		5.8	6.0	6.2	V	
	V1			3.8	4.0	4.2		
	V2			1.8	2.0	2.2		
Bleeder resistance	R_B	VLCD2-VSS, Ta=25°C			40		kΩ	
E.V.R. resistance	R_{EVR}	VLCD1-VLCD2, Ta=25°C			10		kΩ	
Power down detect voltage	VDET			0.8	1.4	2.0	V	
Reset time	Tr	RESb		1.0			μs	
Reset "L" pulse width	Trw	RESb		10.0			μs	
Operating current	IDD1	Power save mode				100	μA	
	IDD2	VDD=5.5V, Output open f_{OSC}=50kHz,				500	μA	
	ILCD1	Power save mode				5	μA	
	ILCD2	VLCD1=10.0V Output open f_{OSC}=50kHz,				1000	μA	

Note 1) The relation : VLCD1≥VLCD2≥V0≥V1≥V2≥VSS must be maintained.

Note 2) RCOM and RSEG are the resistance values between power supply terminals (VSS, VLCD2, or V0, V1, V2) and each common terminal, and supply voltage (VSS, VLCD2, or V0, V1, V2) and each segment terminal respectively, and measured when the current Id is flown on every common and segment terminals at a same time.

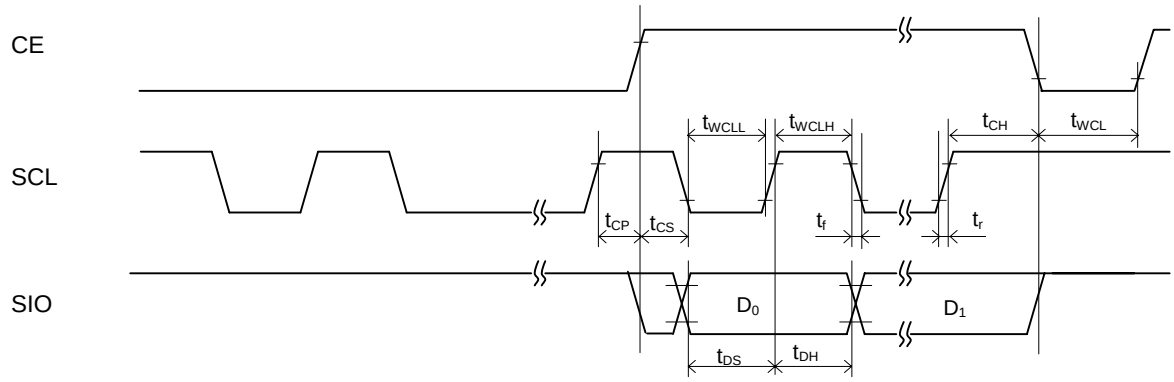
■ AC Characteristics

VDD=2.7 to 5.5V, Ta= - 40 to 85°C

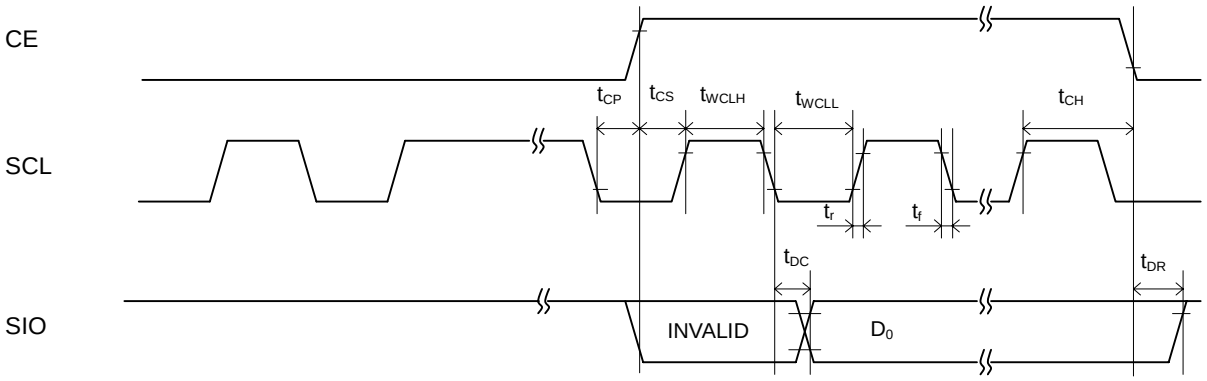
PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT	NOTE
"L" level clock pulse width	t_{WCLL}	SCL	160			ns	
"H" level clock pulse width	t_{WCLH}	SCL	160			ns	
Data setup time	t_{DS}	SCL, SIO	160			ns	
Data hold time	t_{DH}	SCL, SIO	160			ns	
CE wait time	t_{CP}	CE, SCL	160			ns	
CE setup time	t_{CS}	CE, SCL	160			ns	
CE hold time	t_{CH}	CE, SCL	160			ns	
CE "L" level width	t_{WCL}	CE	160			ns	
SIO output delay time	t_{DC}	SIO, Rpu=4.7kΩ, CL=10pF			1.5	µs	1
SIO rise time	t_{DR}	SIO, Rpu=4.7kΩ, CL=10pF			1.5	µs	
SCL rise tine	t_r				15	ns	
SCL fall time	t_f				15	ns	

SO terminal is Open-Drain type output, so that the characteristics of SO terminal are changed by values of pull-up resistance Rpu and CL.

(1) Write operation

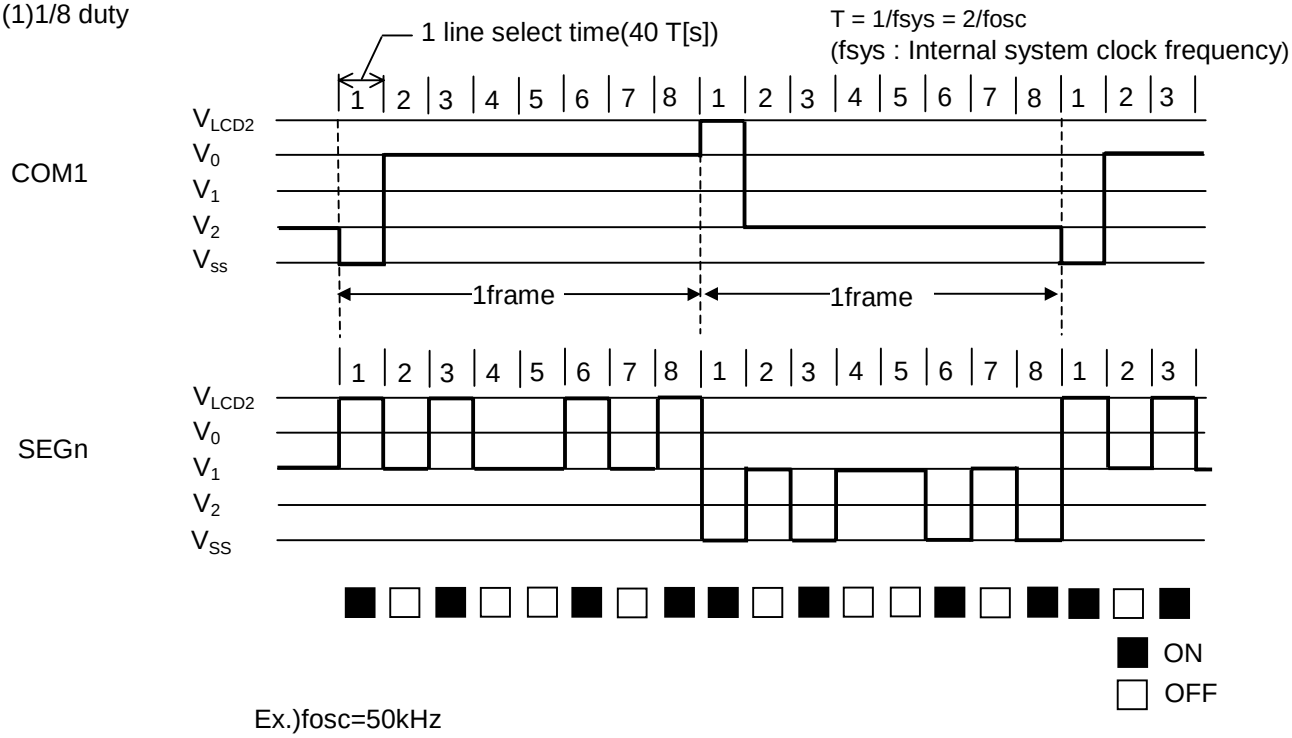


(2) Key data read operation



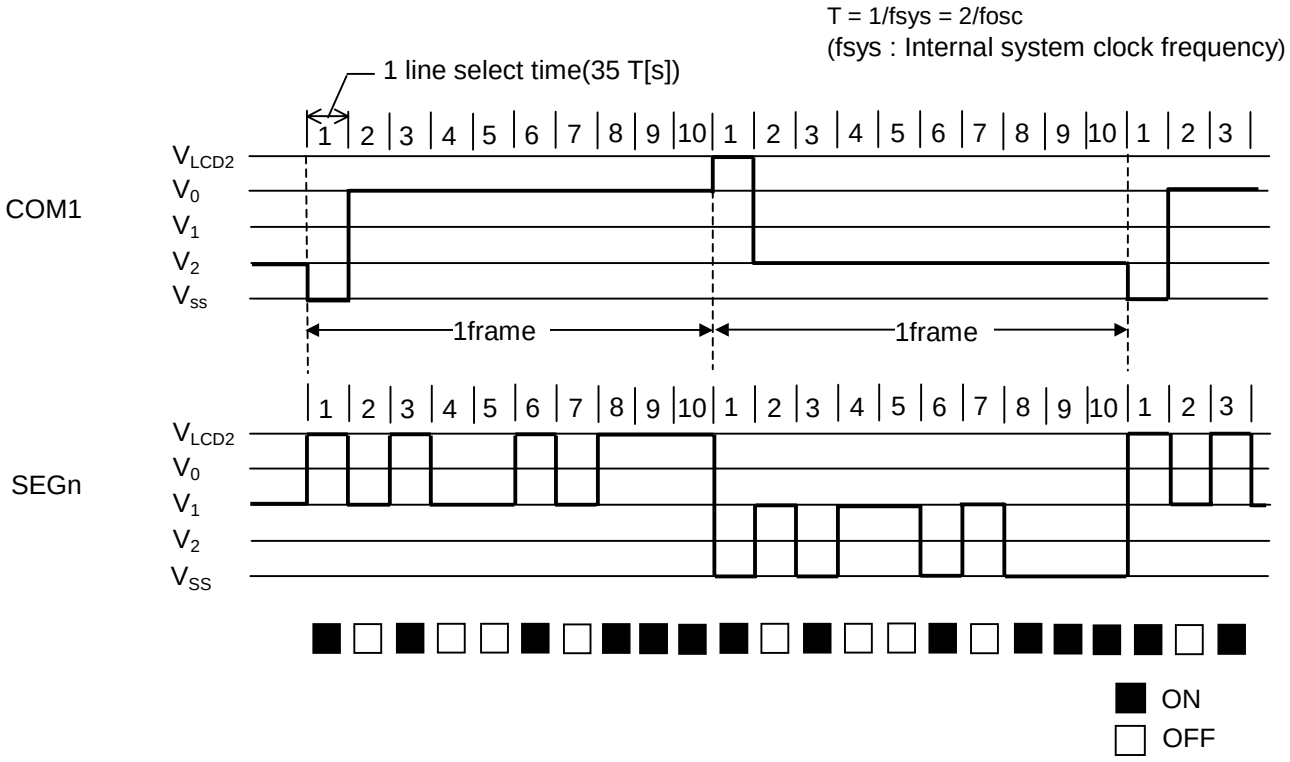
Relation between oscillation frequency and LCD frame frequency

(1)1/8 duty



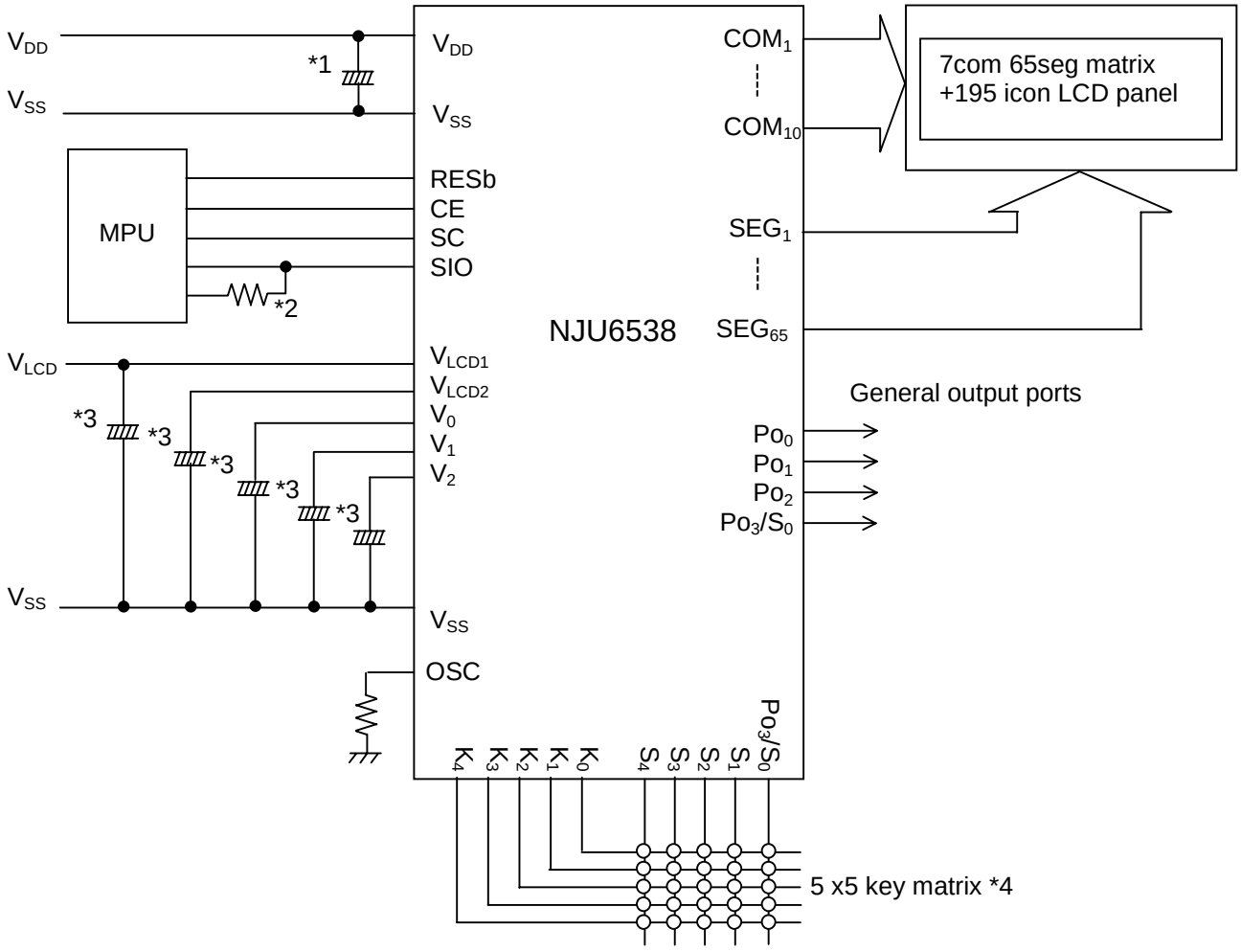
Ex.)fosc=50kHz
Frame frequency =1/(40T x duty)=1/(40 x (2/50kHz) x 8)=78.1(Hz)

(2)1/10 duty



fosc=50kHz
Frame frequency =1/(35T x duty)=1/(35 x (2/50kHz) x 10)=71.4(Hz)

■ APPLICATION CIRCUIT



*1 The rising time of Power source voltage at Power on and the falling time at Power off must keep over than 1ms because of Voltage detection type Reset circuit operation.

*2 SO terminal requires external pull-up resistor connecting to Power source of external MPU because of Open-drain type output.

*3 This capacitor for bias voltage stabilization should be connected in accordance with display quality in application.

*4 P_{O3} / S_0 terminal is general output ports and Key scan signal output duplicated-function terminals. A function must be selected either Segment output or other.