24-CHARACTER 2-LINE DOT MATRIX LCD CONTROLLER DRIVER

■ GENERAL DESCRIPTION

The NJU6406B is a 1 Chip Dot Matrix LCD controller driver for up to 24-character 2-line display.

It contains voltage converter, microprocessor interface circuits, instruction decoder controller, character generator ROM/RAM and high voltage operation common and segment drivers.

The voltage converter generates about twofold voltage (10V or 6V) from single power supply (5V or 3V). Consequently, high-contrast display can be performed though the simple power supply circuits.

The microprocessor interface circuits which operate 2MHz frequency, can be connected directly to 4bit/8bit microprocessor.

The character generator consists of 9,600bits ROM and 64 bytes RAM. The standard version ROM is coded with 240 characters including capital and small letter fonts and some of Japanese fonts.

The high voltage operation 32-common and 60-segment drivers operate by 13.5V or 12V, and drives up to 24-character 2-line LCD panels which divided four common electrode blocks.

■ PACKAGE OUTLINE

NJU6406BC

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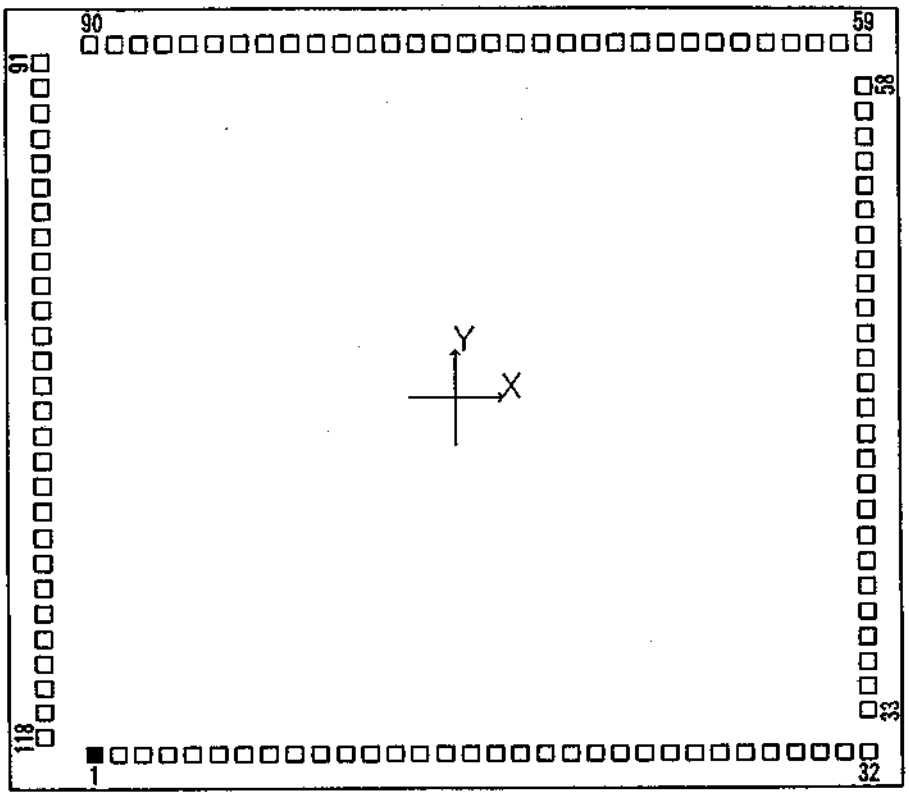
■ FEATURES

- 24-character 2-line Dot Matrix LCD Controller Driver
- 4/8 Bit Microprocessor Direct Interface
- Display Data RAM - 80 x 8 bits ; Maximum 24-character 2-line Display
- Character Generator ROM - 9,600 bits ; 240 Characters for 5 x 7 Dots
- Character Generator RAM - 64 x 8 bits ; 8 Patterns(5x7 Dots)
- Microprocessor can access to Display Data RAM and Character Generator RAM
- High Voltage LCD Driver ; 32-common / 60-segment
- Programmable Duty Ratio ;
  1/16 Duty for 5x 7 Dots + Cursor, 1 Line
  1/32 Duty for 5x 7 Dots + Cursor, 2 Lines
- Number of Maximum Display Characters

Display Line	Duty	Font	Max. Disp. Characters
1 Line	1/16 duty	5 x 7 dots + cursor	24-character 1-line
2 Lines	1/32 duty	5 x 7 dots + cursor	24-character 2-line

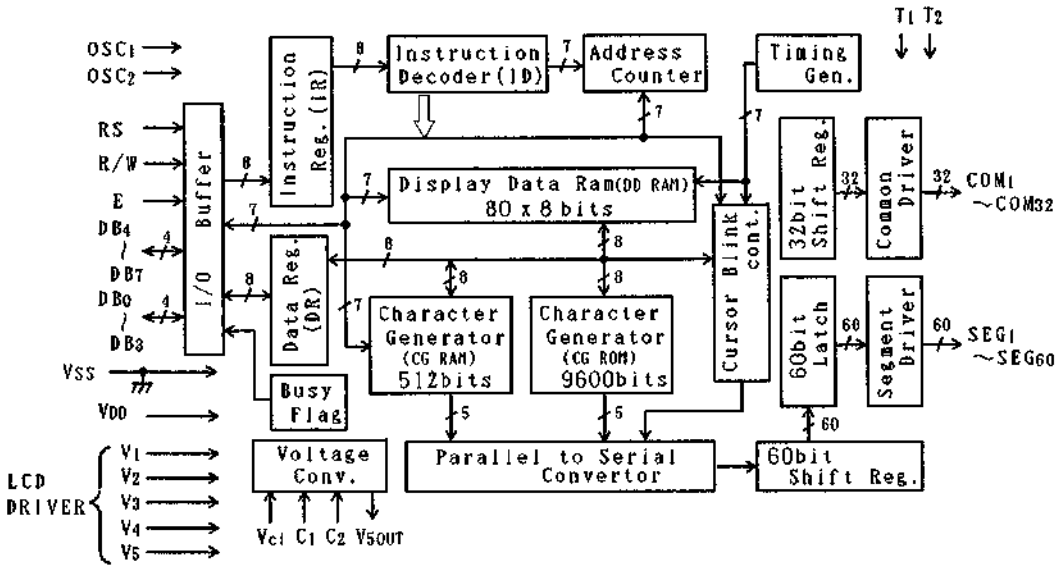
- Useful Instruction Set
  Clear Display, Return Home, Display ON/OFF Cont, Cursor ON/OFF Cont, Display Blink, Cursor Shift, Character Shift
- Power On Initialize On-chip
- Voltage Converter On-chip
- Oscillation Circuit On-chip(External R or Ceramic Resonator required)
- Low Power Consumption
- Operating Voltage --- + 5 V / + 3 V
- Package Outline --- Chip / Bumped Chip
- C-MOS Technology

■ PAD LOCATION



Chip Size : X = 5.73mm , Y = 5.00mm
Chip Thickness : 400um ± 30um
Pad Size : 100um × 100um

■ BLOCK DIAGRAM



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■ COORDINATES

Chip Size X = 5.73mm , Y = 5.00mm
Chip Thickness : 400um ± 30um

Chip Center : X = 0um, Y = 0um

No	Pad Name	X (um)	Y (um)	No	Pad Name	X (um)	Y (um)	No	Pad Name	X (um)	Y (um)
1	SEG_{45}	-2320	-2275	41	V_{5OUT}	2640	- 720	81	SEG_7	- 880	2275
2	SEG_{46}	-2160	-2275	42	C_1	2640	- 560	82	SEG_8	-1040	2275
3	SEG_{47}	-2000	-2275	43	C_2	2640	- 400	83	SEG_9	-1200	2275
4	SEG_{48}	-1840	-2275	44	V_{c1}	2640	- 240	84	SEG_{10}	-1360	2275
5	SEG_{49}	-1680	-2275	45	V_{DD}	2640	- 80	85	SEG_{11}	-1520	2275
6	SEG_{50}	-1520	-2275	46	RS	2640	80	86	SEG_{12}	-1680	2275
7	SEG_{51}	-1360	-2275	47	R/W	2640	240	87	SEG_{13}	-1840	2275
8	SEG_{52}	-1200	-2275	48	E	2640	400	88	SEG_{14}	-2000	2275
9	SEG_{53}	-1040	-2275	49	DB_0	2640	560	89	SEG_{15}	-2160	2275
10	SEG_{54}	- 880	-2275	50	DB_1	2640	720	90	SEG_{16}	-2320	2275
11	SEG_{55}	- 720	-2275	51	DB_2	2640	880	91	SEG_{17}	-2640	2160
12	SEG_{56}	- 560	-2275	52	DB_3	2640	1040	92	SEG_{18}	-2640	2000
13	SEG_{57}	- 400	-2275	53	DB_4	2640	1200	93	SEG_{19}	-2640	1840
14	SEG_{58}	- 240	-2275	54	DB_5	2640	1360	94	SEG_{20}	-2640	1680
15	SEG_{59}	- 80	-2275	55	DB_6	2640	1520	95	SEG_{21}	-2640	1520
16	SEG_{60}	80	-2275	56	DB_7	2640	1680	96	SEG_{22}	-2640	1360
17	COM_9	240	-2275	57	T2	2640	1840	97	SEG_{23}	-2640	1200
18	COM_{10}	400	-2275	58	T1	2640	2000	98	SEG_{24}	-2640	1040
19	COM_{11}	560	-2275	59	COM_{24}	2640	2275	99	SEG_{25}	-2640	880
20	COM_{12}	720	-2275	60	COM_{23}	2480	2275	100	SEG_{26}	-2640	720
21	COM_{13}	880	-2275	61	COM_{22}	2320	2275	101	SEG_{27}	-2640	560
22	COM_{14}	1040	-2275	62	COM_{21}	2160	2275	102	SEG_{28}	-2640	400
23	COM_{15}	1200	-2275	63	COM_{20}	2000	2275	103	SEG_{29}	-2640	240
24	COM_{16}	1360	-2275	64	COM_{19}	1840	2275	104	SEG_{30}	-2640	80
25	COM_{25}	1520	-2275	65	COM_{18}	1680	2275	105	SEG_{31}	-2640	- 80
26	COM_{26}	1680	-2275	66	COM_{17}	1520	2275	106	SEG_{32}	-2640	- 240
27	COM_{27}	1840	-2275	67	COM_8	1360	2275	107	SEG_{33}	-2640	- 400
28	COM_{28}	2000	-2275	68	COM_7	1200	2275	108	SEG_{34}	-2640	- 560
29	COM_{29}	2160	-2275	69	COM_6	1040	2275	109	SEG_{35}	-2640	- 720
30	COM_{30}	2320	-2275	70	COM_5	880	2275	110	SEG_{36}	-2640	- 880
31	COM_{31}	2480	-2275	71	COM_4	720	2275	111	SEG_{37}	-2640	-1040
32	COM_{32}	2640	-2275	72	COM_3	560	2275	112	SEG_{38}	-2640	-1200
33	V_{SS}	2640	-2000	73	COM_2	400	2275	113	SEG_{39}	-2640	-1360
34	OSC_1	2640	-1840	74	COM_1	240	2275	114	SEG_{40}	-2640	-1520
35	OSC_2	2640	-1680	75	SEG_1	80	2275	115	SEG_{41}	-2640	-1680
36	V_1	2640	-1520	76	SEG_2	- 80	2275	116	SEG_{42}	-2640	-1840
37	V_2	2640	-1360	77	SEG_3	- 240	2275	117	SEG_{43}	-2640	-2000
38	V_3	2640	-1200	78	SEG_4	- 400	2275	118	SEG_{44}	-2640	-2160
39	V_4	2640	-1040	79	SEG_5	- 560	2275	-	--	-	-
40	V_5	2640	- 880	80	SEG_6	- 720	2275	-	--	-	-

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■ TERMINAL DESCRIPTION

NO.	SYMBOL	F U N C T I O N
36~40	V_1~V_5	LCD Driving Power Source
45	V_{DD}	Power Source (+ 5V / + 3V)
33	V_{SS}	Power Source (0V)
34,35	OSC_1, OSC_2	Oscillation Terminals; External R or Ceramic Resonator connect to these terminals. For external clock operation, the clock should be input on OSC_1.
46	RS	Register selection signal input "0" : Instruction Register (Writing) Busy Flag (Reading) "1" : Data Register (Writing/Reading)
47	R/W	Read/Write selection signal input "0" : Write , "1" : Read
48	E	Read/Write activation signal input
53~56	DB_4~DB_7	3-state Data Bus(Upper) to transfer the data between MPU and NJU6406B DB_7 is also used for the Busy Flag reading
49~52	DB_0~DB_3	3-state Data Bus(Lower) to transfer the data between MPU and NJU6406B These bus are not used in the 4bit operation
74~67 17~24 66~59 25~32	COM_1 ~COM_8 COM_9 ~COM_{16} COM_{17}~COM_{24} COM_{25}~COM_{32}	LCD Common driving signal No use terminals output no-active signal, or COM_{17}~COM_{32} output no-active signal in the 1/16 duty operation.
75~118 1~16	SEG_1 ~SEG_{44} SEG_{45}~SEG_{80}	LCD Segment driving signal
42,43	C_1 , C_2	Capacitor for Voltage Doubler Connecting Terminal (+) Capacitor for Voltage Doubler Connecting Terminal (-)
44	V_{ci}	Input Terminal for Voltage Doubler (Normally $V_{ci} = V_{DD}$)
41	V_{Sout}	Voltage Doubler Output Terminal
58	T1	Maker Testing Terminal (Normally Open)
57	T2	Maker Testing Terminal (Normally Open)

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■ FUNCTIONAL DESCRIPTION

(1) Description for each blocks

(1－1) Register

The NJU6406B incorporates two 8-bit registers, an Instruction Register(IR) and a Data Register(DR).

The Register(IR) stores instruction codes such as "Clear Display" and "Return Home", and address data for Display Data RAM (DD RAM) and Character Generator RAM(CG RAM). The MPU can write the instruction code and address data to the Register(IR), but it cannot read out from the Register(IR).

The Register (DR) is a temporary stored register, the data stored in the Register (DR) is written into the DD RAM or CG RAM and read out from the DD RAM or CG RAM.

The data in the Register(DR) written by the MPU is transferred automatically to the DD RAM or CG RAM by internal operation.

When the address data for the DD RAM or CG RAM is written into the Register(IR), the addressed data in the DD RAM or CG RAM is transferred to the Register(DR). By the MPU read out the data in the Register(DR), the data transmitting process is performed completely.

After reading the data in the Register(DR) by the MPU, the next address data in the DD RAM or CG RAM is transferred automatically to the Register(DR) to provide for the next MPU reading.

These two registers are selected by the selection signal RS as shown below:

Table 1. shows register operation controlled by RS and R/W signals.

Table 1. Register Operation

RS	R/W	Selected Register	Operation
0	0	IR	Write
0	1		Read busy flag(DB_7) and address counter(DB_0~DB_6)
1	0	DR	Write (DR to DD or CG RAM)
1	1		Read (DD or CG RAM to DR)

(1－2) Busy Flag (BF)

When the internal circuits are in the operation mode, the busy flag is "1", and any instruction reading is inhibited.

The busy flag (BF) is output at DB_7 when RS="0" and R/W="1" as shown in table 1.

The next instruction should be written after busy flag (BF) goes to "0".

(1－3) Address Counter (AC)

The address Counter(AC) addressing the DD RAM and CG RAM.

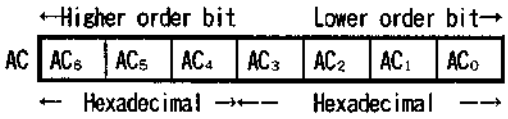
When the address setting instruction is written into the Register(IR), the address information is transferred from Register(IR) to counter(AC). The selection of either the DD RAM or CG RAM is also determined by this instruction.

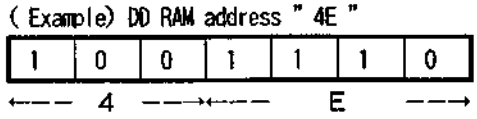
After writing (or reading) the display data to (or from) the DD RAM or CG RAM, the Counter (AC) increments (or decrements) automatically.

The address data in the Counter(AC) is output from DB_6~DB_0 when RS="0" and R/W="1" as shown in Table 1.

(1－4) Display Data RAM (DD RAM)

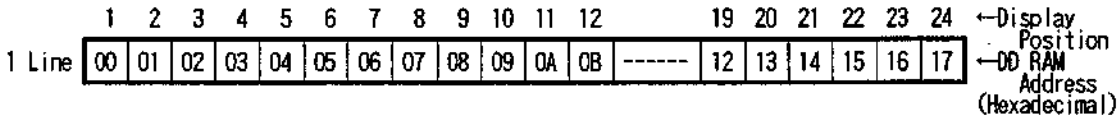
The display data RAM(DD RAM) consists of 80 x 8 bits, stores up to 80-character display data represented in 8-bit code.
The unused display data memory area in the DD RAM can be used as a general data memory area.
The DD RAM address data set in the address Counter(AC) is represented in Hexadecimal.





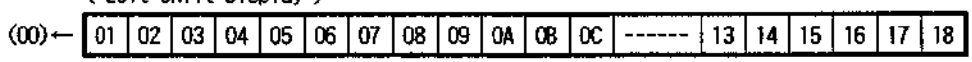
(1－4－1) 1-line Display (Function set code N=0)

(a) 24-character 1-line Display Example
The relation between DD RAM address and display position on the LCD is shown below:

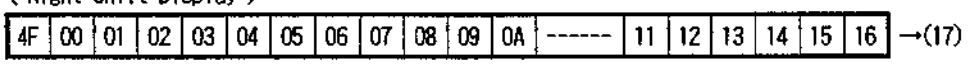


When the display shift is performed, the DD RAM address changes as follows:

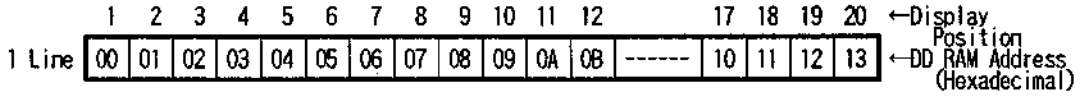
(Left Shift Display)



(Right Shift Display)

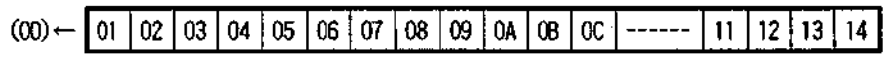


(b) 20-character 1-line Display Example
The relation between DD RAM address and display position on the LCD is shown below:

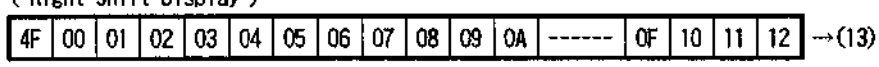


When the display shift is performed, the DD RAM address changes as follows:

(Left Shift Display)



(Right Shift Display)



(C) 12-character 1-line Display Example
The relation between DD RAM address and display position on the LCD is shown below:

	1	2	3	4	5	6	7	8	9	10	11	12	←Display Position
1 Line	00	01	02	03	04	05	06	07	08	09	0A	0B	←DD RAM Address (Hexadecimal)

When the display shift is performed, the DD RAM address changes as follows:

(Left Shift Display)

(00)←	01	02	03	04	05	06	07	08	09	0A	0B	0C

(Right Shift Display)

4F	00	01	02	03	04	05	06	07	08	09	0A	→(0B)

(1−4−2) 2-line Display (Function set code N=1)

(a) 24-character 2-line Display Example
The relation between DD RAM address and display position on the LCD is shown below:

	1	2	3	4	5	6	7	8	9	10	11	12		19	20	21	22	23	24	←Display Position
1st Line	00	01	02	03	04	05	06	07	08	09	0A	0B	------	12	13	14	15	16	17	← DD RAM Add.
2nd Line	40	41	42	43	44	45	46	47	48	49	4A	4B	------	52	53	54	55	56	57	← (Hexadecimal)

Note : In the 2 lines display mode, the 1st line and 2nd address are defined as $(00)_H$ to $(27)_H$ and $(40)_H$ to $(67)_H$. Please note that the end of 1st line address and the beginning of 2nd line address are not consecutive.

When the display shift is performed, the DD RAM address changes as follows:

(Left Shift Display)

(00)←	01	02	03	04	05	06	07	08	09	0A	0B	0C	------	13	14	15	16	17	18
(40)←	41	42	43	44	45	46	47	48	49	4A	4B	4C	------	53	54	55	56	57	58

(Right Shift Display)

27	00	01	02	03	04	05	06	07	08	09	0A	------	11	12	13	14	15	16	→(17)
67	40	41	42	43	44	45	46	47	48	49	4A	------	51	52	53	54	55	56	→(57)

(b) 20-character 2-line Display Example
The relation between DD RAM address and display position on the LCD is shown below:

	1	2	3	4	5	6	7	8	9	10	11	12		17	18	19	20	←Display Position
1st Line	00	01	02	03	04	05	06	07	08	09	0A	0B	------	10	11	12	13	← DD RAM Address
2nd Line	40	41	42	43	44	45	46	47	48	49	4A	4B	------	50	51	52	53	← (Hexadecimal)

When the display shift is performed, the DD RAM address changes as follows:
(Left Shift Display)

(00)←	01	02	03	04	05	06	07	08	09	0A	0B	0C	------	11	12	13	14
(40)←	41	42	43	44	45	46	47	48	49	4A	4B	4C	------	51	52	53	54

(Right Shift Display)

27	00	01	02	03	04	05	06	07	08	09	0A	------	0F	10	11	12	→(13)
67	40	41	42	43	44	45	46	47	48	49	4A	------	4F	50	51	52	→(53)

(C) 12-character 2-line Display Example
The relation between DD RAM address and display position on the LCD is shown below:

	1	2	3	4	5	6	7	8	9	10	11	12	←Display Position
1st Line	00	01	02	03	04	05	06	07	08	09	0A	0B	← DD RAM Address
2nd Line	40	41	42	43	44	45	46	47	48	49	4A	4B	← (Hexadecimal)

When the display shift is performed, the DD RAM address changes as follows:
(Left Shift Display)

(00)←	01	02	03	04	05	06	07	08	09	0A	0B	0C
(40)←	41	42	43	44	45	46	47	48	49	4A	4B	4C

(Right Shift Display)

27	00	01	02	03	04	05	06	07	08	09	0A	→(0B)
67	40	41	42	43	44	45	46	47	48	49	4A	→(4B)

(1－5) Character Generator ROM

The Character Generator ROM (CG ROM) generates 5 x 7 dots character pattern represented in 8-bit character codes.
The storage capacity is up to 240 kinds of 5 x 7 dots character pattern. The correspondence between character code and standard character pattern of NJU6406B is shown in Table 2-1 to 2-5.
User-defined character pattern (Custom Font) are also available by mask option.

Table 2-1. CG ROM Character Pattern (ROM version -00)

Lower 4 bits (Hexadecimal) \ Upper 4 bits (Hexadecimal)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	CG RAM (01)															
1	(02)															
2	(03)															
3	(04)															
4	(05)															
5	(06)															
6	(07)															
7	(08)															
8	(01)															
9	(02)															
A	(03)															
B	(04)															
C	(05)															
D	(06)															
E	(07)															
F	(08)															

Table 2-2. CG ROM Character Pattern (ROM version -01)

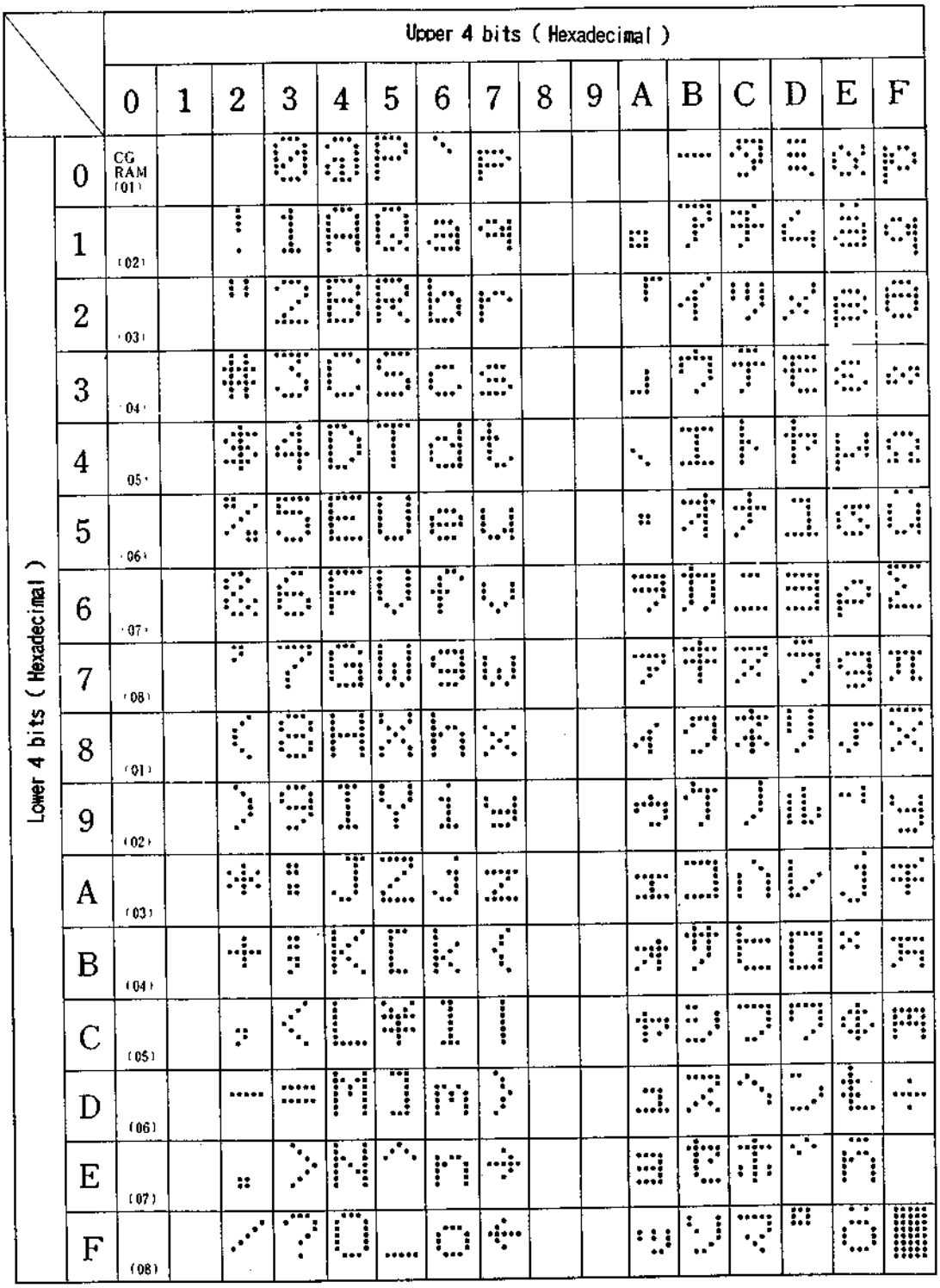


Table 2-3. CG ROM Character Pattern (ROM version -02)

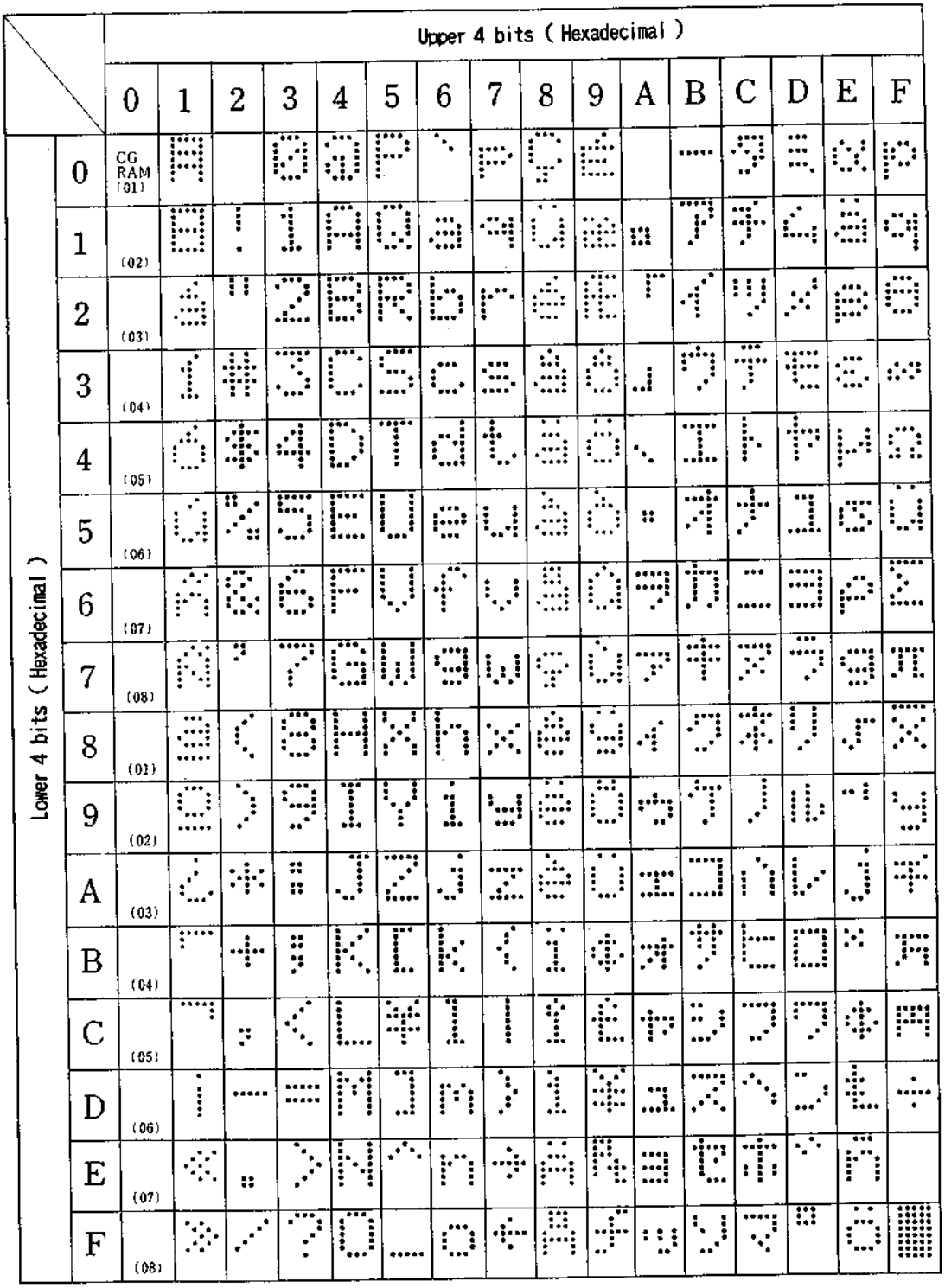


Table 2-4. CG ROM Character Pattern (ROM version -03)

Lower 4 bits (Hexadecimal)	Upper 4 bits (Hexadecimal)																
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	CG RAM (01)															
1	(02)															
2	(03)															
3	(04)															
4	(05)															
5	(06)															
6	(07)															
7	(08)															
8	(01)															
9	(02)															
A	(03)															
B	(04)															
C	(05)															
D	(06)															
E	(07)															
F	(08)															

Table 2-5. CG ROM Character Pattern (ROM version -A3)

Lower 4 bits (Hexadecimal) \ Upper 4 bits (Hexadecimal)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	CG RAM (01)															
1	(02)															
2	(03)															
3	(04)															
4	(05)															
5	(06)															
6	(07)															
7	(08)															
8	(01)															
9	(02)															
A	(03)															
B	(04)															
C	(05)															
D	(06)															
E	(07)															
F	(08)															

(1－6) Character Generator RAM (CG RAM)

The character generator RAM(CG RAM) can store any kinds of character pattern in 5 x 7 dots written by the user program to display user's original character pattern. The CG RAM can store 8 kind of character in 5 X 7 dots mode.

To display user's original character pattern stored in the CG RAM, the address data $(00)_H$ - $(07)_H$ or $(08)_H$ - $(0F)_H$ should be written to the DD RAM as shown in Table 2-1 to 2-5.

Table 3. shows the correspondence among the character pattern, CG RAM address and Data.

Unused memory area of the CG RAM can also be used as the general data memory area.

Table 3. Correspondence of CG RAM address, DD RAM character code and CG RAM character pattern (5 X 7 dots).

Character Code (DD RAM Data)	CG RAM Address		Character Pattern (CG RAM Data)	
7 6 5 4 3 2 1 0 ←— —→ Upper bit Lower bit	5 4 3 ←— Upper bit	2 1 0 —→ Lower bit	7 6 5 4 3 2 1 0 ←— —→ Upper bit Lower bit	
0 0 0 0 ∗ 0 0 0	0 0 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	∗ ∗ ∗ ∗ ∗ ∗	Character Pattern Example(1) ←Cursor Position
0 0 0 0 ∗ 0 0 1	0 0 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	∗ ∗ ∗ ∗ ∗ ∗	Character Pattern Example(2) ←Cursor Position
		0 0 0 0 0 1	∗ ∗ ∗	
⋮	⋮	⋮	⋮	
0 0 0 0 ∗ 1 1 1	1 1 1	1 0 0 1 0 1 1 1 0 1 1 1	∗ ∗ ∗	∗ : Don't Care

Notes : 1. Character code bits 0 to 2 correspond to the CG RAM address 3 to 5 (3 bits : 8 patterns).

2. CG RAM address 0, 1 and 2 designate character pattern line position. The 8th line is the cursor position and the display is performed by logical OR with cursor. Therefore, in case of the cursor display, the 8th line should be "0". If there is "1" in the 8th line, the bit "1" is always displayed on the cursor position regardless of cursor existence.

3. Character pattern row position correspond to the CG RAM data bits 0 to 4 are shown above. The bits 5 to 7 of the CG RAM are not appear on the display (no meaning for the display), but memory elements are existing, therefore it can be used as the general purpose RAM.

4. CG RAM character patterns are selected when character code bits 4 to 7 are all "0" and it is addressed by character code bits 0 to 2. Therefore, the address $(00)_H$ and $(08)_H$, $(01)_H$ and $(09)_H$, -------, $(07)_H$ and $(0F)_H$ select the same character pattern as shown in Table 2-1 to 2-5 and Table 3.

5. "1" for CG RAM data corresponds to display On and "0" to display Off.

(1−7) Timing Generator

The timing generator generates a timing signals for the DD RAM, CG RAM, CG ROM and other internal circuits operation.

RAM read timing for the display and internal operation timing for MPU access are separately generated, so that they may not interfere with each other.

Therefore, when the data write to the DD RAM for example, there will be no undesirable influence, such as flickering, in areas other than the display area.

(1−8) LCD Driver

LCD driver consist of 32-common driver and 60-segment driver.

When the line number is selected by a program, the required common drivers output the common driving waveform and the other common drivers output non-selection waveform automatically.

The 60 bits of character pattern data are shifted in the shift-register and latched when the 60 bits shift performed completely. This latched data controls display driver to output LCD driving waveform.

(1−9) Cursor Blinking Control Circuit

This circuits controls cursor On/Off and cursor position character blinks.

The cursor or blinks appear in the digit residing at the DD RAM address set in the address counter (AC).

When the address counter is $(08)_H$, a cursor position is shown as follows:

AC_6	AC_5	AC_4	AC_3	AC_2	AC_1	AC_0
0	0	0	1	0	0	0

1-line Display

1	2	3	4	5	6	7	8	9	10	11	12	
00	01	02	03	04	05	06	07	08	09	0A	0B	----

← Display position

← DD RAM address (Hexadecimal)

↑ Cursor position

2-line Display

1	2	3	4	5	6	7	8	9	10	11	12	
00	01	02	03	04	05	06	07	08	09	0A	0B	----
40	41	42	43	44	45	46	47	48	49	4A	4B	----

← Display position

← DD RAM address (Hexadecimal)

↑ Cursor position

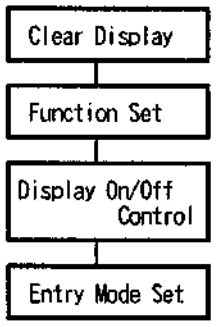
(Note) The cursor or blinks appear when the address counter(AC) selects the CG RAM. But the displayed the cursor and blink are meaningless. If the AC storing the CG RAM address data, the cursor and blink are displayed in the meaningless position.

(2) Power on Initialization by internal circuits

The NJU6406B is automatically initialized by internal power on initialization circuits when the power is turned on. In the internal power on initialization, following instructions are executed.

During the Internal power on initialization, the busy flag (BF) is "1" and this status is kept 10 ms after V_{DD} rises to 4.5V.

Initialization flow is shown below:



DL=1 :8-bit long interface data
N=0 :1-Line Display

D=0 :Display Off
C=0 :Cursor Off
B=0 :Cursor Blink Off

I/D=1:Increment by 1
S=0 :No Shift

NOTE
If the condition of power supply rise time described in the Electrical Characteristics is not satisfied, the internal Power On Initialization Circuits will not operate and initialization will not be performed.
In this case the initialization by MPU software is required.

5

(3) Instructions

The NJU6406B incorporates two registers, an Instruction Register (IR) and a Data Register (DR). These two registers store control information temporarily to allow interface between NJU6406B and MPU or peripheral ICs operating different cycles. The operation of NJU6406B is determined by this control signal from MPU.

The control information includes register selection signals (RS), read/write signals (R/W) and data bus signals (DB_0 to DB_7).

Table 4. shows each instruction and its operating time.

Note) The execution time mentioned in Table 4. based on fcp or fosc=250kHz.
If the oscillation frequency is changed, the execution time is also changed.

Table 4. Table of Instructions

INSTRUCTIONS	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DESCRIPTION	EXEC TIME
Non-operation	0	0	0	0	0	0	0	0	0	0	Non-operation. Only takes judgement machine cycle.	40us
Clear Display	0	0	0	0	0	0	0	0	0	1	Display clear and sets DD RAM address 0 in AC.	1.64ms
Return Home	0	0	0	0	0	0	0	0	1	*	Sets DD RAM address 0 in AC and returns display being shifted to original position. DD RAM contents remain unchanged	1.64ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift of display are performed in data read/write. I/D=1:Increment, I/D=0:Decrement S=1:Accompanies display shift	40us
Display On/Off Control	0	0	0	0	0	0	1	D	C	B	Sets of display On/Off(D), cursor On/Off(C) and blink of cursor position character(B).	40us
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor and shifts display without changing DD RAM contents S/C=1 : Display shift S/C=0 : Cursor shift R/L=1 : Shift to the right R/L=0 : Shift to the left	60us
Function Set	0	0	0	0	1	DL	N	*	*	*	Sets interface data length(DL), number of display lines(N). DL=1 : 8 bits, DL=0 : 4 bits N=1 : 2 lines, N=0 : 1 line	40us
Set CG RAM Address	0	0	0	1	←——	A_{CG}			—→		Sets CG RAM address. After this instruction, the data is transferred on CG RAM.	40us
Set DD RAM Address	0	0	1	←——	A_{DD}				—→		Sets DD RAM address. After this instruction, the data is transferred on DD RAM.	40us
Read Busy Flag & Address	0	1	BF	←——	AC				—→		Reads busy flag and AC contents. BF=1 : Internally operating BF=0 : Can accept instruction	0us
Write Data to CG & DD RAM	1	0	←——	Write Data					—→		Writes data into DD or CG RAMs.	40us
Read Data from CG or DD RAM	1	1	←——	Read Data					—→		Reads data from DD or CG RAMs.	60us
Explanation of Abbreviation	DD RAM : Display data RAM , CG RAM : Character generator RAM A_{CG} : CG RAM address, A_{DD} : DD RAM address, Corresponds to cursor address AC : Address counter used for both of DD and CG RAMs											

5

(3−1) Description of each instructions

(a) NOP (Non operation)

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	0	0	0

Non operation instruction. It consumes certain judgement machine cycles only.

(b) Clear Display

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	0	0	1

Clear display instruction is executed when the code "1" is written into DB_0. When this instruction is executed, the space code $(20)_H$ is written into every DD RAM address, the DD RAM address 0 is set into the address counter and entry mode is set increment. If the cursor or blink are displayed, they are returned to the left end of the LCD(the left end of the 1st line in the 2-line display mode).

The S of entry mode does not change.

Note: The character pattern for character code $(20)_H$ must be blank code in the user-defined character pattern(Custom font).

(c) Return Home

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Code	0	0	0	0	0	0	0	0	1	*	* = Don't care

Return home instruction is executed when the code "1" is written into DB_1. When this instruction is executed, the DD RAM address 0 is set into the address counter. Display is returned its original position if shifted, the cursor or blink are returned to the left end of the LCD(the left end of the 1st line in the 2-line display mode) if the cursor or blink are on the display.

The DD RAM contents do not change.

(d) Entry Mode Set

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	1	I/D	S

Entry mode set instruction which sets the cursor moving direction and display shift On/Off, is executed when the code "1" is written into DB_2 and the codes of (I/D) and (S) are written into DB_1(I/D) and DB_0(S), as shown below.

(I/D) sets the address increment or decrement, and the (S) sets the entire display shift in the DD RAM writing.

I/D	Function
1	Address increment: The address of the DD or CG RAM increment (+1) when the read/write, and the cursor or blink move to the right.
0	Address decrement: The address of the DD or CG RAM decrement (-1) when the read/write, and the cursor or blink move to the left.

S	Function
1	Entire display shift. The shift direction is determined by I/D: shift to the left at I/D=1 and shift to the right at the I/D=0. The shift is operated only for the character, so that it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DD RAM and writing/reading into/from CG RAM.
0	The display does not shifting.

(e) Display On/Off Control

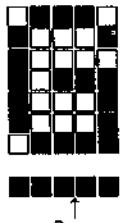
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	1	D	C	B

Display On/Off control instruction which controls the display On/Off, the cursor On/Off and the cursor position character blink, is executed when the code "1" is written into DB_3 and the codes of (D), (C) and (B) are written into DB_2(D), DB_1(C) and DB_0(B), as shown below.

D	Function
1	Display On.
0	Display Off. In this mode, the display data remains in the DD RAM so that it is retrieved immediately on the display when the D change to 1.

C	Function
1	Cursor On. The cursor is displayed by 5 dots on the 8th line.
0	Cursor Off. Even if the display data write, the I/D etc does not change.

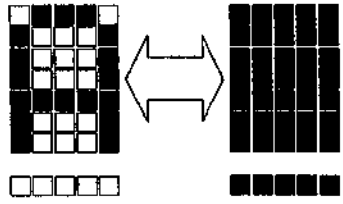
B	Function
1	The cursor position character is blinking. Blinking rate is 455.2ms at f_{CP} or f_{OSC}=270kHz and 491.6ms at f_{CP}=250kHz. The blink is displayed alternatively with all on (it means all black) and characters display. The cursor and the blink can be displayed simultaneously.
0	The character does not blink.



Cursor

Character Font 5 x 7 dots

(1) Cursor display example



Alternating display

(2) Blink display example

(f) Cursor/Display Shift

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Code	0	0	0	0	0	1	S/C	R/L	*	*	* = Don't care

The Cursor/Display shift instruction shifts the cursor position or display to the right or left without writing or reading display data. This function is used to correct or search the display. In the 2-line display, the cursor moves to the 2nd line when it passes the 40th digit of the 1st line. Notice that the 1st and 2nd line displays will shift at the same time. When the displayed data is shifted repeatedly, each line moves only horizontally.

The 2nd line display does not shift into the 1st line position.

The contents of address counter(AC) does not change by operation of the display shift only.

This instruction is executed when the code "1" is written into DB_4 and the codes of (S/C) and (R/L) are written into DB_3(S/C) and DB_2(R/L), as shown below.

S/C	R/L	Function
0	0	Shifts the cursor position to the left ((AC) is decremented by 1)
0	1	Shifts the cursor position to the right ((AC) is incremented by 1)
1	0	Shifts the entire display to the left and the cursor follows it.
1	1	Shifts the entire display to the right and the cursor follows it.

(g) Function Set

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Code	0	0	0	0	1	DL	N	*	*	*	* = Don't care

Function set instruction which sets the interface data length and number of display lines, is executed when the code "1" is written into DB_5 and the codes of (DL) and (N) are written into DB_4(DL) and DB_3(N), as shown below (character font is fixed 5 X 7 dots).

(DL) sets the interface data length and (N) sets the number of display lines either the 1-line or 2-lines.

NOTE

This function set instruction must be performed at the head of the program prior to all other existing instructions(except Busy flag/Address read). This function set instruction can not be executed afterwards unless the interface data length change.

DL	Function
1	Set the interface data length to 8 bits (DB_7 to DB_0)
0	Set the interface data length to 4 bits (DB_7 to DB_4) THe data must be sent or received twice.

N	Display lines	Character Font	Duty Ratio	Note
0	1	5 X 7 dots	1/16	
1	2	5 X 7 dots	1/32	

(h) Set CG RAM Address

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	1	A	A	A	A	A	A
					←Higher order bit				Lower order bit →	

Set CG RAM address instruction is executed when the code "1" is written into DB_6 and the address is written into DB_5 to DB_0 as shown below.

The address data mentioned by binary code "AAAAAA" is written into the address counter(AC) together with the CG RAM addressing condition. After this instruction execution, the data writing/reading is performed into/from the CG RAM.

(i) Set DD RAM Address

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	1	A	A	A	A	A	A	A
				←Higher order bit				Lower order bit→		

Set DD RAM address instruction is executed when the code "1" is written into DB_7 and the address is written into DB_6 to DB_0 as shown above.

The address data mentioned by binary code "AAAAAAA" is written into the address counter(AC) together with the DD RAM addressing condition. After this instruction, the data writing/reading is performed into/from the DD RAM.

Note : In case of the 1-line display, the address data is $(00)_H$ to $(4F)_H$, and during the 2-line display, the address is $(00)_H$ to $(27)_H$ for the 1st line and $(40)_H$ to $(67)_H$ for the 2nd line.

(j) Read Busy Flag & Address

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	1	BF	A	A	A	A	A	A	A
				←Higher order bit				Lower order bit→		

This instruction reads out the internal status of the NJU6406B. When this instruction is executed, the busy flag(BF) which indicate internal operation is read out from DB_7 and the address of CG RAM or DD RAM is read out from DB_6 to DB_0 (the address for CG RAM or DD RAM is determined by the previous instruction).

(BF)=1 indicates that internal operation is in progress. The next instruction is inhibited when (BF)=1. Check the (BF) status before the next write operation.

(k) Write Data to CG or DD RAM

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	0	D	D	D	D	D	D	D	D

←Higher order bit Lower order bit→

Write Data to CG RAM or DD RAM instruction is executed when the code "1" is written into (RS) and code "0" is written into (R/W).

By the execution of this instruction, the binary 8-bit data "DDDDDDDD" are written into the CG RAM or DD RAM. The selection of the CG RAM or DD RAM is determined by the previous instruction.

After this instruction execution, the address increment(+1) or decrement(-1) performed automatically according to the entry mode set. And the display shift is also executed according to the previous entry mode set.

(l) Read Data from CG or DD RAM

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	1	D	D	D	D	D	D	D	D

←Higher order bit Lower order bit→

Read Data from CG RAM or DD RAM instruction is executed when the code "1" is written into (RS) and (R/W).

By the execution of this instruction, the binary 8 bit data "DDDDDDDD" are read out from CG RAM or DD RAM. The selection of the CG RAM or DD RAM is determined by the previous instruction.

Before executing this instruction, either the CG RAM address set or DD RAM address set must be executed, otherwise the first read out data are invalidated.

When this instruction is serially executed, the next address data is normally read from the second read.

The address set instruction is not required if the cursor shift instruction is executed just beforehand(only DD RAM reading).

The cursor shift instruction has same function as the DD RAM address set, so that after reading the DD RAM, the address increment or decrement is executed automatically according to the entry mode.

But display shift does not occur regardless of the entry mode.

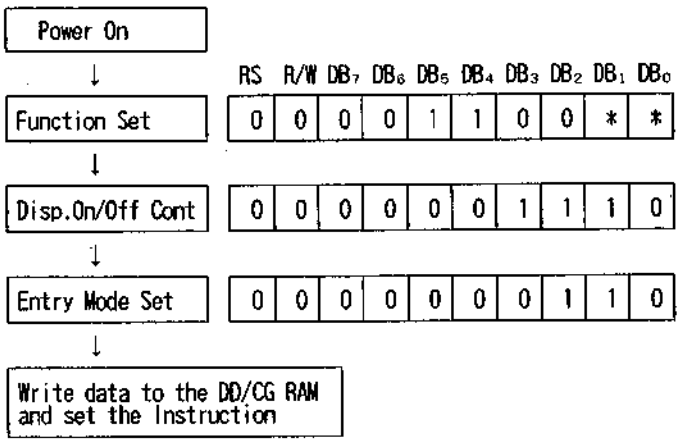
Note: The address counter(AC) is automatically incremented or decremented by 1 after write instructions to either of the CG RAM or DD RAM. Even if the read instruction is executed after this instruction, the addressed data can not be read out correctly. For a correct data read out, either the address set instruction or cursor shift instruction (only with DD RAM) must be implemented just before this instruction or from the second time read out instruction execution if the read out instruction is executed 2 times consecutively.

(3−2) Initialization using the internal reset circuits

(a) 24-character 1-line in 8-bit operation (Using internal reset circuits).

At the 24-character 1-line display, the Function set, Display On/Off Control and Entry Set Instruction must be executed before the data input, as shown below.

The DD RAM of the NJU6406B can store up to 80 characters, as explained before, therefore the advertising moving display is available when combined with display shift operation. Since the display shift operation changes only display position and the DD RAM contents remain unchanged, display data which are entered first can be output when the return home operation is performed.



Initialized.
No display appears.

Set the 8-bit operation/ 1-line display / 5X7dots Font.

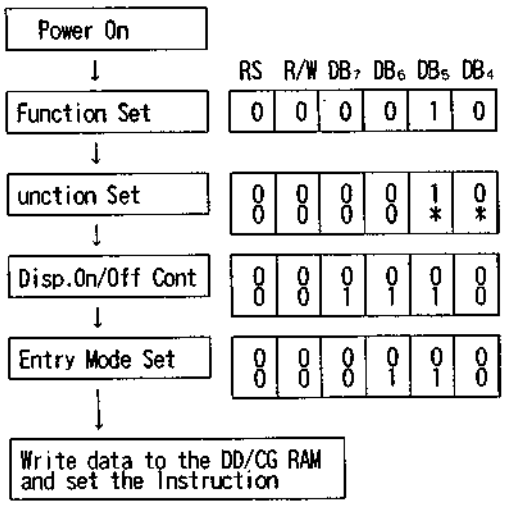
Turns on display and cursor. Entire display is in space mode by the initialization.

Example for set address increment and cursor right shift when the data write to the DD or CG RAM.

(b) 24-character 1-line in 4-bit operation (Using internal reset circuits).

In the 4-bit operation, the function set must be performed by the user programming.

When the power is turned on, 8-bit operation is selected automatically, therefore the first input is performed under 8-bit operation. In this operation, full instruction can not input because of terminals DB_0 to DB_3 are no connection. Therefore, same instruction must be rewritten on the RS, R/W and DB_7 to DB_4, as shown below. Since one operation is completed by the two accesses in the 4-bit operation mode, rewrite is required to set the instruction code in full. 24-character 1-line in 4-bit operation is shown as follows:



Initialized.
No display appears.

Set the 4-bit operation.
This step is executed in 8-bit mode set by the initialization.

Set the 4-bit operation / 1-line display / 5 X 7dots Font.
The 4-bit operation starts from this step.
Turn on display and cursor.
Entire display is in space mode by the initialization.

Example for set address increment and cursor right shift when the data write to the DD or CG RAM.

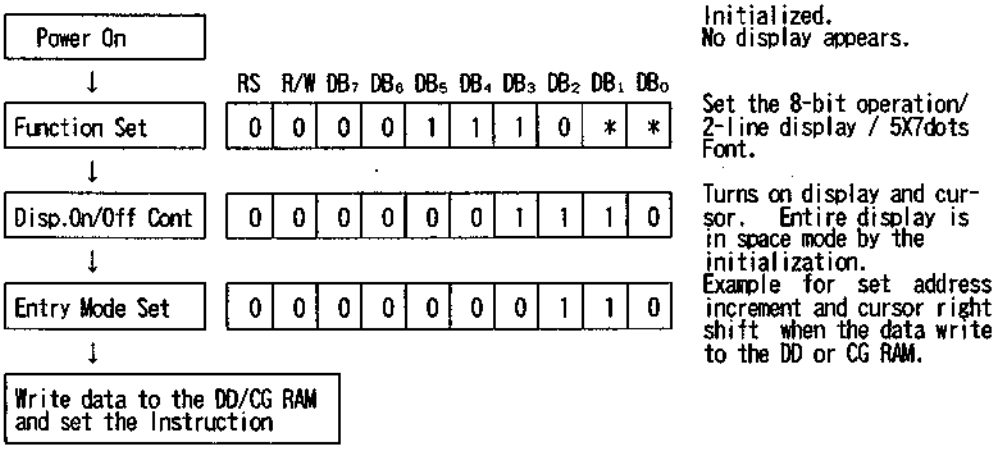
(c) 24-character 2-line in 8-bit operation (Using internal reset circuits).

In the 2-line display, the cursor moves automatically from the 1st to the 2nd line after the 40th character of the 1st line has been written.

Therefore, if the display characters is only 24 character in the 1st line, the DD RAM address must be set by the user programming to change the cursor position to the 2nd line.

The 1st and 2nd line displays will shift at the same time. When the displayed data is shifted repeatedly, each line moves only horizontally.

The 2nd line display does not shift into the 1st line position.



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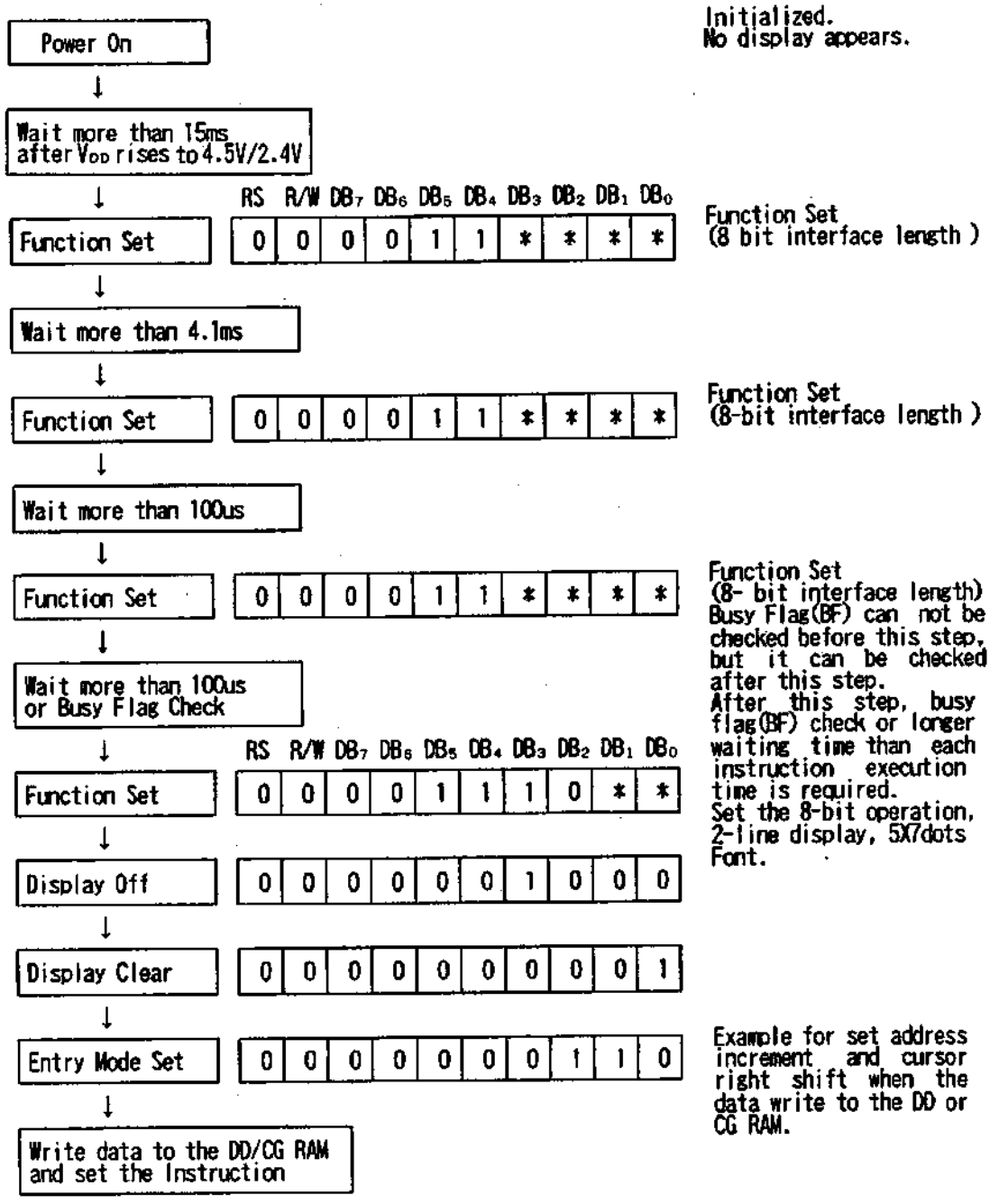
(3-3) Initialization by instruction

If the power supply conditions for the correct operation of the internal reset circuits are not met, the NJU6406B must be initialized by the instruction.

(a) Initialization by Instruction in 8-bit interface



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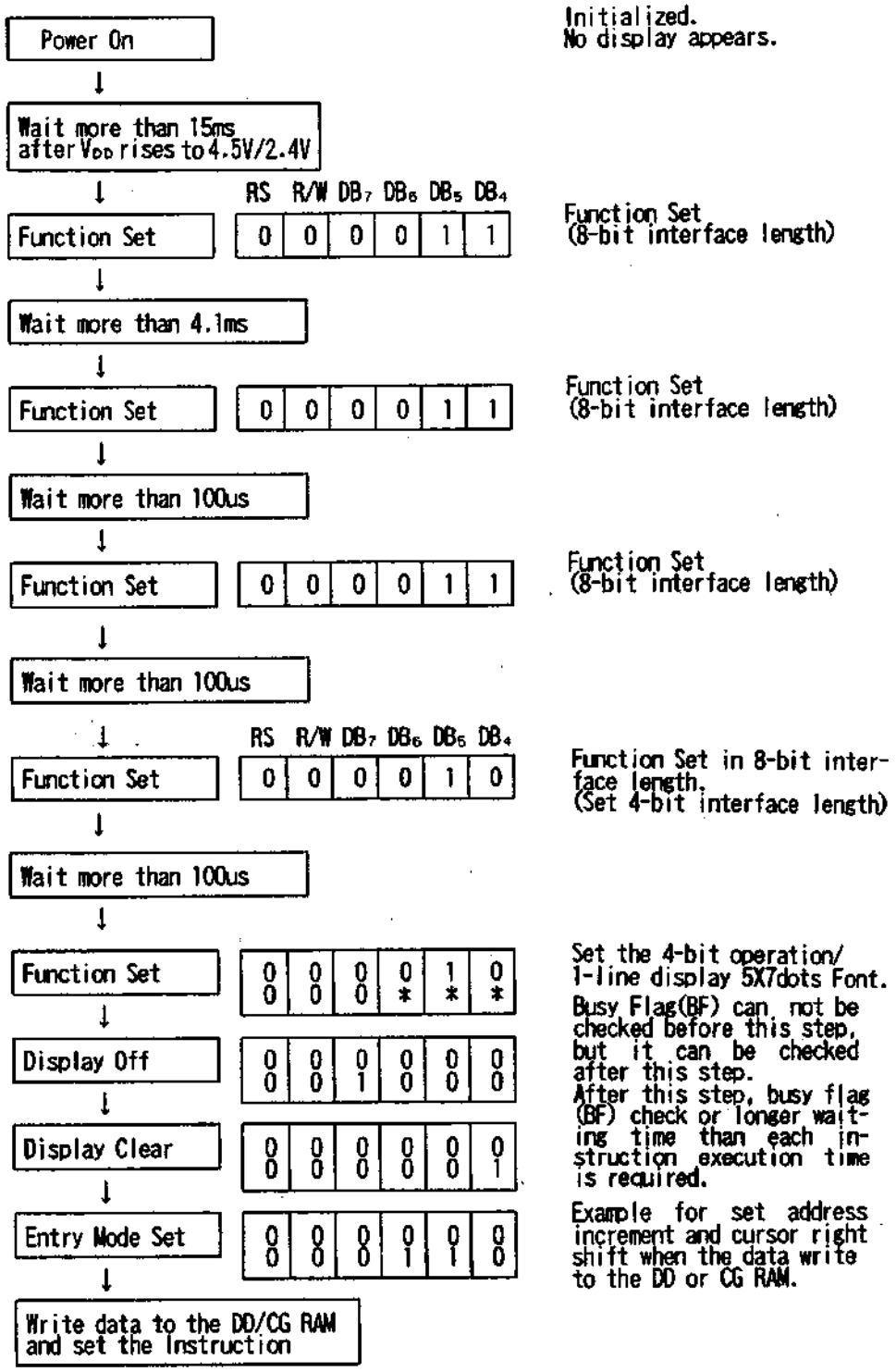
(b) Initialization by Instruction in 4-bit interface



5

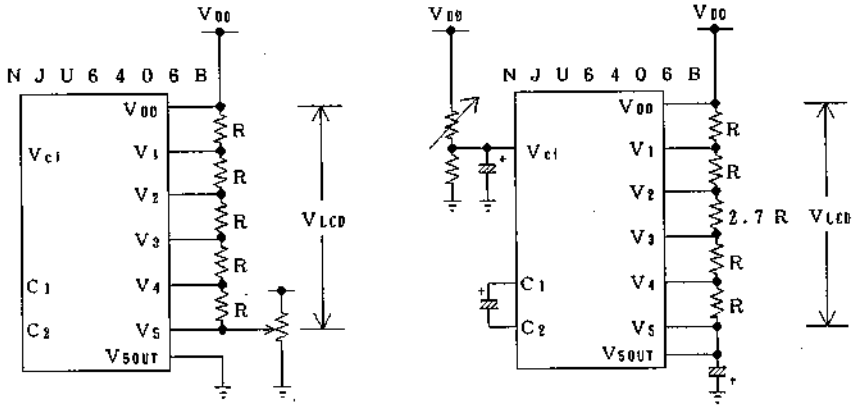
(4) LCD DISPLAY

(4－1) Power Supply for LCD Driving

NJU6406B incorporates voltage doubler to generate the LCD driving high voltage. The voltage doubler generate about twofold voltage from the V_{CI} input voltage (9.5V typ at Iout=2mA and V_{CI}=5V). In order to generate LCD display driving waveform, the NJU6406B required external bleeder resistance. The bleeder resistance must be changed according to the duty ratio as shown below.

LCD Driving Voltage vs Duty Ratio

	Duty Ratio	1/32	1/16
Power Supply	Bias	1/6.7	1/5
	V_1	V_{DD}-1/6.7V_{LCD}	V_{DD}-1/5V_{LCD}
	V_2	V_{DD}-2/6.7V_{LCD}	V_{DD}-2/5V_{LCD}
	V_3	V_{DD}-3/6.7V_{LCD}	V_{DD}-3/5V_{LCD}
	V_4	V_{DD}-4/6.7V_{LCD}	V_{DD}-4/5V_{LCD}
	V_5	V_{DD}-V_{LCD}	V_{DD}-V_{LCD}



(a) 1/5 bias (1/16 Duty)
(Internal Voltage Doubler No-use example)

(b) 1/6.7 bias (1/32 Duty)
(Internal Voltage Doubler using example)

Internal Driving Voltage Supply Examples

(4−2) Relation between oscillation frequency and LCD frame frequency.

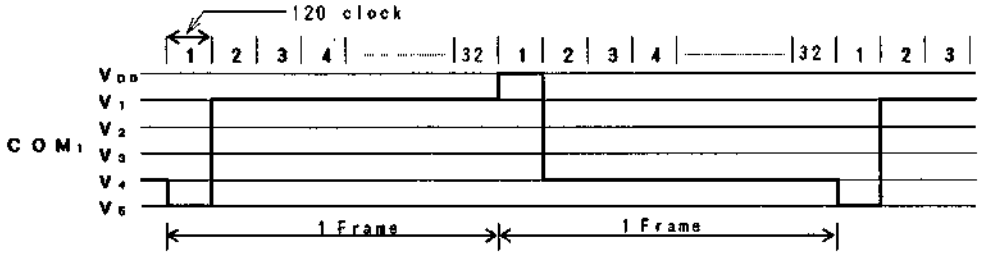
The NJU6406B requires either one of the oscillation resistance(RF) or ceramic resonator for the internal oscillation, or external clock.
In case of the oscillation resistance using, the oscillating frequency is affected by the stray capacitance of the terminals OSC_1 and OSC_2, thus shorter connection length of these terminals are required.
LCD frame frequency example mentioned below is based on 270kHz oscillation (1 clock =3.7us).

LCD frame frequency is calculate by following formula.

$$1 \text{ frame cycle} = \frac{1}{fosc} \times 120(\text{clock}) \times \text{the reciprocal number of duty}$$

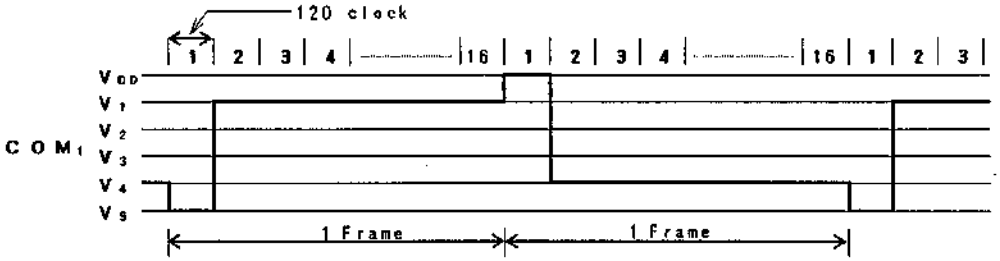
$$1 \text{ frame frequency} = \frac{1}{1 \text{ frame cycle}}$$

(a) 1/32 duty



1 frame = 3.7(us) x 120 x 32 = 14,208(us) = 14.208(ms)
Frame frequency = 1/14.208(ms) = 70.38(Hz)

(b) 1/16 duty



1 frame = 3.7(us) x 120 x 16 = 7,104(us) = 7.104(ms)
Frame frequency = 1/7.104(ms) = 140.77(Hz)

(5) Interface with MPU

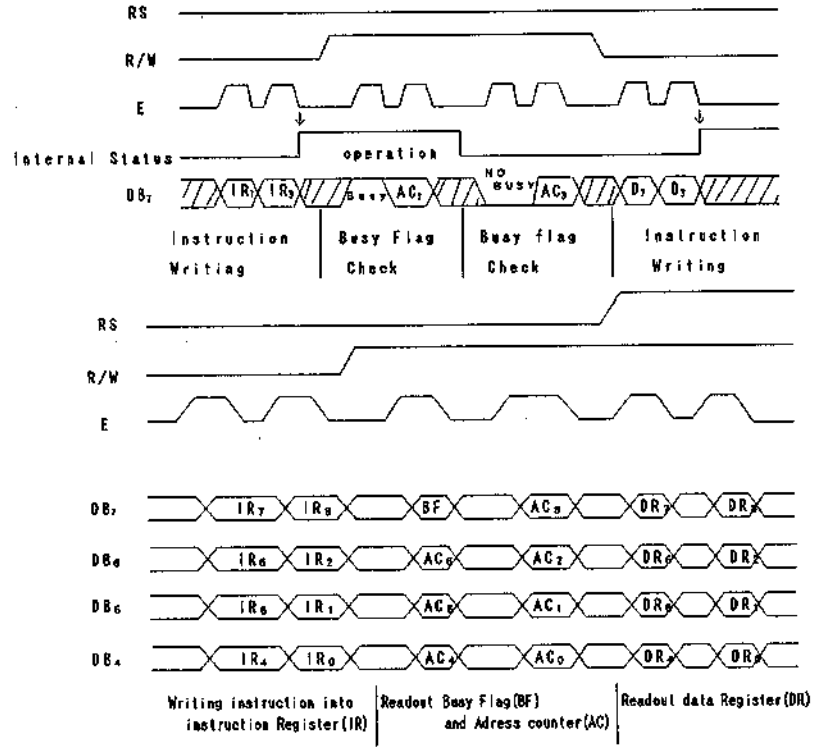
NJU6406B can be interfaced with both of 4/8 bit MPU and the two-time 4-bit or one-time 8-bit data transfer is available.

(5−1) 4-bit MPU interface

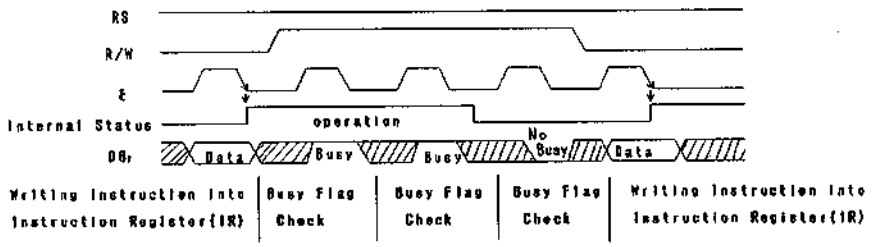
When the interface length is 4-bit, the data transfer is performed by 4 lines connected to DB_4 to DB_7 (DB_0 to DB_3 are not used). The data transfer with the MPU is completed by the two-time 4-bit data transfer.

The data transfer is executed in the sequence of upper 4-bit (the data DB_4 to DB_7 at 8-bit length) and lower 4-bit (the data DB_0 to DB_3 at 8-bit length).

The busy flag check must be executed after two-time 4-bit data transfer (1 instruction execution). In this case the data of busy flag and address counter are also output twice.



(5−2) 8-bit MPU interface



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage (1)	V_{DD}	- 0.3 ~ + 7.0	V
Supply Voltage (2)	V_1~V_5 (3)	V_{DD}- 13.5~ V_{DD}+0.3	V
Input Voltage	V_{IN}	- 0.3 ~ V_{DD}+0.3	V
Operating Temperature	Topr	- 30 ~ + 80	°C
Storage Temperature	Tstg	- 55 ~ + 125	°C

Note 1) If the LSI are used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.
Note 2) All voltage values are specified as V_{SS} = 0 V
Note 3) The relation : $V_{DD} \geqq V_{C1} \geqq V_5 \geqq V_{5OUT}$, $V_{DD} \geqq V_{SS} \geqq V_{5OUT}$, V_{SS}=0V must be maintained.
Note 4) Decoupling capacitor should be connected between V_{C1} and V_{SS} due to the stabilized operation for the voltage doubler.

■ ELECTRICAL CHARACTERISTICS (V_{DD}=5V±10%, V_{SS}=0V, Ta=-20 ~ +75°C)

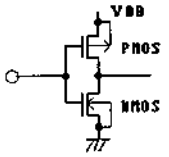
PARAMETER		SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT	
Operating Voltage		V_{DD}			4.5	5.0	5.5	V	
Input Voltage	1	V_{IH1}	All Input and Input/Output Terminals except OSC Terminals		2.3		V_{DD}	V	5
		V_{IL1}					0.8		
	2	V_{IH2}	Only OSC Terminal		V_{DD}-1		V_{DD}		
		V_{IL2}					1.0		
Output Voltage	1	V_{OH1}	Input/Output Terminals	$-I_{OH}$=0.205mA	2.4			V	
		V_{OL1}		I_{OL}=1.6mA			0.4		
	2	V_{OH2}	Output Terminals	$-I_{OH}$=0.04mA	0.9V_{DD}				
		V_{OL2}		I_{OL}=0.04mA			0.1V_{DD}		
Driver On-resist.(COM)		R_{COM}	±I_D=0.05mA(All com.term.)				20	kΩ	6
Driver On-resist.(SEG)		R_{SEG}	±I_D=0.05mA(All seg.term.)				30		
Input Leakage Current		I_{LI}	V_{IN}=0 ~ V_{DD}		- 1		1	uA	7
Pull-up Resist Current		$-I_P$	V_{DD}=5V, RS, R/W, DB		50	125	250		
Operating Current (1)		I_{DD1}	Ceramic resonator V_{DD}=5V, f_{OSC}=250kHz			0.55	0.8	mA	
Operating Current (2)		I_{DD2}	CR Oscillation External-clock Operation V_{DD}=5V, f_{OSC}=f_{CP}=270kHz			0.6	1.0	mA	8
Voltage Doubler	Output Voltage	V_{5out}	I_{OUT}=5mA, Ta=25°C		-2.8	-3.9		V	9
			I_{OUT}=1mA, Ta=25°C		-4.5	-4.7			
	Conversion Efficiency	V_{EF}	R_L=∞		95	99.9		%	
	Input Voltage	V_{C1}			2.5		5.5	V	
Ext. Clk	Operating Freq.	fcp			125	250	350	kHz	
	Duty	DUTY			45	50	55	%	
	Rise Time	trcp					0.2	μs	
	Fall Time	tfcp					0.2		
Int. OSC	Oscillation Frequency	fosc	RF Osc. RF=91kΩ±2%		190	270	350	kHz	10
			Ceramic resonator			250		kHz	
LCD Driving Voltage		V_{LCD}	V_{DD} - V_5	1/5 Bias	V_{DD} -3.0		V_{DD} -13.5	V	11
				1/6.7 Bias					

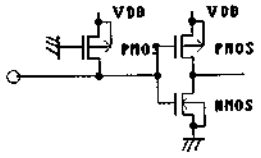
■ ELECTRICAL CHARACTERISTICS (V_{DD}=2.4V~3.6V, V_{SS}=0V, Ta=-20 ~ +75°C)

PARAMETER		SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT	
Operating Voltage		V_{DD}			2.4	3.0	3.6	V	
Input Voltage		V_{IH1}	All Input and Input/Output Terminals		0.8V_{DD}		V_{DD}	V	5
		V_{IL1}					0.2V_{DD}		
Output Voltage	1	V_{OH1}	Input/Output Terminals	$-I_{OH}$=0.205mA	2.0			V	
		V_{OL1}		I_{OL}=1.6mA			0.5		
	2	V_{OH2}	Output Terminals	$-I_{OH}$=0.04mA	0.9V_{DD}				
		V_{OL2}		I_{OL}=0.04mA			0.1V_{DD}		
Driver On-resist.(COM)		R_{COM}	±I_D=0.05mA(All com.term.)				20	kΩ	6
Driver On-resist.(SEG)		R_{SEG}	±I_D=0.05mA(All seg.term.)				30		
Input Leakage Current		I_{LI}	V_{IN}=0 ~ V_{DD}		- 1		1	uA	7
Pull-up Resist Current		$-I_P$	V_{DD}=3V		10	25	50		
Operating Current		I_{DD}	CR Oscillation External-clock Operation V_{DD}=3V, f_{OSC}=f_{CP}=240kHz			0.2	0.3	mA	8
Voltage Doubler	Output Voltage	V_{Sout}	V_{ci}=3V, I_{OUT}=1mA, Ta=25°C		-2.5	-2.75		V	9
	Conversion Efficiency	V_{EF}	R_L=∞		95	99.9		%	
	Input Voltage	V_{ci}			1.8		V_{DD}	V	
Int. OSC	Oscillation Frequency	fosc	RF Osc. RF=91kΩ±2%		160	240	320	kHz	10
LCD Driving Voltage		V_{LCD}	V_{DD}=3V, V_5 Terminal		V_{DD} -3.0		V_{DD} -12.0	V	11

Note 5) Input/Output structure except LCD driver are shown below:

Input Terminal Structure

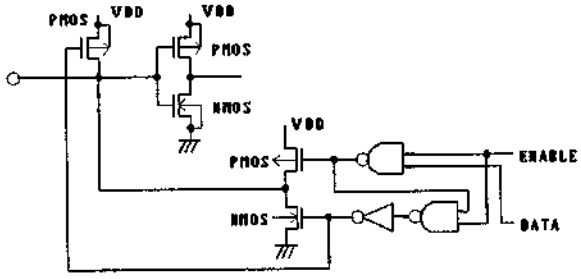




E Terminal

RS,R/W Terminals

Input/Output Terminal Structure



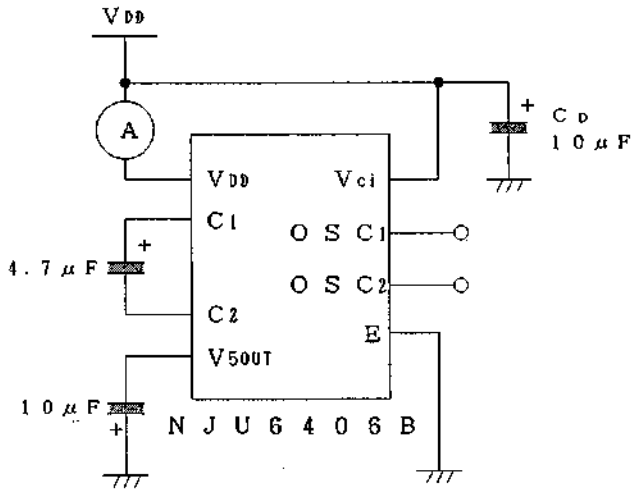
DB_0 to DB_7 Terminals

Note 6) R_{COM} and R_{SEG} are the resistance values between power supply terminals(V_{DD}, V_1, V_4, V_5) and each common terminal (COM_1 to COM_{32}), and supply voltage (V_{DD}, V_2, V_3, V_6) and each segment terminal (SEG_1 to SEG_{60}) respectively, and measured when the current Id is flown on every common and segment terminals at a same time.

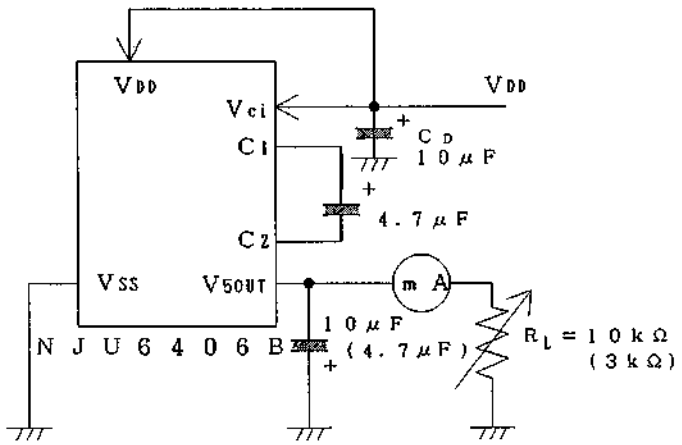
Note 7) Except pull-up resistance current and output driver current.

Note 8) Except Input/output current.
If the input level is medium, current consumption will increase due to the penetration current. Therefore, the input level must be fixed to "H" or "L".

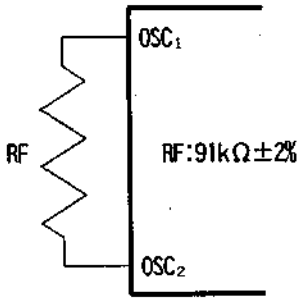
·Operating Current Measuring Circuit

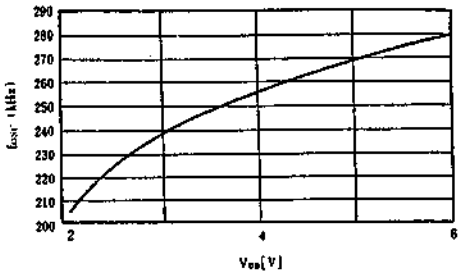


Note 9) Voltage Doubler Characteristics Measuring Circuit.



Note 10) Apply to internal CR oscillation using a oscillation resistance Rf.
As the oscillating frequency is affected by the stray capacitance of the terminals OSC_1 and OSC_2, shorter connection length of these terminals are required.





Note) As this circuit example mentioned only for standard application, it can not guaranty the characteristics of oscillation.
Please check the external parts value before production.

Note 11) Apply to the output voltage from each COM and SEG are less than ±0.15V against the LCD driving constant voltage(V_{DD}, V_1, V_2, V_3, V_4, V_5) at no load condition.

5

· Bus timing characteristics

Write operation sequence (Write from MPU to NJU6406B)
(V_{DD} = 5.0V±10%, V_{SS} = 0V, Ta = -20 ~ +75°C)

PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Enable Cycle Time		t_{CYCE}	500		fig.1	ns
Enable Pulse Width	"High" level	P_{WEH}	220			
Enable Rise Time, Fall Time		t_{Er}, t_{Ef}		20		
Set up Time	RS, R/W, E	t_{AS}	40			
Address Hold Time		t_{AH}	10			
Data Set up Time		t_{DSW}	60			
Data Hold Time		t_H	10			

Write operation sequence (Write from MPU to NJU6406B)
(V_{DD} = 3.0V±20%, V_{SS} = 0V, Ta = -20 ~ +75°C)

PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Enable Cycle Time		t_{CYCE}	1.4		fig.1	μs
Enable Pulse Width	"High" level	P_{WEH}	500			ns
Enable Rise Time, Fall Time		t_{Er}, t_{Ef}		20		
Set up Time	RS, R/W, E	t_{AS}	70			
Address Hold Time		t_{AH}	10			
Data Set up Time		t_{DSW}	140			
Data Hold Time		t_H	10			

Timing Characteristics (Write operation)

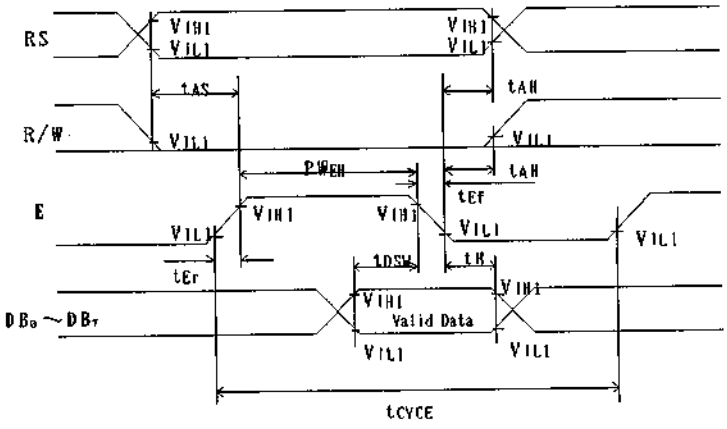


fig. 1 The timing characteristics of the bus write operating sequence.
(Write from MPU to NJU6406B)

Read operation sequence (Read from NJU6406B to MPU)

(V_{DD} = 5.0V±10%, V_{SS} = 0V, Ta = -20 ~ +75°C)

PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Enable Cycle Time		t_{CYCE}	500		fig.2	ns
Enable Pulse Width	"High" level	P_{WEH}	220			
Enable Rise Time, Fall Time		t_{Er}, t_{Ef}		20		
Set up Time	RS, R/W, E	t_{AS}	40			
Address Hold Time		t_{AH}	10			
Data Delay Time		t_{DDW}		120		
Data Hold Time		t_{DDH}	20			

Read operation sequence (Read from NJU6406B to MPU)

(V_{DD} = 3.0V±20%, V_{SS} = 0V, Ta = -20 ~ +75°C)

PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Enable Cycle Time		t_{CYCE}	1.4		fig.2	μs
Enable Pulse Width	"High" level	P_{WEH}	500			ns
Enable Rise Time, Fall Time		t_{Er}, t_{Ef}		20		
Set up Time	RS, R/W, E	t_{AS}	70			
Address Hold Time		t_{AH}	10			
Data Delay Time		t_{DDW}		600		
Data Hold Time		t_{DDH}	20			

Load condition of DB_0 to DB_7 : C_L=100pF

Timing Characteristics (Read operation)

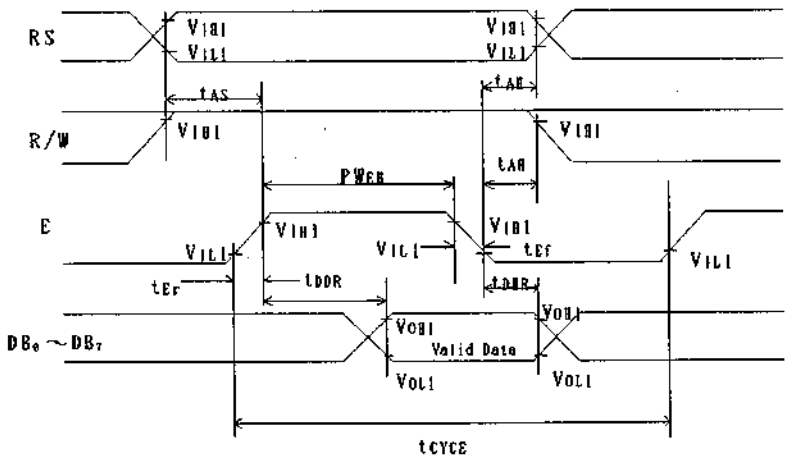


fig. 2 The timing characteristics of the bus read operating sequence.
(Read from NJU6406B to MPU)

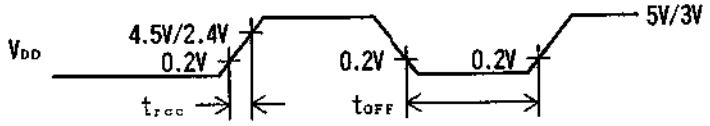
・Power Supply Condition when using the internal initialization circuit
(V_{DD} = 5.0V±10%, V_{SS} = 0V, Ta = -20 ～ +75°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	CONDITION	UNIT
Power Supply Rise Time	t_{rcc}	0.1	—	10		ms
Power Supply OFF Time	t_{OFF}	1	—			

・Power Supply Condition when using the internal initialization circuit
(V_{DD} = 3.0V±20%, V_{SS} = 0V, Ta = -20 ～ +75°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	CONDITION	UNIT
Power Supply Rise Time	t_{rcc}	0.1	—	5		ms
Power Supply OFF Time	t_{OFF}	1	—			

Since the internal initialization circuits will not operate normally unless the above conditions are met, in such a case it must initialize by instruction.
(Refer to initialization by the instruction)

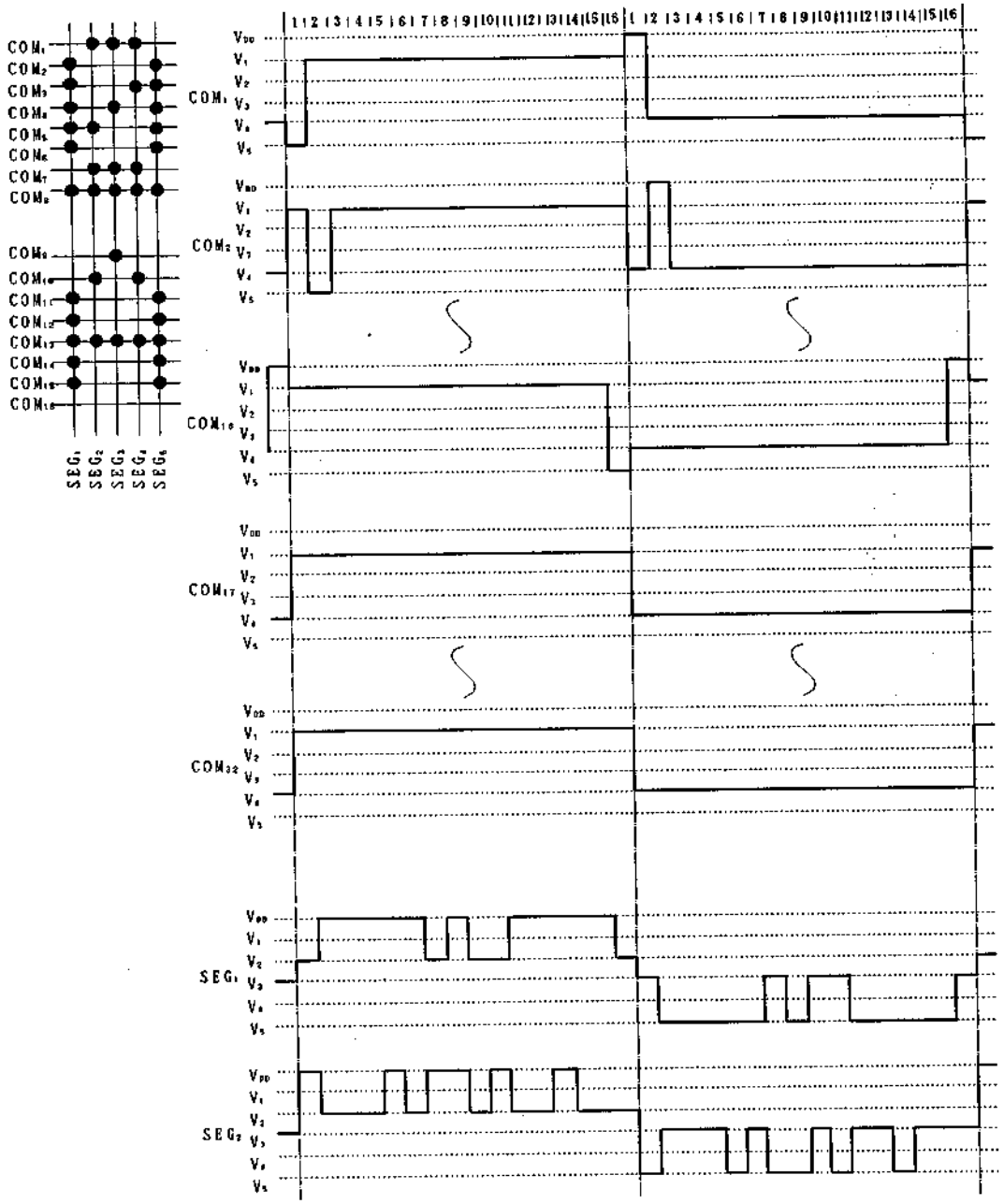


V_{DD}=5V ---- 0.1ms≦t_{rcc}≦10ms　　t_{OFF}≧1ms
V_{DD}=3V ---- 0.1ms≦t_{rcc}≦5ms

t_{OFF} specifies power off time in a short period off or cyclical on/off.

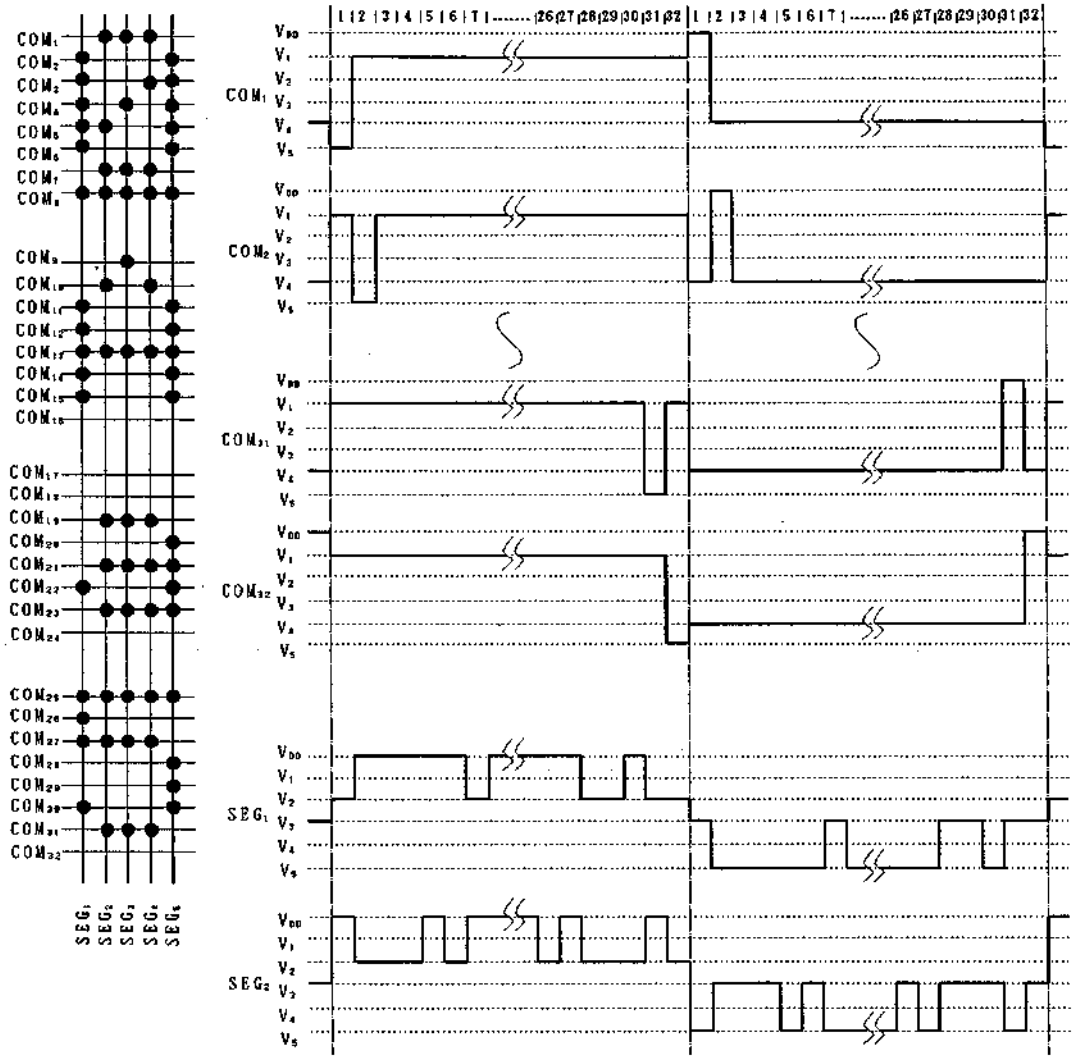
■ LCD DRIVING WAVEFORM

1/16 Duty Driving

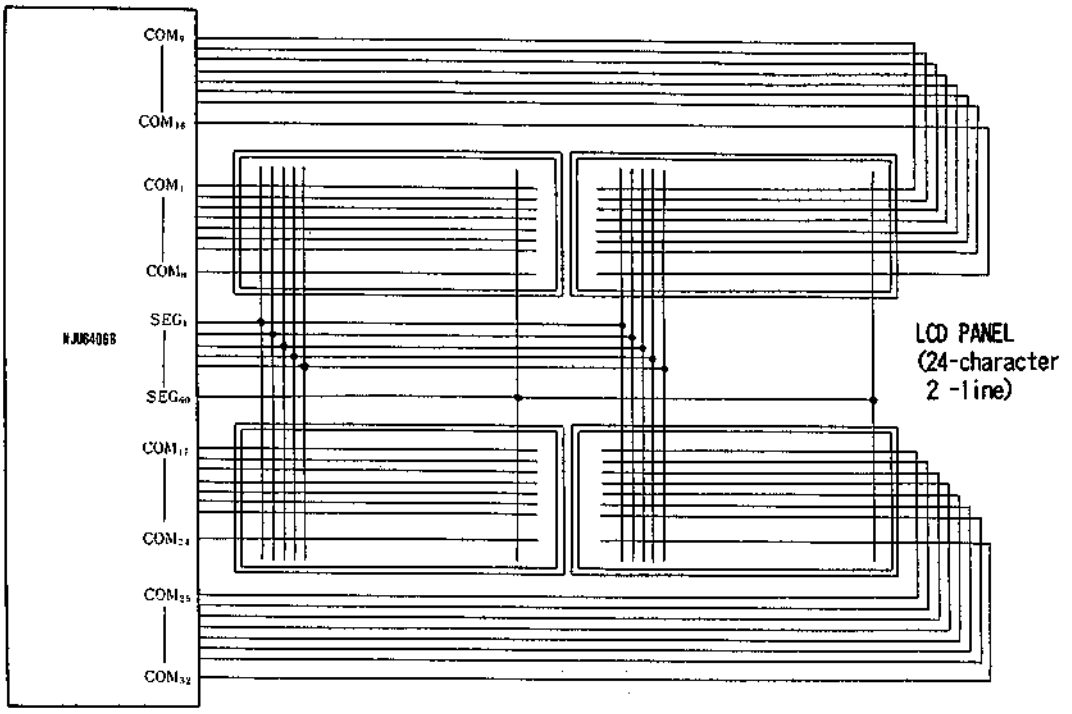


■ LCD DRIVING WAVEFORM

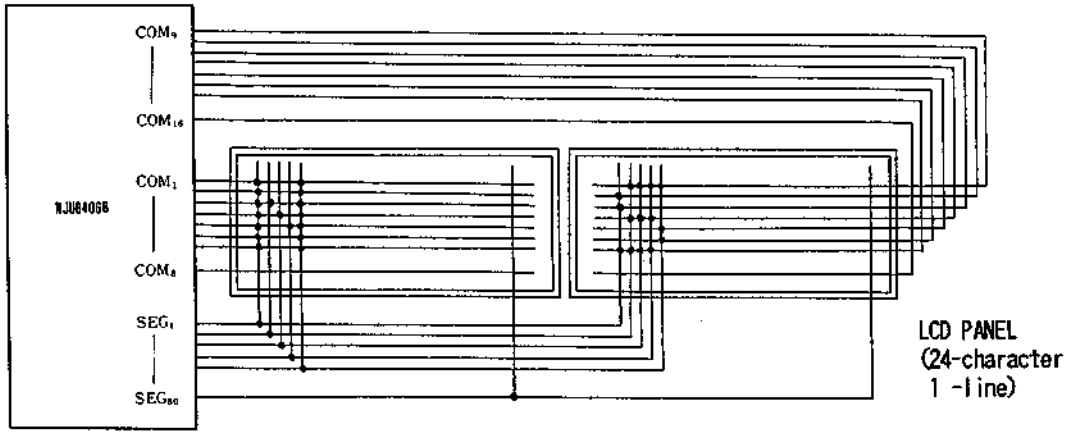
1/32 Duty Driving



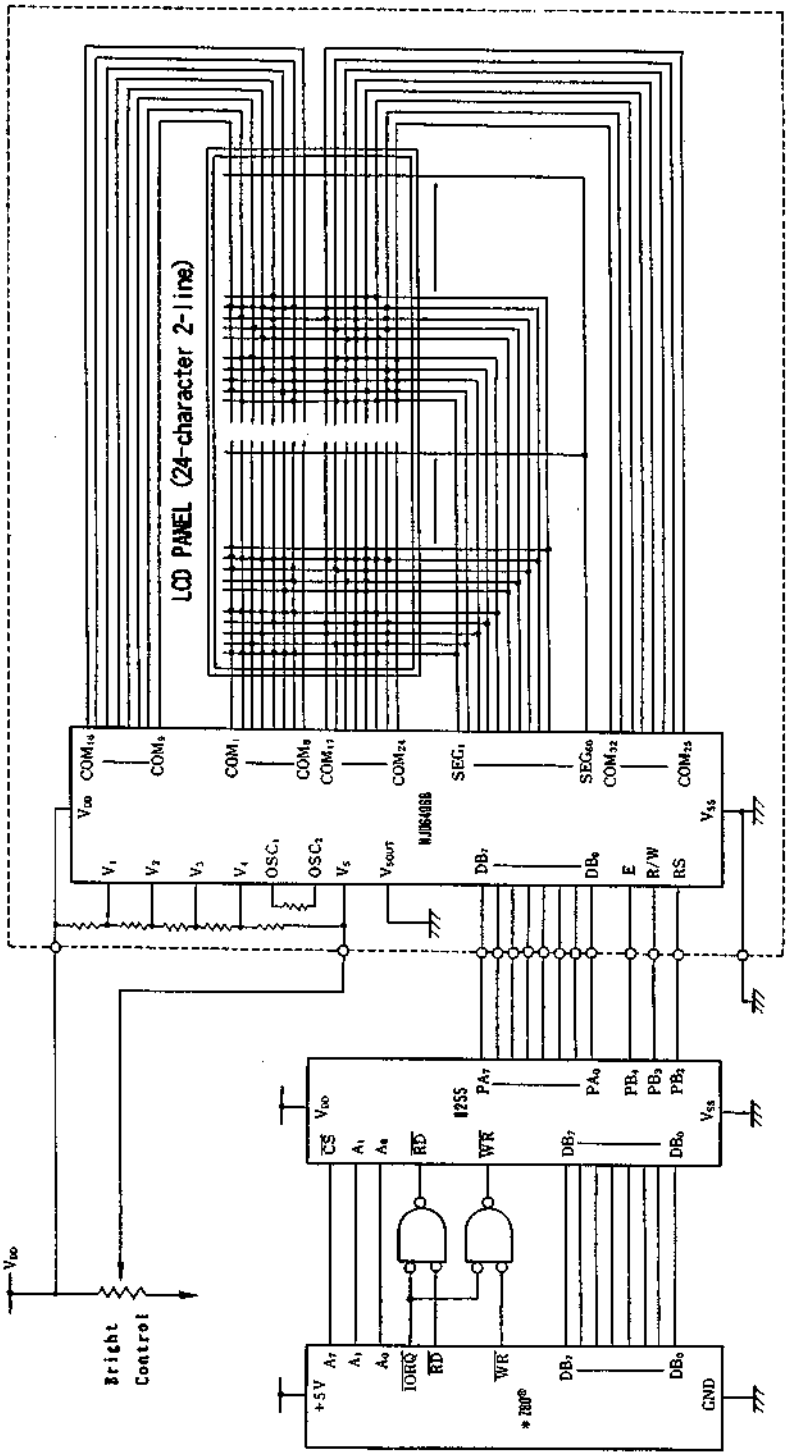
■ APPLICATION CIRCUITS



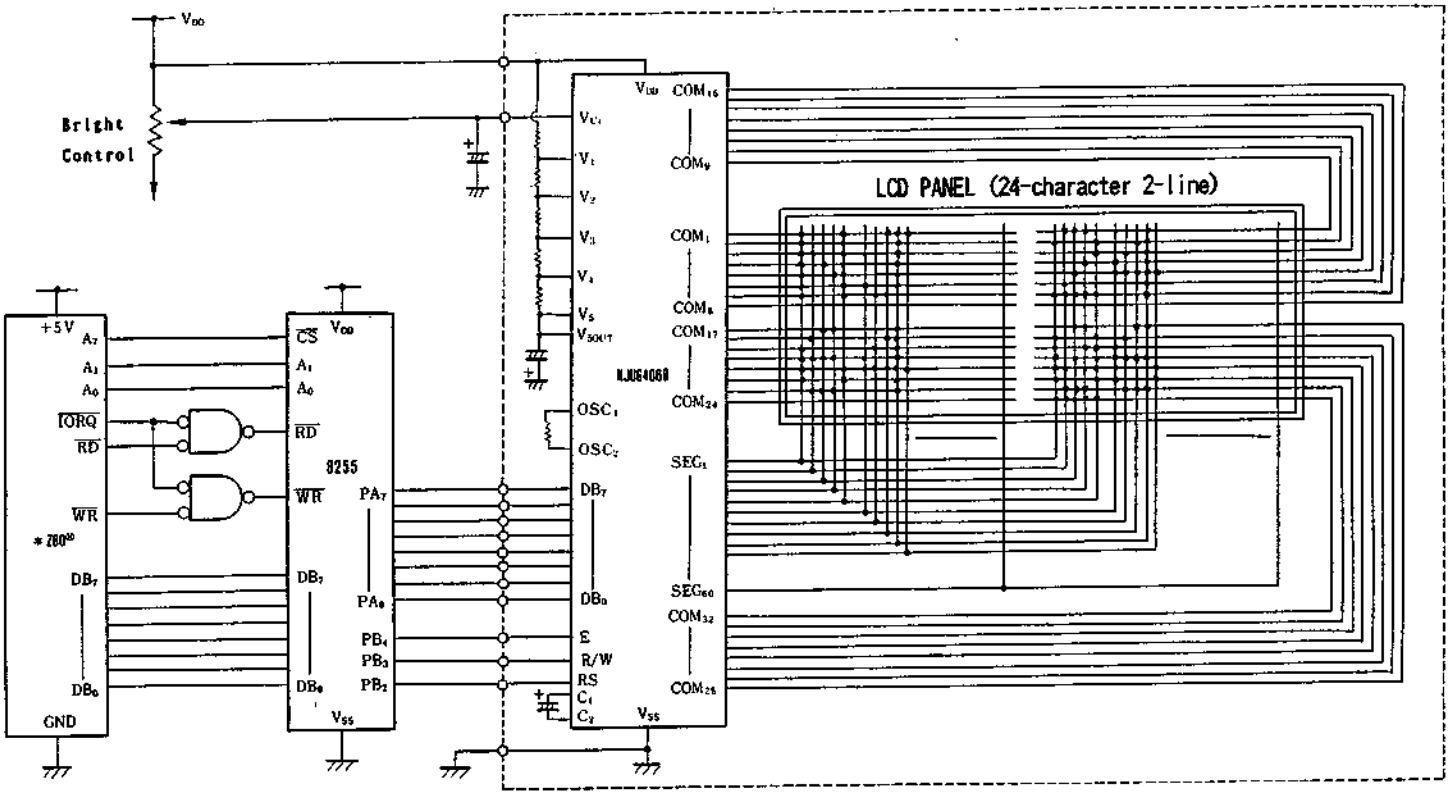
(a) 5 x 7 dots, 24-character 2-line example (1/6.7 Bias, 1/32 Duty)



(b) 5 x 7 dots, 24-character 1-line example (1/5 Bias, 1/16 Duty)



(c) 8-bit MPU interface example
(LCD driving voltage is supplied from external power supply)



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(d) 8-bit MPU interface example
(Single power supply operation, LCD driving voltage is generated by NJU6406B)

MEMO