LG4538

262,144-Color, 240x320-dot Graphics LCD controller driver for a-Si TFT Pnael

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Description

The LG4538 is liquid crystal controller driver LSI with internal frame memory for amorphous silicon TFT panel sized 240RGB x 320-dot at the maximum. The driver supports MIPI DBI Type A,B (18/16/9/8 bits) , Type C (Option 1 and Option 3) and serial peripheral interface as system interface to microcomputer as well as high-speed frame memory write function, enabling efficient data transfer.

The LG4538 is also compliant with MIPI DPI (VSYNC, HSYNC, DOTCLK, ENABLE, and DB[17:0]) for video image display.

The LG4538 incorporates step-up and voltage follower circuits to generate drive voltage required for α-Si TFT panel and dynamic backlight control function to control backlight brightness depending on image data reducing power consumption at the backlight with slightest influence on the display quality.

Other features include 8-color display and power management functions, making the driver best suitable for small or mid sized portable devices such as digital mobile phones, small PDAs and mobile TV devices.

Features

- Single chip driver for 262,144-color TFT 240RGB x 320-dot graphics (with internal source, gate and power supply circuits)

- Supported Interfaces

  – Command set method (Comply with MIPI DCS Version 1.01.00) *DCS: Display Command Set
  – MIPI-DBI (Comply with MIPI DBI Version .00)
  Type A,B 18-/16-/9-/8-bit
  Type C 3-wire (Option 1), 4-wire (Option 3)
  – MIPI-DPI (Comply with MIPI DPI-2 Version 2.00)
  – TE-I/F (MIPI DBI + TE synchronization signal output)

- Abundant color display
  - 262,144-color display
  – Partial display function

- Low-power consumption architecture (allowing direct input of interface I/O power supply)
  – Deep standby mode
  – 8-color mode (Idle Mode)
  – Input power supply voltage:
  Interface I/O power supply: VDD3 = 1.65V ~ 3.3V
  Liquid crystal analog circuit power supply: VCI = 2.5V ~ 3.3V
  VCI≥VDD3

- Dynamic Backlight Control Function

- Internal liquid crystal drive power supply circuit
  – Source/VCOM power supply: AVDD = (GVDD+0.5)V ~6.0V
  VCI-VCL ≤ 6.0V
  – Gate drive power supply: VGH > (AVDD+0.5)V
  VGL < (VCL-0.6)V
  VGH-VGL ≤ 25V
  – VCOM drive power supply: VCOMH = (VCI-0.5)V ~ (AVDD-0.5)V
  VCOML = (VCL+0.5)V ~ 0V
  VCOMH-VCOML ≤ 6.0V

- TFT storage capacitance: Cst only (common VCOM)

- Internal frame memory: 172,800 bytes

- Liquid crystal display drive circuits: 720 source signal lines, 320 gate signal lines

- Single chip, gate output arranged on both sides of the chip for COG mounting

- Separate RGB gamma correction function

- Internal NVM (32 bits for user identification code, 7 bits for VCOM adjustment): Rewriting is guaranteed up to 2 times.

Block Diagram

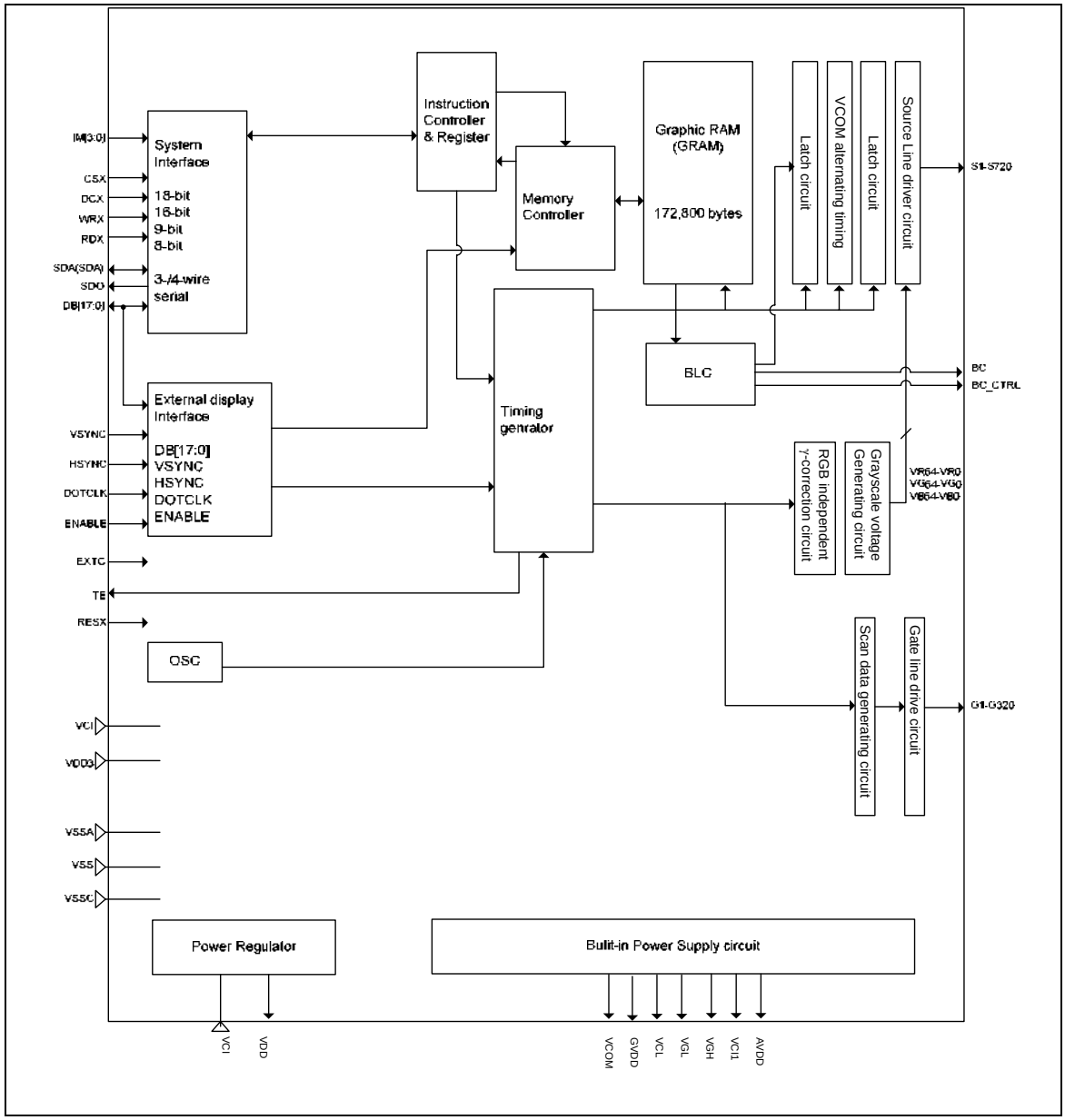


Figure 1

Pin Function

Table 1 Interface Pins

<table>
<tr><th>Signal</th><th>I/O</th><th>Connected to</th><th>Function</th></tr>
<tr><td>IM[3:0],</td><td>I</td><td>GND/
VDD3</td><td>Select the interface mode.
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>Interface Mode</th><th>DB Pins</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>DBI TypeB 8-bit interface</td><td>DB[7:0]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>DBI TypeB 16-bit interface</td><td>DB[15:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>DBI TypeB 9-bit interface</td><td>DB[8:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>DBI TypeB18-bit interface</td><td>DB[17:0]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>DBI Type C option 1 I</td><td>SDA:In/Out</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>DBI Type C option 3 I</td><td>SDA:In/Out</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>DBI TypeA 8-bit interface</td><td>DB[7:0]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>DBI TypeA 16-bit interface</td><td>DB[15:0]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>DBI TypeA 9-bit interface</td><td>DB[8:0]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>DBI TypeA18-bit interface</td><td>DB[17:0]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>DBI Type C option 1 II</td><td>SDI : In
SDO : Out</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>DBI Type C option 3 II</td><td>SDI : In
SDO : Out</td></tr>
<tr><td>ID</td><td>1</td><td>0</td><td>0</td><td>Serial peripheral interface</td><td>SDI : In
SDO : Out</td></tr>
</table></td></tr>
<tr><td>BC</td><td>O</td><td>LED
Driver IC</td><td>Output pin for brightness signals</td></tr>
<tr><td>BC_CTRL</td><td>O</td><td>LED
Driver IC</td><td>Output pin for brightness signals</td></tr>
<tr><td>CSX</td><td>I</td><td>MPU</td><td>Chip select input pin (“Low” enable).
This pin can be permanently fixed “Low” in MPU interface mode only.</td></tr>
<tr><td>DCX
(SCL)</td><td>I</td><td>MPU</td><td>This pin is used to select “Data or Command” in the parallel interface or 4-wire 8-bit
serial data interface.
When DCX = ’1’, data is selected.
When DCX = ’0’, command is selected.
This pin is used serial interface clock in 3-wire 9-bit serial data interface.
If not used, this pin should be connected to VDD3 or VSS.</td></tr>
<tr><td>WRX
(RWX)</td><td>I</td><td>MPU</td><td>This pin is used to “Write Clock” in 80-series parallel interface.
This pin is used to select “Read / Write Operation” in 68-series parallel interface.
This pin is used serial interface clock in 4-wire 8-bit serial data interface.
If not used, this pin should be connected to VDD3 or VSS.</td></tr>
</table>

RDX (E)	I	MPU	This pin is used to “Read Clock” in 80-series parallel interface. This pin is used to “Read / Write Clock” in 68-series parallel interface. If not used, this pin should be connected to VDD3 or VSS.
SDA (SDI)	I/O	MPU	When IM[3] : Low, Serial in/out signal. When IM[3] : High, Serial input signal. The data is applied on the rising edge of the SCL signal. If not used, fix this pin at VDD3 or VSS.
SDO	O	MPU	Serial output signal. The data is outputted on the falling edge of the SCL signal. If not used, open this pin
DB[17:0]	I/O	MPU	When RGB I/F, DB[17:0] are used to RGB interface data bus. When MPU I/F, DB[17:0] are used to MPU parallel interface data bus.
ENABLE	I	MPU	Data enable signal in RGB I/F mode. If not used, fix this pin at VDD3 or VSS.
VSYNC	I	MPU	Vertical sync. Signal in RGB I/F mode. If not used, fix this pin at VDD3 or VSS.
HSYNC	I	MPU	Horizontal sync. Signal in RGB I/F mode. If not used, fix this pin at VDD3 or VSS.
DOTCLK	I	MPU	Pixel clock signal in RGB I/F mode. If not used, fix this pin at VDD3 or VSS.
RESX	I	MPU or External RC Circuit	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.
EXTC	I	MPU	Select to access Manufacturer command (“Low” : User command only, “High” : User command and Manufacturer command)
TE	O	MPU	Tearing effect output pin to synchronize MPU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. If not used, open this pin.

Table 2 Power Supply Pins

Signal	I/O	Connected to	Function
VCI	-	Power supply	Power supply to liquid crystal power supply analog circuit. Connect to an external power supply.
VDD3	-	Power supply	Power supply to the interface pins: RESETB, CSB, WR, RDB, RS, DB17-0, VSYNC, HSYNC, DOTCLK, ENABLE.
VDD	O	Stabilizing capacitor	Internal logic regulator output to be used as a power supply to internal logic. Connect a stabilizing capacitor.
VDD3_P	-	Power supply	Power supply for LED driver interface. (1.65 ~ 3.3V) If LED driver is not used, fix this pin at VSS.
VSSA	-	Power supply	GND for analog circuits.
VSSC	-	Power supply	GND for voltage step-up circuits.

VSS	-	Power supply	GND for logic circuits.
VSS3	-	Power supply	GND for for I/O block provided from outside

Table 3 Step-Up Circuit

Signal	I/O	Connected to	Function
AVDD	I	Stabilizing capacitor	Internally generated voltage output pad for source driver block. Output voltage of 1st step-up circuit (=2 x VCI1) Input voltage to 2nd step-up circuit. Connect a capacitor for storage function.
VCI1	I	Power supply	Reference input voltage for 1st step-up circuit & 3rd step-up circuit . Connect a capacitor for stabilization. <note 1> VCI1 cannot exceed 3V
VGH	I	Stabilizing capacitor	Positive power output of the 2nd step-up circuit. Gate “ON” level voltage. Connect a capacitor for storage function.
VGL	I	Stabilizing capacitor	Negative power output of the 2nd step-up circuit. Gate “OFF” level voltage. Connect a capacitor for storage function.
VCL	I	Stabilizing capacitor	3rd step-up output voltage. Power supply for generating VCOML block. Connect a capacitor for storage function.
VGS	I	GND or external resistor	Reference level for the grayscale voltage generator. The VGS level can be changed by connecting to an external resistor..
GVDD	O	-	Reference voltage input for grayscale voltage generator. Reference voltage input for VCOMH / VCOML voltage generator. An internal register can be used to adjust the GVDD voltage. Connect a capacitor for stabilization.
C11P, C11M C12P, C12M	I/O	Step-up capacitor	Pins to connect capacitors for the step-up circuit 1.
C31P, C31M C21P, C21M C22P, C22M	I/O	Step-up capacitor	Pins to connect capacitors for the step-up circuit 2. Connect capacitors where they are required according to the step-up factor.

Table 4 LCD Drive

Signal	I/O	Connected to	Function

VCOM	O	TFT panel common electrode	Power supply to TFT panel's common electrode. Output AC voltage with the amplitude VCOMH and VCOML. The alternating cycle is changeable by register setting. Also VCOM output can be started and halted by register setting.
S1 ~ S720	O	LCD	Liquid crystal application voltage. To change the shift direction of segment signal outputs, set the SS bit as follows.
G1 ~ G320	O	LCD	Gate line output signals. VGH: gate line select level VGL: gate line non-select level

Table 5 Others (Test, Dummy Pins)

Signal	I/O	Connected to	Function
TREGB	-		Test pins. Connect to GND or open when not in use.
DUMMYR1 DUMMYR2	-		Short-circuited within the chip for COG contact resistance measurement.
DB18_DUMMY ~ DB23_DUMMY	-		Test pins. Connect to GND or open when not in use.
DUMMY	-		Dummy pin. Leave these pads open

PAD Arrangement

- Chip size : T.B.D
- Chip thickness : T.B.D
- PAD Coordination : PAD center
- Coordination origin : Chip center

- Au BUMP size

(1) 40.00um x 56.00um
No.1 ~ No.232

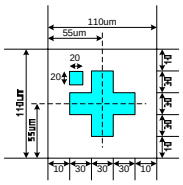
(2) 14.00um x 104.00um
No.233 ~ No.1278

- Au BUMP pitch : see PAD coordination Table
- Au BUMP height : T.B.D
- No. in the figure corresponds to No. in the PAD coordination Table

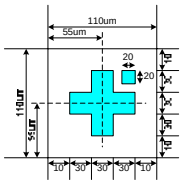
- Alignment mark

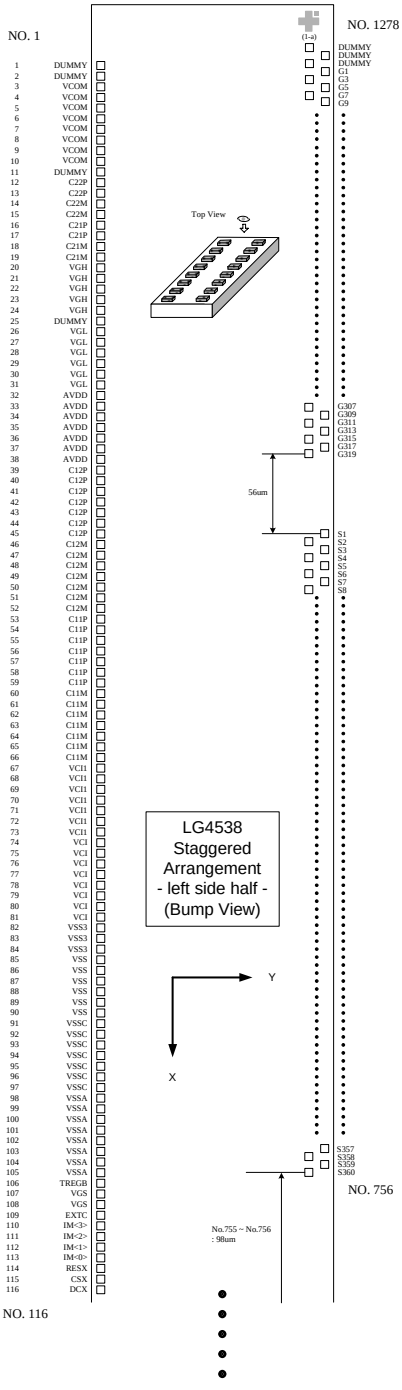
Alignment mark	X	Y
1-a	-7480	260
1-b	7480	260

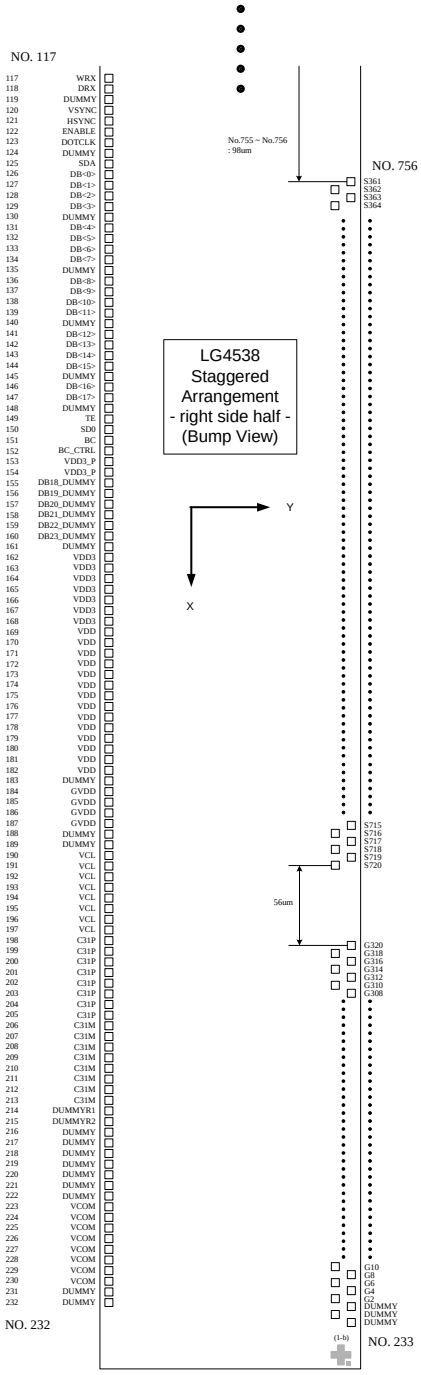
(1-a)



(1-b)







PAD Coordinate

Pad # .	PAD Name	X	Y
1	DUMMY	-7292.5	-285
2	DUMMY	-7232.5	-285
3	VCOM	-7172.5	-285
4	VCOM	-7112.5	-285
5	VCOM	-7052.5	-285
6	VCOM	-6992.5	-285
7	VCOM	-6932.5	-285
8	VCOM	-6872.5	-285
9	VCOM	-6812.5	-285
10	VCOM	-6752.5	-285
11	DUMMY	-6692.5	-285
12	C22P	-6632.5	-285
13	C22P	-6572.5	-285
14	C22M	-6512.5	-285
15	C22M	-6452.5	-285
16	C21P	-6392.5	-285
17	C21P	-6332.5	-285
18	C21M	-6272.5	-285
19	C21M	-6212.5	-285
20	VGH	-6152.5	-285
21	VGH	-6092.5	-285
22	VGH	-6032.5	-285
23	VGH	-5972.5	-285
24	VGH	-5912.5	-285
25	DUMMY	-5852.5	-285
26	VGL	-5792.5	-285
27	VGL	-5732.5	-285
28	VGL	-5672.5	-285
29	VGL	-5612.5	-285
30	VGL	-5552.5	-285
31	VGL	-5492.5	-285
32	AVDD	-5432.5	-285
33	AVDD	-5372.5	-285
34	AVDD	-5312.5	-285
35	AVDD	-5252.5	-285
36	AVDD	-5192.5	-285
37	AVDD	-5132.5	-285
38	AVDD	-5072.5	-285
39	C12P	-5012.5	-285
40	C12P	-4952.5	-285
41	C12P	-4892.5	-285
42	C12P	-4832.5	-285
43	C12P	-4772.5	-285
44	C12P	-4712.5	-285
45	C12P	-4652.5	-285
46	C12M	-4592.5	-285
47	C12M	-4532.5	-285
48	C12M	-4472.5	-285
49	C12M	-4412.5	-285
50	C12M	-4352.5	-285
51	C12M	-4292.5	-285
52	C12M	-4232.5	-285
53	C11P	-4172.5	-285
54	C11P	-4112.5	-285
55	C11P	-4052.5	-285
56	C11P	-3992.5	-285
57	C11P	-3932.5	-285
58	C11P	-3872.5	-285
59	C11P	-3812.5	-285
60	C11M	-3752.5	-285
61	C11M	-3692.5	-285
62	C11M	-3632.5	-285
63	C11M	-3572.5	-285
64	C11M	-3512.5	-285
65	C11M	-3452.5	-285
66	C11M	-3392.5	-285
67	VCI1	-3332.5	-285
68	VCI1	-3272.5	-285
69	VCI1	-3212.5	-285
70	VCI1	-3152.5	-285
71	VCI1	-3092.5	-285
72	VCI1	-3032.5	-285
73	VCI1	-2972.5	-285
74	VCI	-2912.5	-285
75	VCI	-2852.5	-285
76	VCI	-2792.5	-285
77	VCI	-2732.5	-285
78	VCI	-2672.5	-285
79	VCI	-2612.5	-285
80	VCI	-2552.5	-285
81	VCI	-2492.5	-285
82	VSS3	-2432.5	-285
83	VSS3	-2372.5	-285
84	VSS3	-2312.5	-285
85	VSS	-2252.5	-285
86	VSS	-2192.5	-285
87	VSS	-2132.5	-285
88	VSS	-2072.5	-285
89	VSS	-2012.5	-285
90	VSS	-1952.5	-285
91	VSSC	-1892.5	-285
92	VSSC	-1832.5	-285
93	VSSC	-1772.5	-285
94	VSSC	-1712.5	-285
95	VSSC	-1652.5	-285
96	VSSC	-1592.5	-285
97	VSSC	-1532.5	-285
98	VSSA	-1472.5	-285
99	VSSA	-1412.5	-285
100	VSSA	-1352.5	-285
101	VSSA	-1292.5	-285
102	VSSA	-1232.5	-285
103	VSSA	-1172.5	-285
104	VSSA	-1112.5	-285
105	VSSA	-1052.5	-285
106	TREGB	-992.5	-285
107	VGS	-932.5	-285
108	VGS	-872.5	-285
109	EXTC	-812.5	-285
110	IM<3>	-752.5	-285
111	IM<2>	-692.5	-285
112	IM<1>	-632.5	-285
113	IM<0>	-572.5	-285
114	RESX	-512.5	-285
115	CSX	-452.5	-285
116	DCX	-392.5	-285
117	WRX	-332.5	-285
118	RDX	-272.5	-285
119	DUMMY	-212.5	-285
120	VSYNC	-152.5	-285
121	HSYNC	-92.5	-285
122	ENABLE	-32.5	-285
123	DOTCLK	27.5	-285
124	DUMMY	87.5	-285
125	SDA	160	-285
126	DB<0>	245	-285
127	DB<1>	330	-285
128	DB<2>	415	-285
129	DB<3>	500	-285
130	DUMMY	572.5	-285
131	DB<4>	645	-285
132	DB<5>	730	-285
133	DB<6>	815	-285
134	DB<7>	900	-285
135	DUMMY	972.5	-285
136	DB<8>	1045	-285
137	DB<9>	1130	-285
138	DB<10>	1215	-285
139	DB<11>	1300	-285
140	DUMMY	1372.5	-285
141	DB<12>	1445	-285
142	DB<13>	1530	-285
143	DB<14>	1615	-285
144	DB<15>	1700	-285
145	DUMMY	1772.5	-285
146	DB<16>	1845	-285
147	DB<17>	1930	-285

Pad # .	PAD Name	X	Y
148	DUMMY	2002.5	-285
149	TE	2075	-285
150	SD0	2160	-285
151	BC	2245	-285
152	BC_CTRL	2330	-285
153	VDD3_P	2402.5	-285
154	VDD3_P	2462.5	-285
155	DB18_DUMMY	2535	-285
156	DB19_DUMMY	2620	-285
157	DB20_DUMMY	2705	-285
158	DB21_DUMMY	2790	-285
159	DB22_DUMMY	2875	-285
160	DB23_DUMMY	2960	-285
161	DUMMY	3032.5	-285
162	VDD3	3092.5	-285
163	VDD3	3152.5	-285
164	VDD3	3212.5	-285
165	VDD3	3272.5	-285
166	VDD3	3332.5	-285
167	VDD3	3392.5	-285
168	VDD3	3452.5	-285
169	VDD	3512.5	-285
170	VDD	3572.5	-285
171	VDD	3632.5	-285
172	VDD	3692.5	-285
173	VDD	3752.5	-285
174	VDD	3812.5	-285
175	VDD	3872.5	-285
176	VDD	3932.5	-285
177	VDD	3992.5	-285
178	VDD	4052.5	-285
179	VDD	4112.5	-285
180	VDD	4172.5	-285
181	VDD	4232.5	-285
182	VDD	4292.5	-285
183	DUMMY	4352.5	-285
184	GVDD	4412.5	-285
185	GVDD	4472.5	-285
186	GVDD	4532.5	-285
187	GVDD	4592.5	-285
188	DUMMY	4652.5	-285
189	DUMMY	4712.5	-285
190	VCL	4772.5	-285
191	VCL	4832.5	-285
192	VCL	4892.5	-285
193	VCL	4952.5	-285
194	VCL	5012.5	-285
195	VCL	5072.5	-285
196	VCL	5132.5	-285
197	VCL	5192.5	-285
198	C31P	5252.5	-285

Pad # .	PAD Name	X	Y
199	C31P	5312.5	-285
200	C31P	5372.5	-285
201	C31P	5432.5	-285
202	C31P	5492.5	-285
203	C31P	5552.5	-285
204	C31P	5612.5	-285
205	C31P	5672.5	-285
206	C31M	5732.5	-285
207	C31M	5792.5	-285
208	C31M	5852.5	-285
209	C31M	5912.5	-285
210	C31M	5972.5	-285
211	C31M	6032.5	-285
212	C31M	6092.5	-285
213	C31M	6152.5	-285
214	DUMMYR1	6212.5	-285
215	DUMMYR2	6272.5	-285
216	DUMMY	6332.5	-285
217	DUMMY	6392.5	-285
218	DUMMY	6452.5	-285
219	DUMMY	6512.5	-285
220	DUMMY	6572.5	-285
221	DUMMY	6632.5	-285
222	DUMMY	6692.5	-285
223	VCOM	6752.5	-285
224	VCOM	6812.5	-285
225	VCOM	6872.5	-285
226	VCOM	6932.5	-285
227	VCOM	6992.5	-285
228	VCOM	7052.5	-285
229	VCOM	7112.5	-285
230	VCOM	7172.5	-285
231	DUMMY	7232.5	-285
232	DUMMY	7292.5	-285
233	DUMMY	7399	261
234	DUMMY	7385	126
235	DUMMY	7371	261
236	G2	7357	126
237	G4	7343	261
238	G6	7329	126
239	G8	7315	261
240	G10	7301	126
241	G12	7287	261
242	G14	7273	126
243	G16	7259	261
244	G18	7245	126
245	G20	7231	261
246	G22	7217	126
247	G24	7203	261
248	G26	7189	126
249	G28	7175	261

Pad # .	PAD Name	X	Y
250	G30	7161	126
251	G32	7147	261
252	G34	7133	126
253	G36	7119	261
254	G38	7105	126
255	G40	7091	261
256	G42	7077	126
257	G44	7063	261
258	G46	7049	126
259	G48	7035	261
260	G50	7021	126
261	G52	7007	261
262	G54	6993	126
263	G56	6979	261
264	G58	6965	126
265	G60	6951	261
266	G62	6937	126
267	G64	6923	261
268	G66	6909	126
269	G68	6895	261
270	G70	6881	126
271	G72	6867	261
272	G74	6853	126
273	G76	6839	261
274	G78	6825	126
275	G80	6811	261
276	G82	6797	126
277	G84	6783	261
278	G86	6769	126
279	G88	6755	261
280	G90	6741	126
281	G92	6727	261
282	G94	6713	126
283	G96	6699	261
284	G98	6685	126
285	G100	6671	261
286	G102	6657	126
287	G104	6643	261
288	G106	6629	126
289	G108	6615	261
290	G110	6601	126
291	G112	6587	261
292	G114	6573	126
293	G116	6559	261
294	G118	6545	126
295	G120	6531	261
296	G122	6517	126
297	G124	6503	261
298	G126	6489	126
299	G128	6475	261
300	G130	6461	126

Pad # .	PAD Name	X	Y
301	G132	6447	261
302	G134	6433	126
303	G136	6419	261
304	G138	6405	126
305	G140	6391	261
306	G142	6377	126
307	G144	6363	261
308	G146	6349	126
309	G148	6335	261
310	G150	6321	126
311	G152	6307	261
312	G154	6293	126
313	G156	6279	261
314	G158	6265	126
315	G160	6251	261
316	G162	6237	126
317	G164	6223	261
318	G166	6209	126
319	G168	6195	261
320	G170	6181	126
321	G172	6167	261
322	G174	6153	126
323	G176	6139	261
324	G178	6125	126
325	G180	6111	261
326	G182	6097	126
327	G184	6083	261
328	G186	6069	126
329	G188	6055	261
330	G190	6041	126
331	G192	6027	261
332	G194	6013	126
333	G196	5999	261
334	G198	5985	126
335	G200	5971	261
336	G202	5957	126
337	G204	5943	261
338	G206	5929	126
339	G208	5915	261
340	G210	5901	126
341	G212	5887	261
342	G214	5873	126
343	G216	5859	261
344	G218	5845	126
345	G220	5831	261
346	G222	5817	126
347	G224	5803	261
348	G226	5789	126
349	G228	5775	261
350	G230	5761	126
351	G232	5747	261

Pad # .	PAD Name	X	Y
352	G234	5733	126
353	G236	5719	261
354	G238	5705	126
355	G240	5691	261
356	G242	5677	126
357	G244	5663	261
358	G246	5649	126
359	G248	5635	261
360	G250	5621	126
361	G252	5607	261
362	G254	5593	126
363	G256	5579	261
364	G258	5565	126
365	G260	5551	261
366	G262	5537	126
367	G264	5523	261
368	G266	5509	126
369	G268	5495	261
370	G270	5481	126
371	G272	5467	261
372	G274	5453	126
373	G276	5439	261
374	G278	5425	126
375	G280	5411	261
376	G282	5397	126
377	G284	5383	261
378	G286	5369	126
379	G288	5355	261
380	G290	5341	126
381	G292	5327	261
382	G294	5313	126
383	G296	5299	261
384	G298	5285	126
385	G300	5271	261
386	G302	5257	126
387	G304	5243	261
388	G306	5229	126
389	G308	5215	261
390	G310	5201	126
391	G312	5187	261
392	G314	5173	126
393	G316	5159	261
394	G318	5145	126
395	G320	5131	261
396	S720	5075	126
397	S719	5061	261
398	S718	5047	126
399	S717	5033	261
400	S716	5019	126
401	S715	5005	261
402	S714	4991	126

Pad # .	PAD Name	X	Y
403	S713	4977	261
404	S712	4963	126
405	S711	4949	261
406	S710	4935	126
407	S709	4921	261
408	S708	4907	126
409	S707	4893	261
410	S706	4879	126
411	S705	4865	261
412	S704	4851	126
413	S703	4837	261
414	S702	4823	126
415	S701	4809	261
416	S700	4795	126
417	S699	4781	261
418	S698	4767	126
419	S697	4753	261
420	S696	4739	126
421	S695	4725	261
422	S694	4711	126
423	S693	4697	261
424	S692	4683	126
425	S691	4669	261
426	S690	4655	126
427	S689	4641	261
428	S688	4627	126
429	S687	4613	261
430	S686	4599	126
431	S685	4585	261
432	S684	4571	126
433	S683	4557	261
434	S682	4543	126
435	S681	4529	261
436	S680	4515	126
437	S679	4501	261
438	S678	4487	126
439	S677	4473	261
440	S676	4459	126
441	S675	4445	261
442	S674	4431	126
443	S673	4417	261
444	S672	4403	126
445	S671	4389	261
446	S670	4375	126
447	S669	4361	261
448	S668	4347	126
449	S667	4333	261
450	S666	4319	126
451	S665	4305	261
452	S664	4291	126
453	S663	4277	261

Pad # .	PAD Name	X	Y
454	S662	4263	126
455	S661	4249	261
456	S660	4235	126
457	S659	4221	261
458	S658	4207	126
459	S657	4193	261
460	S656	4179	126
461	S655	4165	261
462	S654	4151	126
463	S653	4137	261
464	S652	4123	126
465	S651	4109	261
466	S650	4095	126
467	S649	4081	261
468	S648	4067	126
469	S647	4053	261
470	S646	4039	126
471	S645	4025	261
472	S644	4011	126
473	S643	3997	261
474	S642	3983	126
475	S641	3969	261
476	S640	3955	126
477	S639	3941	261
478	S638	3927	126
479	S637	3913	261
480	S636	3899	126
481	S635	3885	261
482	S634	3871	126
483	S633	3857	261
484	S632	3843	126
485	S631	3829	261
486	S630	3815	126
487	S629	3801	261
488	S628	3787	126
489	S627	3773	261
490	S626	3759	126
491	S625	3745	261
492	S624	3731	126
493	S623	3717	261
494	S622	3703	126
495	S621	3689	261
496	S620	3675	126
497	S619	3661	261
498	S618	3647	126
499	S617	3633	261
500	S616	3619	126
501	S615	3605	261
502	S614	3591	126
503	S613	3577	261
504	S612	3563	126

Pad # .	PAD Name	X	Y
505	S611	3549	261
506	S610	3535	126
507	S609	3521	261
508	S608	3507	126
509	S607	3493	261
510	S606	3479	126
511	S605	3465	261
512	S604	3451	126
513	S603	3437	261
514	S602	3423	126
515	S601	3409	261
516	S600	3395	126
517	S599	3381	261
518	S598	3367	126
519	S597	3353	261
520	S596	3339	126
521	S595	3325	261
522	S594	3311	126
523	S593	3297	261
524	S592	3283	126
525	S591	3269	261
526	S590	3255	126
527	S589	3241	261
528	S588	3227	126
529	S587	3213	261
530	S586	3199	126
531	S585	3185	261
532	S584	3171	126
533	S583	3157	261
534	S582	3143	126
535	S581	3129	261
536	S580	3115	126
537	S579	3101	261
538	S578	3087	126
539	S577	3073	261
540	S576	3059	126
541	S575	3045	261
542	S574	3031	126
543	S573	3017	261
544	S572	3003	126
545	S571	2989	261
546	S570	2975	126
547	S569	2961	261
548	S568	2947	126
549	S567	2933	261
550	S566	2919	126
551	S565	2905	261
552	S564	2891	126
553	S563	2877	261
554	S562	2863	126
555	S561	2849	261

Pad # .	PAD Name	X	Y
556	S560	2835	126
557	S559	2821	261
558	S558	2807	126
559	S557	2793	261
560	S556	2779	126
561	S555	2765	261
562	S554	2751	126
563	S553	2737	261
564	S552	2723	126
565	S551	2709	261
566	S550	2695	126
567	S549	2681	261
568	S548	2667	126
569	S547	2653	261
570	S546	2639	126
571	S545	2625	261
572	S544	2611	126
573	S543	2597	261
574	S542	2583	126
575	S541	2569	261
576	S540	2555	126
577	S539	2541	261
578	S538	2527	126
579	S537	2513	261
580	S536	2499	126
581	S535	2485	261
582	S534	2471	126
583	S533	2457	261
584	S532	2443	126
585	S531	2429	261
586	S530	2415	126
587	S529	2401	261
588	S528	2387	126
589	S527	2373	261
590	S526	2359	126
591	S525	2345	261
592	S524	2331	126
593	S523	2317	261
594	S522	2303	126
595	S521	2289	261
596	S520	2275	126
597	S519	2261	261
598	S518	2247	126
599	S517	2233	261
600	S516	2219	126
601	S515	2205	261
602	S514	2191	126
603	S513	2177	261
604	S512	2163	126
605	S511	2149	261
606	S510	2135	126

Pad # .	PAD Name	X	Y
607	S509	2121	261
608	S508	2107	126
609	S507	2093	261
610	S506	2079	126
611	S505	2065	261
612	S504	2051	126
613	S503	2037	261
614	S502	2023	126
615	S501	2009	261
616	S500	1995	126
617	S499	1981	261
618	S498	1967	126
619	S497	1953	261
620	S496	1939	126
621	S495	1925	261
622	S494	1911	126
623	S493	1897	261
624	S492	1883	126
625	S491	1869	261
626	S490	1855	126
627	S489	1841	261
628	S488	1827	126
629	S487	1813	261
630	S486	1799	126
631	S485	1785	261
632	S484	1771	126
633	S483	1757	261
634	S482	1743	126
635	S481	1729	261
636	S480	1715	126
637	S479	1701	261
638	S478	1687	126
639	S477	1673	261
640	S476	1659	126
641	S475	1645	261
642	S474	1631	126
643	S473	1617	261
644	S472	1603	126
645	S471	1589	261
646	S470	1575	126
647	S469	1561	261
648	S468	1547	126
649	S467	1533	261
650	S466	1519	126
651	S465	1505	261
652	S464	1491	126
653	S463	1477	261
654	S462	1463	126
655	S461	1449	261
656	S460	1435	126
657	S459	1421	261

Pad # .	PAD Name	X	Y
658	S458	1407	126
659	S457	1393	261
660	S456	1379	126
661	S455	1365	261
662	S454	1351	126
663	S453	1337	261
664	S452	1323	126
665	S451	1309	261
666	S450	1295	126
667	S449	1281	261
668	S448	1267	126
669	S447	1253	261
670	S446	1239	126
671	S445	1225	261
672	S444	1211	126
673	S443	1197	261
674	S442	1183	126
675	S441	1169	261
676	S440	1155	126
677	S439	1141	261
678	S438	1127	126
679	S437	1113	261
680	S436	1099	126
681	S435	1085	261
682	S434	1071	126
683	S433	1057	261
684	S432	1043	126
685	S431	1029	261
686	S430	1015	126
687	S429	1001	261
688	S428	987	126
689	S427	973	261
690	S426	959	126
691	S425	945	261
692	S424	931	126
693	S423	917	261
694	S422	903	126
695	S421	889	261
696	S420	875	126
697	S419	861	261
698	S418	847	126
699	S417	833	261
700	S416	819	126
701	S415	805	261
702	S414	791	126
703	S413	777	261
704	S412	763	126
705	S411	749	261
706	S410	735	126
707	S409	721	261
708	S408	707	126

Pad # .	PAD Name	X	Y
709	S407	693	261
710	S406	679	126
711	S405	665	261
712	S404	651	126
713	S403	637	261
714	S402	623	126
715	S401	609	261
716	S400	595	126
717	S399	581	261
718	S398	567	126
719	S397	553	261
720	S396	539	126
721	S395	525	261
722	S394	511	126
723	S393	497	261
724	S392	483	126
725	S391	469	261
726	S390	455	126
727	S389	441	261
728	S388	427	126
729	S387	413	261
730	S386	399	126
731	S385	385	261
732	S384	371	126
733	S383	357	261
734	S382	343	126
735	S381	329	261
736	S380	315	126
737	S379	301	261
738	S378	287	126
739	S377	273	261
740	S376	259	126
741	S375	245	261
742	S374	231	126
743	S373	217	261
744	S372	203	126
745	S371	189	261
746	S370	175	126
747	S369	161	261
748	S368	147	126
749	S367	133	261
750	S366	119	126
751	S365	105	261
752	S364	91	126
753	S363	77	261
754	S362	63	126
755	S361	49	261
756	S360	-49	126
757	S359	-63	261
758	S358	-77	126
759	S357	-91	261

Pad # .	PAD Name	X	Y
760	S356	-105	126
761	S355	-119	261
762	S354	-133	126
763	S353	-147	261
764	S352	-161	126
765	S351	-175	261
766	S350	-189	126
767	S349	-203	261
768	S348	-217	126
769	S347	-231	261
770	S346	-245	126
771	S345	-259	261
772	S344	-273	126
773	S343	-287	261
774	S342	-301	126
775	S341	-315	261
776	S340	-329	126
777	S339	-343	261
778	S338	-357	126
779	S337	-371	261
780	S336	-385	126
781	S335	-399	261
782	S334	-413	126
783	S333	-427	261
784	S332	-441	126
785	S331	-455	261
786	S330	-469	126
787	S329	-483	261
788	S328	-497	126
789	S327	-511	261
790	S326	-525	126
791	S325	-539	261
792	S324	-553	126
793	S323	-567	261
794	S322	-581	126
795	S321	-595	261
796	S320	-609	126
797	S319	-623	261
798	S318	-637	126
799	S317	-651	261
800	S316	-665	126
801	S315	-679	261
802	S314	-693	126
803	S313	-707	261
804	S312	-721	126
805	S311	-735	261
806	S310	-749	126
807	S309	-763	261
808	S308	-777	126
809	S307	-791	261
810	S306	-805	126

Pad # .	PAD Name	X	Y
811	S305	-819	261
812	S304	-833	126
813	S303	-847	261
814	S302	-861	126
815	S301	-875	261
816	S300	-889	126
817	S299	-903	261
818	S298	-917	126
819	S297	-931	261
820	S296	-945	126
821	S295	-959	261
822	S294	-973	126
823	S293	-987	261
824	S292	-1001	126
825	S291	-1015	261
826	S290	-1029	126
827	S289	-1043	261
828	S288	-1057	126
829	S287	-1071	261
830	S286	-1085	126
831	S285	-1099	261
832	S284	-1113	126
833	S283	-1127	261
834	S282	-1141	126
835	S281	-1155	261
836	S280	-1169	126
837	S279	-1183	261
838	S278	-1197	126
839	S277	-1211	261
840	S276	-1225	126
841	S275	-1239	261
842	S274	-1253	126
843	S273	-1267	261
844	S272	-1281	126
845	S271	-1295	261
846	S270	-1309	126
847	S269	-1323	261
848	S268	-1337	126
849	S267	-1351	261
850	S266	-1365	126
851	S265	-1379	261
852	S264	-1393	126
853	S263	-1407	261
854	S262	-1421	126
855	S261	-1435	261
856	S260	-1449	126
857	S259	-1463	261
858	S258	-1477	126
859	S257	-1491	261
860	S256	-1505	126
861	S255	-1519	261

Pad # .	PAD Name	X	Y
862	S254	-1533	126
863	S253	-1547	261
864	S252	-1561	126
865	S251	-1575	261
866	S250	-1589	126
867	S249	-1603	261
868	S248	-1617	126
869	S247	-1631	261
870	S246	-1645	126
871	S245	-1659	261
872	S244	-1673	126
873	S243	-1687	261
874	S242	-1701	126
875	S241	-1715	261
876	S240	-1729	126
877	S239	-1743	261
878	S238	-1757	126
879	S237	-1771	261
880	S236	-1785	126
881	S235	-1799	261
882	S234	-1813	126
883	S233	-1827	261
884	S232	-1841	126
885	S231	-1855	261
886	S230	-1869	126
887	S229	-1883	261
888	S228	-1897	126
889	S227	-1911	261
890	S226	-1925	126
891	S225	-1939	261
892	S224	-1953	126
893	S223	-1967	261
894	S222	-1981	126
895	S221	-1995	261
896	S220	-2009	126
897	S219	-2023	261
898	S218	-2037	126
899	S217	-2051	261
900	S216	-2065	126
901	S215	-2079	261
902	S214	-2093	126
903	S213	-2107	261
904	S212	-2121	126
905	S211	-2135	261
906	S210	-2149	126
907	S209	-2163	261
908	S208	-2177	126
909	S207	-2191	261
910	S206	-2205	126
911	S205	-2219	261
912	S204	-2233	126

Pad # .	PAD Name	X	Y
913	S203	-2247	261
914	S202	-2261	126
915	S201	-2275	261
916	S200	-2289	126
917	S199	-2303	261
918	S198	-2317	126
919	S197	-2331	261
920	S196	-2345	126
921	S195	-2359	261
922	S194	-2373	126
923	S193	-2387	261
924	S192	-2401	126
925	S191	-2415	261
926	S190	-2429	126
927	S189	-2443	261
928	S188	-2457	126
929	S187	-2471	261
930	S186	-2485	126
931	S185	-2499	261
932	S184	-2513	126
933	S183	-2527	261
934	S182	-2541	126
935	S181	-2555	261
936	S180	-2569	126
937	S179	-2583	261
938	S178	-2597	126
939	S177	-2611	261
940	S176	-2625	126
941	S175	-2639	261
942	S174	-2653	126
943	S173	-2667	261
944	S172	-2681	126
945	S171	-2695	261
946	S170	-2709	126
947	S169	-2723	261
948	S168	-2737	126
949	S167	-2751	261
950	S166	-2765	126
951	S165	-2779	261
952	S164	-2793	126
953	S163	-2807	261
954	S162	-2821	126
955	S161	-2835	261
956	S160	-2849	126
957	S159	-2863	261
958	S158	-2877	126
959	S157	-2891	261
960	S156	-2905	126
961	S155	-2919	261
962	S154	-2933	126
963	S153	-2947	261

Pad # .	PAD Name	X	Y
964	S152	-2961	126
965	S151	-2975	261
966	S150	-2989	126
967	S149	-3003	261
968	S148	-3017	126
969	S147	-3031	261
970	S146	-3045	126
971	S145	-3059	261
972	S144	-3073	126
973	S143	-3087	261
974	S142	-3101	126
975	S141	-3115	261
976	S140	-3129	126
977	S139	-3143	261
978	S138	-3157	126
979	S137	-3171	261
980	S136	-3185	126
981	S135	-3199	261
982	S134	-3213	126
983	S133	-3227	261
984	S132	-3241	126
985	S131	-3255	261
986	S130	-3269	126
987	S129	-3283	261
988	S128	-3297	126
989	S127	-3311	261
990	S126	-3325	126
991	S125	-3339	261
992	S124	-3353	126
993	S123	-3367	261
994	S122	-3381	126
995	S121	-3395	261
996	S120	-3409	126
997	S119	-3423	261
998	S118	-3437	126
999	S117	-3451	261
1000	S116	-3465	126
1001	S115	-3479	261
1002	S114	-3493	126
1003	S113	-3507	261
1004	S112	-3521	126
1005	S111	-3535	261
1006	S110	-3549	126
1007	S109	-3563	261
1008	S108	-3577	126
1009	S107	-3591	261
1010	S106	-3605	126
1011	S105	-3619	261
1012	S104	-3633	126
1013	S103	-3647	261
1014	S102	-3661	126

Pad # .	PAD Name	X	Y
1015	S101	-3675	261
1016	S100	-3689	126
1017	S99	-3703	261
1018	S98	-3717	126
1019	S97	-3731	261
1020	S96	-3745	126
1021	S95	-3759	261
1022	S94	-3773	126
1023	S93	-3787	261
1024	S92	-3801	126
1025	S91	-3815	261
1026	S90	-3829	126
1027	S89	-3843	261
1028	S88	-3857	126
1029	S87	-3871	261
1030	S86	-3885	126
1031	S85	-3899	261
1032	S84	-3913	126
1033	S83	-3927	261
1034	S82	-3941	126
1035	S81	-3955	261
1036	S80	-3969	126
1037	S79	-3983	261
1038	S78	-3997	126
1039	S77	-4011	261
1040	S76	-4025	126
1041	S75	-4039	261
1042	S74	-4053	126
1043	S73	-4067	261
1044	S72	-4081	126
1045	S71	-4095	261
1046	S70	-4109	126
1047	S69	-4123	261
1048	S68	-4137	126
1049	S67	-4151	261
1050	S66	-4165	126
1051	S65	-4179	261
1052	S64	-4193	126
1053	S63	-4207	261
1054	S62	-4221	126
1055	S61	-4235	261
1056	S60	-4249	126
1057	S59	-4263	261
1058	S58	-4277	126
1059	S57	-4291	261
1060	S56	-4305	126
1061	S55	-4319	261
1062	S54	-4333	126
1063	S53	-4347	261
1064	S52	-4361	126
1065	S51	-4375	261

Pad # .	PAD Name	X	Y
1066	S50	-4389	126
1067	S49	-4403	261
1068	S48	-4417	126
1069	S47	-4431	261
1070	S46	-4445	126
1071	S45	-4459	261
1072	S44	-4473	126
1073	S43	-4487	261
1074	S42	-4501	126
1075	S41	-4515	261
1076	S40	-4529	126
1077	S39	-4543	261
1078	S38	-4557	126
1079	S37	-4571	261
1080	S36	-4585	126
1081	S35	-4599	261
1082	S34	-4613	126
1083	S33	-4627	261
1084	S32	-4641	126
1085	S31	-4655	261
1086	S30	-4669	126
1087	S29	-4683	261
1088	S28	-4697	126
1089	S27	-4711	261
1090	S26	-4725	126
1091	S25	-4739	261
1092	S24	-4753	126
1093	S23	-4767	261
1094	S22	-4781	126
1095	S21	-4795	261
1096	S20	-4809	126
1097	S19	-4823	261
1098	S18	-4837	126
1099	S17	-4851	261
1100	S16	-4865	126
1101	S15	-4879	261
1102	S14	-4893	126
1103	S13	-4907	261
1104	S12	-4921	126
1105	S11	-4935	261
1106	S10	-4949	126
1107	S9	-4963	261
1108	S8	-4977	126
1109	S7	-4991	261
1110	S6	-5005	126
1111	S5	-5019	261
1112	S4	-5033	126
1113	S3	-5047	261
1114	S2	-5061	126
1115	S1	-5075	261
1116	G319	-5131	126

Pad # .	PAD Name	X	Y
1117	G317	-5145	261
1118	G315	-5159	126
1119	G313	-5173	261
1120	G311	-5187	126
1121	G309	-5201	261
1122	G307	-5215	126
1123	G305	-5229	261
1124	G303	-5243	126
1125	G301	-5257	261
1126	G299	-5271	126
1127	G297	-5285	261
1128	G295	-5299	126
1129	G293	-5313	261
1130	G291	-5327	126
1131	G289	-5341	261
1132	G287	-5355	126
1133	G285	-5369	261
1134	G283	-5383	126
1135	G281	-5397	261
1136	G279	-5411	126
1137	G277	-5425	261
1138	G275	-5439	126
1139	G273	-5453	261
1140	G271	-5467	126
1141	G269	-5481	261
1142	G267	-5495	126
1143	G265	-5509	261
1144	G263	-5523	126
1145	G261	-5537	261
1146	G259	-5551	126
1147	G257	-5565	261
1148	G255	-5579	126
1149	G253	-5593	261
1150	G251	-5607	126
1151	G249	-5621	261
1152	G247	-5635	126
1153	G245	-5649	261
1154	G243	-5663	126
1155	G241	-5677	261
1156	G239	-5691	126
1157	G237	-5705	261
1158	G235	-5719	126
1159	G233	-5733	261
1160	G231	-5747	126
1161	G229	-5761	261
1162	G227	-5775	126
1163	G225	-5789	261
1164	G223	-5803	126
1165	G221	-5817	261
1166	G219	-5831	126
1167	G217	-5845	261

Pad # .	PAD Name	X	Y
1168	G215	-5859	126
1169	G213	-5873	261
1170	G211	-5887	126
1171	G209	-5901	261
1172	G207	-5915	126
1173	G205	-5929	261
1174	G203	-5943	126
1175	G201	-5957	261
1176	G199	-5971	126
1177	G197	-5985	261
1178	G195	-5999	126
1179	G193	-6013	261
1180	G191	-6027	126
1181	G189	-6041	261
1182	G187	-6055	126
1183	G185	-6069	261
1184	G183	-6083	126
1185	G181	-6097	261
1186	G179	-6111	126
1187	G177	-6125	261
1188	G175	-6139	126
1189	G173	-6153	261
1190	G171	-6167	126
1191	G169	-6181	261
1192	G167	-6195	126
1193	G165	-6209	261
1194	G163	-6223	126
1195	G161	-6237	261
1196	G159	-6251	126
1197	G157	-6265	261
1198	G155	-6279	126
1199	G153	-6293	261
1200	G151	-6307	126
1201	G149	-6321	261
1202	G147	-6335	126
1203	G145	-6349	261
1204	G143	-6363	126
1205	G141	-6377	261
1206	G139	-6391	126
1207	G137	-6405	261
1208	G135	-6419	126
1209	G133	-6433	261
1210	G131	-6447	126
1211	G129	-6461	261
1212	G127	-6475	126
1213	G125	-6489	261
1214	G123	-6503	126
1215	G121	-6517	261
1216	G119	-6531	126
1217	G117	-6545	261
1218	G115	-6559	126

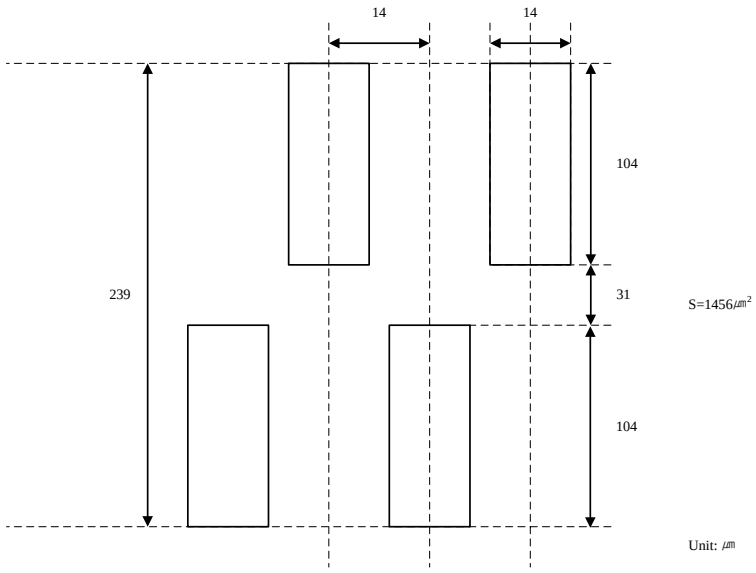
Pad # .	PAD Name	X	Y
1219	G113	-6573	261
1220	G111	-6587	126
1221	G109	-6601	261
1222	G107	-6615	126
1223	G105	-6629	261
1224	G103	-6643	126
1225	G101	-6657	261
1226	G99	-6671	126
1227	G97	-6685	261
1228	G95	-6699	126
1229	G93	-6713	261
1230	G91	-6727	126
1231	G89	-6741	261
1232	G87	-6755	126
1233	G85	-6769	261
1234	G83	-6783	126
1235	G81	-6797	261
1236	G79	-6811	126
1237	G77	-6825	261
1238	G75	-6839	126
1239	G73	-6853	261
1240	G71	-6867	126
1241	G69	-6881	261
1242	G67	-6895	126
1243	G65	-6909	261
1244	G63	-6923	126
1245	G61	-6937	261
1246	G59	-6951	126
1247	G57	-6965	261
1248	G55	-6979	126
1249	G53	-6993	261
1250	G51	-7007	126
1251	G49	-7021	261
1252	G47	-7035	126
1253	G45	-7049	261
1254	G43	-7063	126
1255	G41	-7077	261
1256	G39	-7091	126
1257	G37	-7105	261
1258	G35	-7119	126
1259	G33	-7133	261
1260	G31	-7147	126
1261	G29	-7161	261
1262	G27	-7175	126
1263	G25	-7189	261
1264	G23	-7203	126
1265	G21	-7217	261
1266	G19	-7231	126
1267	G17	-7245	261
1268	G15	-7259	126
1269	G13	-7273	261

Pad # .	PAD Name	X	Y
1270	G11	-7287	126
1271	G9	-7301	261
1272	G7	-7315	126
1273	G5	-7329	261
1274	G3	-7343	126
1275	G1	-7357	261
1276	DUMMY	-7371	126
1277	DUMMY	-7385	261
1278	DUMMY	-7399	126

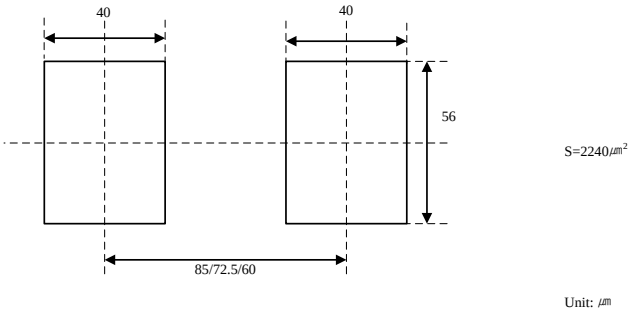
Alignment mark	X	Y
1-a (Left)	-7480	260
1-b (Right)	7480	260

Bump Arrangement

S<1> ~ S<720>
G<1> ~ G<320>
(No. 233 ~ No. 1278)



I/O PINS
(No. 1 ~ No. 232)



Block Function

System Interface

The LG4538 supports MIPI DBI TypeA,B (18/16/9/8 bits), MIPI DBI TypeC (Option1 and Option 3) , a Serial Peripheral Interface(SPI). The interface mode is selected by setting the IM[3:0] pins.

Table 6 Interface Mode Selection

IM[3]	IM[2]	IM[1]	IM[0]	Interface	Used Pin	Available color number
0	0	0	0	MIPI DBI Type B 8bits	DB[7:0]	262,144/65,536 colors
0	0	0	1	MIPI DBI Type B 16bits	DB[15:0]	262,144/65,536 colors
0	0	1	0	MIPI DBI Type B 9bits	DB[8:0]	262,144/65,536 colors
0	0	1	1	MIPI DBI Type B 18bits	DB[17:0]	262,144/65,536 colors
0	1	0	1	MIPI DBI Type C Optoin 1 I	SDA	262,144/65,536 colors
0	1	1	0	MIPI DBI Type C Optoin 3 I	SDA	262,144/65,536 colors
1	0	0	0	MIPI DBI Type A 8bits	DB[7:0]	262,144/65,536 colors
1	0	0	1	MIPI DBI Type A 16bits	DB[15:0]	262,144/65,536 colors
1	0	1	0	MIPI DBI Type A 9bits	DB[8:0]	262,144/65,536 colors
1	0	1	1	MIPI DBI Type A 18bits	DB[17:0]	262,144/65,536 colors
1	1	0	1	MIPI DBI Type C Optoin 1 II	SDI, SDO	262,144/65,536 colors
1	1	1	0	MIPI DBI Type C Optoin 3 II	SDI, SDO	262,144/65,536 colors
ID	1	0	0	Serial peripheral interface	SDI, SDO	262,144/65,536 colors

Set number of colors using set_pixel_format : 3Ah

(a) MIPI DBI Type A,B (18/16/9/8 bits)

The LG4538 supports MIPI DBI TypeA and Type B (18/16/9/8 bits) that uses command method which has 8-bit command registers and 8-bit parameter registers. Also, the LG4538 has an 18-bit write register (WDR) and read register (RDR). The WDR is used to store data temporarily that is automatically written to the internal frame memory through internal operation of the chip.

The RDR is used to temporarily store the data read out from the frame memory. When reading data from the frame memory, the LG4538 first stores the data in the RDR. For this reason, invalid data is sent to the data bus at first and valid data is sent as the LG4538 reads second and subsequent data from the frame memory.

Table 7 Register Selection

Type B		Type A		Function
WRX	RDX	R/W	DCX	
0	1	0	0	Write an index to IR
0	1	0	1	Write to control registers or the internal GRAM via WDR
1	0	1	1	Read from the internal GRAM via RDR

(c) MIPI DBI Type C (Option 1 and Option 3)

The LG4538 supports 9-bit(Option 1) and 8-bit(Option 3) serial interface that uses signals CSX, DCX, SCL, SDI/SDA and SDO.

(d) Serial Peripheral Interface

The LG4538 supports serial perilpheral interface that uses signals CSX, SCL, SDI and SDO.

Table 8 Register Selection (Serial Peripheral Interface)

Start Byte (SPI)		**Function**
R/W	**RS**	
0	0	Write an index to IR
0	1	Write into control registers and the internal GRAM via WDR
1	1	Read from the internal GRAM via RDR

External Display Interface

The LG4538 supports VSYNC and MIPI DPI as external display interface for video image

When DBI is selected, display data is written in synchronization with TE signal which is generated from internal clock to prevent flicker on the panel.

When DPI is selected, externally supplied VSYNC, HSYNC and DOTCLK signals drive the chip. Display data (DB[17:0]) is written in synchronization with those synchronous signals following data ENABLE signal (ENABLE).

This ENABLEs updating image data without flicker on the panel.

Address Counter (AC)

The address counter (AC) gives an address to the frame memory. Address information defined by CDR and PR is transferred to the AC. The AC is automatically incremented/decremented by 1 as the LG4538 writes/reads data to/from the frame memory. Display data is may be written only to the rectangular area defined in the frame memory.

Graphics RAM (GRAM)

GRAM is graphics RAM storing bit-pattern data of 172,800 (240 x 320x 18bit) bytes, using 18 bits per pixel.

Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates a liquid crystal drive voltage according to grayscale data set in the γ-correction register to display in 262,144 colors. For details, see the “γ-Correction Register” section.

Timing Generator

The timing generator generates a timing signal for operation of internal circuits such as the internal GRAM. The timing for the display operation such as RAM read operation and the timing for the internal operation such as access from the MPU are generated in the way not to interfere each other.

Oscillator (OSC)

LG4538 generates RC oscillation with an internal oscillation resistor. The frame rate is adjusted by the register setting.

LCD Driver Circuit

The LCD driver circuit consists of a 720-channel source driver (S1~S720). The display pattern data is latched when 240RGB pixels of data are input. The voltage is output from the source driver according to the latched data. The shift direction of source output can be changed by setting SS bit (C0h).

The gate driver circuit consists of a 320-channel gate driver (G1~G320). The voltage at VGH level or VGL level is output from the gate driver. The shift direction of gate output can be changed by GS bit (C0h). The scan mode of the gate driver can be changed by SM bit (C0h) according to the mounting condition.

LCD Drive Power Supply Circuit

The LCD drive power supply circuit generates the voltage levels GVDD, VGH, VGL and VCOM for driving an LCD.

Internal logic power supply regulator

The internal logic power supply regulator generates internal logic power supply VDD.

Backlight Control Circuit

Backlight control circuit adjusts backlight brightness according to histogram of the image to reduce power consumption at the backlight. Brightness of the backlight and display data is adjusted.

System Interface (Display Bus Interface, DBI)

DBI Type A

The LG4538 adopts 18-/16-/9-/ 8-bit bus display command interface to interface to high-performance host processor. The LG4538 starts transfer the data after storing control information of externally sent 18-/16-/9-/8-bit data in the command register (CDR) and the parameter register (PR).

Write CyCle Sequence

In write cycle, data and/or command are written to the LG4538 via the interface between the LG4538 and the host processor. Each step of write cycle sequence (E low, E high, E low) comprises three control signals (DCX,RWX, E) and 8-, 9-, 16-, or 18bit data. The DCX bit indicates signal that is used to select command or data sent on the data bus.

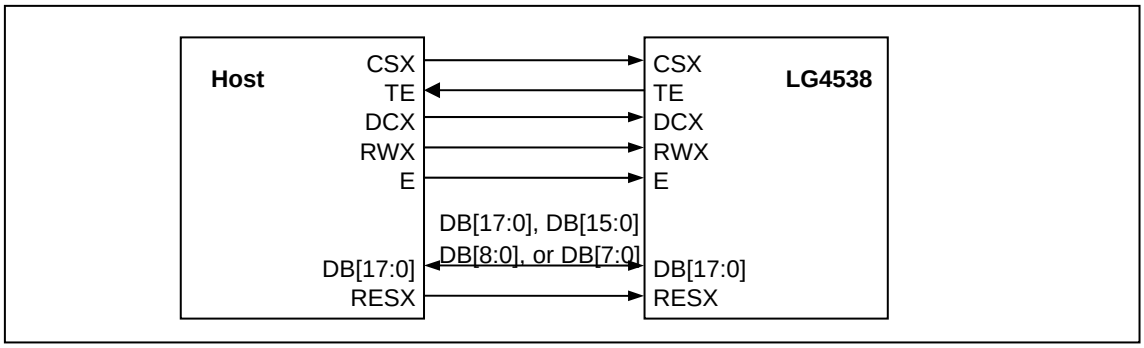
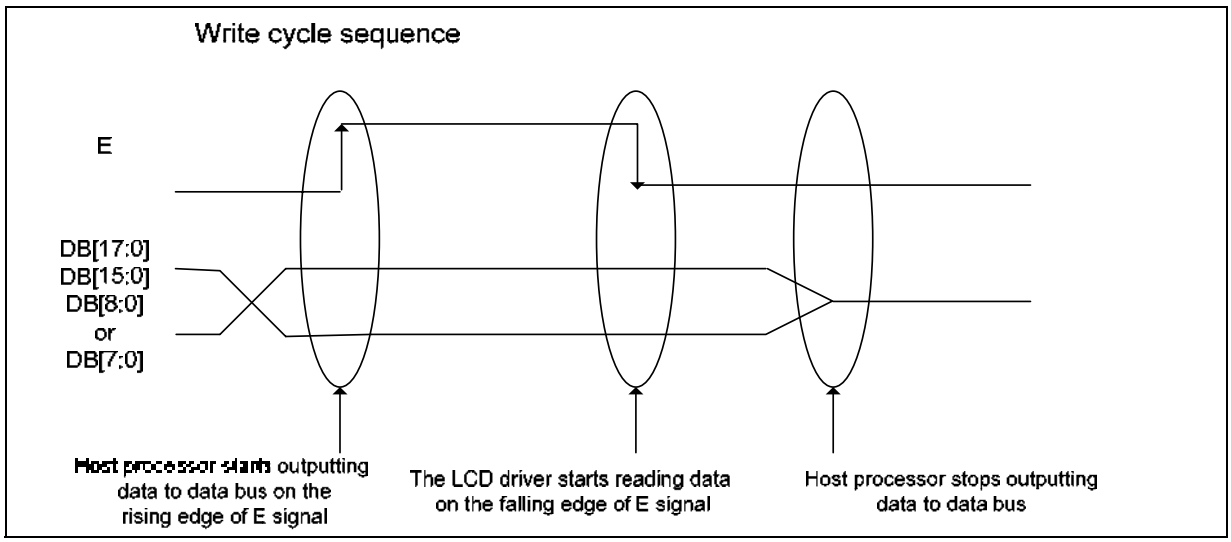


Figure 2 DBI Type A

When DCX=”1”, data on the above data bus is image data or command parameter. When DCX = 0, data is command.

See the figure below for the write cycle sequence.



Note : E is not a synchronous singal (can be halted).

Figure 3 Write Cycle sequence

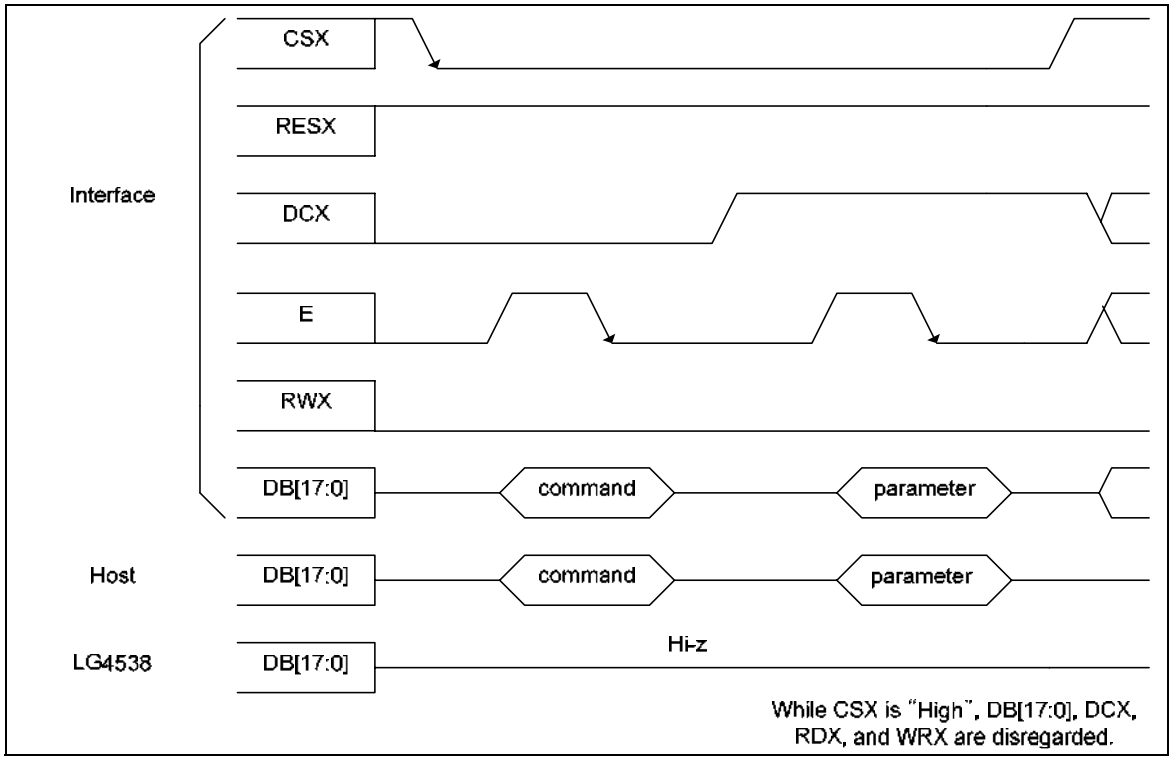
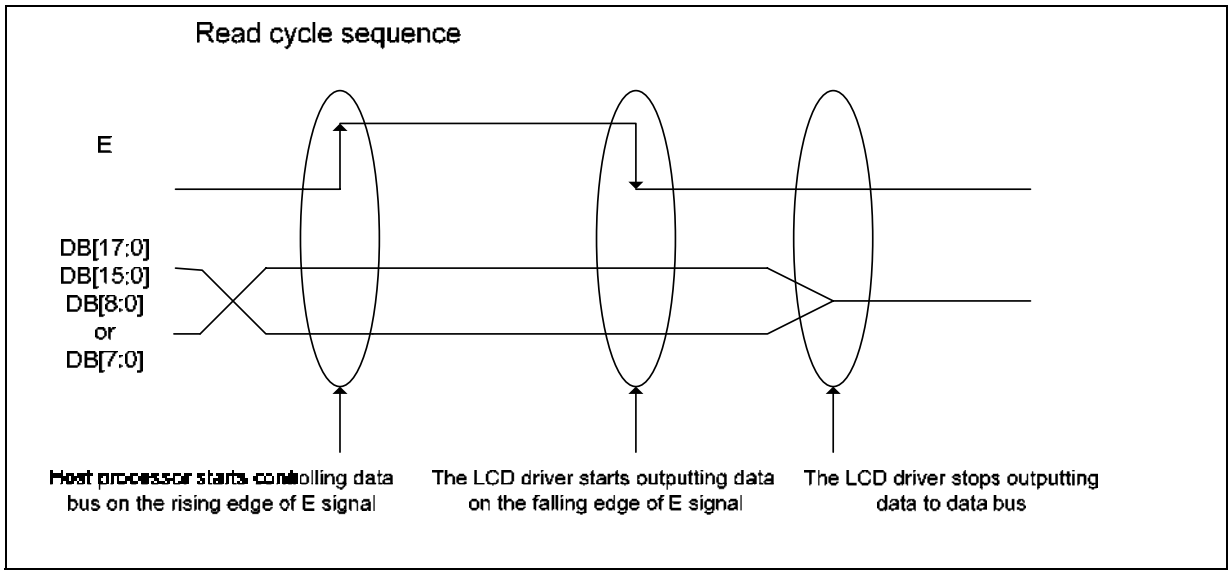


Figure 4 Write Cycle sequence example

Read CyCle Sequence

In read cycle, data and/or commands are read from the LG4538 via the interface between the LG4538 and the host processor. The data (DB[17:0], [15:0], [8:0] or [7:0]) are transmitted from the LG4538 to the host processor on the rising edge of E. The host processor reads the data on the rising falling of E.

See below for the read cycle sequence.



Note : RDX is not a synchronous singal (can be halted).

Figure 5 Read Cycle sequence

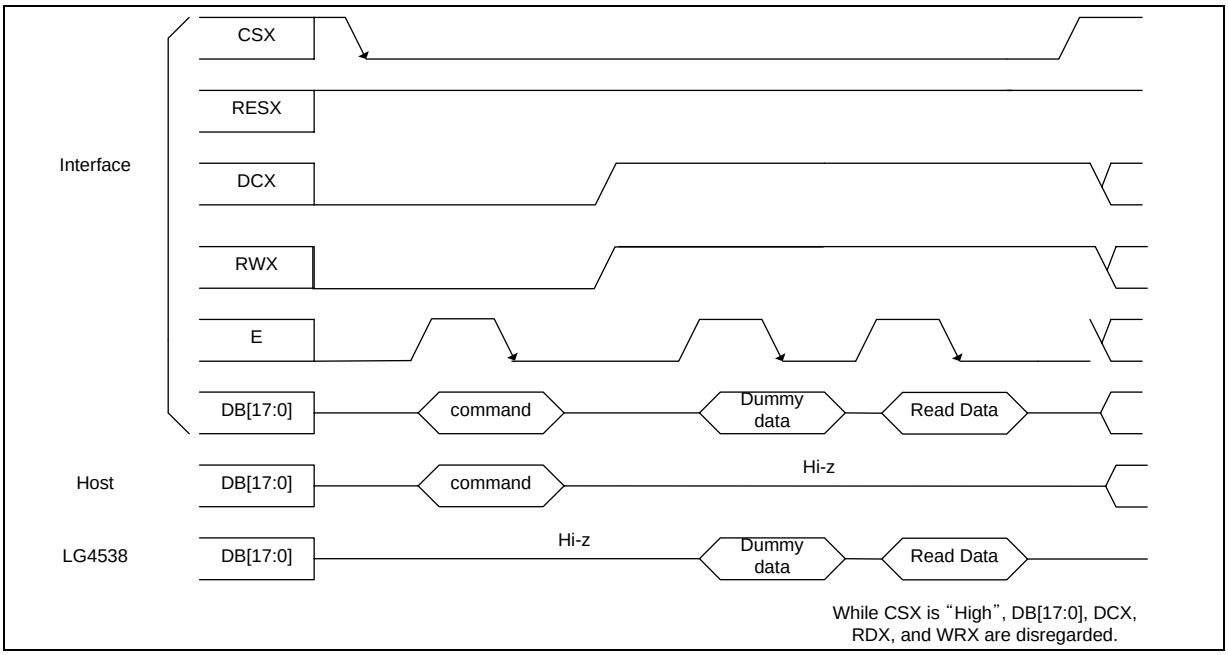


Figure 6 Read Cycle sequence example

Data Trasnfer Break

As shown in the figure below, in the transmission of parameter for command from the host processor to the LG4538, the command parameters sent to the LG4538 before the break occurs are stored in the register of the LG4538 when the following two conditions are met. One is that a break occurs before the last parameter of the command is sent to the LG4538. The other is that the host processor transmits the parameter(s) of a new command, not the parameters of the interrupted command, when the break occurs.

However, those parameters sent after the break is disregarded, and the data in the register is not overwritten.

Note : A break is occurred, for example, by other command input.

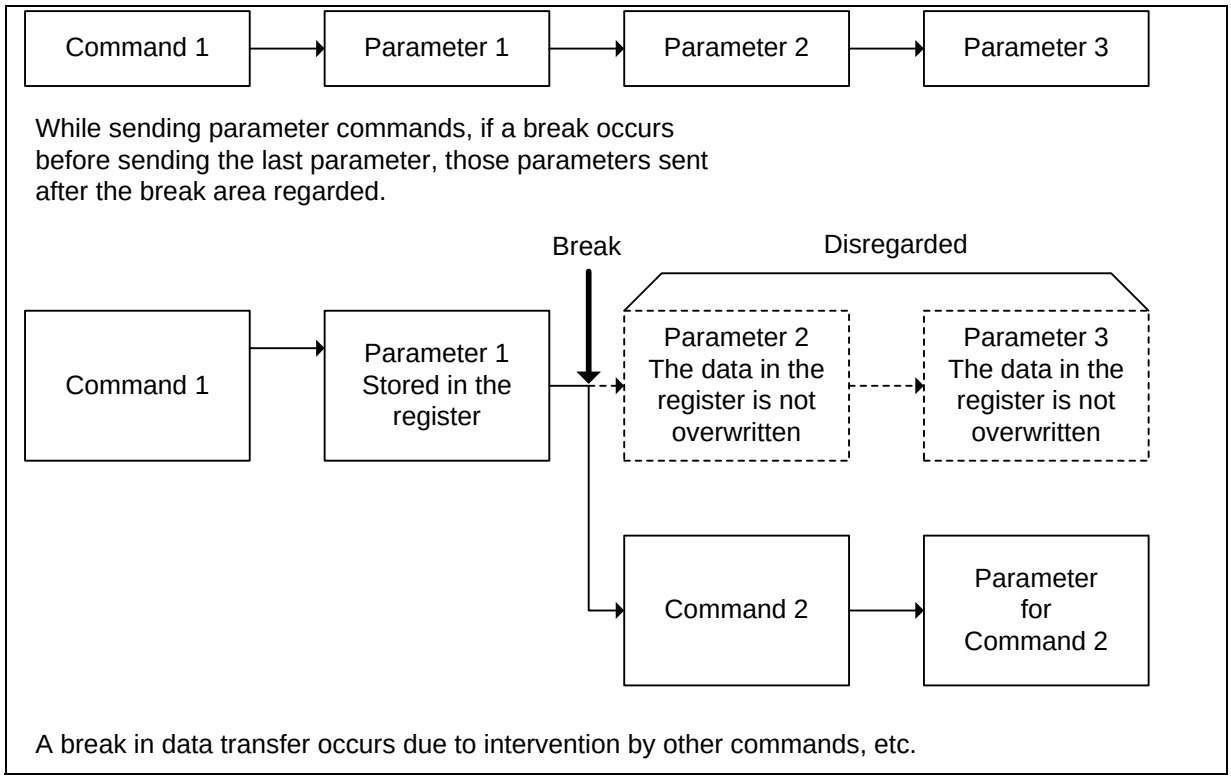


Figure 7

Data Trasnfer Mode

Two methods are available for writing data to the frame memory in the LG4538.

(1) Write Method 1 (Default)

One frame of image daa is written to the frame memory. The amount of the transmitted data is over 1 frame, the data are disregarded. The write operation of the data to the frame memory is terminated when a command intervence in the middle of the course. The LG4538 write the image data to the next frame when write_memory_start command (2Ch) is written. Set WEMODE = 0(Frame Memory Access and Interface setting (B3h)).

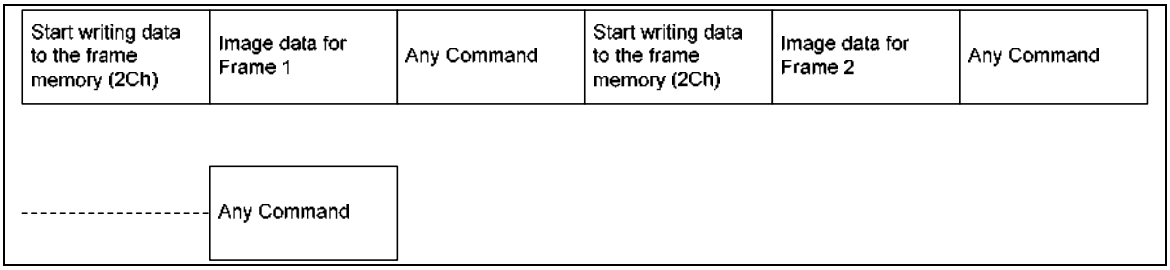


Figure 8

(2) Write Method 2

The image data are written consecutively to the frame memory. The frame memory pointer is reset to the start point when the frame memory becomes full and the driver starts writing the image data of the next frame. Set WEMODE = 1 (Frame Memory Access and Interface setting (B3h)).

Figure 9

Notes : 1. Two write methods are available for all data transfer color meode in 24-/18-/16-/9-/8-bit bus display command I/F.

2. The data write operation to the frame memory is terminated when a command intervenes in the middle of the course. In this case, if write_memory_continue(3Ch) ix executed, the write operaion can be started again from the address where the write operaion is halted.

DBI Type B

The LG4538 adopts 18-/16-/9-/ 8-bit bus display command interface to interface to high-performance host processor. The LG4538 starts transfer the data after storing control information of externally sent 18-/16-/9-/8-bit data in the command register (CDR) and the parameter register (PR).

Write CyCle Sequence

In write cycle, data and/or command are written to the LG4538 via the interface between the LG4538 and the host processor. Each step of write cycle sequence (WRX high, WRX low, WRX high) comprises three control signals (DCX, RDX, WRX) and 8-, 9-, 16-, or 18bit data. The DCX bit indicates signal that is used to select command or data sent on the data bus.

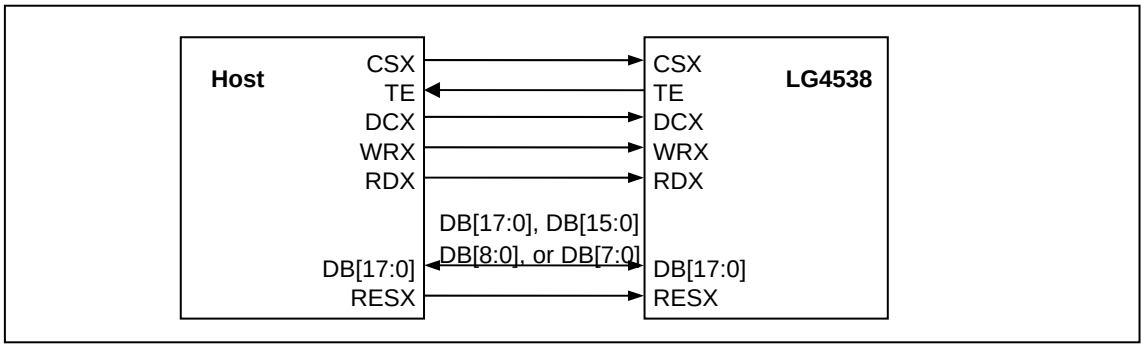
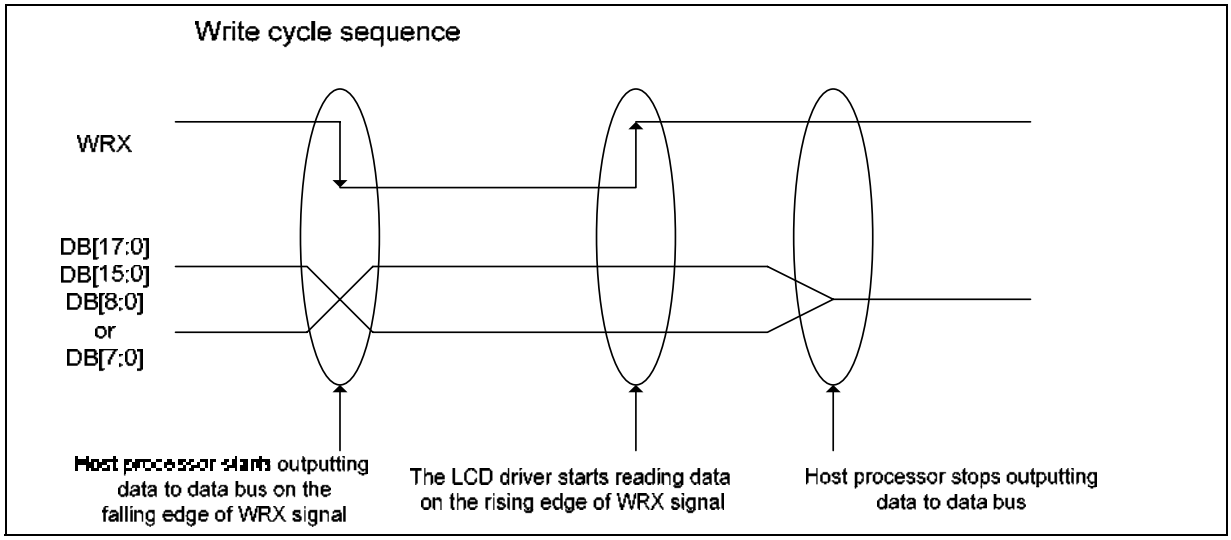


Figure 10 DBI Type B

When DCX="1", data on the above data bus is image data or command parameter. When DCX = 0, data is command.

Setting RDX and WRX to "Low" simultaneously is prohibited. See the figure below for the write cycle sequence.



Note : WRX is not a synchronous singal (can be halted).

Figure 11 Write Cycle sequence

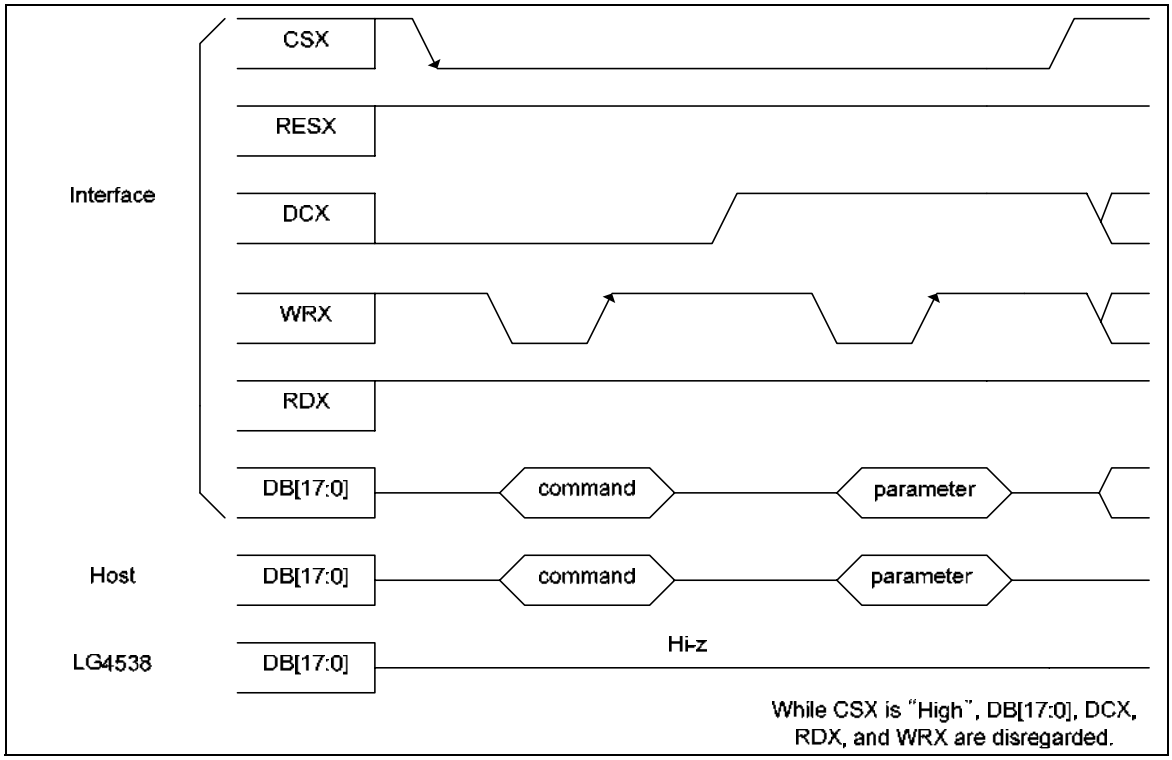
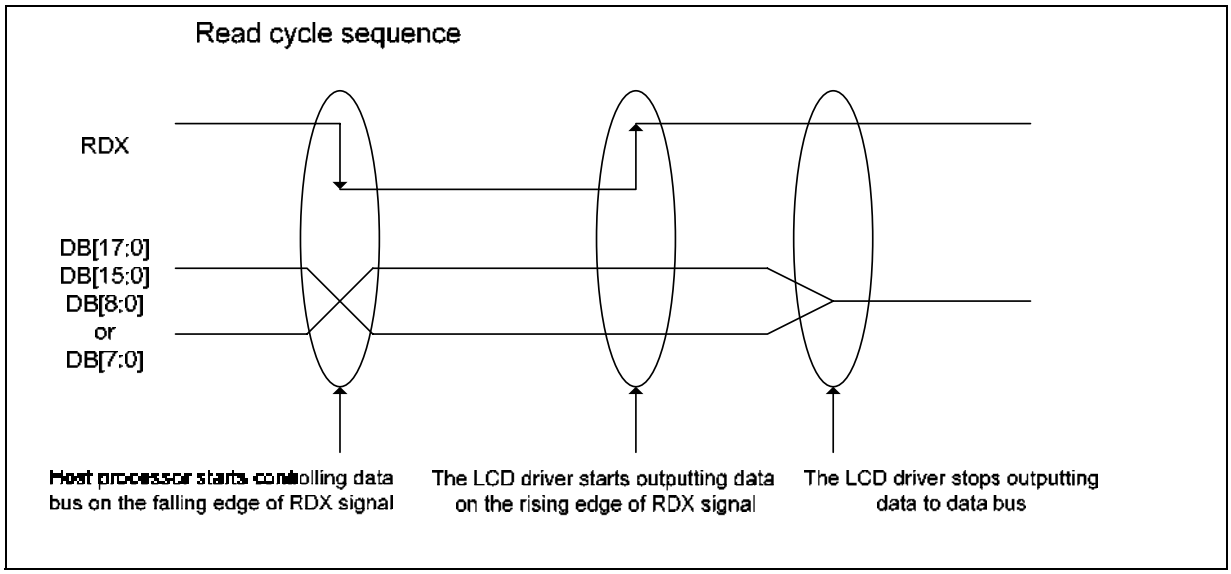


Figure 12 Write Cycle sequence example

Read CyCle Sequence

In read cycle, data and/or commands are read from the LG4538 via the interface between the LG4538 and the host processor. The data (DB[17:0], [15:0], [8:0] or [7:0]) are transmitted from the LG4538 to the host processor on the falling edge of RDX. The host processor reads the data on the rising edge of RDX. Setting RDX and WRX to Low simultaneously is prohibited. See below for the read cycle sequence.



Note : RDX is not a synchronous singal (can be halted).

Figure 13 Read Cycle sequence

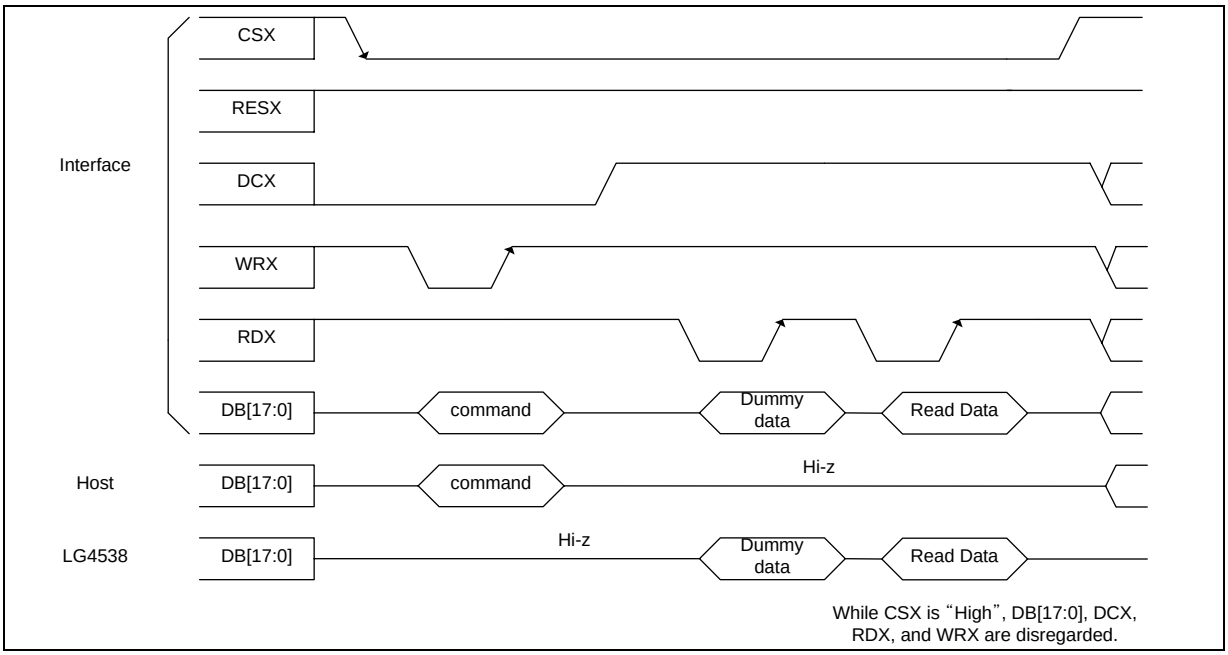


Figure 14 Read Cycle sequence example

Data Trasnfer Break

As shown in the figure below, in the transmission of parameter for command from the host processor to the LG4538, the command parameters sent to the LG4538 before the break occurs are stored in the register of the LG4538 when the following two conditions are met. One is that a break occurs before the last parameter of the command is sent to the LG4538. The other is that the host processor transmits the parameter(s) of a new command, not the parameters of the interrupted command, when the break occurs.

However, those parameters sent after the break is disregarded, and the data in the register is not overwritten.

Note : A break is occurred, for example, by other command input.

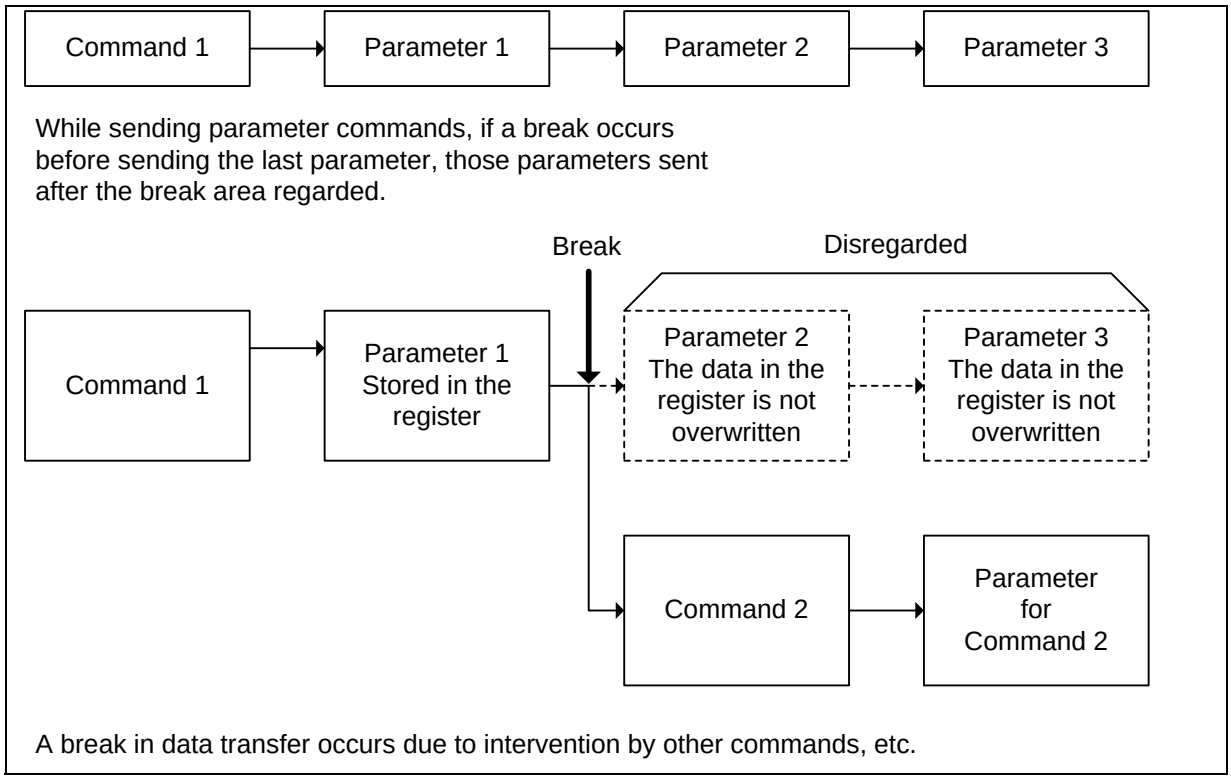


Figure 15

Data Trasnfer Mode

Two methods are available for writing data to the frame memory in the LG4538.

(1) Write Method 1 (Default)

One frame of image daa is written to the frame memory. The amount of the transmitted data is over 1 frame, the data are disregarded. The write operation of the data to the frame memory is terminated when a command intervence in the middle of the course. The LG4538 write the image data to the next frame when write_memory_start command (2Ch) is written. Set WEMODE = 0(Frame Memory Access and Interface setting (B3h)).

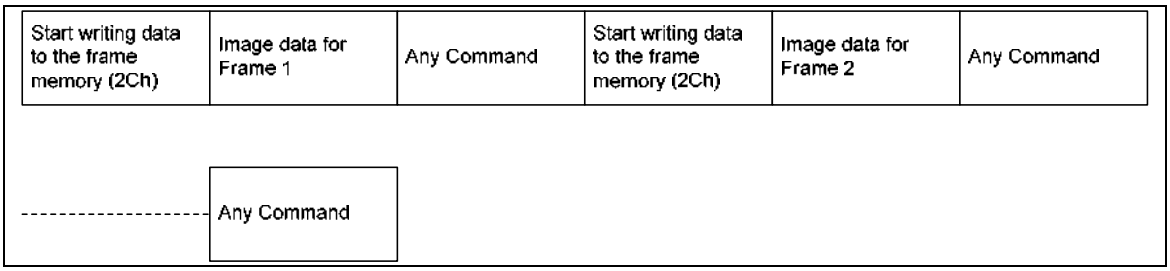


Figure 16

(2) Write Method 2

The image data are written consecutively to the frame memory. The frame memory pointer is reset to the start point when the frame memory becomes full and the driver starts writing the image data of the next frame. Set WEMODE = 1 (Frame Memory Access and Interface setting (B3h)).

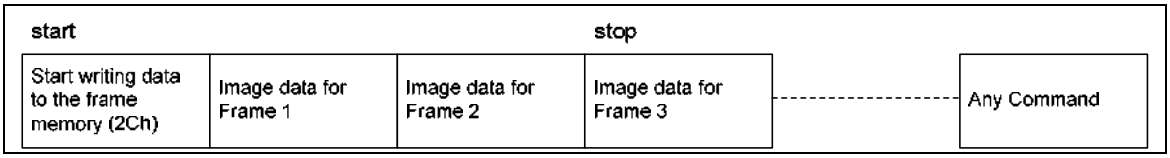


Figure 17

Notes : 1. Two write methods are available for all data transfer color meode in 24-/18-/16-/9-/8-bit bus display command I/F.

2. The data write operation to the frame memory is terminated when a command intervenes in the middle of the course. In this case, if write_memory_continue(3Ch) ix executed, the write operaion can be started again from the address where the write operaion is halted.

DBI Type C

The LG4538 supports serial interface DBI Type C (Option 1 and 3). Nine-/ Eight-bit data, transmitted from the LG4538 to the host processor, is stored in command register (CDR) or parameter register (PR) to start internal operation which is determined by signals from the host processor.

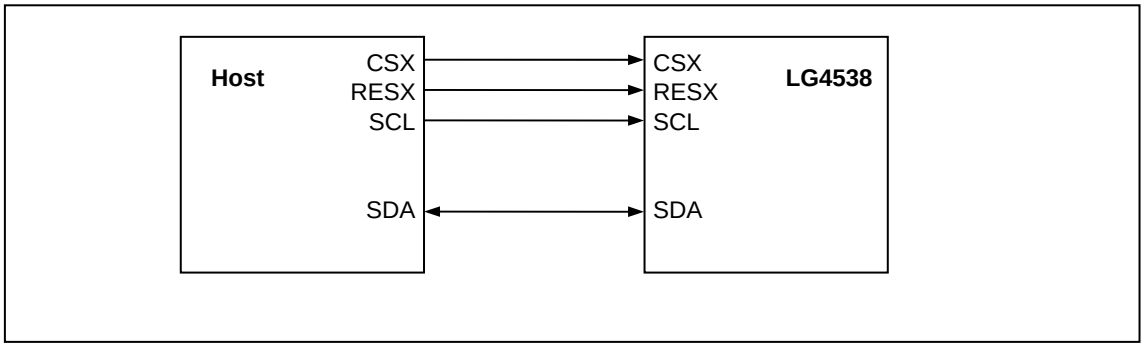


Figure 18 DBI TypeC Option 1 I

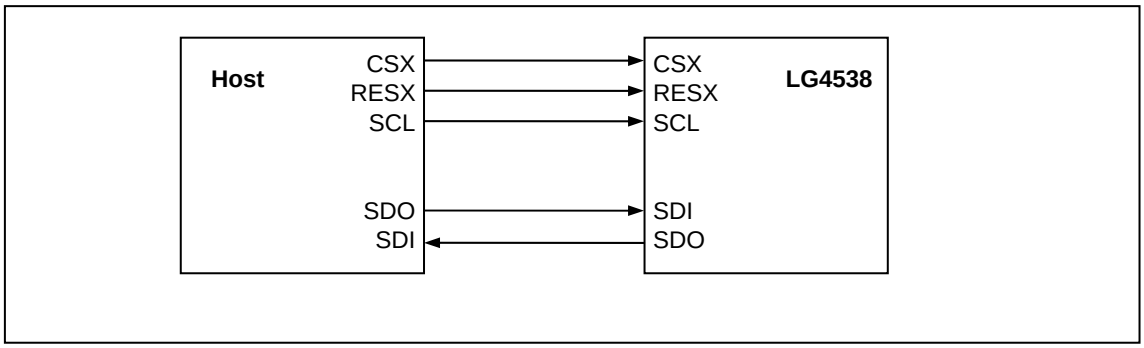


Figure 19 DBI TypeC Option 1 II

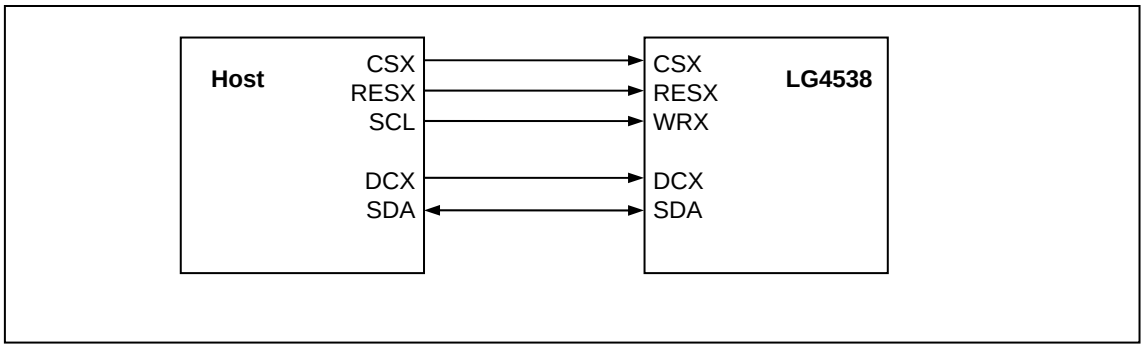


Figure 20 DBI TypeC Option 3 I

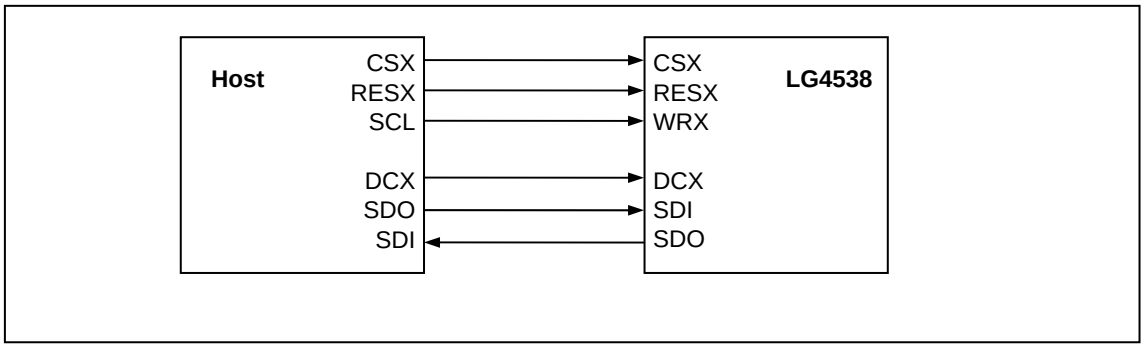
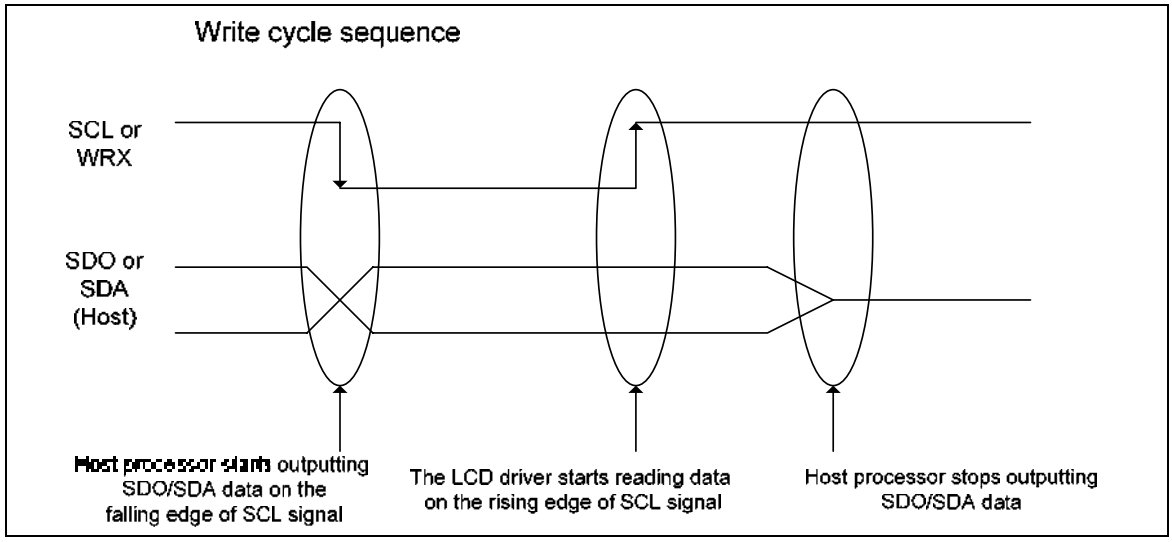


Figure 21 DBI TypeC Option 3 II

Write CyCle Sequence

In write cycle, data and/or command are written to the LG45381 via the interface between the LG4538 and the host processor. Each step of write cycle sequence (SCL High Low High or WRX High Low High) has two or three control signals (DCX, SCL or WRX) and data output from SDO. During Write Cycle Sequence, the host processor outputs data while the LG4538 accepts data at the rising edge of SCL.

If DCX is used in DBI Type C Option 3 operation, data on SDO or SDA are command when DCX="0". When DCX = 1, data on SDO or SDA are image data or command parameter. See next figure for Write Cycle Sequence.



Note : SCL is not synchronous signal (can be halted).

Figure 22 Type C Write Cycle Sequence

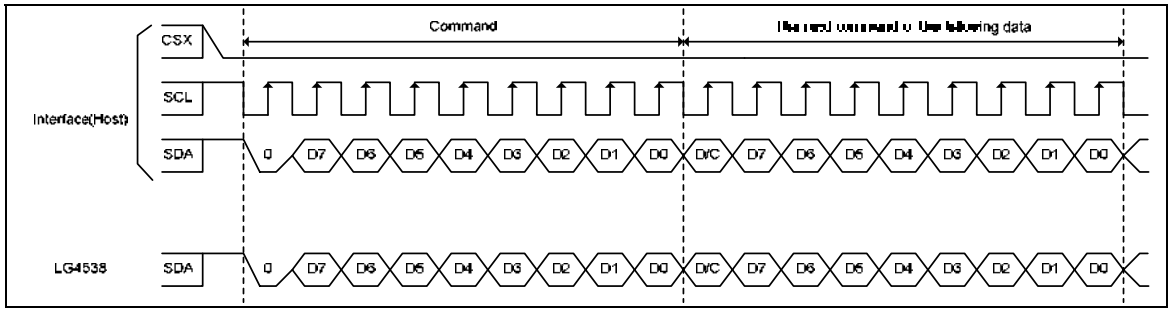


Figure 23 Type C Write Cycle Sequence (Option 1 I)

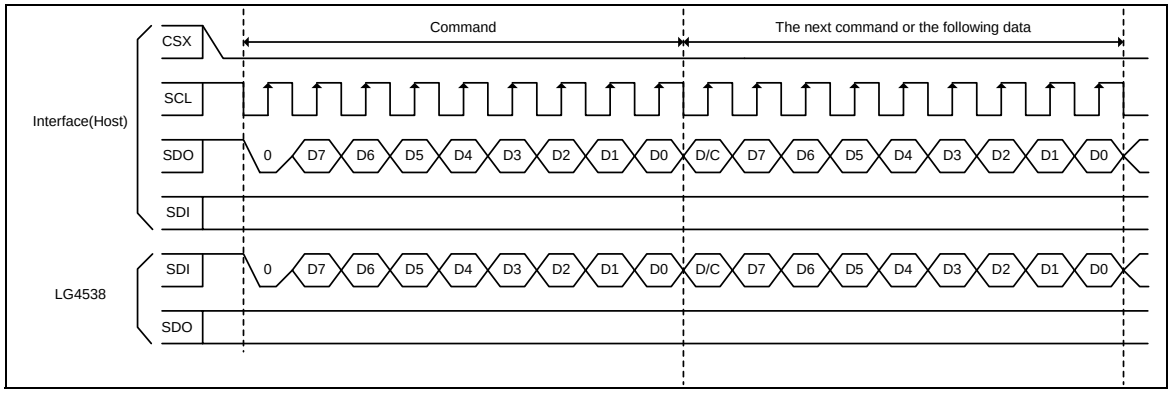


Figure 24 Type C Write Cycle Sequence (Option 1 II)

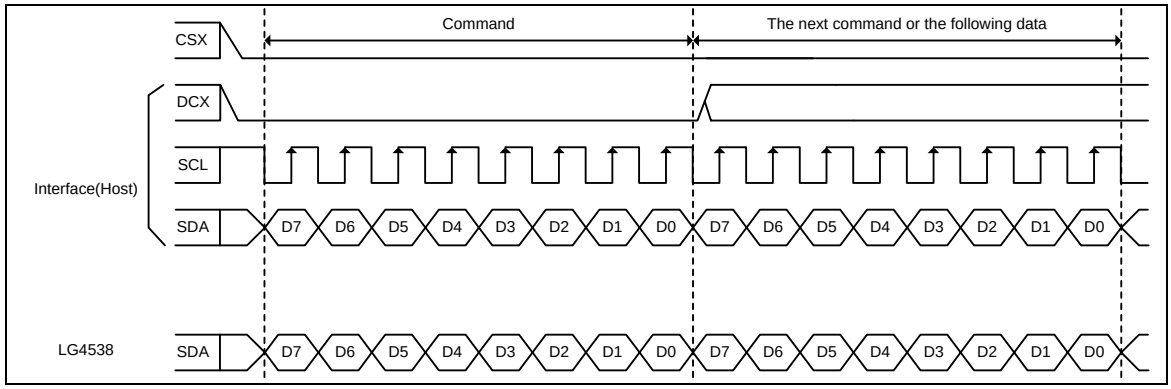


Figure 25 Type C Write Cycle Sequence (Option 3 I)

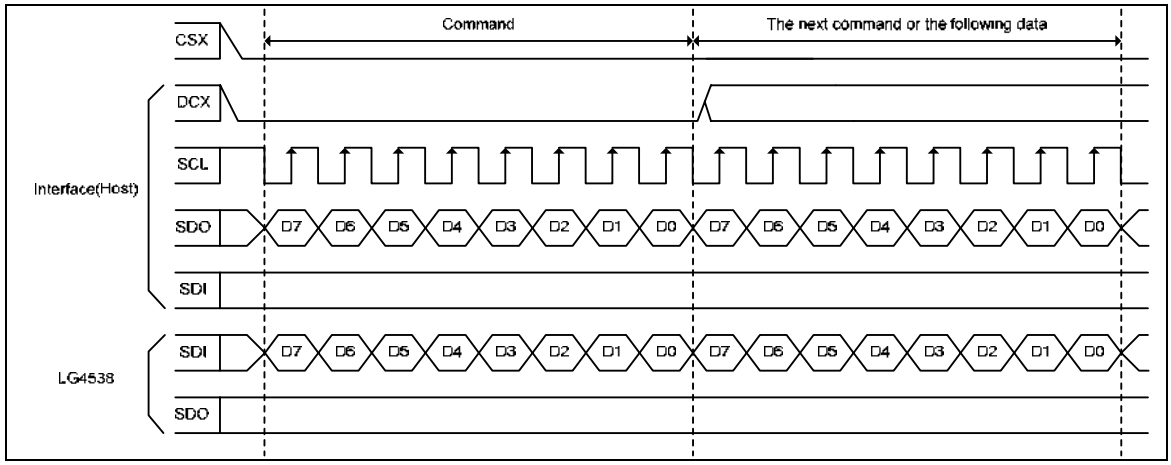
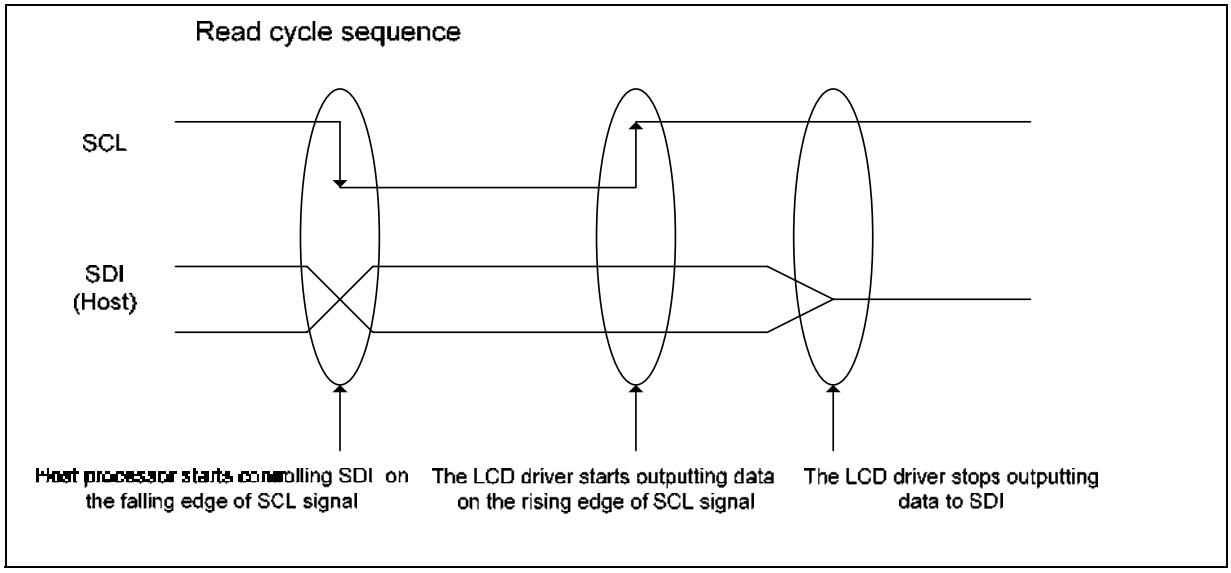


Figure 26 Type C Write Cycle Sequence (Option 3 II)

Read CyCle Sequence

In read cycle, data and/or commands are read from the LG4538 via the interface between the LG4538 and the host processor. Data are transmitted from the LG4538 to the host processor via SDI on the falling edge of SCL. The host processor reads the data on the rising edge of SCL. See next figure for the read cycle sequence.



Note : SCL is not a synchronous singal (can be halted).

Figure 27 Read Cycle sequence

Figure 28 Type C Read Cycle Sequence (Option 1 I)

Figure 29 Type C Read Cycle Sequence (Option 1 II)

Figure 30 Type C Read Cycle Sequence (Option 3 I)

Figure 31 Type C Read Cycle Sequence (Option 3 II)

Data Trasnfer Break

As shown in the figure below, in the transmission of parameter for command from the host processor to the LG4538, the command parameters sent to the LG4538 before the break occurs are stored in the register of the LG4538 when the following two conditions are met. One is that a break occurs before the last parameter of the command is sent to the LG4538. The other is that the host processor transmits the parameter(s) of a new command, not the parameters of the interrupted command, when the break occurs.

However, those parameters sent after the break is disregarded, and the data in the register is not overwritten.

Note : A break is occurred, for example, by other command input.

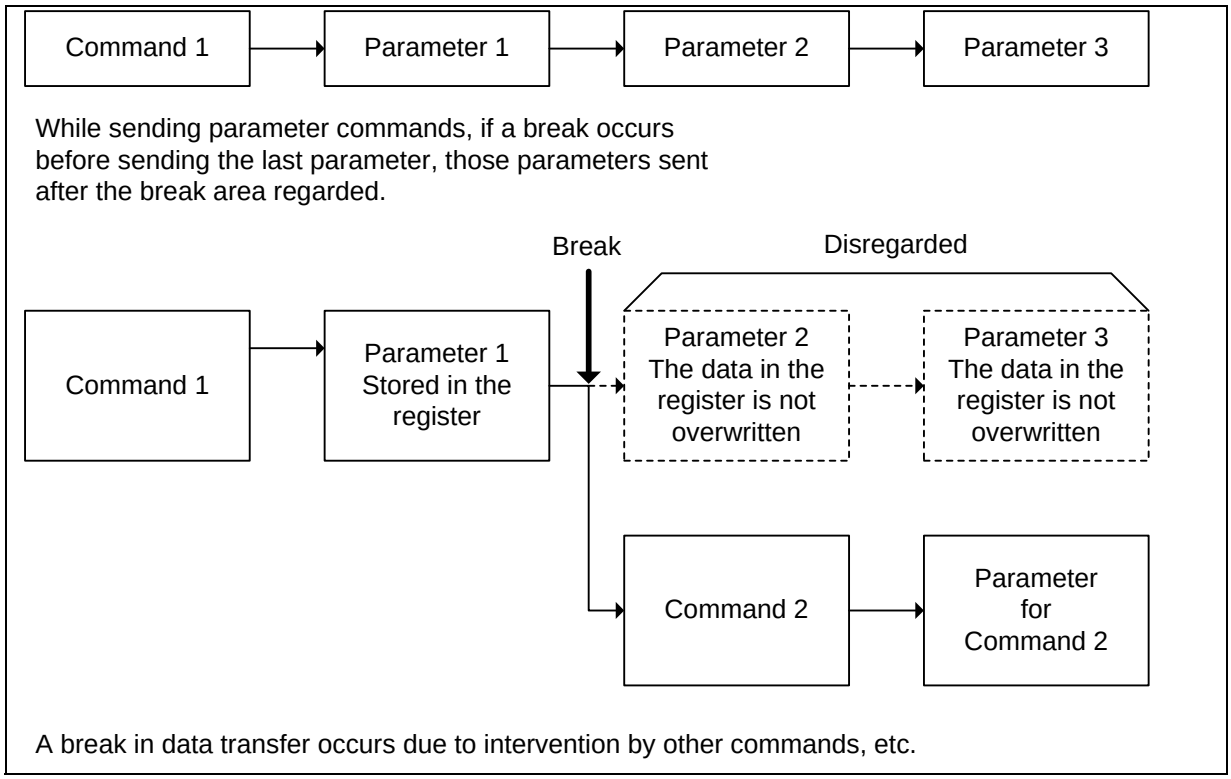


Figure 32

DBI Data Format

The LG4538 supports color formats shown in the table below. At least one color format is supported by each of Type B 18-/16-/9-/8-bit and Type C interface.

Type	IM[3:0]	Data Pin	Color format
Type B	0000	DB[7:0]	16bpp
			18bpp
	0001	DB[15:0]	16bpp
			18bpp (Option 1)
			18bpp (Option 2)
			18bpp (Option 3)
			18bpp (Option 4)
	0010	DB[8:0]	16bpp
			18bpp (Option 1)
			18bpp (Option 2)
	0011	DB[17:0]	16bpp
			18bpp
Type A	1000	DB[7:0]	16bpp
			18bpp
	1001	DB[15:0]	16bpp
			18bpp (Option 1)
			18bpp (Option 2)
			18bpp (Option 3)
			18bpp (Option 4)
	1010	DB[8:0]	16bpp
			18bpp (Option 1)
			18bpp (Option 2)
	1011	DB[17:0]	16bpp
			18bpp
Type C	0101 0110	SDA	16bpp
			18bpp
	1101 1110	SDI/SDO	16bpp
			18bpp

DBI Type B Data Format

Command/Parameter

18-bit Bus Interface

	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Write											D7	D6	D5	D4	D3	D2	D1	D0
Read											D7	D6	D5	D4	D3	D2	D1	D0

16-bit Bus Interface

	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Write									D7	D6	D5	D4	D3	D2	D1	D0
Read									D7	D6	D5	D4	D3	D2	D1	D0

9-bit Bus Interface

	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Write		D7	D6	D5	D4	D3	D2	D1	D0
Read		D7	D6	D5	D4	D3	D2	D1	D0

8-bit Bus Interface

	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Write	D7	D6	D5	D4	D3	D2	D1	D0
Read	D7	D6	D5	D4	D3	D2	D1	D0

Figure 33

18-bit Bus Interface

set_pixel_fomat = 5(16bpp), DFM = *

	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Write			R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

set_pixel_fomat = 6(18bpp), DFM = *

	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Write	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

set_pixel_fomat = *, DFM = *

	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Read	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]

16-bit Bus Interface

set_pixel_fomat = 5(16bpp), DFM = *

	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Write	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

set_pixel_fomat = 6(18bpp), DFM = 0

		DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Write	1st transmission	R1[5]	R1[4]	R1[3]	R1[2]	R1[1]	R1[0]			G1[5]	G1[4]	G1[3]	G1[2]	G1[1]	G1[0]		
	2nd transmission	B1[5]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]			R2[5]	R2[4]	R2[3]	R2[2]	R2[1]	R2[0]		
	3rd transmission	G2[5]	G2[4]	G2[3]	G2[2]	G2[1]	G2[0]			B2[5]	B2[4]	B2[3]	B2[2]	B2[1]	B2[0]		

set_pixel_fomat = 6(18bpp), DFM = 1

		DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Write	1st transmission	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]			G[5]	G[4]	G[3]	G[2]	G[1]	G[0]		
	2nd transmission	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]										

set_pixel_fomat = 6(18bpp), DFM = 2

		DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Write	1st transmission	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]
	2nd transmission	B[1]	B[0]														

set_pixel_fomat = 6(18bpp), DFM = 3

		DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Write	1st transmission															R[5]	R[4]
	2nd transmission	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

set_pixel_fomat = *, DFM = 0

		DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Read	1st transmission	r1[7]	r1[6]	r1[5]	r1[4]	r1[3]	r1[2]	r1[1]	r1[0]	g1[7]	g1[6]	g1[5]	g1[4]	g1[3]	g1[2]	g1[1]	g1[0]
	2nd transmission	b1[7]	b1[6]	b1[5]	b1[4]	b1[3]	b1[2]	b1[1]	b1[0]	r2[7]	r2[6]	r2[5]	r2[4]	r2[3]	r2[2]	r2[1]	r2[0]
	3rd transmission	g2[7]	g2[6]	g2[5]	g2[4]	g2[3]	g2[2]	g2[1]	g2[0]	b2[7]	b2[6]	b2[5]	b2[4]	b2[3]	b2[2]	b2[1]	b2[0]

set_pixel_fomat = *, DFM = 1

		DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Read	1st transmission	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]			g[5]	g[4]	g[3]	g[2]	g[1]	g[0]		
	2nd transmission	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]										

9-bit Bus Interface

set_pixel_fomat = 5(16bpp), DFM = *

		DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Write	1st transmission		R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]
	2nd transmission		G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

set_pixel_fomat = 5(16bpp), DFM = 0

		DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Write	1st transmission	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]
	2nd transmission	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

set_pixel_fomat = 5(16bpp), DFM = 1

		DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Write	1st transmission		R[5]	R[4]	R[3]	R[2]	R[1]	R[0]		
	2nd transmission		G[5]	G[4]	G[3]	G[2]	G[1]	G[0]		
	3rd transmission		B[5]	B[4]	B[3]	B[2]	B[1]	B[0]		

set_pixel_fomat = *, DFM = *

		DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Read	1st transmission	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]
	2nd transmission	g[2]	g[1]	g[0]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]

8-bit Bus Interface

set_pixel_fomat = 5(16bpp), DFM = *

		DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Write	1st transmission	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]
	2nd transmission	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

set_pixel_fomat = 6(18bpp), DFM = *

		DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Write	1st transmission	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]		
	2nd transmission	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]		
	3rd transmission	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]		

set_pixel_fomat = *, DFM = *

		DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Read	1st transmission	r[7]	r[6]	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]
	2nd transmission	g[7]	g[6]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]
	3rd transmission	b[7]	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]

Figure 34

Extended Format for 18bit/pixel data

Set_pixel_format	EPF	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
16bpp	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
16bpp	2'h0	R[4]	R[3]	R[2]	R[1]	R[0]	R[4]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	B[4]
	2'h1	R[4]	R[3]	R[2]	R[1]	R[0]	R[4]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	B[4]
	2'h2	R[4]	R[3]	R[2]	R[1]	R[0]	1'b0	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	1'b0
	2'h3	R[4]	R[3]	R[2]	R[1]	R[0]	1'b1	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	1'b1

Special process for 16 bits/pixel Data : R[4:0], B[4:0] = 5'h1F -> Frame Memory Data = 6'hFF
R[4:0], B[4:0] = 5'h00 -> Frame Memory Data = 6'h00

Figure 35

DBI Type C Data Format

Type C Data Format

	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Command/Parameter Write	D/	D6	D5	D4	D3	D2	D1	D0
Command/Parameter Read	D/	D6	D5	D4	D3	D2	D1	D0

set_pixel_fomat = 5(16bpp), DFM = *

		DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Write	1st transmission	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]
	2nd transmission	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

set_pixel_fomat = 6(18bpp), DFM = *

		DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Write	1st transmission	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]		
	2nd transmission	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]		
	3rd transmission	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]		

set_pixel_fomat = *, DFM = *

		DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Read	1st transmission	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]		
	2nd transmission	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]		
	3rd transmission	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]		

Figure 36

Serial Peripheral Interface (SPI)

The serial interface is selected by setting the IM[2:0] = 100. The data is transferred via chip select line (CSX), serial transfer clock line (SCL), serial data input line (SDI), and serial data output line (SDO). In serial interface operation, the DB[17:0] pins, not used in this mode, must be fixed at either VDD3 or GND level.

The LG4538 recognizes the start of data transfer on the falling edge of CSX input and starts transferring the start byte. It recognizes the end of data transfer on the rising edge of CSX input. The LG4538 is selected when the 6-bit chip address in the start byte transferred from the transmission unit and the 6-bit device identification code assigned to the LG4538 are compared and both 6-bit data match, and then the LG4538 starts taking in data. The least significant bit of the device identification code is set with the ID pin. Send "01110" to the five upper bits of the device identification code. Two different chip addresses must be assigned to the LG4538 because the seventh bit of the start byte is assigned to the register select bit (RS). When RS = 0, an index register write operation is executed. When RS = 1, either an instruction write operation or a RAM read/write operation is executed. The eighth bit of the start byte is to select either read or write operation (R/W bit). The LG4538 receives data when the R/W = 0, and transfers data when the R/W = 1.

When writing data to the GRAM via serial interface, the data is written to the GRAM after it is transferred in two bytes. The LG4538 writes data to the GRAM in units of 24 bits by adding the same bits as the MSBs to the LSB of R and B dot data.

After receiving the start byte, the LG4538 starts transferring or receiving data in units of bytes. The LG4538 executes data transfer from the MSB. The LG4538's instruction takes 8-bit format and they are executed inside after it is transferred in two bytes (16 bits: D15-0) from the MSB.
In case of reading data from the GRAM, the LG4538 does not transfer valid data until first five bytes of data are read from the GRAM following the start byte. The LG4538 starts sending valid data as it reads the sixth and subsequent byte data.

Table 9 Start byte format

Transferred bits	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
Start byte format	Device ID code						RS	R/W
	0	1	1	1	0	ID		

Note: ID bit is selected by setting the IM0/ID pin.

Table 10

RS	**R/W**	**Function**
0	0	Set an index register
0	1	Read a status
1	0	Write an instruction or RAM data
1	1	Read an instruction or RAM data

Write Cycle Sequence

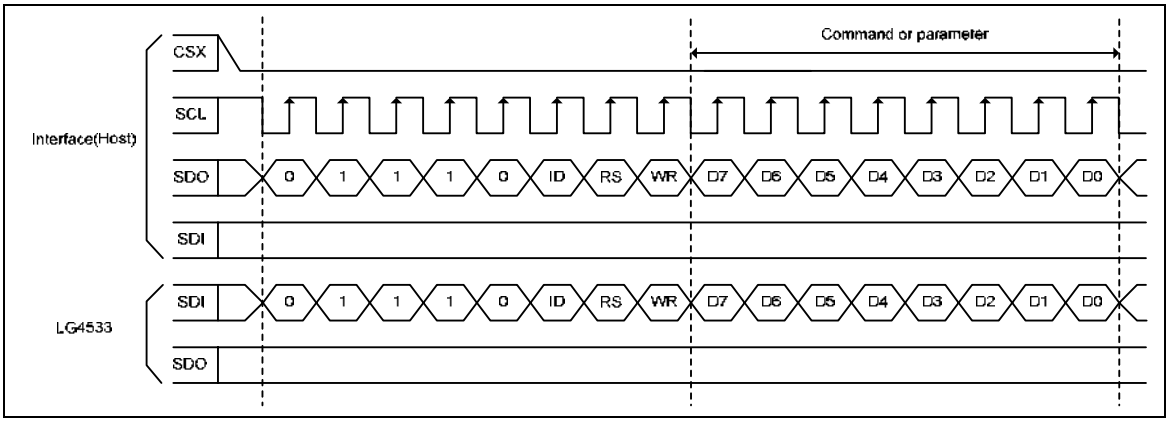


Figure 37

Read Cycle Sequence

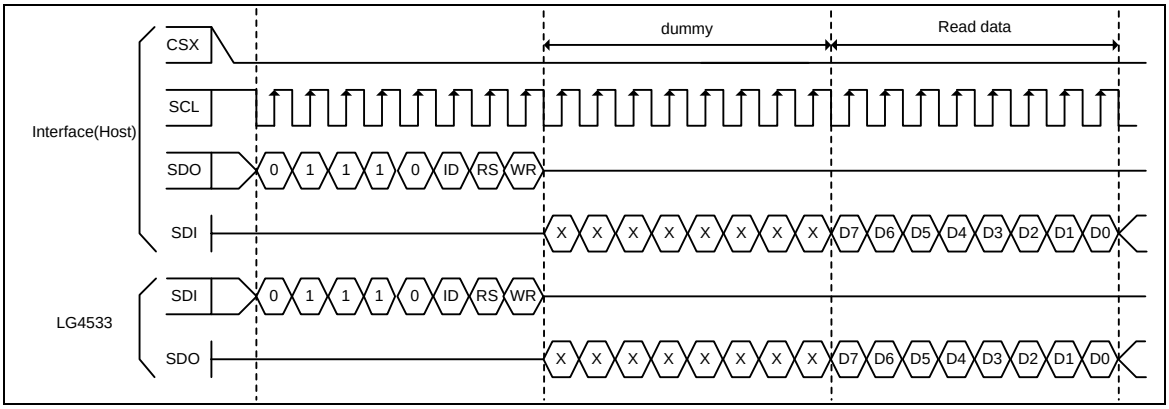


Figure 38

SPI Data Format

SPI Data Format

	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Command/Parameter Write	D7	D6	D5	D4	D3	D2	D1	D0
Command/Parameter Read	D7	D6	D5	D4	D3	D2	D1	D0

set_pixel_fomat = 5(16bpp), DFM = *

		DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Write	1st transmission	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]
	2nd transmission	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

set_pixel_fomat = 6(18bpp), DFM = *

		DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Write	1st transmission	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]		
	2nd transmission	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]		
	3rd transmission	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]		

set_pixel_fomat = *, DFM = *

		DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Read	1st transmission	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]		
	2nd transmission	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]		
	3rd transmission	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]		

Extended Format for 18bit/pixel data

Set_pixel_format	EPF	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
16bpp	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
16bpp	2'h0	R[4]	R[3]	R[2]	R[1]	R[0]	R[4]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	B[4]
	2'h1	R[4]	R[3]	R[2]	R[1]	R[0]	R[4]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	B[4]
	2'h2	R[4]	R[3]	R[2]	R[1]	R[0]	1'b0	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	1'b0
	2'h3	R[4]	R[3]	R[2]	R[1]	R[0]	1'b1	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	1'b1

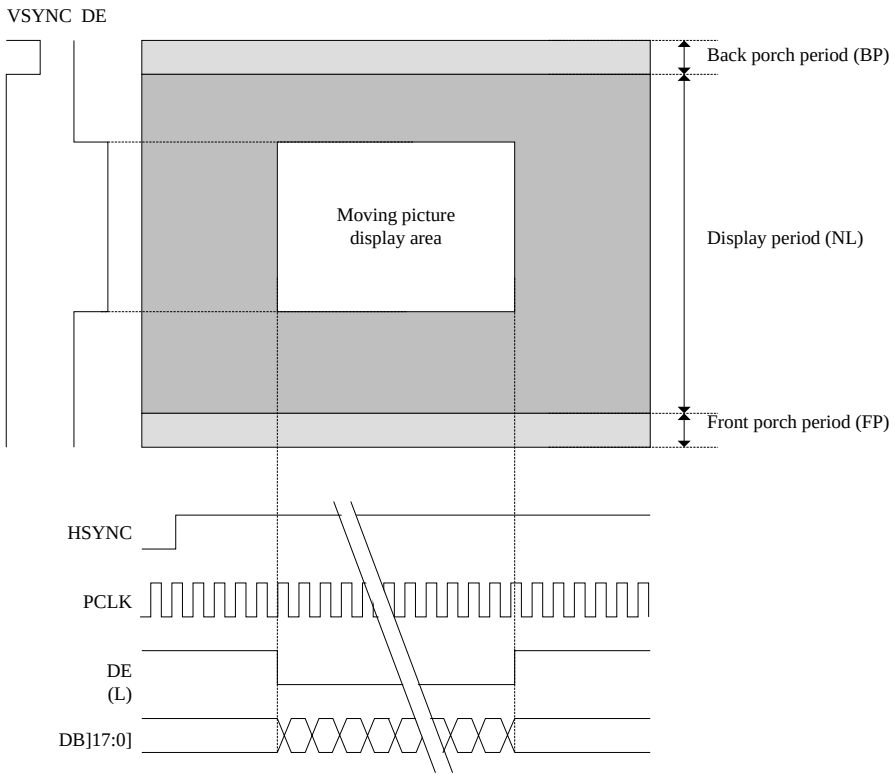
Special process for 16 bits/pixel Data : R[4:0], B[4:0] = 5'h1F -> Frame Memory Data = 6'hFF
R[4:0], B[4:0] = 5'h00 -> Frame Memory Data = 6'h00

Figure 39

Display Pixel Interface (DPI)

Display Pixel Interface (DPI)

In Display Pixel Interface (DPI) operation, display operation is in synchronization with ynchronization signals VSYNC, HSYNC and DOTCLK. By using Window Address Function in accordance with the cycle of frame memory write operation, the data are transferred only to the video image area so that the LG4538 consumes only a small amount of power. In DPI operation, front and back porch periods must be made before and after the display period. Commands must be transferred via DBI Type B serial interface.



VSYNC : Frame synchronization signal. Specifies the start position of a frame.
HSYNC : Line synchronization signal. Specifies the start position of a horizontal line.
PCLK: Pixel Clock. Data is accepted at the rising edge of this signal (CKPL= 0)
DE : Data enable signal. DE = Low menas the LG4553 is in data enable period (DEPL = 0).
D[17:0] : Display data (RGB)

Back porch period (BP) BP >= 2H
Front porch period (FP) FP >= 3H
Display period (DP) NL <= 320H
Number of line in 1 Frame period = FP + NL + BP

Figure 40

DPI Timing

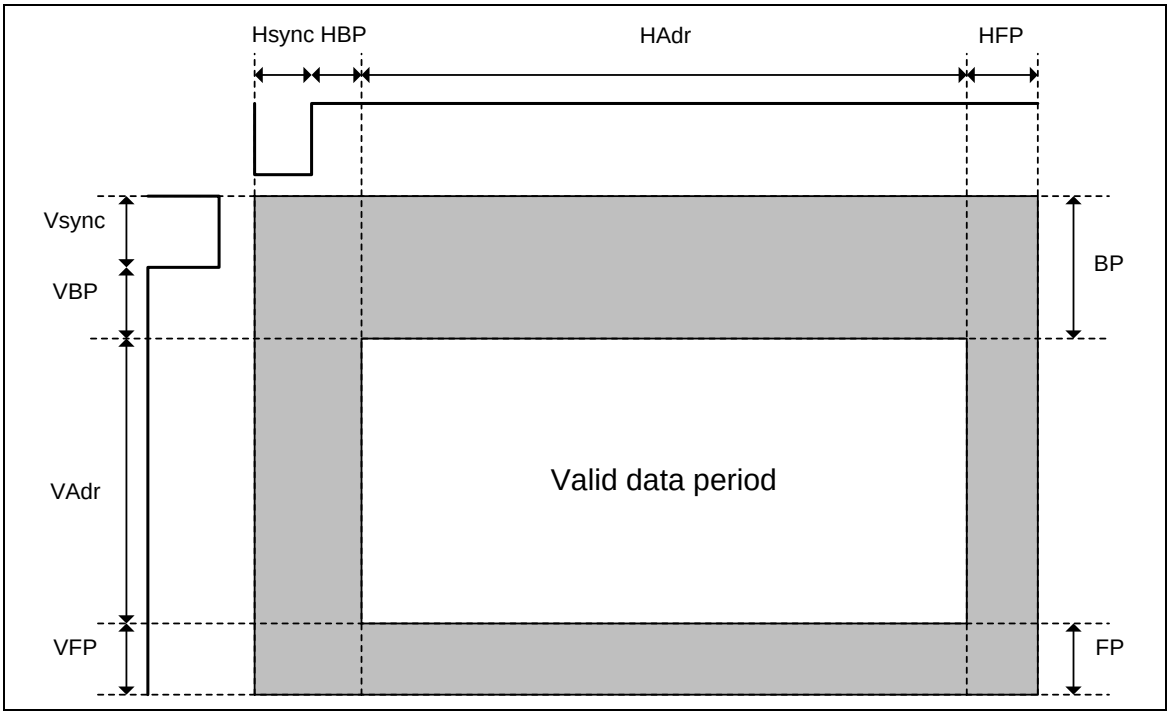


Figure 41

Table 11

Parameters	Symbols	Min.	Typ.	Max.	Step	Unit
Horizontal Synchronization	Hsync	2	10	16	1	DOTCLKCYC
Horizontal Back Porch	HBP	2	20	24	1	DOTCLKCYC
Horizontal Address	HAdr	-	240	-	1	DOTCLKCYC
Horizontal Front Porch	HFP	2	10	16	1	DOTCLKCYC
Vertical Synchronization	Vsync	1	2	4	1	Line
Vertical Back Porch	VBP	1	2	-	1	Line
Vertical Address	VAdr	-	320	-	1	Line
Vertical Front Porch	VFP	3	4	-	1	Line

Video Image Display via DPI

The LG4538 supports video image capable DPI and frame memory to store display data so that the driver has strong points such as

1. The window address function can minimize data transfer by specifying a moving picture RAM area
2. The data transfer is limited to a moving picture RAM area.
3. The reduction in data transfer contributes to the reduction in power consumption by the entire system
4. The combined use with system interface allows updating data in the still picture area, such as icons, while displaying a moving picture via DPI.

To access Frame Memory via System Interface (DBI) in DPI operation

Frame memory can be accessed via system interface in DPI operation as well. However in DPI operation, the frame memory is always written in synchronization with DOTCLK when ENABLE=”High”. Therefore, make sure to stop display data write operation via DPI to write data to frame memory via system interface. If RM=0, the frame memory is accessed via system interface. To return to DPI operation, make write/read bus cycle time and then set RM=1 and execute a write_memory_start command (2Ch) and then start frame memory access. If both interfaces are used to access the frame memory, write data are not guaranteed.

The following figure shows an example of video image display via DPI and display data rewrite in the still picture area via system interface.

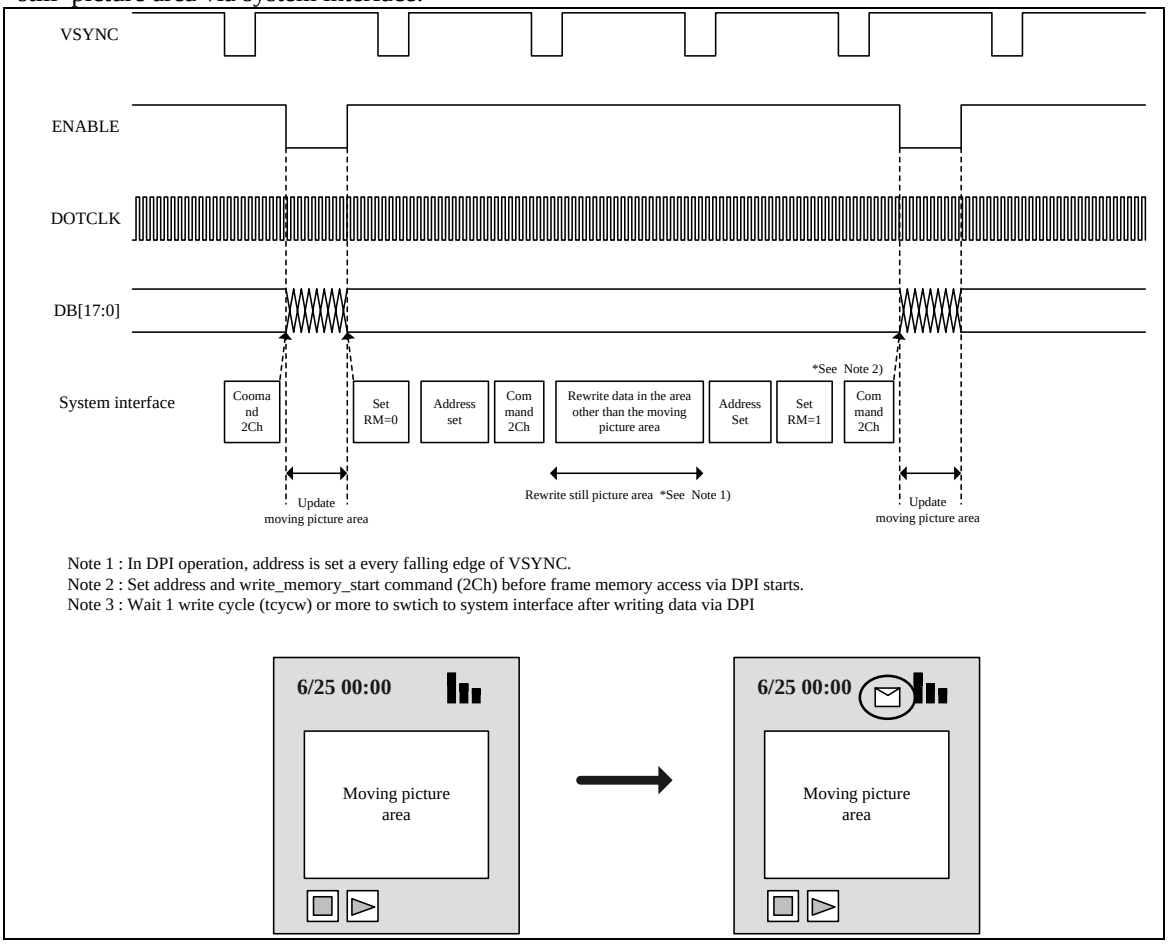


Figure 42

6-bit DPI Connection

Image is displayed in synchronization with synchronization signals VSYNC, HSYNC and DOTCLK. 6-bit RGB data (DB[5:0]) is transferred to internal frame memory in synchronization with data ENABLE signal ENABLE and display operation.

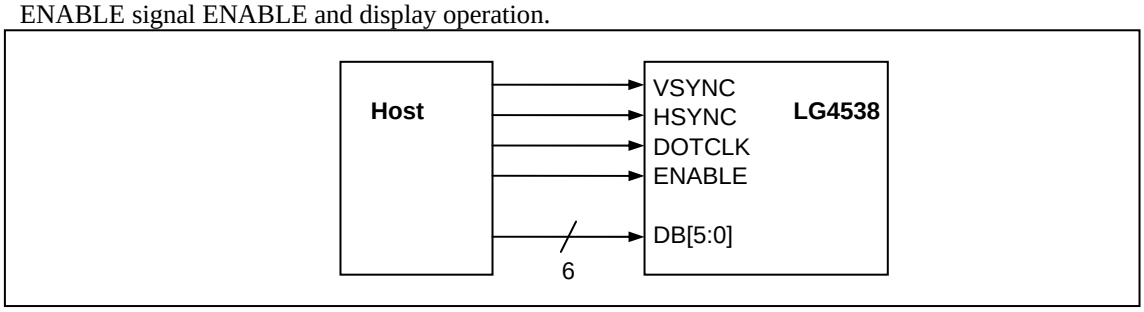


Figure 43

18-bit DPI Connection

Image is displayed in synchronization with synchronization signals VSYNC, HSYNC and DOTCLK. 18-bit RGB data (DB[17:0]) is transferred to internal frame memory in synchronization with data ENABLE signal ENABL and display operation.

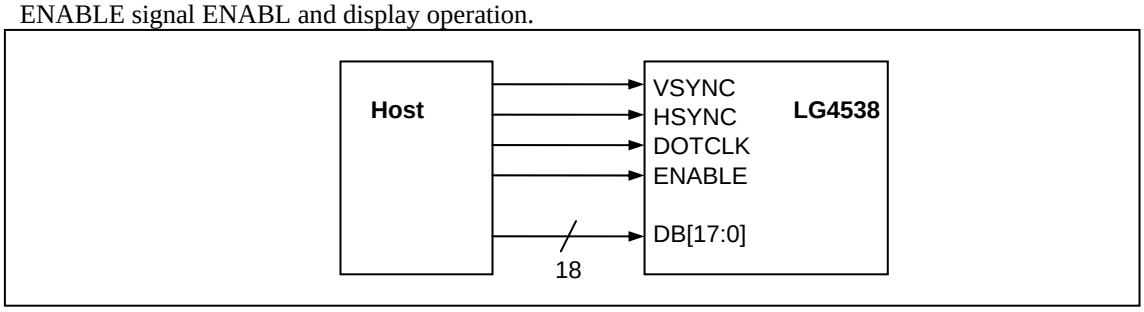


Figure 44

Note to DPI

a. In DPI operation, functions noted “disabled” in the table below are invalid.

Table 12

Function	DPI
Partial display function	disabled
Scrolling function	disabled
Idle mode	disabled

b. It is necessary to supply VSYNC, HSYNC and DOTCLK all the time during DPI operation.

c. Panel control signal reference clock is DOTCLK in DPI operation unlike usual internal oscillation clock.

d. Make sure to follow mode switching seqeuence to transit from/to display by internal operation mode to/from display via DPI.

e. Address is set every frame on the falling edge of VSYNC during DPI operation.

DPI Data Format

The LG4538 support color formats as below:

Table 13

DPIPF[3:0]	Data Pin		Color format
	RM = 0	RM = 1	
3’h6	DB[17:0] (1 transfer/ pixel)	DB[5:0] (3 transfer / pixel)	18bpp
3’h5	DB[15:0] (1 transfer/ pixel)	DB[5:0] (3 transfer / pixel)	16bpp

See next figure for connection of host processor and the LG4538’s pins.

18-bit Bus Interface

set_pixel_fomat = 6(18bpp)

		DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Write	1st transmission	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

set_pixel_fomat = 5(16bpp)

		DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Write	1st transmission			R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

6-bit Bus Interface

set_pixel_fomat = 6(18bpp)

		DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Write	1st transmission	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]
	2nd transmission	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]
	3rd transmission	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

set_pixel_fomat = 5(16bpp)

		DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Write	1st transmission	R[4]	R[3]	R[2]	R[1]	R[0]	
	2nd transmission	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]
	3rd transmission	B[4]	B[3]	B[2]	B[1]	B[0]	

Figure 45

Command List

Table 14 User Commnad

Operational Code (Hex)	Command	Command(C) /Read (R) /Write (W)	Number of Parameter	MIPI DCS Type 1 Requirement	LG4538 Implementation	Note
00h	Nop	C	0	Yes	Yes	
01h	soft_reset	C	0	Yes	Yes	
06h	get_red_channel	R	1	No	No	
07h	get_green_channel	R	1	No	No	
08h	get_blue_channel	R	1	No	No	
0Ah	get_power_mode	R	1	Yes	Yes	
0Bh	get_address_mode	R	1	Yes	Yes	
0Ch	get_pixel_format	R	1	Yes	Yes	
0Dh	get_display_mode	R	1	Yes	Yes	1
0Eh	get_signal_mode	R	1	Yes	Yes	
0Fh	get_diagnostic_ result	R	1	Bit7/6 : Yes Bit5/4 : Optional	No	
10h	enter_sleep_mode	C	0	Yes	Yes	
11h	exit_sleep_mode	C	0	Yes	Yes	
12h	enter_partial_mode	C	0	Yes	Yes	
13h	enter_normal_mode	C	0	Yes	Yes	
20h	exit_invert_mode	C	0	Yes	Yes	
21h	enter_invert_mode	C	0	Yes	Yes	
26h	set_gamma_curve	W	1	Yes	No	1
28h	set_display_off	C	0	Yes	Yes	
29h	set_display_on	C	0	Yes	Yes	
2Ah	set_column_address	W	4	Yes	Yes	
2Bh	set_page_address	W	4	Yes	Yes	
2Ch	write_memory_start	W	Variable	Yes	Yes	2
2Dh	wrtie_LUT	W	Variable	Optional	No	
2Eh	read_memory_start	R	Variable	Yes	Yes	2
30h	set_partial_area	W	4	Yes	Yes	
33h	set_scroll_area	W	6	Yes	Yes	
34h	set_tear_off	C	0	Yes	Yes	
35h	set_tear_on	W	1	Yes	Yes	
36h	set_address_mode	W	1	Yes	Yes	
37h	set_scroll_start	W	2	Yes	Yes	
38h	exit_idle_mode	C	0	Yes	Yes	
39h	enter_idle_mode	C	0	Yes	Yes	
3Ah	set_pixel_format	W	1	Yes	Yes	

3Ch	write_memory_ continue	W	Variable	Yes	Yes	2
3Eh	read_memory_ continue	R	Variable	Yes	Yes	2
44h	set_tear_scanline	W	2	Yes	Yes	
45h	get_scanline	R	2	Yes	Yes	
A1h	read_DDB_start	R	5	Yes	Yes	
A8h	read_DDB_ continue	R	Variable	Yes	Yes	

Notes : 1. The LG4538 supports one type of gamma curve specified by gamma adjustment register GC0. Therefore, D[2:0] bit (get_display_mode, 0Dh) is fiexed to at 0.
2. See DBI and DPI Data Formats for details on data write to the frame memory and data read from the frame memory.

Command Table

Table 15 User Commnad

Name	Addr	Size	R/W	D/nC	b7	b6	b5	b4	b3	b2	b1	b0	Default
NOP	00h	0	W	0									-
SWRESET	01h	0	W	0	SWRST = 1 (self cleared after a fixed delay)								-
RDDPM	0Ah	1	R	0									
				1	0	IDM	PTL	SLP	NOR	DISP	0	0	08h
RDDMADCTL	0Bh	1	R	0									
				1	MY	MX	MV	ML	BGR	0	FH	FV	00h
RDDCOLMOD	0Ch	1	R	0									
				1	0	DPIPF[2:0]			0	DBIPF[2:0]			66h
RDDIM	0Dh	1	R	0									
				1	VSCR	0	INV	0	0	0	0	0	00h
RDDSM	0Eh	1	R	0									
				1	TE	TEM	0	0	0	0	0	0	00h
SLPIN	10h	0	W	0	SLP = 1								1
SLPOUT	11h	0	W	0	SLP = 0								
PTLON	12h	0	W	0	PTL = 1								0
NORON	13h	0	W	0	NOR = 1 (equivalently PTL = 0 and VSCR = 0)								1
INVOFF	20h	0	W	0	INV = 0								0
INVON	21h	0	W	0	INV = 1								
DISPOFF	28h	0	W	0	DISP = 0								0
DISPON	29h	0	W	0	DISP = 1								
CASET	2Ah	4	W	0									
				1								SC [8]	00h
				1	SC[7:0]								00h
				1								EC [8]	00h
				1	EC[7:0]								EFh
PASET	2Bh	4	W	0									
				1								SP[8]	00h
				1	SP[7:0]								00h
				1								EP [0]	01h
				1	EP[7:0]								3Fh
RAMWR	2Ch	variable	W	0									
				1	DB[23:0]								-
RAMRD	2Eh	variable	R	0									
				1	DB[23:0]								-
PTLAR	30h	4	W	0									
				1								SR [8]	00h
				1	SR[7:0]								00h
				1								ER [8]	01h
				1	ER[7:0]								3Fh
VSCRDEF	33h	6	W	0									
				1								TFA [8]	00h
				1	TFA[7:0]								00h

				1								VSA [8]		01h
				1	VSA[7:0]									3Fh
				1								BFA [8]		00h
				1	BFA[7:0]									00h
TEOFF	34h	0	W	0	TE = 0									
TEON	35h	1	W	0	TE = 1									
				1								TEM		00h
MADCTL	36h	1	W	0										
				1	MY	MX	MV		BGR		FH	FV		00h
VSCRADD	37h	2	W	0	VSCR = 1									
				1								VSP [8]		00h
				1	VSP[7:0]									00h
IDMOFF	38h	0	W	0	IDM = 0									0
IDMON	39h	0	W	0	IDM = 1									
COLMOD	3Ah	1	W	0										
				1		DPIPF[2:0]				DBIPF[2:0]				66h
RAMWRC	3Ch	variable	W	0										
				1	DB[17:0]									-
RAMRDC	3Eh	variable	R	0										
				1	DB[17:0]									-
TELINE	44h	2	W	0										
				1										00h
				1	TELINE[7:0]									00h
SCANLINE	45h	2	R	0										
				1							SCANLINE [9:8]			XXh
				1	SCANLINE[7:0]									XXh
RDDDB	A1h	variable	R	0										
				1	DB[17:0]									-
RDDDBC	A8h	variable	R	0										
				1	DB[17:0]									-

Table 16 Manufactureer Commnad

Name	Addr	Size	R/W	D/Cb	7	6	5	4	3	2	1	0	Default
LPMS	B1h	1	R/W	0									
				1				OSCEN				DSTB	00h
RGBIF	B2h	1	R/W	0									
				1					CKPL	HSPL	VSPL	ENPL	00h
FMAS	B3h	3	R/W	0									
				1	DFM[1:0]		EPF[1:0]					WEMODE	00h
				1						TEI[2:0]			00h
				1						DENC[2:0]			00h
DMFMW	B4h	2	R/W	0									
				1	BYPASS			RM			DM[1:0]		00h
												ENDIAN	00h
DISPMODE	B5h	1	R/W	0									
				1				DITH			DEPF[1:0]		00h
PANELDRV	B8h	4	R/W	0									
				1			GS	SM		NDL		REV	00h
				1		NL[6:0]							4Fh
				1		SCN[6:0]							00h
				1			BC0	EOR				NW	00h
DISPCTL	B9h	4	R/W	0									
				1	BP[7:0]								08h
				1	FP[7:0]								08h
				1						PTS[2:0]			00h
				1	ISC[3:0]							PTG	00h
PWRCTL1	BAh	5	R/W	0									
				1						VC[2:0]			00h
				1						BT[2:0]			00h
				1					VRH[3:0]				03h
				1						AP[2:0]			03h
				1						SAP[2:0]			03h
PWRCTL2	BBh	3	R/W	0									
				1				VDV[4:0]					13h
				1		VCM[6:0]							60h
				1								VCOMG	01h
PWRCTL3	BCh	3	R/W	0									
				1								DSEN	00h
				1						DC0[2:0]			03h

				1						DC1[2:0]		03h
VDDSET	BDh	2	R/W	0								
				1		RSET[2:0]				RI[2:0]		40h
				1		RV[2:0]				RCONT[2:0]		20h
GAMMASET	C0h	1	R/W	0								
				1						SGE	EN_MA PS	00h
RGAMMAP	C1h	9	R/W	0								
				1		PKP1[2:0]				PKP0[2:0]		00h
				1		PKP3[2:0]				PKP2[2:0]		00h
				1		PKP5[2:0]				PKP4[2:0]		00h
				1		PRP1[2:0]				PRP0[2:0]		00h
				1				VRP0[4:0]				00h
				1				VRP1[4:0]				00h
				1		PFP1[2:0]				PFP0[2:0]		11h
				1		PFP3[2:0]				PFP2[2:0]		11h
				1						PMP[2:0]		01h
RGAMMAN	C2h	9	R/W	0								
				1		PKN1[2:0]				PKN0[2:0]		00h
				1		PKN3[2:0]				PKN2[2:0]		00h
				1		PKN5[2:0]				PKN4[2:0]		00h
				1		PRN1[2:0]				PRN0[2:0]		00h
				1				VRN0[4:0]				00h
				1				VRN1[4:0]				00h
				1		PFN1[2:0]				PFN0[2:0]		11h
				1		PFN3[2:0]				PFN2[2:0]		11h
				1						PMN[2:0]		01h
GGAMMAP	C3h	9	R/W	0								
				1		PKP1[2:0]				PKP0[2:0]		00h
				1		PKP3[2:0]				PKP2[2:0]		00h
				1		PKP5[2:0]				PKP4[2:0]		00h
				1		PRP1[2:0]				PRP0[2:0]		00h
				1				VRP0[4:0]				00h
				1				VRP1[4:0]				00h
				1		PFP1[2:0]				PFP0[2:0]		11h
				1		PFP3[2:0]				PFP2[2:0]		11h
				1						PMP[2:0]		01h
GGAMMAN	C4h	9	R/W	0								
				1		PKN1[2:0]				PKN0[2:0]		00h
				1		PKN3[2:0]				PKN2[2:0]		00h

				1		PKN5[2:0]				PKN4[2:0]						00h
				1		PRN1[2:0]				PRN0[2:0]						00h
				1				VRN0[4:0]								00h
				1				VRN1[4:0]								00h
				1		PFN1[2:0]				PFN0[2:0]						11h
				1		PFN3[2:0]				PFN2[2:0]						11h
				1						PMN[2:0]						01h
BGAMMAP	C5h	9	R/W	0												
				1		PKP1[2:0]				PKP0[2:0]						00h
				1		PKP3[2:0]				PKP2[2:0]						00h
				1		PKP5[2:0]				PKP4[2:0]						00h
				1		PRP1[2:0]				PRP0[2:0]						00h
				1				VRP0[4:0]								00h
				1				VRP1[4:0]								00h
				1		PFP1[2:0]				PFP0[2:0]						11h
				1		PFP3[2:0]				PFP2[2:0]						11h
				1						PMP[2:0]						01h
BGAMMAN	C6h	9	R/W	0												
				1		PKN1[2:0]				PKN0[2:0]						00h
				1		PKN3[2:0]				PKN2[2:0]						00h
				1		PKN5[2:0]				PKN4[2:0]						00h
				1		PRN1[2:0]				PRN0[2:0]						00h
				1				VRN0[4:0]								00h
				1				VRN1[4:0]								00h
				1		PFN1[2:0]				PFN0[2:0]						11h
				1		PFN3[2:0]				PFN2[2:0]						11h
				1						PMN[2:0]						01h
DISPTSET	D0h	2	R/W	0												
				1										DIV[1:0]		00h
				1					RTN[7:0]							9Bh
SCVMTSET	D1h	5	R/W	0												
				1		EQ2[2:0]				EQ1[2:0]						00h
				1						MCP[3:0]						00h
				1						NOW[3:0]						00h
				1						SDT[3:0]						00h
				1			SEQC[1:0]			SEQ[2:0]						00h
BLCTL	D2h	6	R/W	0												
				1					DBV[7:0]							00h
				1			BCTRL		DO	BL	BLONEN	BLON				00h

				1							CABC[1:0]		00h
				1	CMB[7:0]								00h
				1	CDSP[3:0]				CDMP[3:0]				00h
				1	PWMP						FPWM[1:0]		00h
				1	PF[7:0]								00h
RDDISBV	D3h	1	R	0									
				1	DBV[7:0]								-
FRSET	D4h	2	R/W	0									
				1								OHZ	00h
				1						FRS[2:0]			05h
GATE_CTL	D5h	1	R/W	0									
				1				ALLOFF				ALLON	
VREF_CTL	D6h	1	R/W	0									
				1				VREFT				VREFEN	00h
				1				VREFVR				VREFDD	00h
TEST1	F0h	8	R/W	0									
				1				TDFN			TDLY[1:0]		00h
				1				TOSC			TVCOM[1:0]		00h
				1				REGULPD		TSAP		TSHZ	00h
				1				TPATE		TPAT[2:0]			00h
				1				TSD_EN			TSD[1:0]		00h
				1		LINEINV		TVON		HaltVreg		MultiVCOM	01h
				1	STBN		RDSM[1:0]				WRPW[1:0]		00h
				1		D_SHIZ	H_HIZ	L_HIZ	SBC	S_SCV	SWP		00h
TEST2	F1h	2	R/W	0									
				1								AUTO	01h
				1					MEN4	MEN3	MEN2	MEN1	00h
OTP1	F2h	3	R/W	0									
				1	PTM[1:0]				PRD	PWE	VPP	PPROG	00h
				1	APRG						PA[1:0]		80h
				1	PDIN[7:0]								00h
OTP2	F3h	1	R/W	0									00h

				1	VCMSEL[1:0]	MSEL[1:0]			RA[1:0]		30h
OTP3	F4h	0	W	0	AUTO_WR = 1						
OTP4	F5h	1	R/W	0							
				1	OTP_WP[7:0]						00h
OTP5	F6h	4	R/W	0							
				1	OTP_WD[7:0]						FFh
				1	OTP_WD[15:8]						FFh
				1	OTP_WD[23:16]						FFh
				1	OTP_WD[31:24]						FFh
OTP6	F7h	1	R/W	0							
				1							OTP_DSEL	00h
OTP7	F8h	3	R/W	0							
				1				TRSEL			RSEL	00h
				1				REFTR[4:0]				
				1		REFRS[6:0]						
OTP8	F9h	1	R	0							
				1	PDOUT[7:0]							-
OTP9	FAh	4	R	0							
				1	DID[7:0]							-
				1	DID[15:8]							-
				1	DID[23:16]							-
				1	DID[31:24]							-
OTP10	FBh	2	R	0								
				1				REFTR_OUT[4:0]				-
				1		REFRS_OUT[6:0]						-

Command Accessibilty

In initial state, only User Command and B0h Manufacturer Command Access Protect command are accessible. Other commands are treated as nop.

Manufacturer Command(B0h-FFh) defined in the table below

Table 17 User Commnad

Operational Code (Hex)	Command	Command Accessibility				
		Normal Mode On Idle Mode Off Sleep Mode Off	Normal Mode On Idle Mode On Sleep Mode Off	Partial Mode On Idle Mode Off Sleep Mode Off	Partial Mode On Idle Mode On Sleep Mode Off	Sleep Mode On
00h	Nop	Yes	Yes	Yes	Yes	Yes
01h	soft_reset	DM = 0 (Note)	DM = 0 (Note)	DM = 0 (Note)	DM = 0 (Note)	Yes
0Ah	get_power_mode	Yes	Yes	Yes	Yes	Yes
0Bh	get_address_mode	Yes	Yes	Yes	Yes	Yes
0Ch	get_pixel_format	Yes	Yes	Yes	Yes	Yes
0Dh	get_display_mode	Yes	Yes	Yes	Yes	Yes
0Eh	get_signal_mode	DM = 0 (Note)	DM = 0 (Note)	DM = 0 (Note)	DM = 0 (Note)	Yes
0Fh	get_diagnostic_ result	Yes	Yes	Yes	Yes	Yes
10h	enter_sleep_mode	DM = 0 (Note)	DM = 0 (Note)	DM = 0 (Note)	DM = 0 (Note)	Yes
11h	exit_sleep_mode	DM = 0 (Note)	DM = 0 (Note)	DM = 0 (Note)	DM = 0 (Note)	Yes
12h	enter_partial_mode	DM = 0 (Note)	DM = 0 (Note)	DM = 0 (Note)	DM = 0 (Note)	Yes
13h	enter_normal_mode	Yes	Yes	Yes	Yes	Yes
20h	exit_invert_mode	Yes	Yes	Yes	Yes	Yes
21h	enter_invert_mode	Yes	Yes	Yes	Yes	Yes
28h	set_display_off	Yes	Yes	Yes	Yes	Yes
29h	set_display_on	Yes	Yes	Yes	Yes	Yes
2Ah	set_column_address	Yes	Yes	Yes	Yes	Yes
2Bh	set_page_address	Yes	Yes	Yes	Yes	Yes
2Ch	write_memory_start	Yes	Yes	Yes	Yes	Yes
2Eh	read_memory_start	DM = 0 (Note)	DM = 0 (Note)	DM = 0 (Note)	DM = 0 (Note)	Yes
30h	set_partial_area	DM = 0 (Note)	DM = 0 (Note)	DM = 0 (Note)	DM = 0 (Note)	Yes
33h	set_scroll_area	DM = 0 (Note)	DM = 0 (Note)	DM = 0 (Note)	DM = 0 (Note)	Yes
34h	set_tear_off	DM = 0 (Note)	DM = 0 (Note)	DM = 0 (Note)	DM = 0 (Note)	Yes
35h	set_tear_on	DM = 0 (Note)	DM = 0 (Note)	DM = 0 (Note)	DM = 0 (Note)	Yes
36h	set_address_mode	Yes	Yes	Yes	Yes	Yes
37h	set_scroll_start	DM = 0 (Note)	DM = 0 (Note)	DM = 0 (Note)	DM = 0 (Note)	Yes
38h	exit_idle_mode	DM = 0 (Note)	DM = 0 (Note)	DM = 0 (Note)	DM = 0 (Note)	Yes
39h	enter_idle_mode	DM = 0 (Note)	DM = 0 (Note)	DM = 0 (Note)	DM = 0 (Note)	Yes
3Ah	set_pixel_format	Yes	Yes	Yes	Yes	Yes

3Ch	write_memory_ continue	DM = 0 (Note)	DM = 0 (Note)	DM = 0 (Note)	DM = 0 (Note)	Yes
3Eh	read_memory_ continue	DM = 0 (Note)	DM = 0 (Note)	DM = 0 (Note)	DM = 0 (Note)	Yes
44h	set_tear_scanline	DM = 0 (Note)	DM = 0 (Note)	DM = 0 (Note)	DM = 0 (Note)	Yes
45h	get_scanline	DM = 0 (Note)	DM = 0 (Note)	DM = 0 (Note)	DM = 0 (Note)	No
A1h	read_DDB_start	Yes	Yes	Yes	Yes	Yes

Note : Command may be accessed only when DM= 0 (display operation is in synchrnonization with internal oscillation clock).
To access these commands is disabled when DM = 1 and DPI is selected.

Table 18 Manufacturer Commnad

Operational Code (Hex)	**Command**	**Command Accessibility**				
		Normal Mode On Idle Mode Off Sleep Mode Off	**Normal Mode On Idle Mode On Sleep Mode Off**	**Partial Mode On Idle Mode Off Sleep Mode Off**	**Partial Mode On Idle Mode On Sleep Mode Off**	**Sleep Mode On**
B1h	Low Power Setting	No	No	No	No	Yes
B2h	DPI Setting	Yes	Yes	Yes	Yes	Yes
B3h	Frame Memory Access and Interface Setting	Yes	Yes	Yes	Yes	Yes
B4h	Display Mode and Frame Memory Write Mode Setting	Yes	Yes	Yes	Yes	Yes
B5h	Display Mode Control	Yes	Yes	Yes	Yes	Yes
B8h	Panel Driving Setting	Yes	Yes	Yes	Yes	Yes
B9h	Display Control	Yes	Yes	Yes	Yes	Yes
BAh	Power Setting - Common Mode	Yes	Yes	Yes	Yes	Yes
BBh	Power Setting - VCOM Setting	Yes	Yes	Yes	Yes	Yes
BCh	Power Setting - Step-up Frequency Setting	Yes	Yes	Yes	Yes	Yes
BDh	VDD Regulator Setting	Yes	Yes	Yes	Yes	Yes
C0h	Gamma Select Setting	Yes	Yes	Yes	Yes	Yes
C1h	Gamma Set A “+” polarity	Yes	Yes	Yes	Yes	Yes
C2h	Gamma Set A “-” Polarity	Yes	Yes	Yes	Yes	Yes

C3h	Gamma Set B “+” Polarity	Yes	Yes	Yes	Yes	Yes
C4h	Gamma Set B “-” Polarity	Yes	Yes	Yes	Yes	Yes
C5h	Gamma Set C “+” Polarity	Yes	Yes	Yes	Yes	Yes
C6h	Gamma Set C “-” polarity	Yes	Yes	Yes	Yes	Yes
D0h	Display Timing Setting	Yes	Yes	Yes	Yes	Yes
D1h	Source/VCOM/Gate Driving Timing Setting	Yes	Yes	Yes	Yes	Yes
D2h	Backlight Setting	Yes	Yes	Yes	Yes	Yes
D3h	Read Display Brightness Value	Yes	Yes	Yes	Yes	Yes
D4h	Frame Rate Control	Yes	Yes	Yes	Yes	Yes
D5h	Gate Control	Yes	Yes	Yes	Yes	Yes
D6h	VREF Control	Yes	Yes	Yes	Yes	Yes
F0h	Test Control	Yes	Yes	Yes	Yes	Yes
F1h	Test Control	Yes	Yes	Yes	Yes	Yes
F27h	EPROM Control Setting1	Yes	Yes	Yes	Yes	Yes
F3h	EPROM Control Setting2	Yes	Yes	Yes	Yes	Yes
F4h	EPROM Control Setting3	Yes	Yes	Yes	Yes	Yes
F5h	EPROM Control Setting4	Yes	Yes	Yes	Yes	Yes
F6h	EPROM Control Setting5	Yes	Yes	Yes	Yes	Yes
F7h	EPROM Control Setting6	Yes	Yes	Yes	Yes	Yes
F8h	EPROM Control Setting7	Yes	Yes	Yes	Yes	Yes
F9h	EPROM Data Read	Yes	Yes	Yes	Yes	Yes
FAh	EPROM Data Read	Yes	Yes	Yes	Yes	Yes
FBh	EPROM Data Read	Yes	Yes	Yes	Yes	Yes

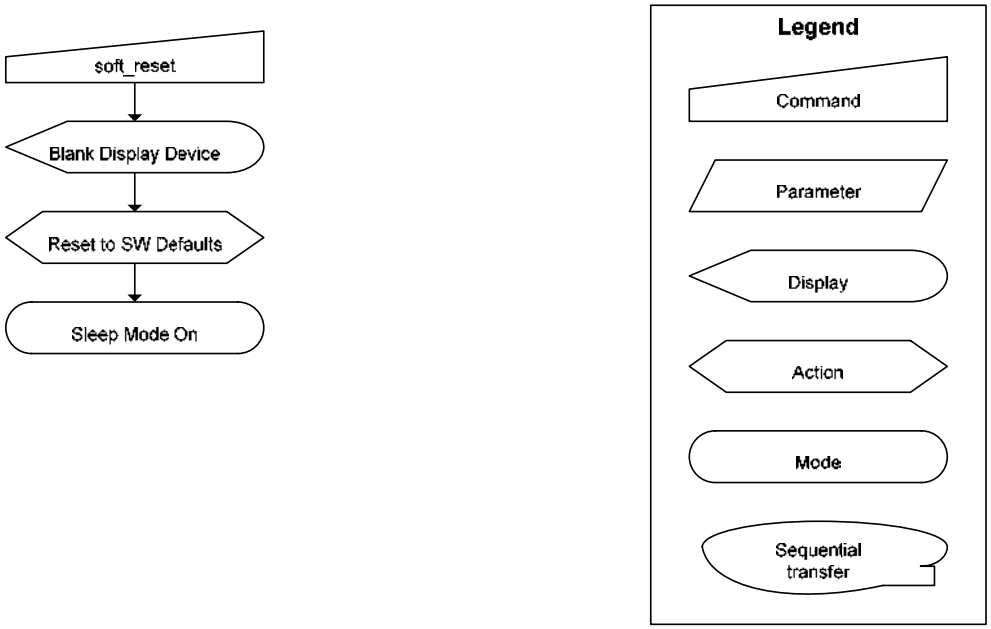
nop : 00h

00h	nop												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	0	0	0	0	0	0	0	0	00h
Parameter	None												
Description	This Command is an empty command: it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read. X = Don't care												
Restriction	-												
Flow Chart	-												

soft_reset : 01h

01h	soft_reset												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	0	0	0	0	0	0	0	1	01h
Parameter	None												
Description	The display module performs a software reset. Commands and parameters are written with their SW Reset default values. (See “Default Modes and Values”) Note : The Frame Memory contents are unaffected by this command.												
Restriction	If a soft_reset is sent when the display module is in Sleep Mode, the host processor must wait 120 milliseconds before sending an exit_sleep_mode command. Soft_reset should not be sent during exit_sleep_mode sequence. No new command setting is allowed until the LG4538 enters the Sleep Mode. See “State & Command sequence” for sequence to enter Sleep Mode. If a soft_reset is sent when the display module is in Sleep Mode, data in NVM are read. No new command setting is inhibited when data are read (5ms).												

Flow Chart



get_power_mode : 0Ah

0Ah	get_power_mode												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	0	0	0	0	1	0	1	0	0Ah
Parameter	1	↑	1	X	0	IDMON	PTLON	SLPOUT	NORON	DSPON	0	0	xxh

Description

The display module returns the current power mode.

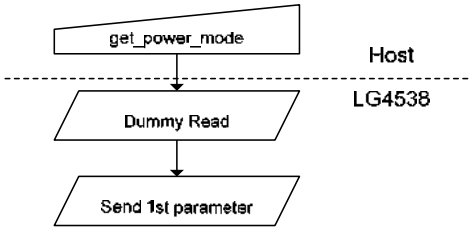
Bit	Description	Comment	Command list Symbol
D7	Reserved	Set to “0”	-
D6	Idle Mode On/Off		IDMON
D5	Partial Mode On/Off		PTLON
D4	Sleep Mode On/Off		SLPOUT
D3	Display Noraml Mode On/Off		NORON
D2	Dsiplay On/Off		DSPON
D1	Reserved		-
D0	Reserved		-

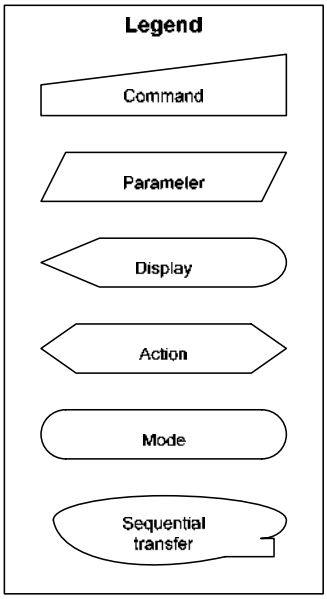
- Bit D7 – Not defined
  This bit is not used. “0” is read.
- Bit D6 – Idle Mode On/Off
  ‘0’ = Idle Mode Off
  ‘1’ = Idle Mode On
- Bit D5 – Partial Mode On/Off
  ‘0’ = Partial Mode Off
  ‘1’ = Partial Mode On
- Bit D4 – Sleep Mode On/Off
  ‘0’ = Sleep Mode Off
  ‘1’ = Sleep Mod On
- Bit D3 – Display Normal Mode On/Off
  ‘0’ = Display Normal Mode Off
  ‘1’ = Display Normal Mode On
- Bit D2 – Display On/Off
  ‘0’ = Display is Off
  ‘1’ = Display is On
- Bit D1 – Not defined
  This bit is not used. “0” is read.
- Bit D0 – Not defined
  This bit is not used. “0” is read.

X = Don’t care

Restriction -

Flow Chart


get_power_mode
Host
LG4538
Dummy Read
Send 1st parameter


Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

get_address_mode : 0Bh

0Bh	get_address_mode												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	0	0	0	0	1	0	1	1	0Bh
Parameter	1	↑	1	X	B7	B6	B5	B4	B3	B2	B1	B0	xxh

The display module returns the current power mode.

Bit	Description	Comment	Command list Symbol
D7	Page Address Order		B7
D6	Column Address Order		B6
D5	Page/Column Order		B5
D4	Line Address Order		B4
D3	RGB/BGR Order		B3
D2	Display Data Latch Order		B2
D1	Flip Horizontal		B1
D0	Flip Vertical		B0

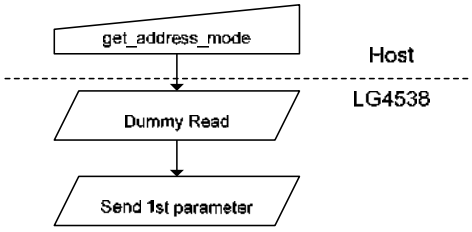
Description

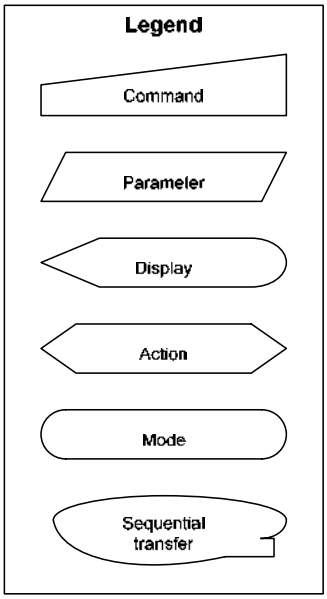
- Bit D7 – Page Address Order
  ‘0’ = Top to Bottom (When set_address_mode D7= ‘0’)
  ‘1’ = Bottom to Top (When set_address_mode D7= ‘1’)
- Bit D6 – Column Address Order
  ‘0’ = Left ro Right (When set_address_mode D6= ‘0’)
  ‘1’ = Right to Left (When set_address_mode D6= ‘1’)
- Bit D5 – Page/Column Order
  ‘0’ = Normal Mode (When set_address_mode D5= ‘0’)
  ‘1’ = Reverse Mode (When set_address_mode D5= ‘1’)
- Bit D4 – Line Address Order
  ‘0’ = LCD Refresh Top to Bottom (When set_address_mode D4= ‘0’)
  ‘1’ = LCD Refresh Bottom to Top (When set_address_mode D4= ‘1’)
- Bit D3 – RGB/BGR Order
  ‘0’ = Pixel in RGB order (When set_address_mode D3= ‘0’)
  ‘1’ = Pixel in BGR order (When set_address_mode D3= ‘1’)
- Bit D2 – Display Data Latch Data Order
  ‘0’ = LCD Refresh Left to Right (When set_address_mode D2= ‘0’)
  ‘1’ = LCD Refresh Right to Left (When set_address_mode D2= ‘1’)
- Bit D1 – Flip Horizontal
  ‘0’ = Normal (When set_address_mode D1= ‘0’)
  ‘1’ = Flip (When set_address_mode D1= ‘1’)
- Bit D0 – Flip Vertcal
  ‘0’ = Normal (When set_address_mode D0= ‘0’)
  ‘1’ = Flip (When set_address_mode D0= ‘1’)

X = Don’t care

Restriction -

Flow Chart


get_address_mode
Host
LG4538
Dummy Read
Send 1st parameter


Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

get_pixel_format : 0Ch

0Ch	get_pixel_format												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	0	0	0	0	1	1	0	0	0Ch
Parameter	1	↑	1	X	0	D6	D5	D4	0	D2	D1	D0	xxh

Description

The display module returns the current power mode.

Bit	Description	Comment	Command list Symbol
D7	Reserved	Set to “0”	-
D6	DPI (RGB Interface Color Format)		-
D5			
D4			
D3	Reserved	Set to “0”	-
D2	DBI (System Interface Color Format)		-
D1			
D0			

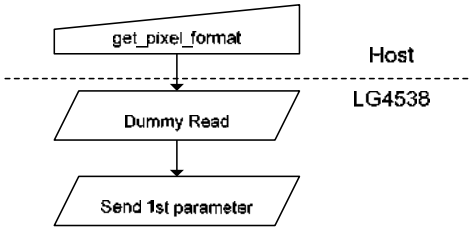
- Bit D[6:4] – DPI Pixel Format (RGB Interface Color Format Selection)
- Bit D[2:0] – DBI Pixel Format(System Interface Color Format Selection)
- Bit D7 and D3 – This Bits are not used.
  This bit is not used. “0” is read.

See description of command set_pixel_format(3Ah).

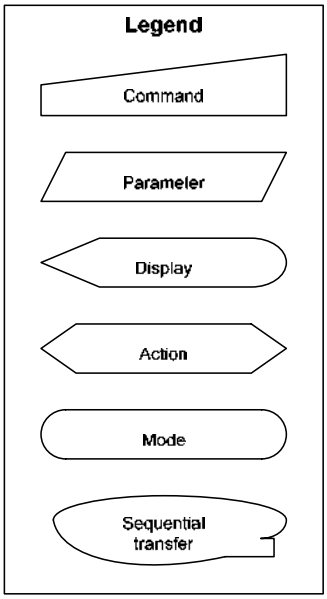
Control Interface Color Format	**D6/D2**	**D5/D1**	**D4/D0**
Setting disabled	0	0	0
Setting disabled	0	0	1
Setting disabled	0	1	0
Setting disabled	0	1	1
Setting disabled	1	0	0
16bit/pixel (65,536 colors)	1	0	1
18bit/pixel (262,144 colors)	1	1	0
Setting disabled	1	1	1

X = Don’t care

Restriction -


get_pixel_format
Host
LG4538
Dummy Read
Send 1st parameter

Flow Chart


Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

get_display_mode : 0Dh

0Dh	get_display_mode												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	0	0	0	0	1	1	0	1	0Dh
Parameter	1	↑	1	X	VSCR	0	INV	0	0	0	0	0	xxh

Description

The display module returns the current status of the display as described in the table below.
This command setting depends on set_address_mode (36h).

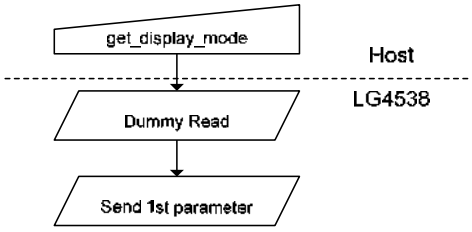
Bit	Description	Comment	Command list Symbol
D7	Vertiacal Scrolling On/Off		VSCR
D6	Reserved	Set to “0”	-
D5	Inversion On/Off		INV
D4	Reserved	Set to “0”	-
D3	Reserved	Set to “0”	-
D2	Gamma Curve Selection	Set to “0”	-
D1	Gamma Curve Selection	Set to “0”	-
D0	Gamma Curve Selection	Set to “0”	-

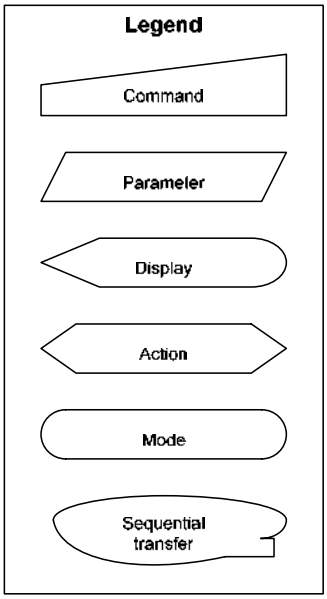
- Bit D7 – Vertical Scrolling On/Off
  ‘0’ = Vertical Scrolling Off
  ‘1’ = Vertical Scrolling On
- Bit D6 – Reserved
  This bit is not used. “0” is read.
- ‘Bit D5 – Inversion On/Off
  ‘0’ = Inversion Off
  ‘1’ = Inversion On
- Bit D4, D3 – Reserved
  These bits are not used. “0” is read.
- Bit D2,D1,D0 – Gamma Curve Selection
  These bits are not used. “0” is read.

X = Don’t care

Restriction -

Flow Chart


get_display_mode
Host
LG4538
Dummy Read
Send 1st parameter


Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

get_signal_mode : 0Eh

0Eh	get_signal_mode												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	0	0	0	0	1	1	1	0	0Eh
Parameter	1	↑	1	X	TE ON	TE M	0	0	0	0	0	0	xxh

Description

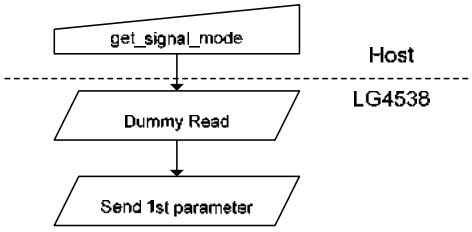
The display module returns the current power mode.

Bit	Description	Comment	Command list Symbol
D7	Tearing Effect line On/Off		TEON
D6	Tearing Effect line Ouput Mode		TEM
D5	Reserved	Set to “0”	-
D4	Reserved	Set to “0”	-
D3	Reserved	Set to “0”	-
D2	Reserved	Set to “0”	-
D1	Reserved	Set to “0”	-
D0	Reserved	Set to “0”	-

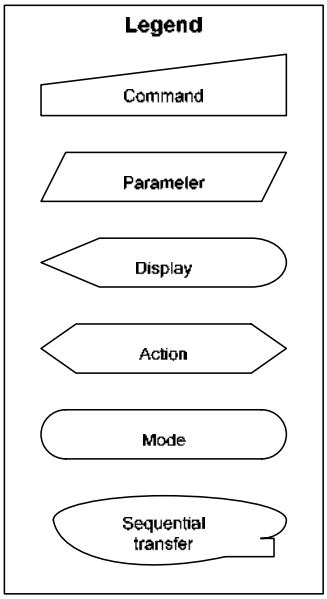
- Bit D7 – Tearing Effect Line On/Off
  ‘0’ = Tearing Effect line Off
  ‘1’ = Tearing Effect On
- Bit D6 – Tearing Effect Line Output Mode (See “set_tear_on: 35h)
  ‘0’ = Mode 1
  ‘1’ = Mode 2
- Bit D5-D0 – Reserved
  These bits are not used. “0” is read.

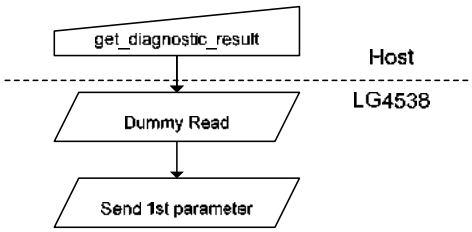
X = Don’t care

Restriction -

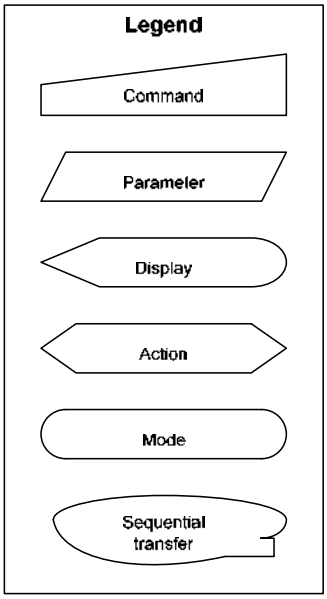


Flow Chart

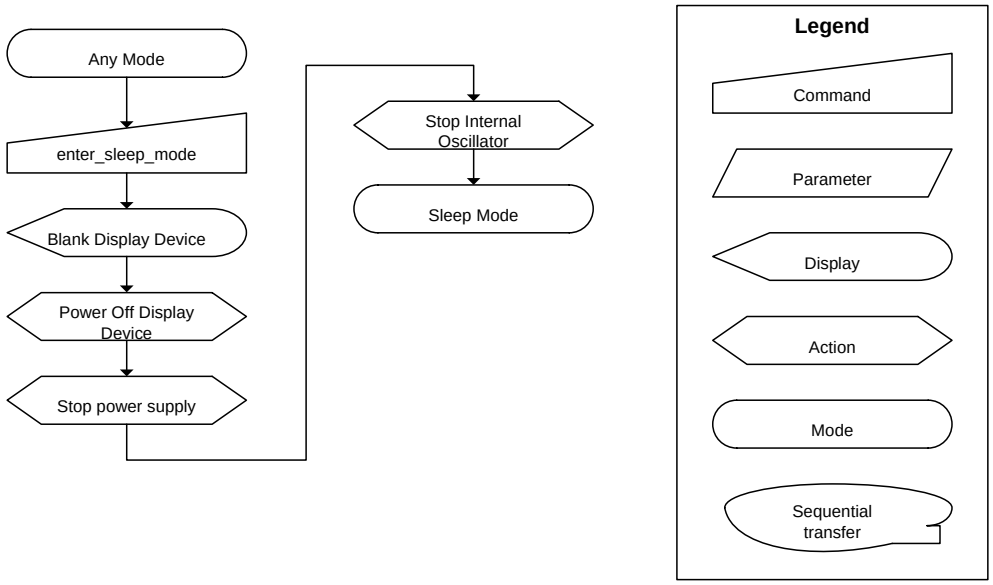




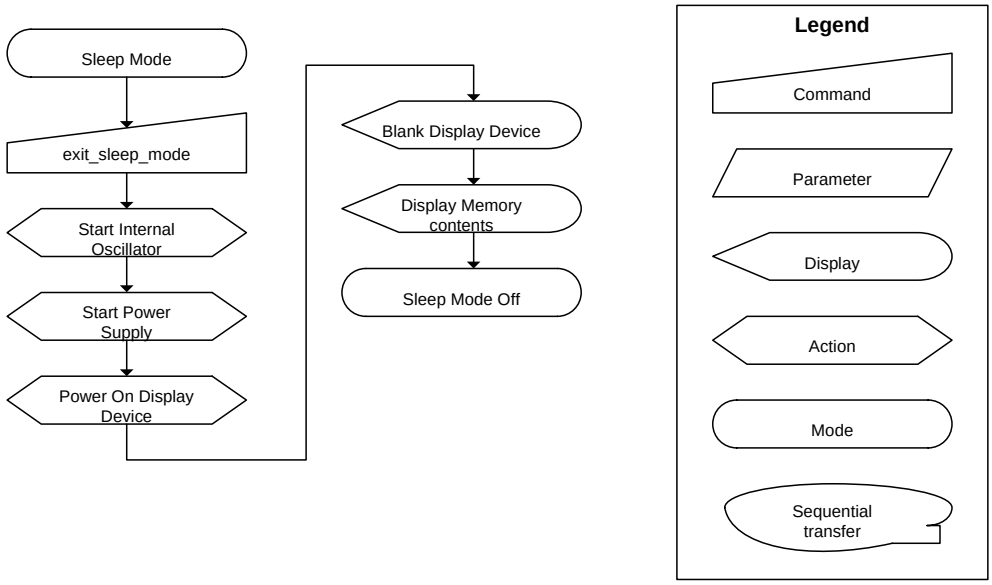
Flow Chart



enter_sleep_mode : 10h

10h	enter_sleep_mode												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	0	0	0	1	0	0	0	0	10h
Parameter	None												
Description	This command causes the LCD module to enter the Sleep mode. In this mode, the DC/DC converter, internal oscillator and panel scanning stop. See “State & Command sequence” for Sleep In sequence. DBI remains operational and the memory maintains its conditaion. See “state Transition Diagram” for each stage of transition X = Don’t care												
Restriction	This command has no effect when the module is already in Sleep mode. Sleep mode can be exited only when the exit_sleep_mode (11h) is transmitted. Sending a new command is prohibited while the LG4538 perfoms either power supply OFF sequence or blank scan.												
Flow Chart													

exit_sleep_mode : 11h

11h	exit_sleep_mode												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	0	0	0	1	0	0	0	1	11h
Parameter	None												
Description	This command causes the LCD module to exit the Sleep mode. DC/DC converter, internal oscillator and panel scanning start. See “State & Command sequence” for exit_sleep_mode. See “state Transition Diagram” for each stage of transition X = Don’t care												
Restriction	This command shall not cause any visual effect on display device when the display module is not in sleep mode. No new command setting is allowed during power supply On sequence. Operation may continue for more than 120msec due to power supply On sequence setting. Do not send any command aloes in this case. The host processor must wait 120msec after sending an enter_sleep_mode command before sending an exit_sleep_mode command. The display runs the self-diagnostic function after this command is received.												
Flow Chart													

enter_partial_mode : 12h

12h	enter_partial_mode												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	0	0	0	1	0	0	1	0	12h
Parameter	None												
Description	This command causes the LCD module to enter the Partial mode. The Partial Display Mode window is described by the set_partial_area command (30h). To leave Partial Display Mode, the enter_normal_mode (13h) should be written. X = Don't care Note : When a command breaks in the middle of frame period in Normal mode, the command is enabled from the next frame period.												
Restriction	This command has no effect when the module is already in Partial mode. This command causes scrolling function disabled.												
Flow Chart	See set_partial_area (30h)												

enter_normal_mode : 13h

13h	enter_normal_mode												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	0	0	0	1	0	0	1	1	13h
Parameter	None												
Description	This command causes the display module to enter the Normal mode. Noraml Mode means Partial mode and Scroll mode are off. X = Don’t care Note : When a command breaks in the middle of frame period in Partail mode, that command becomes valid from the next frame period.												
Restriction	This command has no effect when Normal mode is already active.												
Flow Chart	See the description of commands set_partial_area (30h) and set_scroll_area (33h) when using this command.												

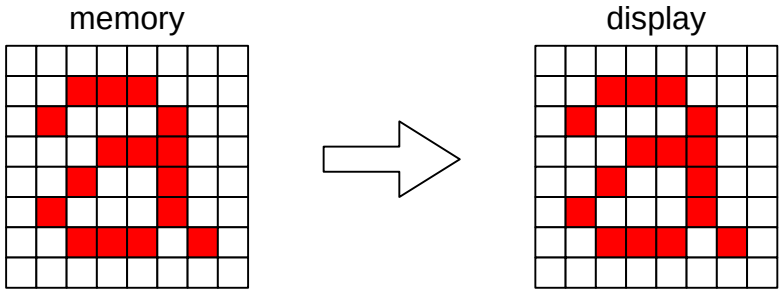
exit_invert_mode : 20h

20h	exit_invert_mode												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	0	0	1	0	0	0	0	0	20h
Parameter	None												

Description

This command causes the display module to stop inverting the image data on the display device. The frame memory contents remain unchanged. No status bits are changed.

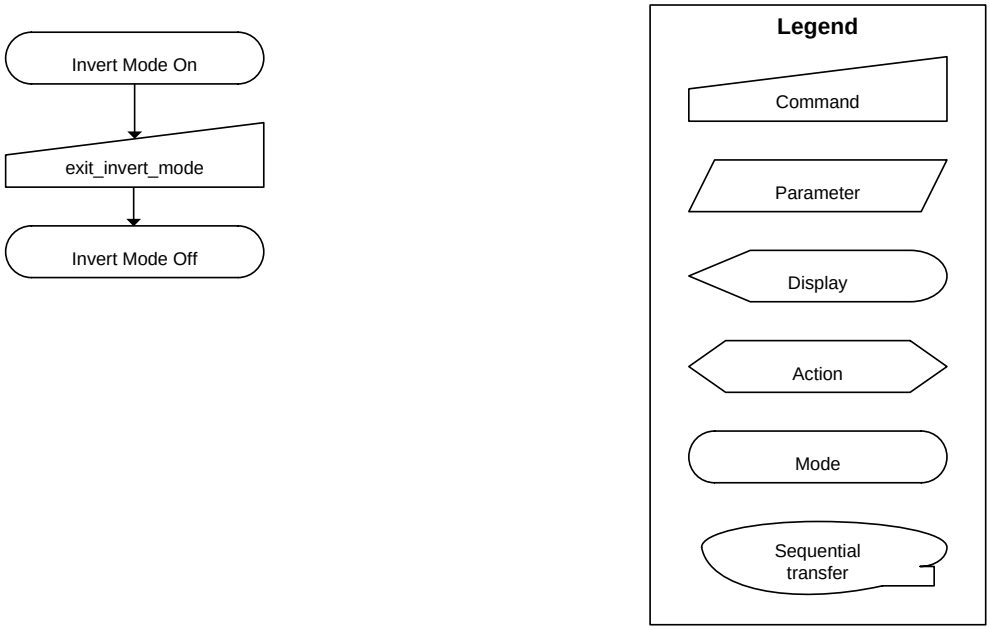
(Example)



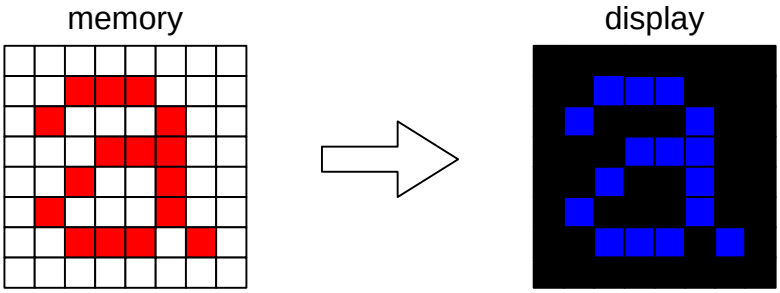
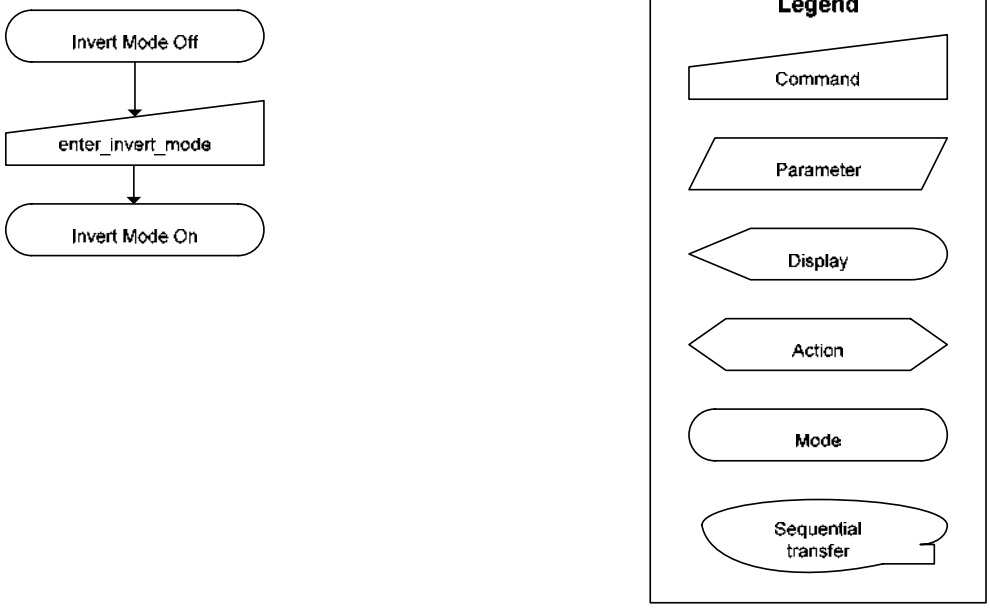
X = Don't care

Restriction This command has no effect when the module is already in Inversion Off.

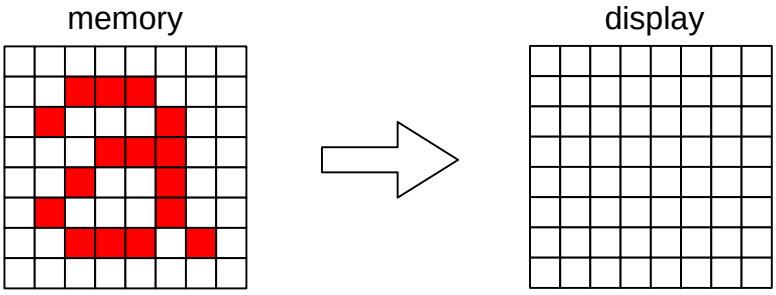
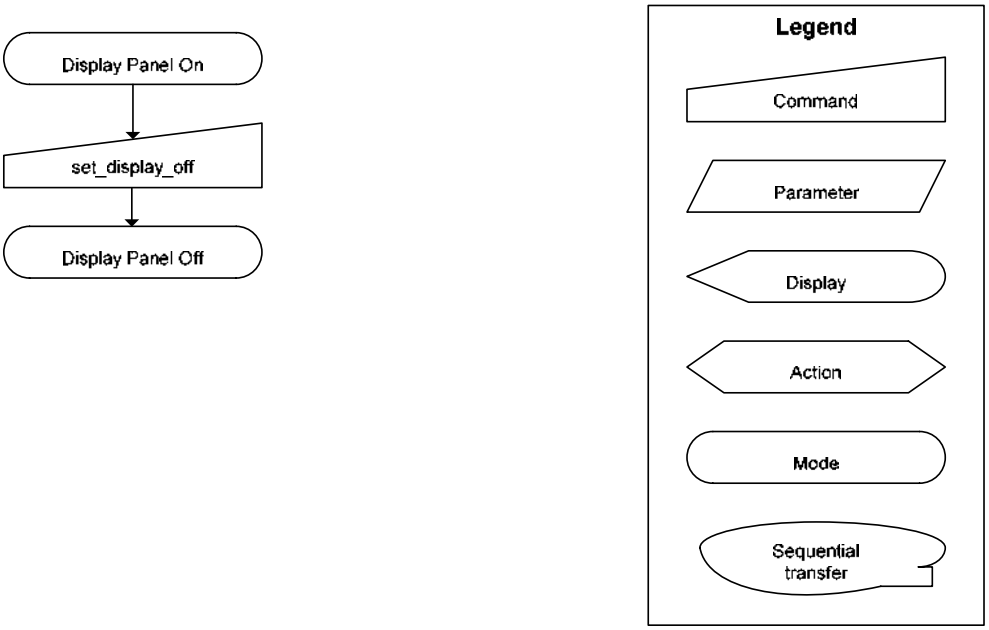
Flow Chart



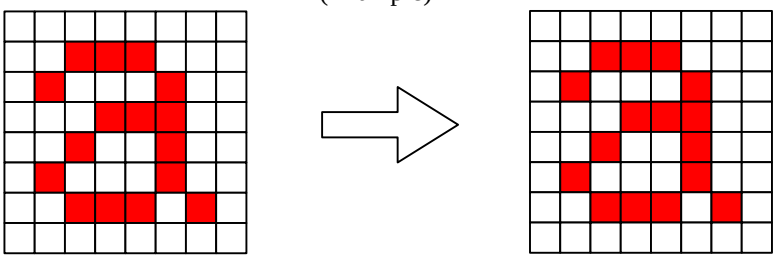
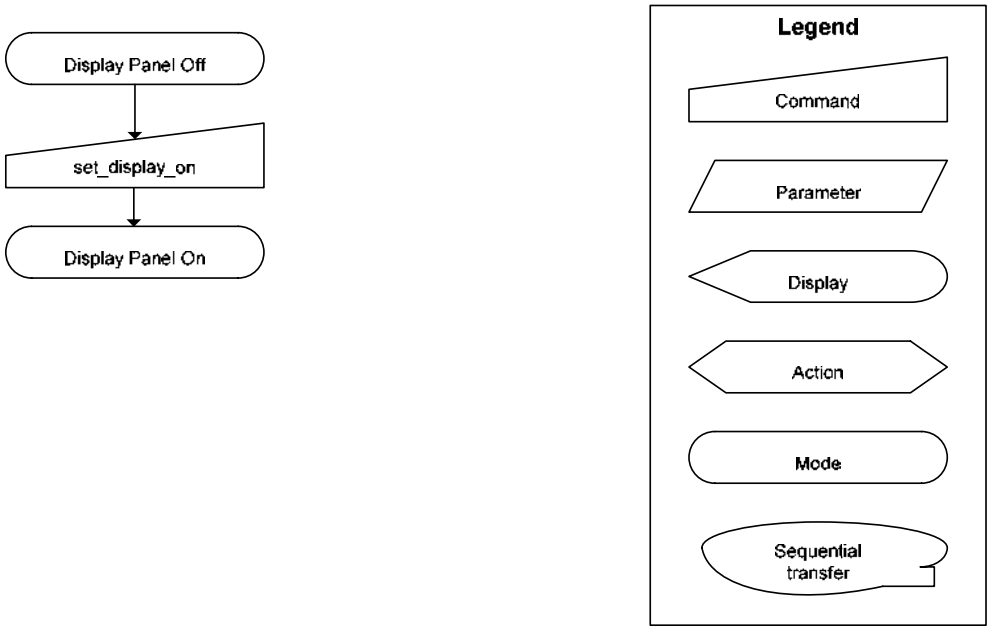
enter_invert_mode : 21h

21h	enter_invert_mode												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	0	0	1	0	0	0	0	1	21h
Parameter	None												
Description	This command causes the display module to invert the image data only on the display device. The frame memory contents remain unchanged. All bits send from the frame memory to the display invert. No status bits are changed. (Example)  X = Don't care												
Restriction	This command has no effect when the display module is already inverting the display image..												
Flow Chart													

set_display_off : 28h

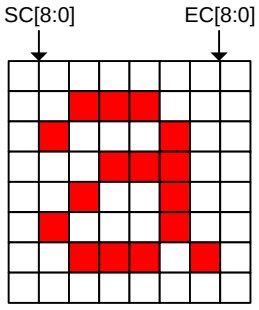
28h	set_display_off												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	0	0	1	0	1	0	0	0	28h
Parameter	None												
Description	This command causes the display module to stop displaying the image data on the display device. The frame memory contents remain unchanged. No status bits are changed. (Example)  See Panel Driving setting (xxh) X = Don't care												
Restriction	This command has no effect when the display panel is already off.												
Flow Chart													

set_display_on : 29h

29h	set_display_on												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	0	0	1	0	1	0	0	1	29h
Parameter	None												
Description	This command causes the display module to start displaying the image data on the display device. The frame memory contents remain unchanged. No status bits are changed. (Example)  X = Don't care												
Restriction	This command has no effect when the display panel is already on.												
Flow Chart													

set_column_address : 2Ah

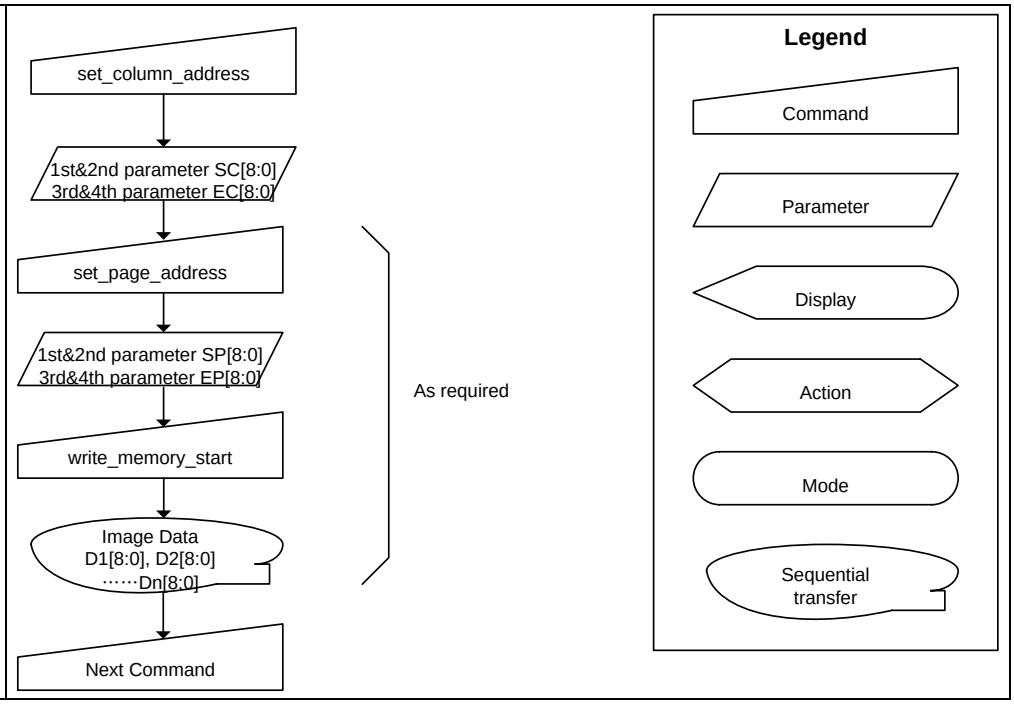
<table>
<tr><td>2Ah</td><td colspan="13">set_column_address</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>DB[17:8]</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td><td>Hex</td></tr>
<tr><td>command</td><td>0</td><td>1</td><td>↑</td><td>X</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>2Ah</td></tr>
<tr><td>1st parameter</td><td>1</td><td>1</td><td>↑</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>SC[8]</td><td rowspan="2">000h
….
1AFh</td></tr>
<tr><td>2nd parameter</td><td>1</td><td>1</td><td>↑</td><td>X</td><td>SC[7]</td><td>SC[6]</td><td>SC[5]</td><td>SC[4]</td><td>SC[3]</td><td>SC[2]</td><td>SC[1]</td><td>SC[0]</td></tr>
<tr><td>3rd parameter</td><td>1</td><td>1</td><td>↑</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>EC[8]</td><td rowspan="2">000h
….
1AFh</td></tr>
<tr><td>4th parameter</td><td>1</td><td>1</td><td>↑</td><td>X</td><td>EC[7]</td><td>EC[6]</td><td>EC[5]</td><td>EC[4]</td><td>EC[3]</td><td>EC[2]</td><td>EC[1]</td><td>EC[0]</td></tr>
<tr><td>Description</td><td colspan="13">This command defines the column extent of the frame memory accessed by the host processor.
The values of SC[8:0] and EC[8:0] are referred when write_memory_start (2Ch) and read_memory_start (2Eh) commands are written. No status bits are changed.

(Example)
 

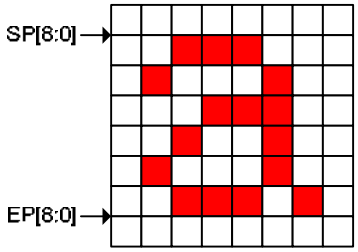
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">SC [8:0] must be equal to or less than EC[8:0]. Set the 1st parameter B5 in set_address_mode (36h) inadvance.

Note: The parameters are disregarded in following cases.
• If set_address_mode B5 = 0: SC[8:0] or EC[8:0] > 0EFh
• If set_address_mode B5 = 1: SC[8:0] or EC[8:0] > 1AFh</td></tr>
</table>

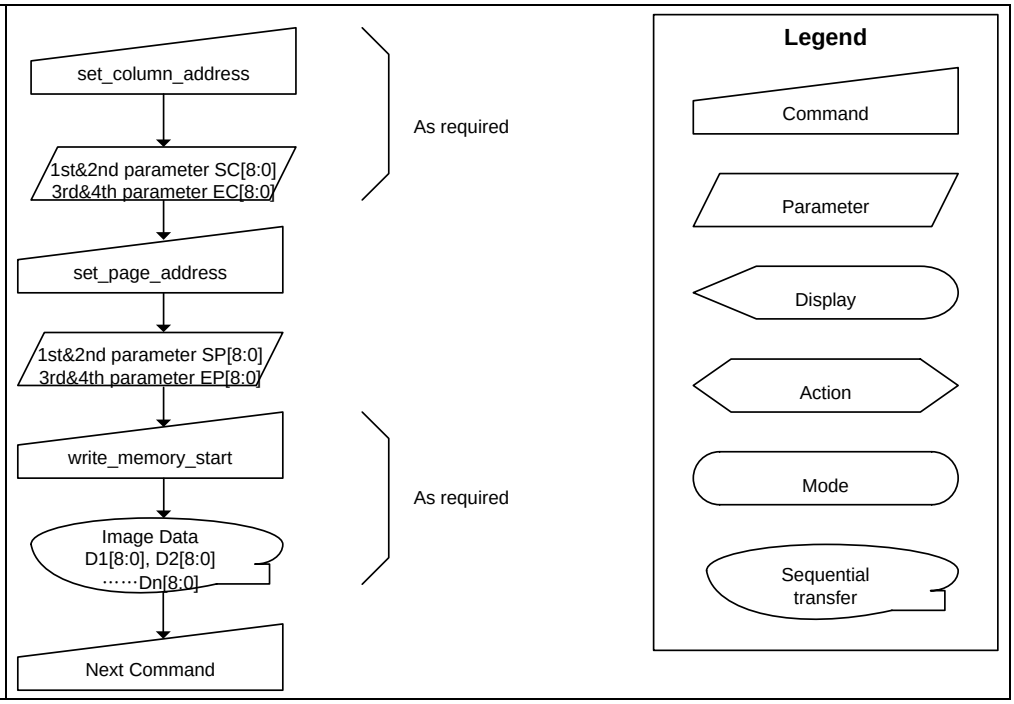
Flow Chart


set_column_address
1st&2nd parameter SC[8:0]
3rd&4th parameter EC[8:0]
set_page_address
1st&2nd parameter SP[8:0]
3rd&4th parameter EP[8:0]
write_memory_start
Image Data
D1[8:0], D2[8:0]
·····Dn[8:0]
Next Command
As required
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

set_page_address : 2Bh

2Bh	set_page_address												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	0	0	1	0	1	0	1	1	2Bh
1st parameter	1	1	↑	X	0	0	0	0	0	0	0	SP[8]	000h …. 1AFh
2nd parameter	1	1	↑	X	SP[7]	SP[6]	SP[5]	SP[4]	SP[3]	SP[2]	SP[1]	SP[0]	
3rd parameter	1	1	↑	X	0	0	0	0	0	0	0	EP[8]	000h …. 1AFh
4th parameter	1	1	↑	X	EP[7]	EP[6]	EP[5]	EP[4]	EP[3]	EP[2]	EP[1]	EP[0]	
Description	This command defines the page extent of the frame memory accessed by the host processor. No status bits are changed. The values of SP[8:0] and EP[8:0] are referred when write_memory_start (2Ch) and read_memory_start (2Eh) commands are written. (Example)  X = Don’t care												
Restriction	SP[8:0] must always be equal to or less than EP[8:0]. Set the 1st parameter B5 in set_address_mode (36h) in advance. Note: The parameters are disregarded in following cases. • If set_address_mode B5 = 0: SP[8:0] or EP[8:0] > 1AFh • If set_address_mode B5 = 1: SP[8:0] or EP[8:0] > 0EFh												

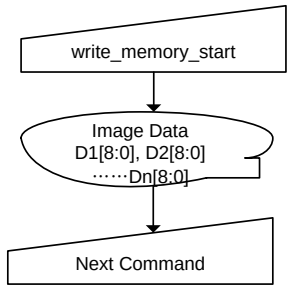
Flow Chart

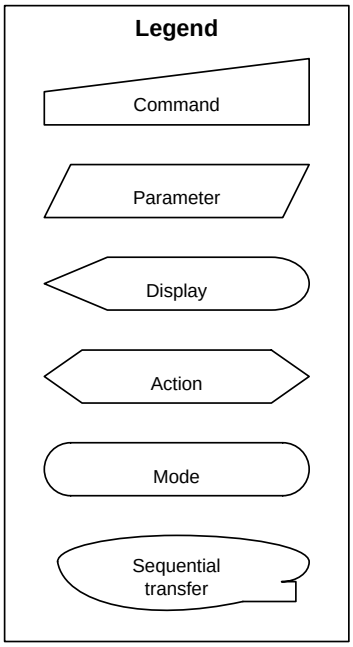

set_column_address
1st&2nd parameter SC[8:0]
3rd&4th parameter EC[8:0]
set_page_address
1st&2nd parameter SP[8:0]
3rd&4th parameter EP[8:0]
write_memory_start
Image Data
D1[8:0], D2[8:0]
……Dn[8:0]
Next Command
As required
As required
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

write_memory_start : 2Ch

2Ch	write_memory_start												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	0	0	1	0	1	1	0	0	2Ch
1st parameter	1	1	↑	D1[17:8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	000h ….. 3FFh
2nd parameter	1	1	↑	D2[17:8]	D2[7]	D2[6]	D2[5]	D2[4]	D2[3]	D2[2]	D2[1]	D2[0]	000h ….. 3FFh
:	1	1	↑	Dx[17:8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	000h ….. 3FFh
nth parameter	1	1	↑	Dn[17:8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	000h ….. 3FFh
Description	This command transfers image data from the host processor to the display module's frame memory. No status bits are changed. If this command is received, the column and page registers are set to the Start Column (SC) and Start Page (SP) respectively. After pixel data 1 is stored in frame memory at (SC, SP), address counter's direction differs depending on Bits 5, 6, 7 of set_address_mode (36h). See "Host Processor to Memory Write/Read Direction". If Frame Memory Access and Interface setting (B3h) WEMOENABLE = 0: If the number of pixels in transfer data exceed (EC-SC+1)*(EP-SP+1), the extra pixels are ignored. If Frame Memory Access and Interface setting (B3h) WEMOENABLE = 1 When the number of pixels in transfer data exceed (EC-SC+1)*(EP-SP+1), the column register and the page register are set to the Start Column and Start Page respectively. Then subsequent data are written to the frame memory. Sending any other command will stop writing to the frame memory. See DBI Data Format and DPI Data Format for write data formats in DBI Type B 18-/16-/9-/8-bit bus interface, Type C serial interface, and DPI. X=Don't care.												
Restriction	In all color modes, there are no restrictions on the length of parameters.												

Flow Chart

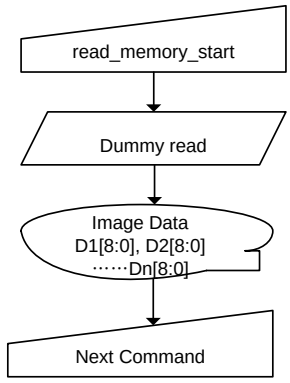

write_memory_start
Image Data
D1[8:0], D2[8:0]
……Dn[8:0]
Next Command

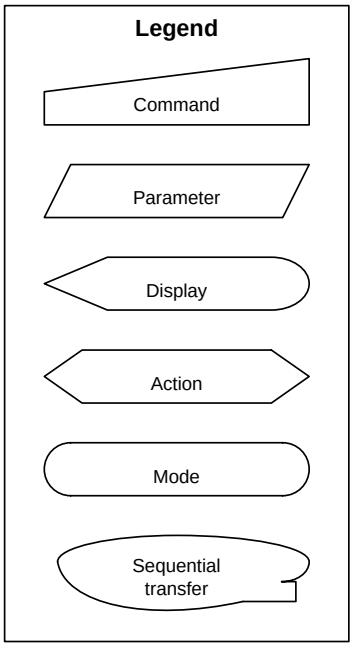

Legend
Command
Parameter
Display
Action
Mode
Sequential
transfer

read_memory_start : 2Eh

2Eh	read_memory_start												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	0	0	1	0	1	1	1	0	2Eh
1st parameter	1	↑	1	D1[17:8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	000h ….. 3FFh
2nd parameter	1	↑	1	D2[17:8]	D2[7]	D2[6]	D2[5]	D2[4]	D2[3]	D2[2]	D2[1]	D2[0]	000h ….. 3FFh
:	1	↑	1	Dx[17:8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	000h ….. 3FFh
nth parameter	1	↑	1	Dn[17:8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	000h ….. 3FFh
Description	This command transfers image data from the frame memory to the host processor. No status bits are changed. If this command is received, the column and page registers are set to the Start Column (SC) and Start Page (SP) respectively. After pixel data I are read from the frame memory at (SC, SP), address counter's direction differs depending on Bits 5, 6, 7 of set_address_mode (36h). See "Host Processor to Memory Write/Read Direction". If read operation continued after (EP, EC) data are read, the last data (EP, EC) continue to be read. Any other written command stops frame memory read. See DBI Data Format for read data formats in DBI Type B 18-/16-/ 9-/8-bit bus interface and Type C serial interface operations. X = Don't care.												
Restriction	In all color modes, the Frame read is always 24 bits so there is no restriction on the length of parameters.												

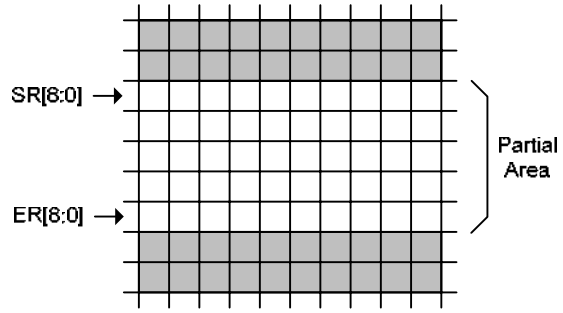
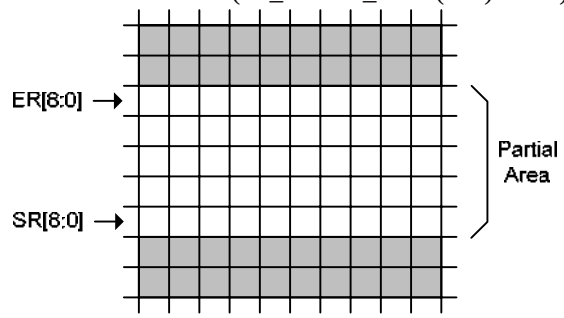
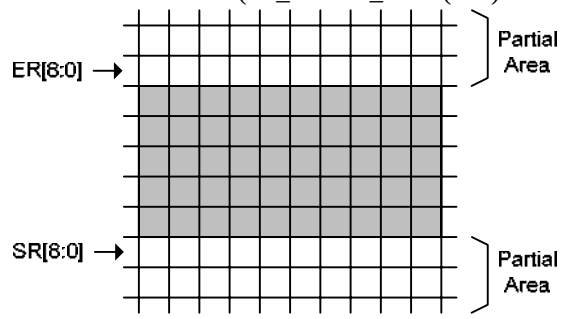
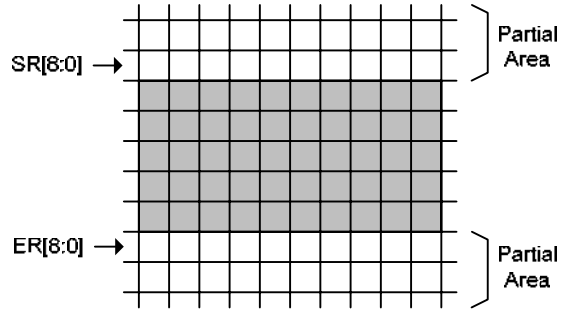
Flow Chart

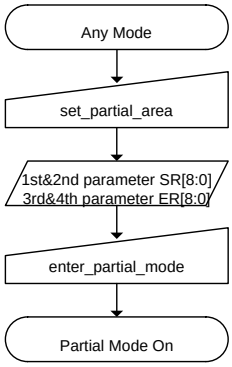
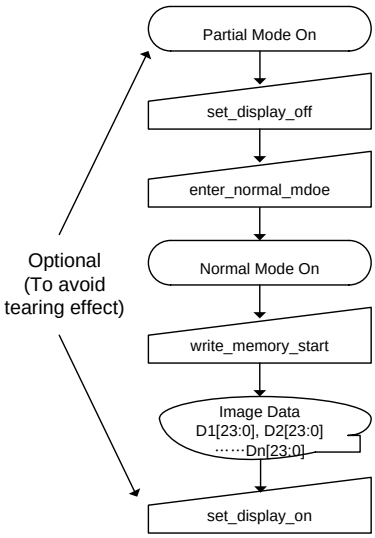
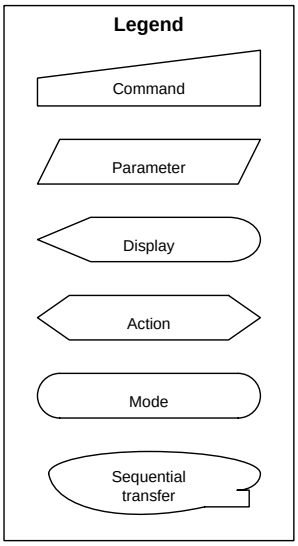

read_memory_start
Dummy read
Image Data
D1[8:0], D2[8:0]
……Dn[8:0]
Next Command


Legend
Command
Parameter
Display
Action
Mode
Sequential
transfer

set_partial_area : 30h

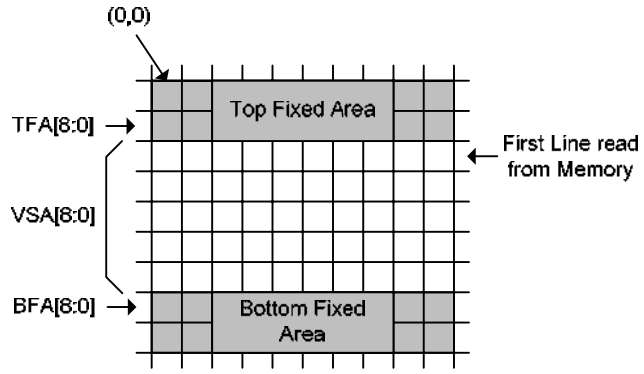
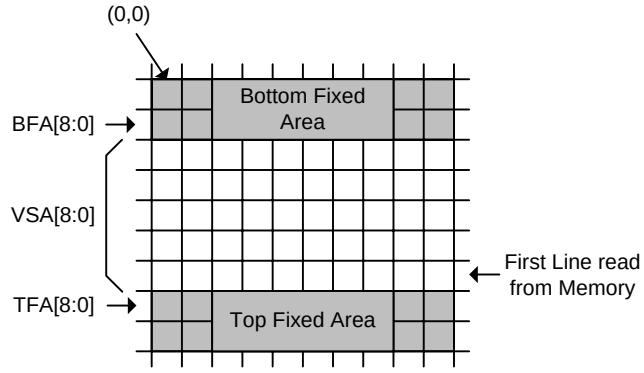
30h	set_partial_area												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	0	0	1	1	0	0	0	0	30h
1st parameter	1	1	↑	X	0	0	0	0	0	0	0	SR[8]	000h …. 1AFh
2nd parameter	1	1	↑	X	SR[7]	SR[6]	SR[5]	SR[4]	SR[3]	SR[2]	SR[1]	SR[0]	
3rd parameter	1	1	↑	X	0	0	0	0	0	0	0	ER[8]	000h …. 1AFh
4th parameter	1	1	↑	X	ER[7]	ER[6]	ER[5]	ER[4]	ER[3]	ER[2]	ER[1]	ER[0]	

Description	This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer. End Row > Start Row (set_address_mode(36h) B4=0)  End Row > Start Row(set_address_mode(36h) B4=1)  End Row < Start Row (set_address_mode(36h) B4=0)  End Row < Start Row (set_address_mode(36h) B4=1)  If End Row = Start Row, the partial area will be one row deep. X = Don't care

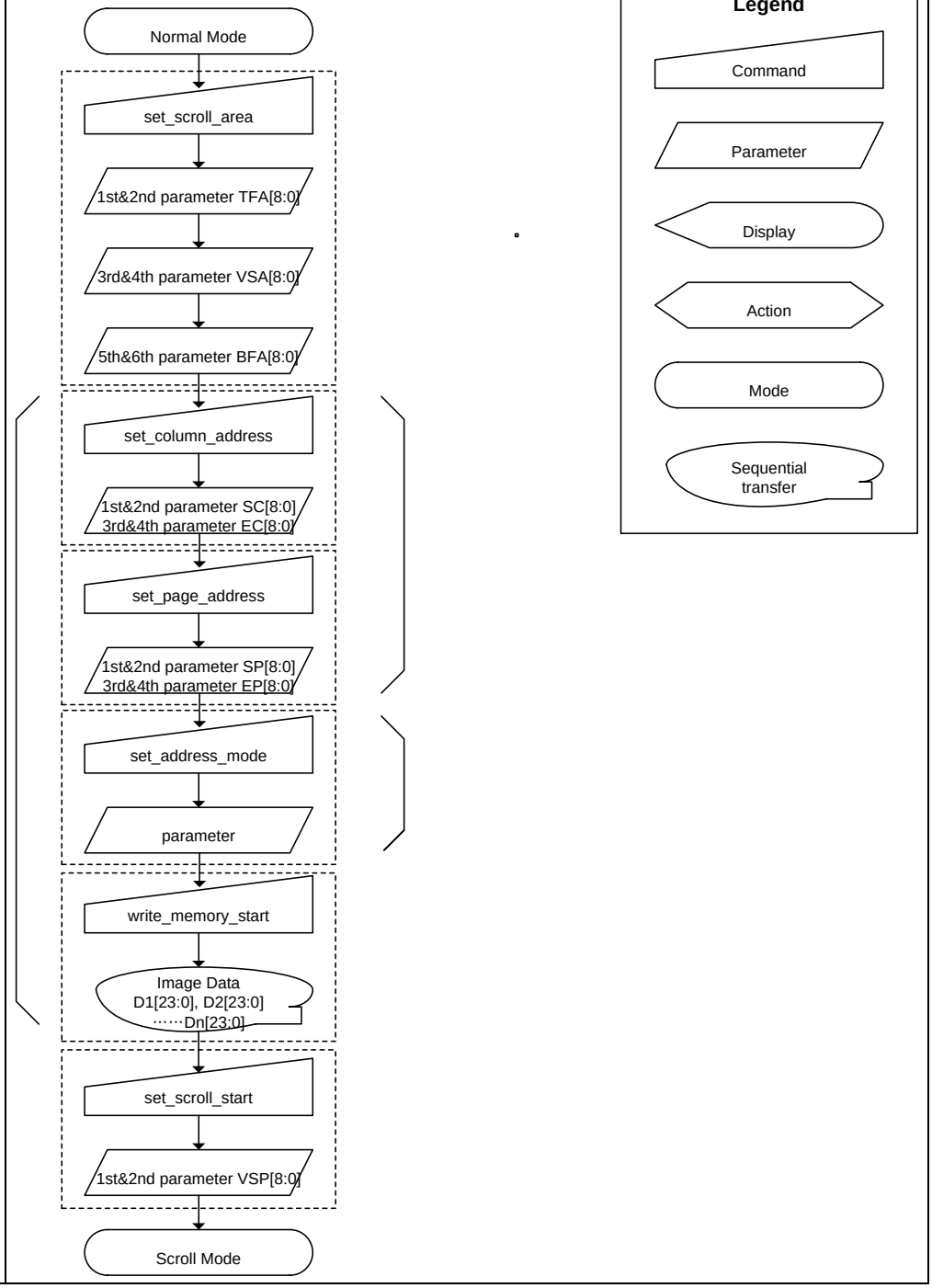
Restriction	SR[8:0] and ER[8:0] must not be greater than 1AFh. The bits other than SR[8:0] and ER[8:0] are “Don’t care”.
Flow Chart	1. To enter Partial mode  2. To exit Partial mode  Enter Normal Mode turns Partial Mode off 

set_scroll_area : 33h

33h	set_scroll_area												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	0	0	1	1	0	0	1	1	33h
1st parameter	1	1	↑	X	0	0	0	0	0	0	0	TFA [8]	000h …. 1AFh
2nd parameter	1	1	↑	X	TFA [7]	TFA [6]	TFA [5]	TFA [4]	TFA [3]	TFA [2]	TFA [1]	TFA [0]	
3rd parameter	1	1	↑	X	0	0	0	0	0	0	0	VSA [8]	000h …. 1AFh
4th parameter	1	1	↑	X	VSA [7]	VSA [6]	VSA [5]	VSA [4]	VSA [3]	VSA [2]	VSA [1]	VSA [0]	
5th parameter	1	1	↑	X	0	0	0	0	0	0	0	BFA [8]	000h …. 1AFh
6th parameter	1	1	↑	X	BFA [7]	BFA [6]	BFA [5]	BFA [4]	BFA [3]	BFA [2]	BFA [1]	BFA [0]	

Description	This command defines the display module's Vertical Scrolling Area. The 1st & 2nd parameter, TFA[8:0], describes the Top Fixed Area in number of lines from the top of the frame memory. The top of the frame memory and top of the display device are aligned. The 3rd & 4th parameter, VSA[8:0], describes the height of the Vertical Scrolling Area in number of lines of frame memory from the Vertical Scrolling Start Address. The first line of the Vertical Scrolling Area starts immediately after the bottom most line of the Top Fixed Area. The last line of the Vertical Scrolling Area ends immediately before the top most line of the Bottom Fixed Area. The 5th & 6th parameter, BFA[8:0], describes the Bottom Fixed Area in number of lines from the bottom of the frame memory. The bottom of the frame memory and bottom of the display device are aligned. TFA, VSA and BFA refer to the Frame Memory Line Pointer. If set_address_mode B4 = 0:  If set_address_mode B4 = 1:  X = Don't care
Restriction	The sum of TFA, VSA and BFA must equal the number of the display device's horizontal lines (pages), otherwise Scrolling mode is undefined. In Vertical Scroll Mode, set_address_mode B5 should be set to '0' – this only affects the Frame Memory Write.

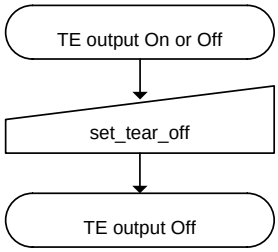
Flow Chart

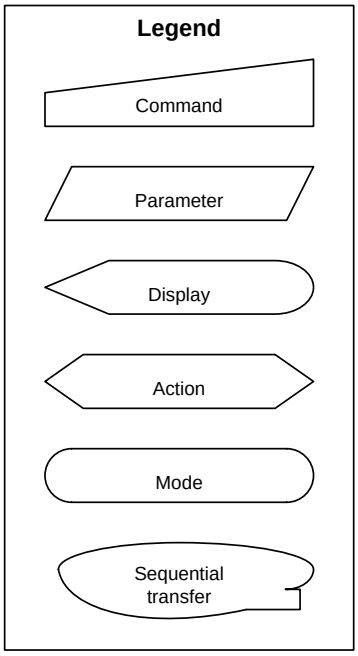

Normal Mode
set_scroll_area
1st&2nd parameter TFA[8:0]
3rd&4th parameter VSA[8:0]
5th&6th parameter BFA[8:0]
set_column_address
1st&2nd parameter SC[8:0]
3rd&4th parameter EC[8:0]
set_page_address
1st&2nd parameter SP[8:0]
3rd&4th parameter EP[8:0]
set_address_mode
parameter
write_memory_start
Image Data
D1[23:0], D2[23:0]
·····Dn[23:0]
set_scroll_start
1st&2nd parameter VSP[8:0]
Scroll Mode
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

set_tear_off : 34h

34h	set_tear_off												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	0	0	1	1	0	1	0	0	34h
Parameter	None												
Description	This command turns off the Tearing Effect output signal from the TE signal line. X = Don't care												
Restriction	This command has no effect when Tearing Effect output is already off.												

Flow Chart





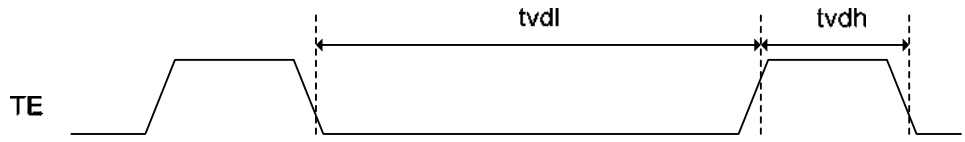
set_tear_on : 35h

35h	set_tear_on												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	0	0	1	1	0	1	0	1	35h
Parameter	1	↑	1	X	X	X	X	X	X	X	X	TEM	xxh

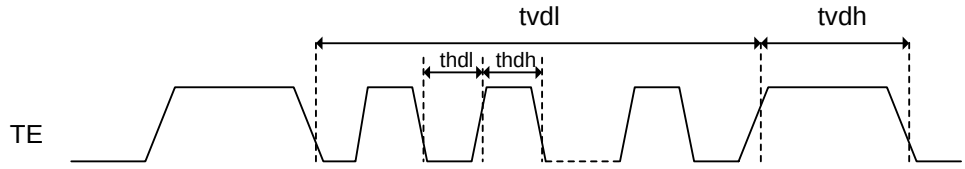
Description

This command turns on the display module's Tearing Effect output signal on the TE signal line.
The TE signal is not affected by changing set_address_mode (36h) bit B4 (Line Refresh order).
The Tearing Effect Line On has one parameter, TELON, that describes the Tearing Effect Output Line mode.
See TE Pin Output Signal" for detail.

TEM = 0: The Tearing Effect Output line consists of V-Blanking information only.
The Tearing Effect Output line shall be high during vertical blanking period.



TEM = 1: The Tearing Effect Output line consists of both V-blanking and H-blanking information.



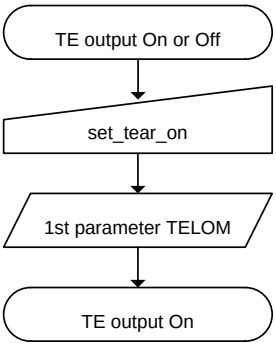
Vertical blanking period: Non-lit display period in (back porch + front porch)
Note: The Tearing Effect Output line shall be active low when the display module is in Sleep mode.

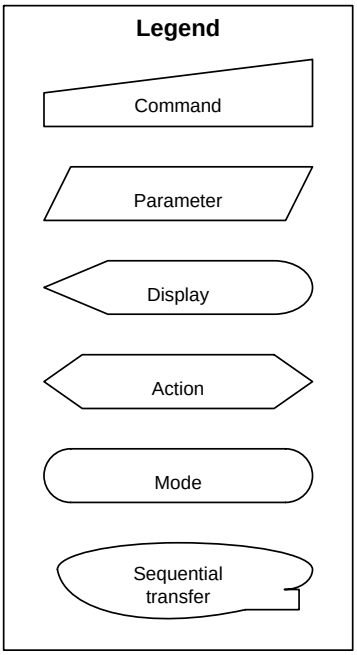
X = Don't care

Restriction

This command has no effect when Tearing Effect output is already ON. Changes in parameter TEM is ENABLEd from the next frame period.

Flow Chart


TE output On or Off
set_tear_on
1st parameter TELOM
TE output On


Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

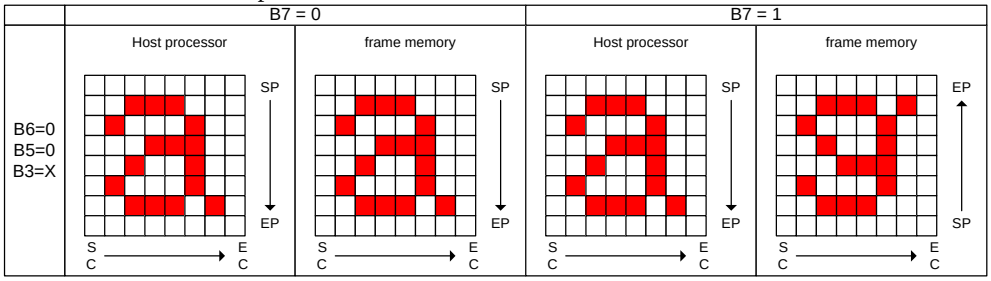
set_address_mode : 36h

36h	set_address_mode												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	0	0	1	1	0	1	1	0	36h
Parameter	1	1	↑	X	B7	B6	B5	B4	B3	B2	B1	B0	xxh

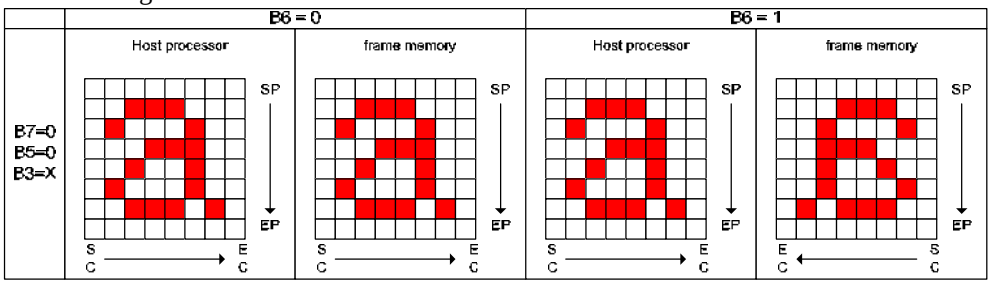
Description The display module returns the current power mode.

Bit	Description	Comment	Command list Symbol
D7	Page Address Order		B7
D6	Column Address Order		B6
D5	Page/Column Order		B5
D4	Line Address Order		B4
D3	RGB/BGR Order		B3
D2	Display Data Latch Order		B2
D1	Flip Horizontal		B1
D0	Flip Vertical		B0

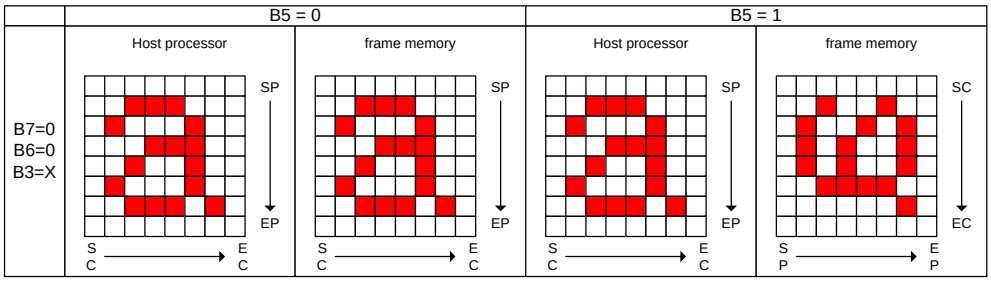
- Bit B7 – Page Address Order
  ‘0’ = Top to Bottom
  ‘1’ = Bottom to Top



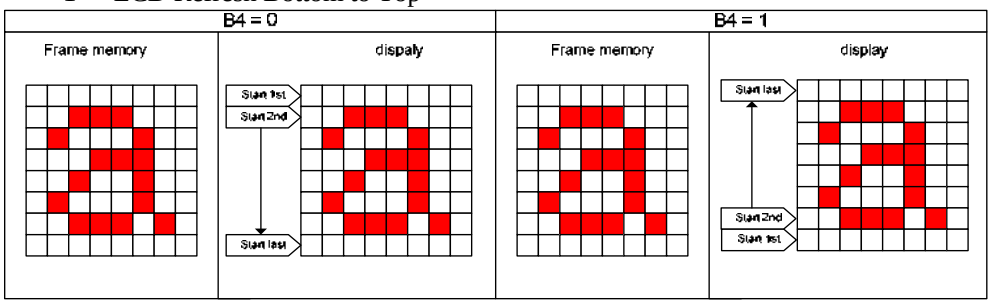
- Bit B6 – Column Address Order
  ‘0’ = Left ro Right
  ‘1’ = Right to Left



- Bit B5 – Page/Column Order
  ‘0’ = Normal Mode
  ‘1’ = Reverse Mode



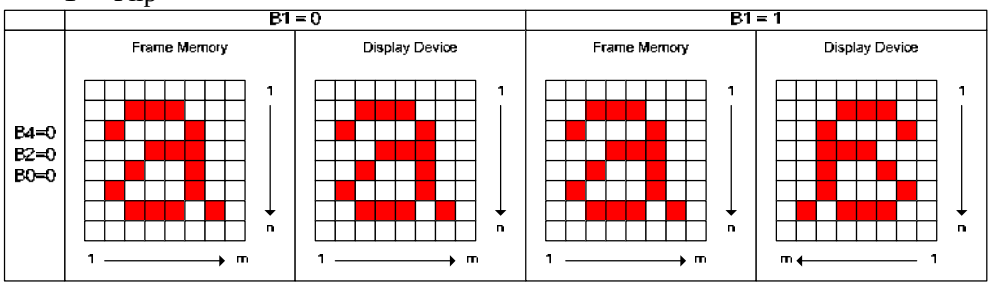
- Bit B4 – Line Address Order
  ‘0’ = LCD Refresh Top to Bottom
  ‘1’ = LCD Refresh Bottom to Top



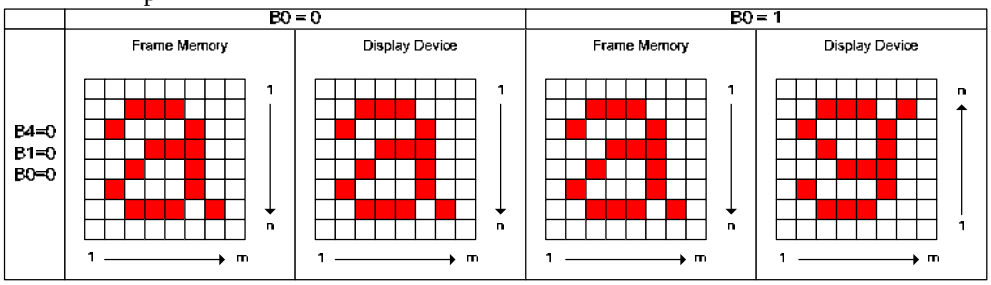
- Bit B3 – RGB/BGR Order
  ‘0’ = Pixel in RGB order
  ‘1’ = Pixel in BGR order

- Bit B2 – Display Data Latch Data Order
  ‘0’ = LCD Refresh Left to Right
  ‘1’ = LCD Refresh Right to Left

- Bit B1 – Flip Horizontal
  ‘0’ = Normal
  ‘1’ = Flip



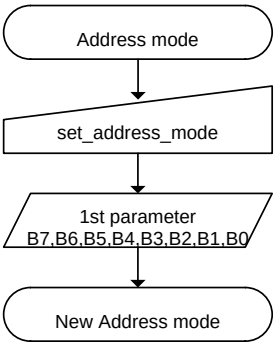
- Bit B0 – Flip Vertcal
  ‘0’ = Normal
  ‘1’ = Flip

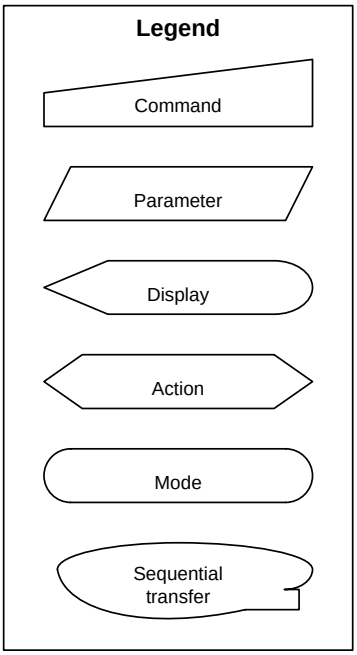


X = Don’t care

Restriction -

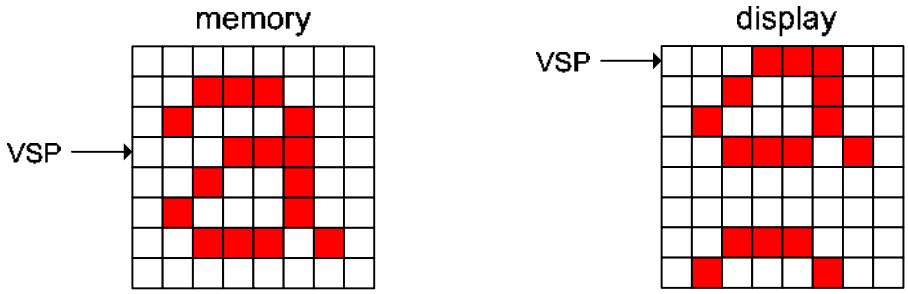
Flow Chart

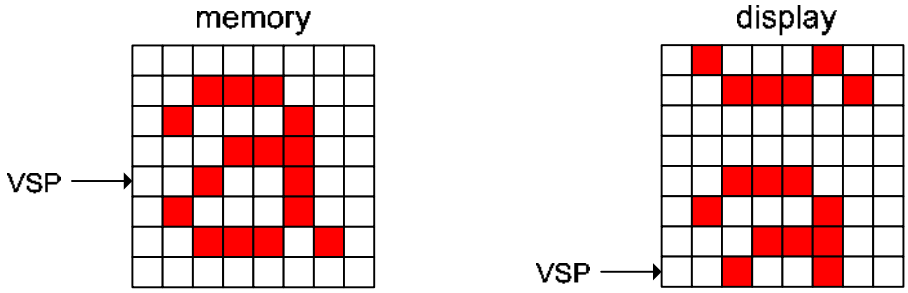

Address mode
set_address_mode
1st parameter
B7,B6,B5,B4,B3,B2,B1,B0
New Address mode


Legend
Command
Parameter
Display
Action
Mode
Sequential
transfer

set_scroll_start : 37h

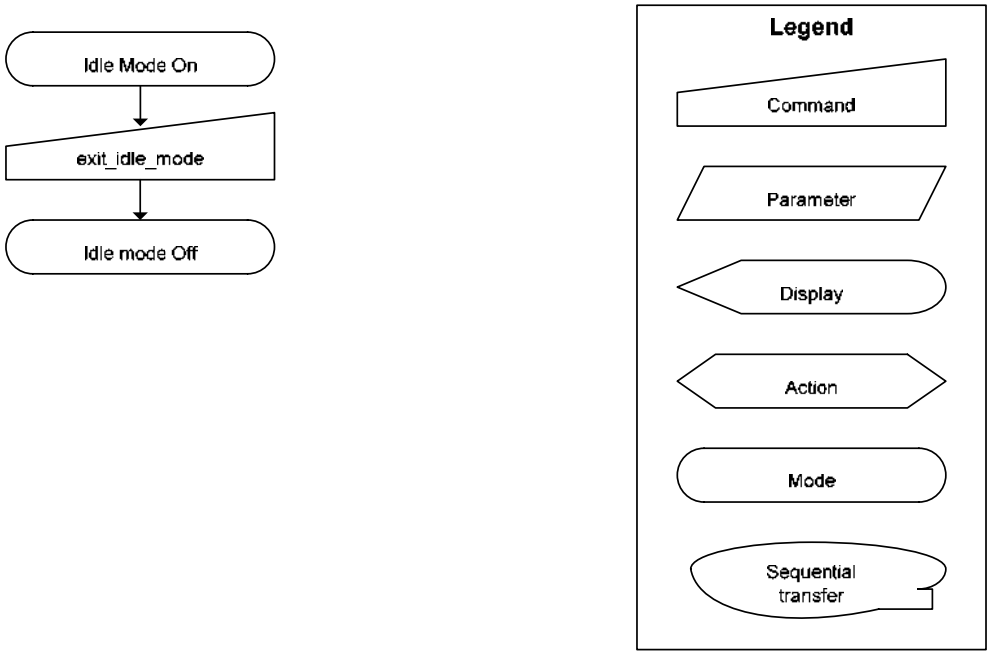
<table>
<tr><td>37h</td><td colspan="13">set_scroll_start</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>DB[17:8]</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td><td>Hex</td></tr>
<tr><td>command</td><td>0</td><td>1</td><td>↑</td><td>X</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>37h</td></tr>
<tr><td>1st parameter</td><td>1</td><td>1</td><td>↑</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>VSP[8]</td><td rowspan="2">000h
….
1AFh</td></tr>
<tr><td>2nd parameter</td><td>1</td><td>1</td><td>↑</td><td>X</td><td>VSP[7]</td><td>VSP[6]</td><td>VSP[5]</td><td>VSP[4]</td><td>VSP[3]</td><td>VSP[2]</td><td>VSP[1]</td><td>VSP[0]</td></tr>
<tr><td>Description</td><td colspan="13">This command sets the start of the vertical scrolling area in the frame memory. The vertical scrolling area is fully defined when this command is used with the set_scroll_area command

set_address_mode B4 = 0
 

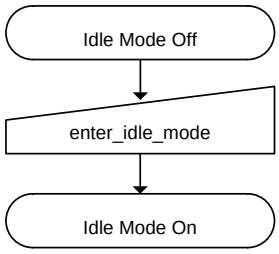
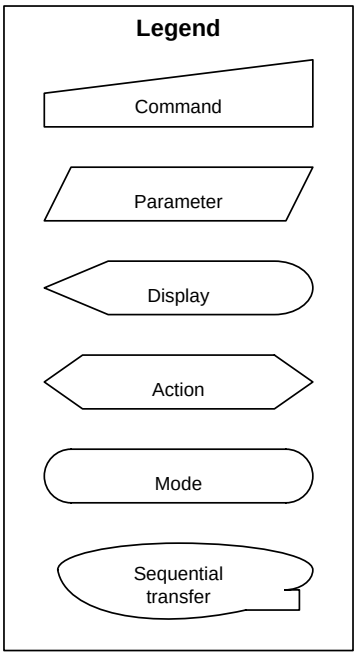
set_address_mode B4 = 1
 

X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">If set_address_mode B4 = 0, TFA[8:0] - 1< VSP[8:0] < 1AFh - BFA[8:0].
If set_address_mode B4 = 1, BFA[8:0] - 1 < VSP[8:0] < 1AFh - TFA[8:0].</td></tr>
<tr><td>Flow Chart</td><td colspan="13">See set_scroll_area (33h)</td></tr>
</table>

exit_idle_mode : 38h

38h	exit_idle_mode												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	0	0	1	1	1	0	0	0	38h
Parameter	None												
Description	This command causes the display module to exit Idle mode. LCD can display up to maximum 262,144 colors. If the operation of the LG4538 is in synchronization with internal oscillation clock (DM=0), the frame rate and liquid crystal alternating cycle can be adjusted for every display mode (Normal, Partial, Idle (Normal/Partial) modes X = Don't care												
Restriction	This command has no effect when the display module is not in Idle mode.												
Flow Chart													

enter_idle_mode : 39h

39h	enter_idle_mode												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	0	0	1	1	1	0	0	1	39h
Parameter	None												
Description	This command causes the display module to enter Idle mode. In Idle mode, color expression is reduced. Eight color depth data are displayed using MSB of each R, G and B color components in the Frame Memory. In this mode, only grayscale levels V0 and V63 are used and power supply for other levels V1-V62 are halted, reducing power consumption. If the operation of the LG4538 is in synchronization with internal oscillation clock (DM=0), the frame rate and liquid crystal alternating cycle can be adjusted for every display mode (Normal, Partial, Idle (Normal/Partial) modes). X = Don't care												
Restriction	This command has no effect when module is already in Idle mode.												
Flow Chart	 												

set_pixel_format : 3Ah

3Ah	set_pixel_format												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	0	0	1	1	1	0	1	0	3Ah
Parameter	1	↑	1	X	0	D6	D5	D4	0	D2	D1	D0	xxh

Description

This command is used to define the format of RGB picture data, which are to be transferred via the DBI/DPI.

The formats are shown in the following table:
Bit D[6:4] – DPI Pixel Format (RGB Interface Color Format Selection)
Bit D[2:0] – DBI Pixel Format (Control Interface Color Format Selection)
Bit D7 and D3 – These bits are not used. Set to “0” is read.

Control Interface Color Format	D6/D2	D5/D1	D4/D0
Setting disabled	0	0	0
Setting disabled	0	0	1
Setting disabled	0	1	0
Setting disabled	0	1	1
Setting disabled	1	0	0
16bit/pixel (65,536 colors)	1	0	1
18bit/pixel (262,144 colors)	1	1	0
Setting disabled	1	1	1

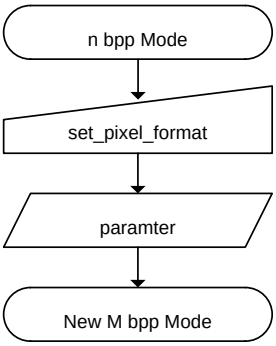
See “DBI Data Format” and “DPI Data Format” “Data Format List” for each type of interfaces.

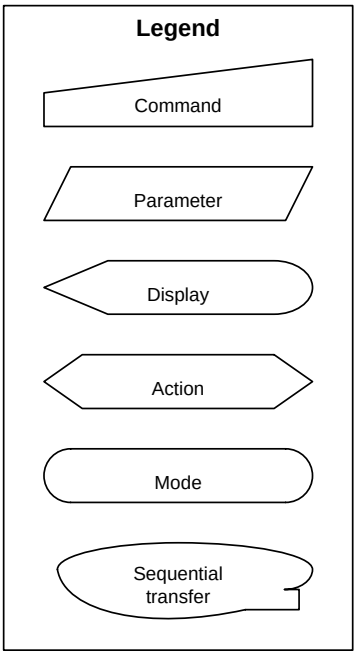
Note 1: When the setting disabled bits are set, undesirable image will be displayed on the panel.
Note 2: When DBI Type B is selected, set D[2:0]=5 (16bit/pixel) or 6 (18 bit/pixel). Other settings are disabled.
Note 3: When DBI Type C serial interface operation is selected, set D[2:0] = 5 (16bit/pixel) or 6 (18bit/pixel). Other settings are disabled.

X = Don’t care

Restriction -

Flow Chart

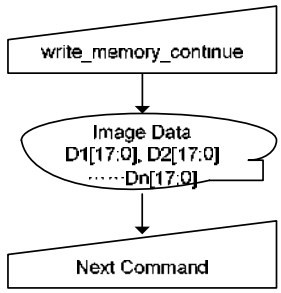

n bpp Mode
set_pixel_format
paramter
New M bpp Mode

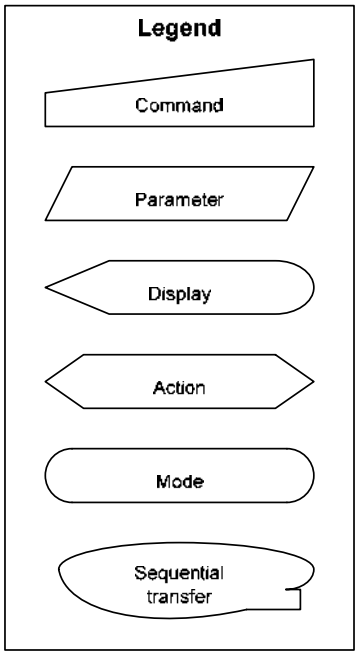

Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

write_memory_continue : 3Ch

3Ch	write_memory_continue												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	0	0	1	1	1	1	0	0	3Ch
1st parameter	1	1	↑	D1[17:8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	000h ….. 3FFh
2nd parameter	1	1	↑	D2[17:8]	D2[7]	D2[6]	D2[5]	D2[4]	D2[3]	D2[2]	D2[1]	D2[0]	000h ….. 3FFh
:	1	1	↑	Dx[17:8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	000h ….. 3FFh
nth parameter	1	1	↑	Dn[17:8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	000h ….. 3FFh
Description	This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command. Frame Memory Access and Interface setting (B3h): WEMODE = 0 If the number of pixels in the transfer data exceed (EC-SC+1)*(EP-SP+1), the extra pixels are ignored. Frame Memory Access and Interface setting (B3h): WEMODE = 1 When the number of pixels in the transfer data exceed (EC-SC+1)*(EP-SP+1), the column register and the page register are reset to the Start Column/Start Page positions, and the subsequent data are written to the frame memory. X=Don't care.												
Restriction	If write_memory_continue command is executed without setting set_column_address (2Ah), set_page_address (2Bh), and set_address_mode (36h), there is no guarantee that data are correctly written to the frame memory.												

Flow Chart

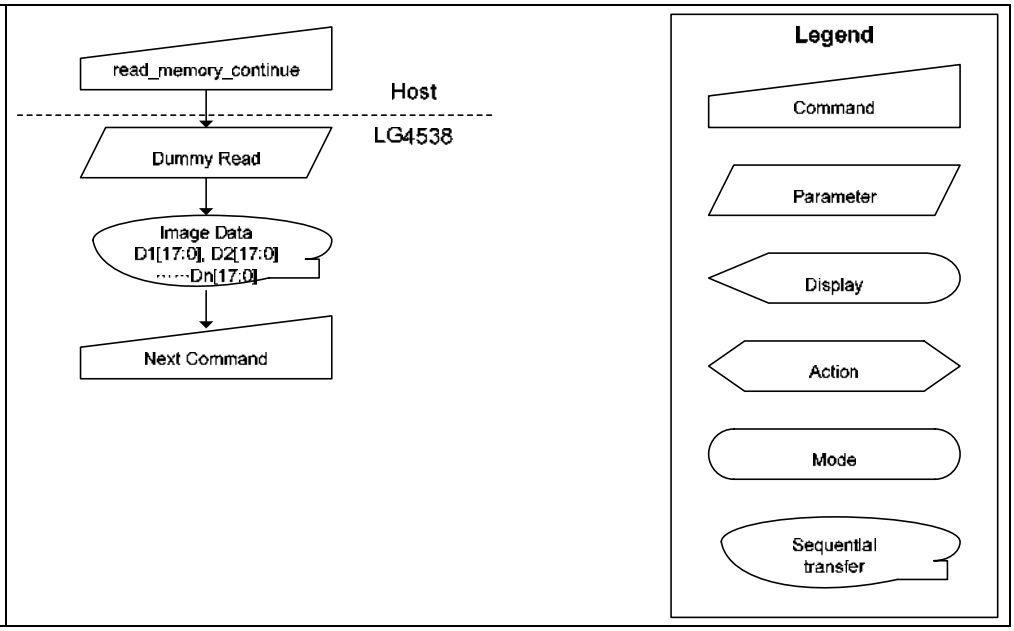

write_memory_continue
Image Data
D1[17:0], D2[17:0]
……Dn[17:0]
Next Command


Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

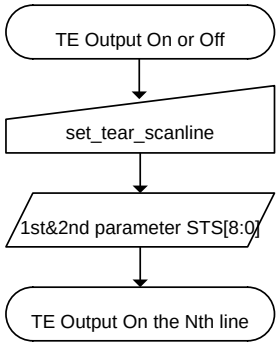
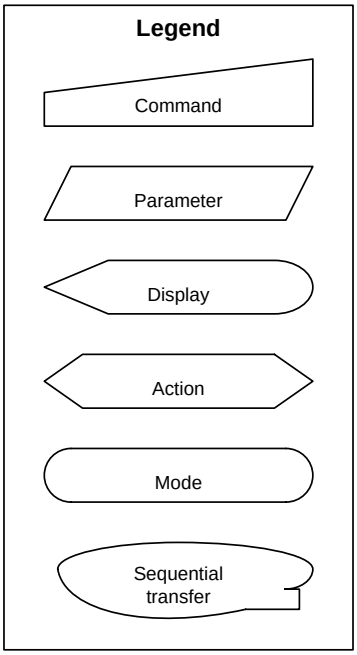
read_memory_continue : 3Eh

3Eh	read_memory_continue												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	0	0	1	1	1	1	1	0	3Eh
1st parameter	1	↑	1	D1[17:8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	000h ….. 3FFh
2nd parameter	1	↑	1	D2[17:8]	D2[7]	D2[6]	D2[5]	D2[4]	D2[3]	D2[2]	D2[1]	D2[0]	000h ….. 3FFh
:	1	↑	1	Dx[17:8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	000h ….. 3FFh
nth parameter	1	↑	1	Dn[17:8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	000h ….. 3FFh
Description	This command transfers image data from the display module's frame memory to the host processor continuing from the location following the previous read_memory_continue or read_memory_start command. If read operation is executed after (EP. EC) is read, the last data (EP, EC) continue to output. After pixel data 1 are written to frame memory (SC, SP), address counter's direction differs depending on setting of set_address_mode (36h)'s Bits 5, 6, 7. See "Host Processor to Memory Write/Read Direction". X = Don't care												
Restriction	-												

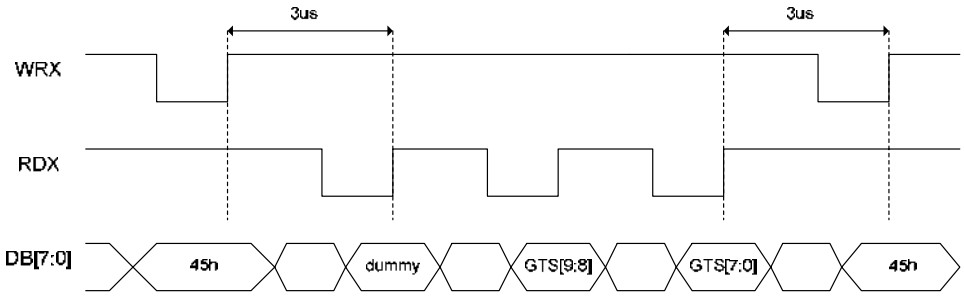
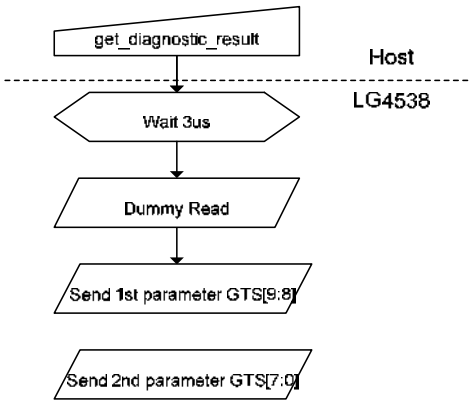
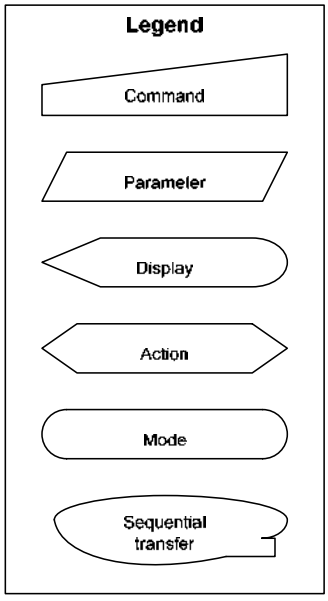
Flow Chart


read_memory_continue
Host
LG4538
Dummy Read
Image Data
D1[17:0], D2[17:0]
……Dn[17:0]
Next Command
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

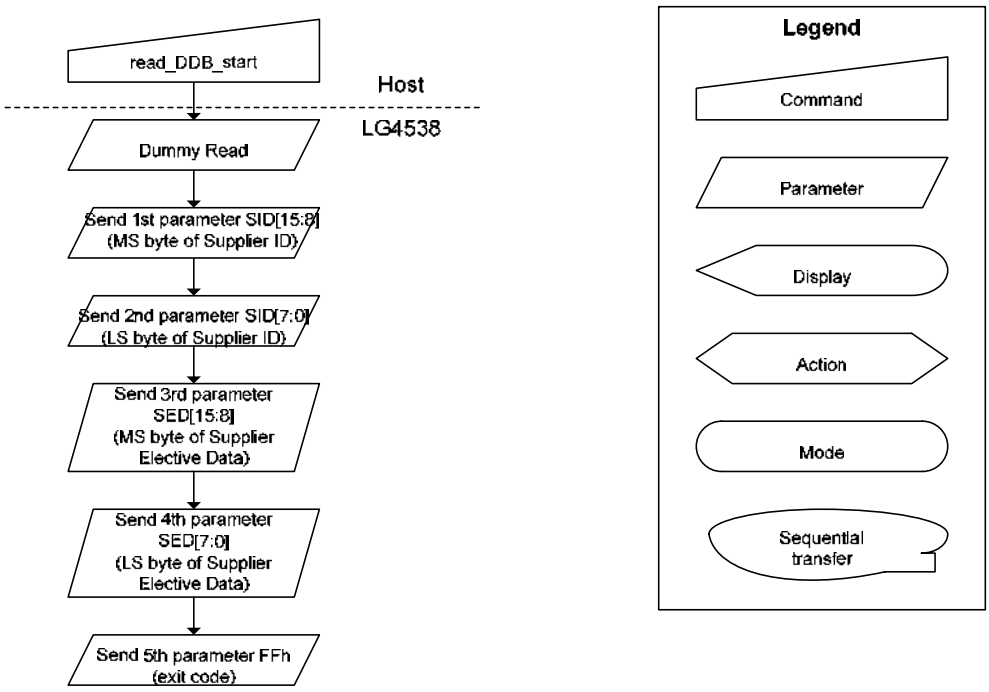
set_tear_scanline : 44h

44h	set_tear_scanline												
	DCX	RDX	WR X	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	0	1	0	0	0	1	0	0	44h
1st parameter	1	1	↑	X	0	0	0	0	0	0	0	TEL [8]	Xxh
2nd parameter	1	1	↑	X	TEL [7]	TEL [6]	TEL [5]	TEL [4]	TEL [3]	TEL [2]	TEL [1]	TEL [0]	Xxh
Description	This command turns on the display module's Tearing Effect output signal on the TE signal line when the display module reaches line N defined by TEL [8:0]. TE line is unaffected by change in B4 bit of set_address_mode command. See figure in "TE Pin Output Signal". X = Don't care												
Restriction	The command takes affect on the frame following the current frame. Therefore, if the TE signal is already ON, TE signal is output according to the old set_tear_on and set_tear_scanline commands until the end of currently scanned frame. Setting is disabled when TEM=1 of set_tear_on (35h). Make sure that TEL [8:0] ≤ NL (number of line) + 1.												
Flow Chart	 												

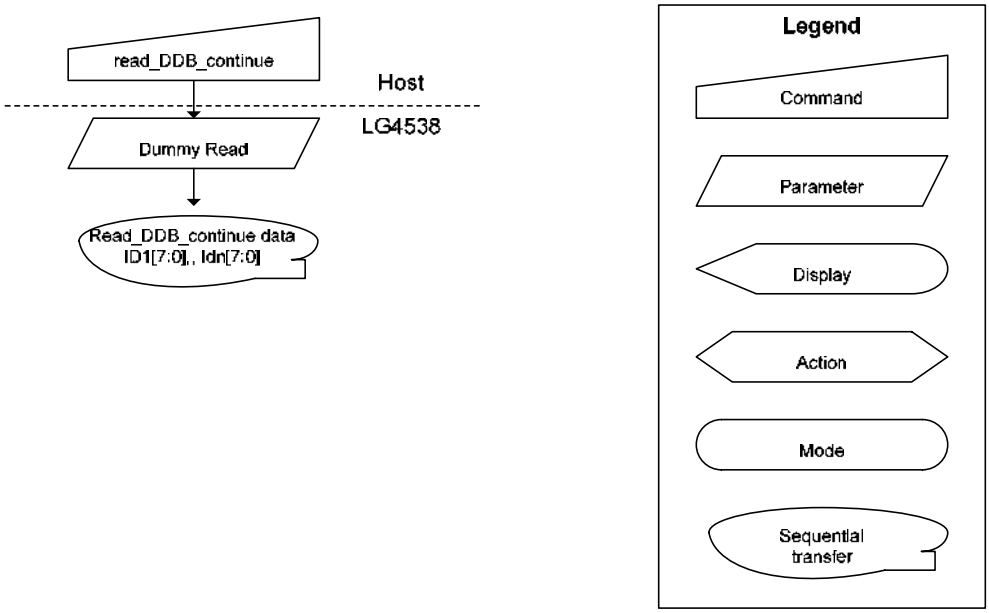
get_scanline : 45h

45h	set_tear_scanline												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	0	1	0	0	0	1	0	1	45h
1st parameter	1	↑	1	X	0	0	0	0	0	0	GTS [9]	GTS [8]	Xxh
2nd parameter	1	↑	1	X	GTS [7]	GTS [6]	GTS [5]	GTS [4]	GTS [3]	GTS [2]	GTS [1]	GTS [0]	Xxh
Description	The display module returns the current scan line. The total number of scan lines is defined as (BP + NL + FP). The first scan line of back portch period is defined as line 0. In sleep mode, the value returned by get_scanline is undefined. X = Don't care												
Restriction	After get_scanline command is input, it takes 3us or more to read it. After parameters are read, wait 3 us or more to reinput this command. 												
Flow Chart	 												

read_DDB_start : A1h

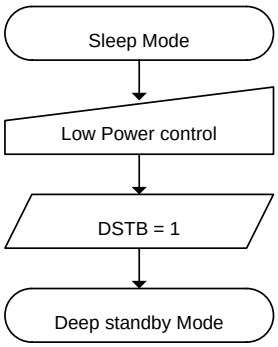
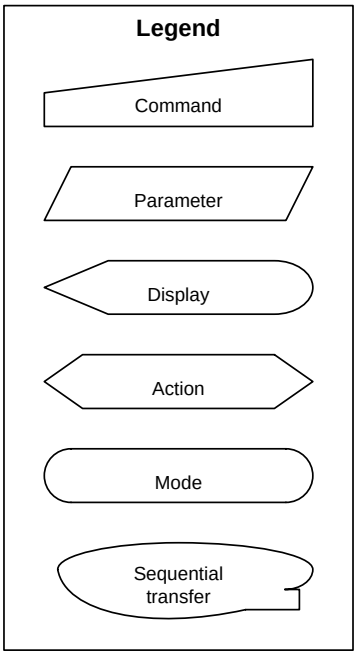
A1h	read_DDB_start												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	1	0	1	0	0	0	0	1	A1h
1st parameter	1	↑	1	X	SID [15]	SID [14]	SID [13]	SID [12]	SID [11]	SID [10]	SID [9]	SID [8]	Xxh
2nd parameter	1	↑	1	X	SID [7]	SID [6]	SID [5]	SID [4]	SID [3]	SID [2]	SID [1]	SID [0]	Xxh
3rd parameter	1	↑	1	X	SED [15]	SED [14]	SED [13]	SED [12]	SED [11]	SED [10]	SED [9]	SED [8]	XXh
4th parameter	1	↑	1	X	SED [7]	SED [6]	SED [5]	SED [4]	SED [3]	SED [2]	SED [1]	SED [0]	XXh
5th parameter	1	↑	1	X	1	1	1	1	1	1	1	1	XXh
Description	The command returns information from the display module as follows: 1st parameter& 2nd parameter : Supplier ID 3rd parameter & 4th parameter: Supplier Elective Data 5th parameter: Exit Code (FFh) Supplier ID = 16'h012A Supplier Elective Data = 16'h4538 X = Don't care												
Restriction	-												
Flow Chart													

read_DDB_continue : A8h

A8h	read_DDB_continue												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	1	0	1	0	1	0	0	0	A8h
1st parameter	1	↑	1	X	ID1 [7]	ID1 [6]	ID1 [5]	ID1 [4]	ID1 [3]	ID1 [2]	ID1 [1]	ID1 [0]	XXh
:	1	↑	1	X	IDx [7]	Idx [6]	Idx [5]	Idx [4]	Idx [3]	Idx [2]	Idx [1]	Idx [0]	XXh
nth parameter	1	↑	1	X	Idn [7]	Idn [6]	Idn [5]	Idn [4]	Idn [3]	Idn [2]	Idn [1]	Idn [0]	XXh
Description	This Command returns Supplier's ID and Supplier Elective Data from the point where read_DDB_start command was interrupt by an other command. e.g. read_DDB_start was interrupted after 3rd parameter . The first parameter (ID1[7:0]), what read_DDB_continue is returing, is SED[7:0] X = Don't care												
Restriction	-												
Flow Chart													

Manufacturer Command

Low Power Setting (B1h)

B1h	Low Power Setting												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	1	0	1	1	0	0	0	1	B0h
1st parameter	1	#A	#B	X	0	0	0	OSC EN	0	0	0	DSTB	XXh
Description	Write #A="1" #B="↑" Read #A="↑" #B=" 1" & Insert dummy read **DSTB :** The driver enters the Deep Standby Mode when DSTB=1. Internal logic power supply circuit (VDD) is turned down enabling low power consumption. In the Deep Standby mode, data stored in the Frame Memory and the Instructions are not retained. Rewrite them after the Deep Standby mode is exited. See Deep Standby Mode IN/EXIT Sequence in "State and Command Sequence". OSCEN : Oscillator operation control													
	OSCEN	**Oscillator In sleep mode**											
	0	Stop											
	1	Operation											
Restriction	-												
Flow Chart	 												

DPI contol : (B2h)

B2h	DPI Control												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	1	0	1	1	0	0	1	0	B2h
1st parameter	1	#A	#B	X	0	0	0	0	CKPL	HSPL	VSPL	ENPL	XXh
Description	Write #A="1" #B="↑" Read #A="↑" #B=" 1" & Insert dummy read **CKPL :** DOTCLK polarity 0 : Rising edge 1 : Falling edge **HSPL** : HSYNC polarity 0 : Active Low 1 : Active High **VSPL** : VSYNC polarity 0 : Active Low 1: Active High **ENPL** : ENABLE polarity 0 : Active Low 1 : Active High See "Display Pixel Interface" for details in setting the bits.												
Restriction	-												

Frame Memory Access and Interface setting : (B3h)

B3h	Frame Memory Access and Interface setting												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	1	0	1	1	0	0	1	1	B3h
1st parameter	1	#A	#B	X	DFM [1]	DFM [0]	EPF [1]	EPF [0]	0	0	0	WEMODE	XXh
2nd parameter	1	#A	#B	X	0	0	0	0	0	TEI[2]	TEI[1]	TEI[0]	XXh
3rd parameter	1	#A	#B	X	0	0	0	0	0	DENC [2]	DENC [1]	DENC [0]	XXh

Description

Write #A="1" #B="↑"
Read #A="↑" #B=" 1" & Insert dummy read

DFM[1:0] : The bit is used to define image data write/read format to the Frame Memory in DBI Type B 16 bit bus interface and DBI Type C serial interface operation. See "DBI Data Format" for details.

EPF[1:0] : This bit is used to set data format when 16bpp (R,G,B) data are converted to 18bpp (r,g,b) stored in internal frame memory (18bpp).

EPF[1:0]	**16bpp(R,B) -> 18bpp (r,b)**
2'h0, 2'h1	r[5:0]={ R[4:0], R[4] } g[5:0]={ G[5:0] } b[5:0]={ B[4:0],B[4] }
2'h2	r[5:0]={ R[4:0], 1'b0 } g[5:0]={ G[5:0] } b[5:0]={ B[4:0], 1'b0 }
2'h3	r[5:0]={ R[4:0], 1'b1} } g[5:0]={ G[5:0] } b[5:0]={ B[4:0], 1'b1}

WEMODE : After frame memory write operation reaches to the end of window address area, the next write start position is selected.

WEMODE = 0: The write start position is not reset to the start of window address, and the subsequent data are disregarded. (Default)
WEMODE = 1: The write start position is reset to the start of window address area to overwrite the subsequent data to the previous data.

TEI[2:0] : The bit is used to define interval between outputs of TE signal. Set in accordance with update cycle and transfer rate of the display data.

TEI[2]	**TEI[1]**	**TEI[1]**	**Interval**
0	0	0	Every frame

	0	0	1	2 frames
	0	1	1	4 frames
	1	0	1	6 frames
	Other setting			Setting disabled
	DENC[2:0] : The bit is used to define Frame Memory write cycle in DPI operation. Set in accordance with update cycle of the display data.			
	DENC[2]	**DENC[1]**	**DENC[0]**	**Frame Memory Write Cycle**
	0	0	0	Every frame
	0	0	1	1 frame
	0	1	0	2 frames
	0	1	1	3 frames
	1	0	0	4 frames
	1	0	1	5 frames
	1	1	0	6 frames
	1	1	1	7 frames
Restriction	-			

Display Mode and Frame Memory Write Mode Setting : (B4h)

<table>
<tr><td>B4h</td><td colspan="13">Display Mode and Frame Memory Write Mode Setting</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>DB[17:8]</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td><td>Hex</td></tr>
<tr><td>command</td><td>0</td><td>1</td><td>↑</td><td>X</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>B4h</td></tr>
<tr><td>1st parameter</td><td>1</td><td>#A</td><td>#B</td><td>X</td><td>BYPASS</td><td>0</td><td>0</td><td>RM</td><td>0</td><td>0</td><td>DM[1]</td><td>DM[0]</td><td>XXh</td></tr>
<tr><td>2nd parameter</td><td>1</td><td>#A</td><td>#B</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>ENDIAN</td><td>XXh</td></tr>
<tr><td>Description</td><td colspan="13">Write #A=”1” #B=”↑”
Read #A=”↑” #B=” 1” & Insert dummy read

RM : The bit is used to select an interface for the Frame Memory access operation. The Frame Memory is accessed only via the interface defined by RM bit. Because the interface can be selected separately from display operation mode, writing data to the Frame Memory is possible via system interface when RM = 0, even in the DPI display operation . RM setting is enabled from the next frame. Wait 1 frame to transfer data after setting RM.</td></tr>
<tr><td></td><td colspan="2">RM</td><td colspan="11">Frame Memory Access Interface</td></tr>
<tr><td></td><td colspan="2">0</td><td colspan="11">DBI</td></tr>
<tr><td></td><td colspan="2">1</td><td colspan="11">DPI</td></tr>
<tr><td></td><td colspan="13">DM[1:0] : The bit is used to select display operation mode. The setting allows switching between display operation in synchronization with internal oscillation clock or DIP signal.
Change the bit setting during the Sleep mode.</td></tr>
<tr><td></td><td>DM[1]</td><td>DM[0]</td><td colspan="10">Display Mode</td></tr>
<tr><td></td><td>0</td><td>0</td><td colspan="10">Internal Oscillation clock</td></tr>
<tr><td></td><td>0</td><td>1</td><td colspan="10">DPI signal</td></tr>
<tr><td></td><td>1</td><td>0</td><td colspan="10">Setting disabled</td></tr>
<tr><td></td><td>1</td><td>1</td><td colspan="10">Setting disabled</td></tr>
<tr><td></td><td colspan="13">ENDIAN : Select little endian interface bit. At little endian mode, the host sends LSB data first.</td></tr>
<tr><td></td><td>ENDIAN</td><td colspan="12">Data transfer Mode</td></tr>
<tr><td></td><td>0</td><td colspan="12">Normal (MSB first)</td></tr>
<tr><td></td><td>1</td><td colspan="12">Little Endian (LSB first)</td></tr>
<tr><td>Restriction</td><td colspan="13">-</td></tr>
</table>

Panel Driving Setting: (B8h)

B8h	Panel Driving Setting												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	1	0	1	1	1	0	0	0	B8h
1st parameter	1	#A	#B	X	0	0	GS	SM	0	NDL	0	REV	XXh
2nd parameter	1	#A	#B	X	0	NL[6]	NL[5]	NL[4]	NL[3]	NL[2]	NL[1]	NL[0]	XXh
3rd parameter	1	#A	#B	X	0	SCN [6]	SCN [5]	SCN [4]	SCN [3]	SCN [2]	SCN [1]	SCN [0]	XXh
4th parameter	1	#A	#B	X	0	0	BC0	EOR	0	0	0	NW	XXh

Description

Write #A="1" #B="↑"
Read #A="↑" #B=" 1" & Insert dummy read

GS : Gate scan direction
0: Forward scan
1: Reverse scan

SM
0: Left/right interchanging scan
1: Left/right one-side scan

The LG4538 allows changing gate driver assignment and the scan mode by combination of SM and GS bits. Set the bits in accordance with the configuration of the module. For details, see "Scan Mode Setting".

NDL : The bit is used to define source output level in the non-lit display area. The polarity of grayscale voltage is inverted.

NDL	**Non-lit display area**	
	Positive polarity	**Negative Polarity**
0	V63	V0
1	V0	V63

REV : The grayscale is reversed by setting REV = 1. This enables the LG4538 to display the same image from the same set of data on both normally white and black panels. The source output level during the non-lit display period is determined by register settings, and NDL, respectively.

REV	**Frame Memory data**	**Source output level in display area**	
		Positive polarity	**Negative polarity**
0	18'h00000 : 18'hFFFFF	V63 : V0	V0 : V63
1	18'h00000 : 18'hFFFFF	V0 : V63	V63 : V0

Description

NL[6:0] : Sets the number of lines to drive the LCD at an interval of 8lines. The GRAM address mapping is not affected by the number of lines set with NL[6:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

NL[6:0]	**Number of drive line**
7’h00	4
7’h01	8
:	:
7’h4F	320
7’h6C-7’h7F	**Setting inhibited**

SCN[6:0] : The bit is used to set scanning start position.

SCN[7:0]	**Scanning start position**			
	SM=0		**SM= 1**	
	GS=0	**GS=1**	**GS=0**	**GS=1**
7’h00	G1	G(N)	G1	G(N)
7’h01	G5	G(N-4)	G9	G(N-8)
7’h02	G9	G(N-8)	G17	G(N-16)
7’h03	G13	G(N-12)	G25	G(N-24)
:	:	:		
7’h35	G213	G(N-212)	G2	G(N-1)
:	:	:	:	
7’h5D	G309	G(N-308)	G298	G(N-297)
7’h5E	G313	G(N-312)	G306	G(N-305)
7’h4F	G317	G(N-316)	G314	G(N-313)

N: Number of line(s) defined by NL[6:0].

To set SCAN, follow the restriction below.

GS	**SM**	**Restriction**
0	0	(Scanning start position -1) + (Number of line (NL bit)) ≤ 432
0	1	Scanning start position ≤ 432
1	0	(Scanning start position -1)/2 + (Number of line (NL bit)) ≤ 432
1	1	Scanning start position ≤ 432

<table>
<tr><td></td><td>
BC0 : Selects the liquid crystal drive waveform VCOM. See “Line Inversion AC Drive” for details.
0: frame inversion waveform is selected.
1: Line inversion waveform is selected.
In either liquid crystal drive method, the polarity inversion is halted in blank periods (back and front porch periods).

EOR : When EOR=1, alternation occurred by applying EOR(Exclusive OR) operation to an odd/even frame selecting signal and 1 or 2 line inversion signal while a C-pattern waveform is generated(BC0=1).

NW : This bit sets the number of lines for inversion liquid crystal drive by line inversion waveform (BC0=1)
<table>
<tr><td>NW</td><td>Number of Line</td></tr>
<tr><td>0</td><td>1 line</td></tr>
<tr><td>1</td><td>2 lines</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td>-</td></tr>
</table>

Display Control: (B9h)

B9h	Display Control												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	1	0	1	1	1	0	0	1	B9h
1st parameter	1	#A	#B	X	BP[7]	BP[6]	BP[5]	BP[4]	BP[3]	BP[2]	BP[1]	BP[0]	XXh
2nd parameter	1	#A	#B	X	FP[7]	FP[6]	FP[5]	FP[4]	FP[3]	FP[2]	FP[1]	FP[0]	XXh
3rd parameter	1	#A	#B	X	0	0	0	0	0	PTS[2]	PTS[1[	PTS[0]	XXh
4th parameter	1	#A	#B	X	ISC[3]	ISC[2]	ISC[1]	ISC[0]	0	0	0	PTG	XXh

Description

Write #A="1" #B="↑"
Read #A="↑" #B=" 1" & Insert dummy read

BP[7:0], FP[7:0] : These parameters define the retrace period (i.e. front and back porches) which appears before and after the display area. FP[7:0] bits define number of front porch lines while BP[7:0] bits define number of back porch lines.

BP[7:0]/FP[7:0]	**Number of lines for the back/front porches**
8'h00	Setting disabled
8'h01	Setting disabled

Description

8'h2	2 lines
8'h3	3 lines
8'h4	4 lines
:	:
8'hFD	253 lines
8'hFE	254 lines
8'hFF	255 lines

PTS[2:0] : The bit is used to define low-power consumption operation. PTS[1:0] defines output level in the non-lit display area. PTS[2] defines the operation of the grayscale amplifier and the step-up clock frequency.

PTS[2:0]	**Source output level**		**Garyscale amplifier In operation**	**Step-up clock Frequency**
	Positive polarity	**Negative polarity**		
3'h0	V255	V0	V0 to V255	Register setting (DC0, DC1)
3'h1	Setting disabled	Setting disabled	-	-
3'h2	GND	GND	V0 to V255	Register setting (DC0, DC1)
3'h3	Hi-Z	Hi-Z	V0 to V255	Register setting (DC0, DC1)
3'h4	V255	V0	V0 and V255	

<table>
<tr><td></td><td>3’h5</td><td>Setting disabled</td><td>Setting disabled</td><td>-</td><td></td></tr>
<tr><td></td><td>3’h6</td><td>GND</td><td>GND</td><td>V0 and V255</td><td></td></tr>
<tr><td></td><td>3’h7</td><td>Hi-Z</td><td>Hi-Z</td><td>V0 and V255</td><td></td></tr>
<tr><td></td><td colspan="5">ISC[3:0] : The bit is used to set gate interval scan when PTG bit sets interval scan in non-lit display area. The scan interval is always of odd number. The polarity of liquid crystal drive waveform is inverted in the same timing as the interval scan.</td></tr>
<tr><td></td><td colspan="2">ISC[3:0]</td><td>Scan inverval</td><td>ISC[3:0]</td><td>Scan interval</td></tr>
<tr><td></td><td colspan="2">4’h0</td><td>Setting disabled</td><td>4’h8</td><td>17 frames</td></tr>
<tr><td></td><td colspan="2">4’h1</td><td>3 frames</td><td>4’h9</td><td>19 frames</td></tr>
<tr><td></td><td colspan="2">4’h2</td><td>5 frames</td><td>4’hA</td><td>21 frames</td></tr>
<tr><td></td><td colspan="2">4’h3</td><td>7 frames</td><td>4’hB</td><td>23 frames</td></tr>
<tr><td></td><td colspan="2">4’h4</td><td>9 frames</td><td>4’hC</td><td>25 frames</td></tr>
<tr><td></td><td colspan="2">4’h5</td><td>11 frames</td><td>4’hD</td><td>27 frames</td></tr>
<tr><td></td><td colspan="2">4’h6</td><td>13 frames</td><td>4’hE</td><td>29 frames</td></tr>
<tr><td></td><td colspan="2">4’h7</td><td>15 frames</td><td>4’hF</td><td>31 frames</td></tr>
<tr><td></td><td colspan="5">PTG : The bit is used to select gate scan mode in non-lit display area.</td></tr>
<tr><td></td><td>PTG</td><td colspan="4">Gate output in non-lit display area</td></tr>
<tr><td></td><td>0</td><td colspan="4">Normal scan</td></tr>
<tr><td></td><td>1</td><td colspan="4">Interval scan</td></tr>
<tr><td>Restriction</td><td colspan="5">-</td></tr>
</table>

Power Setting: (BAh)

BAh	Power Setting – common setting												
	DCX	RDX	WRX	DB [17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	1	0	1	1	1	0	1	0	BAh
1st parameter	1	#A	#B	X	0	0	0	0	0	VC[2]	VC[1]	VC[0]	XXh
2nd parameter	1	#A	#B	X	0	0	0	0	0	BT[2]	BT[1]	BT[0]	XXh
3rd parameter	1	#A	#B	X	0	0	0	0	VRH [3]	VRH [2]	VRH [1]	VRH [0]	XXh
4th parameter	1	#A	#B	X	0	0	0	0	0	AP[2]	AP[1]	AP[0]	XXh
5th parameter	1	#A	#B	X	0	0	0	0	0	SAP [2]	SAP [1]	SAP [0]	XXh

Description

Write #A="1" #B="↑"
Read #A="↑" #B=" 1" & Insert dummy read

VC[2:0] : The bits define volate level VCIOUT.

VC[2:0]	**VCIOUT (Reference Voltage) (VCI1 Voltage)**
3'h0	1.00 x VCI
3'h1	0.92 x VCI
3'h2	0.90 x VCI
3'h3	0.87 x VCI
3'h4	0.85 x VCI
3'h5	0.83 x VCI
3'h6	0.73 x VCI
3'h7	Setting disabled

Description

BT[2:0] : Sets the factor used in the step-up circuits. Use an optimal step-up factor for the voltage in use. To reduce power consumption, set a smaller factor.

BT[2:0]	**AVDD**	**VGH**	**VGL**	**Capacitor connection Pins**
3'h0	VCI1 x 2 [x 2]	AVDD x 3 [x 6]	–(VCI1 + AVDD x 2) [x –5]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C13±, C21±, C22±
3'h1			–(AVDD x 2) [x –4]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C21±, C22±
3'h2			–(VCI1 + AVDD) [x –3]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C13±, C21±, C22±
3'h3		VCI1 + AVDD x 2 [x 5]	–(VCI1 + AVDD x 2) [x –5]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C13±, C21±, C22±
3'h4			–(AVDD x 2) [x –4]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C21±, C22±
3'h5			–(VCI1 + AVDD) [x –3]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C13±, C21±, C22±

	3’h6		AVDD x 2 [x 4]	–(AVDD x 2) [x –4]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C21±, C22±
	3’h7			–(VCI1 + AVDD) [x –3]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C13±, C21±, C22±

Note: 1. The step-up factor from VCI1 are shown in the brackets [ ].
2. Connect capacitors where required when using AVDD, VGH, VGL voltages.
3. Set the following voltages within the respective ranges:
AVDD = (GVDD+0.5)V~6.0V, VGH-VGL≤25V, VGH>AVDD+0.5V,
VGL<VCL-0.6V

VRH[3:0] : Sets the factor to generate GVDD from VCI

VRH[3:0]	**GVDD Voltage**	**VRH[3:0]**	**GVDD Voltage**
4’h0	VCIOUT x 1.27	4’h8	Setting disabled
4’h1	VCIOUT x 1.32	4’h9	VCIOUT x 1.62
4’h2	VCIOUT x 1.37	4’hA	VCIOUT x 1.67
4’h3	VCIOUT x 1.42	4’hB	VCIOUT x 1.72
4’h4	VCIOUT x 1.47	4’hC	VCIOUT x 1.77
4’h5	VCIOUT x 1.52	4’hD	VCIOUT x 1.82
4’h6	VCIOUT x 1.57	4’hE	VCIOUT x 1.87
4’h7	Setting disabled	4’hF	VCIOUT x 1.92

AP[2:0] : These bits adjust the constant current in the operational amplifier circuit in the LCD power supply circuit. The larger constant current will enhance the drivability of the LCD, however more current will be consumed. Adjust the constant current taking the trade-off between the display quality and the current consumption into account.

AP[2:0]	**LCD power supply circuits**	**Grayscale voltage generating circuit**
3’h0	Halt operation	Halt operation
3’h1	Setting disabled	Setting disabled
3’h2	Normal operation	0.5
3’h3	Normal operation	0.75
3’h4	Normal operation	1
3’h5	Normal operation	1.25
3’h6	Normal operation	1.5
3’h7	Setting disabled	Setting disabled

Description

Note: In this table, the constant current in operational amplifiers is shown by the ratio to the constant current when AP[1:0] is set to 2’h3.

SAP[2:0] : Adjust the constant current for the operational amplifier circuit in the source driver. A larger constant current stabilizes the operational amplifier circuit, but current consumption increases. Adjust the constant current taking the display quality-current consumption trade-off into account. During a period showing no display, set SAP = 0 to halt the operational amplifier circuit to reduce current consumption.

SAP[2:0]	**Constant current (ratio to 3)**
3’h0	Halt operation amplifier
3’h1	Constant current (ratio to 3) : 0.65
3’h2	Constant current (ratio to 3) : 0.8
3’h3	Constant current (ratio to 3) : 1.00

	3’h4	Constant current (ratio to 3) : 1.35
	3’h5	Constant current (ratio to 3) : 1.60
	3’h6	Setting disabled
	3’h7	Setting disabled
Restriction	-	

Power Setting : (BBh)

BBh	Power Setting – VCOM setting												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	1	0	1	1	1	0	1	1	BBh
1st parameter	1	#A	#B	X	0	0	0	VDV [4]	VDV [3]	VDV [2]	VDV [1]	VDV [0]	XXh
2nd parameter	1	#A	#B	X	0	VCM [6]	VCM [5]	VCM [4]	VCM [3]	VCM [2]	VCM [1]	VCM [0]	XXh
3rd parameter	1	#A	#B	X	0	0	0	0	0	0	0	VCOMG	XXh

Description

Write #A="1" #B="↑"
Read #A="↑" #B=" 1" & Insert dummy read

VDV[4:0] : Sets the alternating amplitudes of VCOM AC voltage. These bits amplify VCOM by from 0.6 to 1.23 times the GVDD voltage. If VCOMG = 0, VDV[4:0] bits are disabled.

VDV[4:0]	VCOM amplitude	VDV[4:0]	VCOM amplitude
5'h00	GVDD x 0.60	5'h10	GVDD x 1.05
5'h01	GVDD x 0.63	5'h11	GVDD x 1.08
5'h02	GVDD x 0.66	5'h12	GVDD x 1.11
5'h03	GVDD x 0.69	5'h13	GVDD x 1.14
5'h04	GVDD x 0.72	5'h14	GVDD x 1.17
5'h05	GVDD x 0.75	5'h15	GVDD x 1.20
5'h06	GVDD x 0.78	5'h16	GVDD x 1.23
5'h07	GVDD x 0.81	5'h17	GVDD x 1.26
5'h08	GVDD x 0.84	5'h18	GVDD x 1.29
5'h09	GVDD x 0.87	5'h19	GVDD x 1.32
5'h0A	GVDD x 0.90	5'h1A	GVDD x 1.35
5'h0B	GVDD x 0.93	5'h1B	GVDD x 1.38
5'h0C	GVDD x 0.96	5'h1C	GVDD x 1.41
5'h0D	GVDD x 0.99	5'h1D	GVDD x 1.44
5'h0E	GVDD x 1.02	5'h1E	GVDD x 1.47
5'h0F	Setting disabled	5'h1F	GVDD x 1.50

Description

Note : Set the VCOML voltage from (VCL + 0.5)V to 0V

VCM[6:0] : Sets the VCOMH level (the higher voltage of VCOM alternating drive). VCM[6:0] specifies the voltage by GVDD x n, where n is a discrete number from 0.400 to 0.875. To halt internal volume and adjust VCOMH with an external resistor from VCOMR, set VCM[6:0] = "1111111".

VCM [6:0]	VCOMH	VCM [6:0]	VCOMH	VCM [6:0]	VCOMH	VCM [6:0]	VCOMH
7'h00	GVDD x 0.400	7'h20	GVDD x 0.560	7'h40	GVDD x 0.720	7'h60	GVDD x 0.880

	7'h01	GVDD x 0.405	7'h21	GVDD x 0.565	7'h41	GVDD x 0.725	7'h61	GVDD x 0.885
	7'h02	GVDD x 0.410	7'h22	GVDD x 0.570	7'h42	GVDD x 0.730	7'h62	GVDD x 0.890
	7'h03	GVDD x 0.415	7'h23	GVDD x 0.575	7'h43	GVDD x 0.735	7'h63	GVDD x 0.895
	7'h04	GVDD x 0.420	7'h24	GVDD x 0.580	7'h44	GVDD x 0.740	7'h64	GVDD x 0.900
	7'h05	GVDD x 0.425	7'h25	GVDD x 0.585	7'h45	GVDD x 0.745	7'h65	GVDD x 0.905
	7'h06	GVDD x 0.430	7'h26	GVDD x 0.590	7'h46	GVDD x 0.750	7'h66	GVDD x 0.910
	7'h07	GVDD x 0.435	7'h27	GVDD x 0.595	7'h47	GVDD x 0.755	7'h67	GVDD x 0.915
	7'h08	GVDD x 0.440	7'h28	GVDD x 0.600	7'h48	GVDD x 0.760	7'h68	GVDD x 0.920
	7'h09	GVDD x 0.445	7'h29	GVDD x 0.605	7'h49	GVDD x 0.765	7'h69	GVDD x 0.925
	7'h0A	GVDD x 0.450	7'h2A	GVDD x 0.610	7'h4A	GVDD x 0.770	7'h6A	GVDD x 0.930
	7'h0B	GVDD x 0.455	7'h2B	GVDD x 0.615	7'h4B	GVDD x 0.775	7'h6B	GVDD x 0.935
	7'h0C	GVDD x 0.460	7'h2C	GVDD x 0.620	7'h4C	GVDD x 0.780	7'h6C	GVDD x 0.940
	7'h0D	GVDD x 0.465	7'h2D	GVDD x 0.625	7'h4D	GVDD x 0.785	7'h6D	GVDD x 0.945
	7'h0E	GVDD x 0.470	7'h2E	GVDD x 0.630	7'h4E	GVDD x 0.790	7'h6E	GVDD x 0.950
	7'h0F	GVDD x 0.475	7'h2F	GVDD x 0.635	7'h4F	GVDD x 0.795	7'h6F	GVDD x 0.955
	7'h10	GVDD x 0.480	7'h30	GVDD x 0.640	7'h50	GVDD x 0.800	7'h70	GVDD x 0.960
	7'h11	GVDD x 0.485	7'h31	GVDD x 0.645	7'h51	GVDD x 0.805	7'h71	GVDD x 0.965
	7'h12	GVDD x 0.490	7'h32	GVDD x 0.650	7'h52	GVDD x 0.810	7'h72	GVDD x 0.970
	7'h13	GVDD x 0.495	7'h33	GVDD x 0.655	7'h53	GVDD x 0.815	7'h73	GVDD x 0.975
	7'h14	GVDD x 0.500	7'h34	GVDD x 0.660	7'h54	GVDD x 0.820	7'h74	GVDD x 0.980
	7'h15	GVDD x 0.505	7'h35	GVDD x 0.665	7'h55	GVDD x 0.825	7'h75	Setting disabled
	7'h16	GVDD x 0.510	7'h36	GVDD x 0.670	7'h56	GVDD x 0.830	7'h76	Setting disabled
	7'h17	GVDD x 0.515	7'h37	GVDD x 0.675	7'h57	GVDD x 0.835	7'h77	Setting disabled
	7'h18	GVDD x 0.520	7'h38	GVDD x 0.680	7'h58	GVDD x 0.840	7'h78	Setting disabled
	7'h19	GVDD x 0.525	7'h39	GVDD x 0.685	7'h59	GVDD x 0.845	7'h79	Setting disabled
	7'h1A	GVDD x 0.530	7'h3A	GVDD x 0.690	7'h5A	GVDD x 0.850	7'h7A	Setting disabled
	7'h1B	GVDD x 0.535	7'h3B	GVDD x 0.695	7'h5B	GVDD x 0.855	7'h7B	Setting disabled
	7'h1C	GVDD x 0.540	7'h3C	GVDD x 0.700	7'h5C	GVDD x 0.860	7'h7C	Setting disabled
	7'h1D	GVDD x 0.545	7'h3D	GVDD x 0.705	7'h5D	GVDD x 0.865	7'h7D	Setting disabled
	7'h1E	GVDD x 0.550	7'h3E	GVDD x 0.710	7'h5E	GVDD x 0.870	7'h7E	Setting disabled
	7'h1F	GVDD x 0.555	7'h3F	GVDD x 0.715	7'h5F	GVDD x 0.875	7'h7F	Setting disabled
	VCOMG : When VCOMG = 1, the LG4538 can output a negative voltage level for VCOML (0V ~ (VCL + 0.5V) Max.). When VCOMG = 0, the output of VCOML is fixed to GND level, and setting of the VDV[4:0] bits become invalid. And LG4538 halts the amplifier for negative voltage to save power. In this case, adjust the amplitude of (VCOMH-VCOML) voltage only with VCM[6:0] bits. VCOMG = 1 is valid only when PON = 1. So set PON = 1 ahead, before setting VCOMG = 1. In addition, set CMFPD = 1 ahead, before setting VCOMG = 0 on the frame inversion driving mode.							
Restriction	-							

Power Setting : (BCh)

BCh	Power Setting – Step-up Frequency setting												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	1	0	1	1	1	1	0	0	BCh
1st parameter	1	#A	#B	X	0	0	0	0	0	0	0	DSEN	XXh
2nd parameter	1	#A	#B	X	0	0	0	0	0	DC0[2]	DC0[1]	DC0[0]	XXh
3rd parameter	1	#A	#B	X	0	0	0	0	0	DC1[2]	DC1[1]	DC1[0]	XXh

Description

Write #A="1" #B="↑"
Read #A="↑" #B=" 1" & Insert dummy read

DSEN : This bit enables the operation of clock synchronization mode.
DSEN = 0: Step-up is operated by divided oscillator clock.
DSEN = 1: Step-up is operated by synchronized line or frame clock.

DC0[2:0] : These bits set the step-up clock frequency of the step-up circuit 1.

DC0[2:0]	**Step-up circuit 1 : step-up frequency (fDCDC1)**	
	DSEN = 0	**DSEN = 1**
3'h0	fosc/8	Internal clock / 8
3'h1	fosc/16	Internal clock / 16
3'h2	fosc/32	Internal clock / 32
3'h3	fosc/64	Internal clock / 64
3'h4	fosc/128	Internal clock / 128
3'h5	fosc/256	Internal clock / 256
3'h6	fosc/512	Setting disabled
3'h7	Halt step-up circuit 1	Halt step-up circuit 1

DC1[2:0] : These bits set the step-up clock frequency of the step-up circuit 2.

DC1[2:0]	**Step-up circuit 1 : step-up frequency (fDCDC1)**	
	DSEN = 0	**DSEN = 1**
3'h0	fosc/32	Setting disabled
3'h1	fosc/64	Line frequency / 2
3'h2	fosc/128	Line frequency / 4
3'h3	fosc/256	Line frequency / 8
3'h4	fosc/512	Line frequency / 16
3'h5	fosc/1024	Line frequency / 32
3'h6	fosc/2048	Line frequency / 64
3'h7	Halt step-up circuit 1	Halt step-up circuit 1

Restriction	-

VDD Regulator Setting : (BDh)

<table>
<tr><td>BDh</td><td colspan="13">VDD Regulator setting</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>DB[17:8]</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td><td>Hex</td></tr>
<tr><td>command</td><td>0</td><td>1</td><td>↑</td><td>X</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>BDh</td></tr>
<tr><td>1st parameter</td><td>1</td><td>#A</td><td>#B</td><td>X</td><td>0</td><td>RSET[2]</td><td>RSET[1]</td><td>RSET[0]</td><td>0</td><td>RI[2]</td><td>RI[0]</td><td>RI[0]</td><td>XXh</td></tr>
<tr><td>2nd parameter</td><td>1</td><td>#A</td><td>#B</td><td>X</td><td>0</td><td>RV[2]</td><td>RV[1]</td><td>RV[0]</td><td>0</td><td>RCONT[2]</td><td>RCONT[1]</td><td>RCONT[0]</td><td>XXh</td></tr>
<tr><td rowspan="13">Description</td><td colspan="13">Write #A=”1” #B=”↑”
Read #A=”↑” #B=” 1” & Insert dummy read

RSET[2:0] : These bits control the main bias.</td></tr>
<tr><td colspan="2">RSET[2:0]</td><td colspan="11">Main bias current</td></tr>
<tr><td colspan="2">3’h0</td><td colspan="11">x 0.39</td></tr>
<tr><td colspan="2">3’h1</td><td colspan="11">x 0.43</td></tr>
<tr><td colspan="2">3’h2</td><td colspan="11">x 0.48</td></tr>
<tr><td colspan="2">3’h3</td><td colspan="11">x 0.56</td></tr>
<tr><td colspan="2">3’h4</td><td colspan="11">x 0.65</td></tr>
<tr><td colspan="2">3’h5</td><td colspan="11">x 0.79</td></tr>
<tr><td colspan="2">3’h6</td><td colspan="11">x 1.00 (default)</td></tr>
<tr><td colspan="2">3’h7</td><td colspan="11">x 1.36</td></tr>
<tr><td colspan="13">
RI[2:0] : These bits control the bias current of internal logic regulator.</td></tr>
<tr><td colspan="2">RI[2:0]</td><td colspan="11">Logic regulator bias current</td></tr>
<tr><td colspan="2">3’h0</td><td colspan="11">x 1</td></tr>
<tr><td rowspan="13"></td><td colspan="2">3’h1</td><td colspan="11">x 2</td></tr>
<tr><td colspan="2">3’h2</td><td colspan="11">x 3</td></tr>
<tr><td colspan="2">3’h3</td><td colspan="11">x 4</td></tr>
<tr><td colspan="2">3’h4</td><td colspan="11">x 5</td></tr>
<tr><td colspan="2">3’h5</td><td colspan="11">x 6</td></tr>
<tr><td colspan="2">3’h6</td><td colspan="11">x 7</td></tr>
<tr><td colspan="2">3’h7</td><td colspan="11">x 8</td></tr>
<tr><td colspan="13">
RV[2:0] : These bits control the output voltage of internal logic regulator.</td></tr>
<tr><td colspan="2">RV[2:0]</td><td colspan="11">Vdd Voltage</td></tr>
<tr><td colspan="2">3’h0</td><td colspan="11">VCI x 0.80</td></tr>
<tr><td colspan="2">3’h1</td><td colspan="11">VCI x 0.75</td></tr>
<tr><td colspan="2">3’h2</td><td colspan="11">VCI x 0.70</td></tr>
<tr><td colspan="2">3’h3</td><td colspan="11">VCI x 0.65</td></tr>
</table>

	3’h4	VCI x 0.60
	3’h5	VCI x 0.55
	3’h6	VCI x 0.50
	3’h7	VCI x 0.45
	RCONT[2:0] : These bits control the input voltage of main bias op_amp.	
	3’h0	VCI x 0.25
	3’h1	Setting disabled
	3’h2	Open
	3’h3	VCI x 0.30
	3’h4	Setting disabled
	3’h5	Setting disabled
	3’h6	VCI x 0.20
	3’h7	Setting disabled
Restriction	-	

Gamma Select Setting (C0h)

<table>
<tr><td>C0h</td><td colspan="13">Gamma Select Setting</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>DB[17:8]</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td><td>Hex</td></tr>
<tr><td>command</td><td>0</td><td>1</td><td>↑</td><td>X</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>C0h</td></tr>
<tr><td>1st parameter</td><td>1</td><td>#A</td><td>#B</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>SGE</td><td>EN_MA</td><td>PS</td><td>XXh</td></tr>
<tr><td>Description</td><td colspan="13">Write #A=”1” #B=”↑”
Read #A=”↑” #B=” 1” & Insert dummy read

SGE : Sets the R/G/B gamma register.</td></tr>
<tr><td></td><td colspan="2">SGE</td><td colspan="11">Gamma register</td></tr>
<tr><td></td><td colspan="2">0</td><td colspan="11">R/G/B gamma register : C1, C2h</td></tr>
<tr><td></td><td colspan="2">1</td><td colspan="11">R gamma register : C1,C2h
G gamma register : C3,C4h
B gamma register : C4,C6h</td></tr>
<tr><td></td><td colspan="13">EN_MA : This bit specify the PFN0-5/PFP0-1/PMN/PMP registers Manual setting enable signal</td></tr>
<tr><td></td><td colspan="3"></td><td colspan="2">EN_MA</td><td colspan="2">PS</td></tr>
<tr><td></td><td colspan="2">Auto</td><td colspan="2">TN mode</td><td colspan="2">0</td><td colspan="2">0</td></tr>
<tr><td></td><td colspan="2"></td><td colspan="2">VA mode</td><td colspan="2">0</td><td colspan="2">1</td></tr>
<tr><td></td><td colspan="2">Manual</td><td colspan="2">User setting</td><td colspan="2">1</td><td colspan="2">x</td></tr>
<tr><td></td><td colspan="13">PS : This ibt specifies the VA mode enable signal.</td></tr>
<tr><td></td><td colspan="2">PS</td><td colspan="11">Mode</td></tr>
<tr><td></td><td colspan="2">0</td><td colspan="11">TN Mode</td></tr>
<tr><td></td><td colspan="2">1</td><td colspan="11">VA mode</td></tr>
<tr><td>Restriction</td><td colspan="13">-</td></tr>
</table>

Gamma Set A "+" polarity (C1h)

C1h	Gamma Set A "+" polarity												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	1	1	0	0	0	0	0	1	C1h
1st parameter	1	#A	#B	X	0	PKP1[2]	PKP1[1]	PKP1[0]	0	PKP0[2]	PKP0[1]	PKP0[0]	XXh
2nd parameter	1	#A	#B	X	0	PKP3[2]	PKP3[1]	PKP3[0]	0	PKP2[2]	PKP2[1]	PKP2[0]	XXh
3rd parameter	1	#A	#B	X	0	PKP5[2]	PKP5[1]	PKP5[0]	0	PKP4[2]	PKP4[1]	PKP4[0]	XXh
4th parameter	1	#A	#B	X	0	PRP1[2]	PRP1[1]	PRP1[0]	0	PRP0[2]	PRP0[1]	PRP0[0]	XXh
5th parameter	1	#A	#B	X	0	0	0	VRP0[4]	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]	XXh
6th parameter	1	#A	#B	X	0	0	0	VRP1[4]	VRP1[3]	VRP1[2]	VRP1[1]	VRP1[0]	XXh
7th parameter	1	#A	#B	X	0	PFP1[2]	PFP1[1]	PFP1[0]	0	PFP0[2]	PFP0[1]	PFP0[0]	XXh
8th parameter	1	#A	#B	X	0	PFP3[2]	PFP3[1]	PFP3[0]	0	PFP2[2]	PFP2[1]	PFP2[0]	XXh
9th parameter	1	#A	#B	X	0	0	0	0	0	PMP[2]	PMP[1]	PMP[0]	XXh
Description	Write #A="1" #B="↑" Read #A="↑" #B=" 1" & Insert dummy read **PKP5-0[2 :0]** : γ fine-adjustment register for positive polarity **PRP1-0[2 :0]** : γ gradient-adjustment register for positive polarity **VRP0[3:0], VRP1[4 :0] :** γ amplitude-adjustment register for positive polarity **PFP3-0[2:0] :** γ fine adjustment register bits for positive polarity **PMP[2:0] :** γ fine adjustment register bits for positive polarity For details, see "γ-Correction Function" section												
Restriction	-												

Gamma Set A "–" polarity (C2h)

C2h	Gamma Set A "-" polarity												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	1	1	0	0	0	0	1	0	C2h
1st parameter	1	#A	#B	X	0	PKN1[2]	PKN1[1]	PKN1[0]	0	PKN0[2]	PKN0[1]	PKN0[0]	XXh
2nd parameter	1	#A	#B	X	0	PKN3[2]	PKN3[1]	PKN3[0]	0	PKN2[2]	PKN2[1]	PKN2[0]	XXh
3rd parameter	1	#A	#B	X	0	PKN5[2]	PKN5[1]	PKN5[0]	0	PKN4[2]	PKN4[1]	PKN4[0]	XXh
4th parameter	1	#A	#B	X	0	PRN1[2]	PRN1[1]	PRN1[0]	0	PRN0[2]	PRN0[1]	PRN0[0]	XXh
5th parameter	1	#A	#B	X	0	0	0	VRN0[4]	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]	XXh
6th parameter	1	#A	#B	X	0	0	0	VRN1[4]	VRN1[3]	VRN1[2]	VRN1[1]	VRN1[0]	XXh
7th parameter	1	#A	#B	X	0	PFN1[2]	PFN1[1]	PFN1[0]	0	PFN0[2]	PFN0[1]	PFN0[0]	XXh
8th parameter	1	#A	#B	X	0	PFN3[2]	PFN3[1]	PFN3[0]	0	PFN2[2]	PFN2[1]	PFN2[0]	XXh
9th parameter	1	#A	#B	X	0	0	0	0	0	PMN[2]	PMN[1]	PMN[0]	XXh
Description	Write #A="1" #B="↑" Read #A="↑" #B=" 1" & Insert dummy read **PKN5-0[2 :0] :** γ fine-adjustment register for negative polarity **PRN1-0[2 :0] :** γ gradient-adjustment register for negative polarity **VRN0[3:0], VRN1[4 :0] :** γ amplitude-adjustment register for negative polarity **PFN3-0[2:0] :** γ fine adjustment register bits for negative polarity **PMN[2:0] :** γ fine adjustment register bits for negative polarity For details, see "γ-Correction Function" section												
Restriction	-												

Gamma Set B "+" polarity (C3h)

C3h	Gamma Set B "+" polarity												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	1	1	0	0	0	0	1	1	C3h
1st parameter	1	#A	#B	X	0	PKP1[2]	PKP1[1]	PKP1[0]	0	PKP0[2]	PKP0[1]	PKP0[0]	XXh
2nd parameter	1	#A	#B	X	0	PKP3[2]	PKP3[1]	PKP3[0]	0	PKP2[2]	PKP2[1]	PKP2[0]	XXh
3rd parameter	1	#A	#B	X	0	PKP5[2]	PKP5[1]	PKP5[0]	0	PKP4[2]	PKP4[1]	PKP4[0]	XXh
4th parameter	1	#A	#B	X	0	PRP1[2]	PRP1[1]	PRP1[0]	0	PRP0[2]	PRP0[1]	PRP0[0]	XXh
5th parameter	1	#A	#B	X	0	0	0	VRP0[4]	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]	XXh
6th parameter	1	#A	#B	X	0	0	0	VRP1[4]	VRP1[3]	VRP1[2]	VRP1[1]	VRP1[0]	XXh
7th parameter	1	#A	#B	X	0	PFP1[2]	PFP1[1]	PFP1[0]	0	PFP0[2]	PFP0[1]	PFP0[0]	XXh
8th parameter	1	#A	#B	X	0	PFP3[2]	PFP3[1]	PFP3[0]	0	PFP2[2]	PFP2[1]	PFP2[0]	XXh
9th parameter	1	#A	#B	X	0	0	0	0	0	PMP[2]	PMP[1]	PMP[0]	XXh
Description	Write #A="1" #B="↑" Read #A="↑" #B=" 1" & Insert dummy read **PKP5-0[2 :0]** : γ fine-adjustment register for positive polarity **PRP1-0[2 :0]** : γ gradient-adjustment register for positive polarity **VRP0[3:0], VRP1[4 :0] :** γ amplitude-adjustment register for positive polarity **PFP3-0[2:0] :** γ fine adjustment register bits for positive polarity **PMP[2:0] :** γ fine adjustment register bits for positive polarity For details, see "γ-Correction Function" section												
Restriction	-												

Gamma Set B "–" polarity (C4h)

C4h	Gamma Set B "-" polarity												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	1	1	0	0	0	1	0	0	C4h
1st parameter	1	#A	#B	X	0	PKN1[2]	PKN1[1]	PKN1[0]	0	PKN0[2]	PKN0[1]	PKN0[0]	XXh
2nd parameter	1	#A	#B	X	0	PKN3[2]	PKN3[1]	PKN3[0]	0	PKN2[2]	PKN2[1]	PKN2[0]	XXh
3rd parameter	1	#A	#B	X	0	PKN5[2]	PKN5[1]	PKN5[0]	0	PKN4[2]	PKN4[1]	PKN4[0]	XXh
4th parameter	1	#A	#B	X	0	PRN1[2]	PRN1[1]	PRN1[0]	0	PRN0[2]	PRN0[1]	PRN0[0]	XXh
5th parameter	1	#A	#B	X	0	0	0	VRN0[4]	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]	XXh
6th parameter	1	#A	#B	X	0	0	0	VRN1[4]	VRN1[3]	VRN1[2]	VRN1[1]	VRN1[0]	XXh
7th parameter	1	#A	#B	X	0	PFN1[2]	PFN1[1]	PFN1[0]	0	PFN0[2]	PFN0[1]	PFN0[0]	XXh
8th parameter	1	#A	#B	X	0	PFN3[2]	PFN3[1]	PFN3[0]	0	PFN2[2]	PFN2[1]	PFN2[0]	XXh
9th parameter	1	#A	#B	X	0	0	0	0	0	PMN[2]	PMN[1]	PMN[0]	XXh
Description	Write #A="1" #B="↑" Read #A="↑" #B=" 1" & Insert dummy read **PKN5-0[2 :0] :** γ fine-adjustment register for negative polarity **PRN1-0[2 :0] :** γ gradient-adjustment register for negative polarity **VRN0[3:0], VRN1[4 :0] :** γ amplitude-adjustment register for negative polarity **PFN3-0[2:0] :** γ fine adjustment register bits for negative polarity **PMN[2:0] :** γ fine adjustment register bits for negative polarity For details, see "γ-Correction Function" section												
Restriction	-												

Gamma Set C "+" polarity (C5h)

C5h	Gamma Set C "+" polarity												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	1	1	0	0	0	1	0	1	C5h
1st parameter	1	#A	#B	X	0	PKP1[2]	PKP1[1]	PKP1[0]	0	PKP0[2]	PKP0[1]	PKP0[0]	XXh
2nd parameter	1	#A	#B	X	0	PKP3[2]	PKP3[1]	PKP3[0]	0	PKP2[2]	PKP2[1]	PKP2[0]	XXh
3rd parameter	1	#A	#B	X	0	PKP5[2]	PKP5[1]	PKP5[0]	0	PKP4[2]	PKP4[1]	PKP4[0]	XXh
4th parameter	1	#A	#B	X	0	PRP1[2]	PRP1[1]	PRP1[0]	0	PRP0[2]	PRP0[1]	PRP0[0]	XXh
5th parameter	1	#A	#B	X	0	0	0	VRP0[4]	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]	XXh
6th parameter	1	#A	#B	X	0	0	0	VRP1[4]	VRP1[3]	VRP1[2]	VRP1[1]	VRP1[0]	XXh
7th parameter	1	#A	#B	X	0	PFP1[2]	PFP1[1]	PFP1[0]	0	PFP0[2]	PFP0[1]	PFP0[0]	XXh
8th parameter	1	#A	#B	X	0	PFP3[2]	PFP3[1]	PFP3[0]	0	PFP2[2]	PFP2[1]	PFP2[0]	XXh
9th parameter	1	#A	#B	X	0	0	0	0	0	PMP[2]	PMP[1]	PMP[0]	XXh
Description	Write #A="1" #B="↑" Read #A="↑" #B=" 1" & Insert dummy read **PKP5-0[2 :0]** : γ fine-adjustment register for positive polarity **PRP1-0[2 :0]** : γ gradient-adjustment register for positive polarity **VRP0[3:0], VRP1[4 :0] :** γ amplitude-adjustment register for positive polarity **PFP3-0[2:0] :** γ fine adjustment register bits for positive polarity **PMP[2:0] :** γ fine adjustment register bits for positive polarity For details, see "γ-Correction Function" section												
Restriction	-												

Gamma Set C "–" polarity (C6h)

C6h	Gamma Set C "-" polarity												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	1	1	0	0	0	1	1	0	C6h
1st parameter	1	#A	#B	X	0	PKN1[2]	PKN1[1]	PKN1[0]	0	PKN0[2]	PKN0[1]	PKN0[0]	XXh
2nd parameter	1	#A	#B	X	0	PKN3[2]	PKN3[1]	PKN3[0]	0	PKN2[2]	PKN2[1]	PKN2[0]	XXh
3rd parameter	1	#A	#B	X	0	PKN5[2]	PKN5[1]	PKN5[0]	0	PKN4[2]	PKN4[1]	PKN4[0]	XXh
4th parameter	1	#A	#B	X	0	PRN1[2]	PRN1[1]	PRN1[0]	0	PRN0[2]	PRN0[1]	PRN0[0]	XXh
5th parameter	1	#A	#B	X	0	0	0	VRN0[4]	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]	XXh
6th parameter	1	#A	#B	X	0	0	0	VRN1[4]	VRN1[3]	VRN1[2]	VRN1[1]	VRN1[0]	XXh
7th parameter	1	#A	#B	X	0	PFN1[2]	PFN1[1]	PFN1[0]	0	PFN0[2]	PFN0[1]	PFN0[0]	XXh
8th parameter	1	#A	#B	X	0	PFN3[2]	PFN3[1]	PFN3[0]	0	PFN2[2]	PFN2[1]	PFN2[0]	XXh
9th parameter	1	#A	#B	X	0	0	0	0	0	PMN[2]	PMN[1]	PMN[0]	XXh
Description	Write #A="1" #B="↑" Read #A="↑" #B=" 1" & Insert dummy read **PKN5-0[2 :0] :** γ fine-adjustment register for negative polarity **PRN1-0[2 :0] :** γ gradient-adjustment register for negative polarity **VRN0[3:0], VRN1[4 :0] :** γ amplitude-adjustment register for negative polarity **PFN3-0[2:0] :** γ fine adjustment register bits for negative polarity **PMN[2:0] :** γ fine adjustment register bits for negative polarity For details, see "γ-Correction Function" section												
Restriction	-												

Display Timing Setting (D0h)

<table>
<tr><td>D0h</td><td colspan="13">Display Timing Setting</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>DB[17:8]</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td><td>Hex</td></tr>
<tr><td>command</td><td>0</td><td>1</td><td>↑</td><td>X</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>D0h</td></tr>
<tr><td>1st parameter</td><td>1</td><td>#A</td><td>#B</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>DIV[1]</td><td>DIV[0]</td><td>XXh</td></tr>
<tr><td>2nd parameter</td><td>1</td><td>#A</td><td>#B</td><td>X</td><td>RTN[7]</td><td>RTN[6]</td><td>RTN[5]</td><td>RTN[4]</td><td>RTN[3]</td><td>RTN[2]</td><td>RTN[1]</td><td>RTN[0]</td><td>XXh</td></tr>
<tr><td>Description</td><td colspan="13">Write #A=”1” #B=”↑”
Read #A=”↑” #B=” 1” & Insert dummy read

DIV[1:0] : Sets the division ratio of the internal clock frequency. The LG4538’s internal operation is synchronized with the frequency divided display clock. When changing the DIV[1:0] bits, the width of the reference clock for liquid crystal panel control signals is changed. The frame frequency can be adjusted by register setting (RTNI and DIVI bits). When changing the number of lines to drive the liquid crystal panel, adjust the frame frequency too.

For details, see “Frame- Frequency Adjustment Function”.

Frame Frequency Calculation

Frame frequency = fosc/(clock cycles per line x division ratio x (active line + BP + FP))</td></tr>
<tr><td></td><td colspan="4">DIV[1:0]</td><td colspan="4">Division Ratio</td><td colspan="5">Internal operation clock unit</td></tr>
<tr><td></td><td colspan="4">2’h0</td><td colspan="4">1/2</td><td colspan="5">2 clocks</td></tr>
<tr><td></td><td colspan="4">2’h1</td><td colspan="4">1/4</td><td colspan="5">4 clocks</td></tr>
<tr><td></td><td colspan="4">2’h2</td><td colspan="4">1/8</td><td colspan="5">8 clocks</td></tr>
<tr><td></td><td colspan="4">2’h3</td><td colspan="4">1/16</td><td colspan="5">16 clocks</td></tr>
<tr><td></td><td colspan="13">RTN[7:0] : Sets 1H (line) period. This setting is enabled while the LG4538’s display operation is synchronized with internal clock. RTNI[7:0] should be greater than or equal to 120 (=78h).</td></tr>
<tr><td></td><td colspan="4">RTN[7:0]</td><td colspan="9">Clock per Line</td></tr>
<tr><td></td><td colspan="4">8’h00 – 8’h77</td><td colspan="9">Setting disabled</td></tr>
<tr><td></td><td colspan="4">8’h78</td><td colspan="9">120 clocks</td></tr>
<tr><td></td><td colspan="4">8’h7A</td><td colspan="9">122 clocks</td></tr>
<tr><td></td><td colspan="4">8’h7C</td><td colspan="9">124 clocks</td></tr>
<tr><td></td><td colspan="4">:</td><td colspan="9">:</td></tr>
<tr><td></td><td colspan="4">8’hFC</td><td colspan="9">252 clocks</td></tr>
<tr><td></td><td colspan="4">8’hFE</td><td colspan="9">254 clocks</td></tr>
<tr><td>Restriction</td><td colspan="13">-</td></tr>
</table>

Source/VCOM/Gate Driving Timing Setting (D1h)

D1h	Display Timing Setting												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	1	1	0	1	0	0	0	1	D1h
1st parameter	1	#A	#B	X	0	EQ2[2]	EQ2[1]	EQ2[0]	0	EQ1[2]	EQ1[1]	EQ1[0]	XXh
2nd parameter	1	#A	#B	X	0	0	0	0	MCP[3]	MCP[2]	MCP[1]	MCP[0]	XXh
3rd parameter	1	#A	#B	X	0	0	0	0	NOW[3]	NOW[2]	NOW[1]	NOW[0]	XXh
4th parameter	1	#A	#B	X	0	0	0	0	SDT[3]	SDT[2]	SDT[1]	SDT[0]	XXh
5th parameter	1	#A	#B	X	0	0	SEQC[1]	SEQC[0]	0	SEQ[2]	SEQ[1]	SEQ[0]	XXh

Description

Write #A="1" #B="↑"
Read #A="↑" #B=" 1" & Insert dummy read

EQ2[2:0] / EQ1[2:0] : Sets equalization period.

EQ2[2:0]	**Equalization period**	**EQ1[2:0]**	**Equalization period**
3'h0	0 (display clock period)	3'h0	0 (display clock period)
3'h1	2	3'h1	2
3'h2	4	3'h2	4
3'h3	6	3'h3	6
3'h4	8	3'h4	8
3'h5	10	3'h5	10
3'h6	12	3'h6	12
3'h7	14	3'h7	14

MCP[3:0] : Sets the VCOM output timing by the number of internal clock from a reference point. The setting is enabled in display operation in synchronization with internal clock.

MCP[3:0]	**VCOM output position**	**MCP[3:0]**	**VCOM output position**
4'h0	0 (display clock period)	4'h8	16
4'h1	2	4'h9	18
4'h2	4	4'hA	20
4'h3	6	4'hB	22
4'h4	8	4'hC	24
4'h5	10	4'hD	26
4'h6	12	4'hE	28

<table>
<tr><td></td><td>4’h7</td><td>14</td><td>4’hF</td><td>30</td></tr>
<tr><td></td><td colspan="4">NOW[3:0] : Sets the non-overlap period of adjacent gate outputs. The setting is enabled in display operation in synchronization with internal clock.</td></tr>
<tr><td rowspan="28">Description</td><td>NOW[3:0]</td><td>Non-overlap period</td><td>NOW[3:0]</td><td>Non-overlap period</td></tr>
<tr><td>4’h0</td><td>0 (display clock period)</td><td>4’h8</td><td>16</td></tr>
<tr><td>4’h1</td><td>2</td><td>4’h9</td><td>18</td></tr>
<tr><td>4’h2</td><td>4</td><td>4’hA</td><td>20</td></tr>
<tr><td>4’h3</td><td>6</td><td>4’hB</td><td>22</td></tr>
<tr><td>4’h4</td><td>8</td><td>4’hC</td><td>24</td></tr>
<tr><td>4’h5</td><td>10</td><td>4’hD</td><td>26</td></tr>
<tr><td>4’h6</td><td>12</td><td>4’hE</td><td>28</td></tr>
<tr><td>4’h7</td><td>14</td><td>4’hF</td><td>30</td></tr>
<tr><td colspan="4">SDT[3:0] : Sets the source output timing by the number of internal clock from a reference point. The setting is enabled in display operation in synchronization with internal clock.</td></tr>
<tr><td>SDT[3:0]</td><td>Source output position</td><td>SDT[3:0]</td><td>Source output position</td></tr>
<tr><td>4’h0</td><td>0 (display clock period)</td><td>4’h8</td><td>16</td></tr>
<tr><td>4’h1</td><td>2</td><td>4’h9</td><td>18</td></tr>
<tr><td>4’h2</td><td>4</td><td>4’hA</td><td>20</td></tr>
<tr><td>4’h3</td><td>6</td><td>4’hB</td><td>22</td></tr>
<tr><td>4’h4</td><td>8</td><td>4’hC</td><td>24</td></tr>
<tr><td>4’h5</td><td>10</td><td>4’hD</td><td>26</td></tr>
<tr><td>4’h6</td><td>12</td><td>4’hE</td><td>28</td></tr>
<tr><td>4’h7</td><td>14</td><td>4’hF</td><td>30</td></tr>
<tr><td colspan="4">SEQC[1:0] : Sets Source equalization level</td></tr>
<tr><td colspan="2">SEQ[1:0]</td><td colspan="2">Source equalization level</td></tr>
<tr><td colspan="2">2’h0</td><td colspan="2">Normal operation</td></tr>
<tr><td colspan="2">2’h1</td><td colspan="2">GND</td></tr>
<tr><td colspan="2">2’h2</td><td colspan="2">VCI</td></tr>
<tr><td colspan="2">2’h3</td><td colspan="2">Hiz</td></tr>
<tr><td colspan="4">SEQ[2:0] : Sets Source equalization period.</td></tr>
<tr><td colspan="2">SEQ[2:0]</td><td colspan="2">Source equalization period</td></tr>
<tr><td colspan="2">3’h0</td><td colspan="2">0 (display clock period)</td></tr>
<tr><td colspan="2">3’h1</td><td colspan="2">2</td></tr>
<tr><td colspan="2">3’h2</td><td colspan="2">4</td></tr>
<tr><td colspan="2">3’h3</td><td colspan="2">6</td></tr>
<tr><td colspan="2">3’h4</td><td colspan="2">8</td></tr>
<tr><td colspan="2">3’h5</td><td colspan="2">10</td></tr>
<tr><td colspan="2">3’h6</td><td colspan="2">12</td></tr>
<tr><td colspan="2">3’h7</td><td colspan="2">14</td></tr>
<tr><td>Restriction</td><td colspan="4">-</td></tr>
</table>

Backlight Setting (D2h)

D2h	Backlight Setting												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	1	1	0	1	0	0	1	0	D2h
1st parameter	1	#A	#B	X	DBV[7]	DBV[6]	DBV[5]	DBV[4]	DBV[3]	DBV[2]	DBV[1]	DBV[0]	XXh
2nd parameter	1	#A	#B	X	0	0	BCTRL	0	DO	BL	BLONEN	BLON	XXh
3rd parameter	1	#A	#B	X	0	0	0	0	0	0	CABC[1]	CABC[0]	XXh
4th parameter	1	#A	#B	X	CMB[7]	CMB[6]	CMB[5]	CMB[4]	CMB[3]	CMB[2]	CMB[1]	CMB[0]	XXh
5th parameter	1	#A	#B	X	CDSP[3]	CDSP[2]	CDSP[1]	CDSP[0]	CDMP[3]	CDMP[2]	CDMP[1]	CDMP[0]	XXh
6th parameter	1	#A	#B	X	PWMP	0	0	0	0	0	FPWM[1]	FPWM[0]	
Description	**DBV[7:0] :** Sets. **BCTRL :** Sets **DO :** Sets **BL :** Sets **CABC[1:0] :** Sets **CMB[7:0] :** Sets												
Restriction	-												

Read Display Brightness Value (D3h)

D3h	Brightness Setting												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	1	1	0	1	0	0	1	1	D3h
1st parameter	1	#A	#B	X	DBV[7]	DBV[6]	DBV[5]	DBV[4]	DBV[3]	DBV[2]	DBV[1]	DBV[0]	XXh
Description	Read #A="↑" #B=" 1" & Insert dummy read **DBV[7:0]** : Get.												
Restriction	-												

Frame Rate Control (D4h)

<table>
<tr><td>D4h</td><td colspan="12">Frame Rate Control</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>DB[17:8]</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td><td>Hex</td></tr>
<tr><td>command</td><td>0</td><td>1</td><td>↑</td><td>X</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>D4h</td></tr>
<tr><td>1st parameter</td><td>1</td><td>#A</td><td>#B</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>OHZ</td><td>XXh</td></tr>
<tr><td>2nd parameter</td><td>1</td><td>#A</td><td>#B</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>FRS[2]</td><td>FRS[1]</td><td>FRS[0]</td><td>XXh</td></tr>
<tr><td>Description</td><td colspan="12">Write #A=”1” #B=”↑”
Read #A=”↑” #B=” 1” & Insert dummy read

OHZ: Set the test mode
OHZ = 0 – FMARK pin is normal output..
OHZ = 1 – FMARK pin is clock input for test.

FRS[2:0] : Set the frame rate when the internal resistor is used for oscillator circuit.
Sets the source output timing by the number of internal</td></tr>
<tr><td></td><td colspan="3">FRS[2:0]</td><td colspan="3">Ratio of Frequency</td><td colspan="3">FRS[2:0]</td><td colspan="3">Ratio of Frequency</td></tr>
<tr><td></td><td colspan="3">3’h0</td><td colspan="3">x 0.50</td><td colspan="3">3’h4</td><td colspan="3">x 0.91</td></tr>
<tr><td></td><td colspan="3">3’h1</td><td colspan="3">x 0.61</td><td colspan="3">3’h5</td><td colspan="3">x 1.00 (default)</td></tr>
<tr><td></td><td colspan="3">3’h2</td><td colspan="3">x 0.71</td><td colspan="3">3’h6</td><td colspan="3">x 1.09</td></tr>
<tr><td></td><td colspan="3">3’h3</td><td colspan="3">x 0.81</td><td colspan="3">3’h7</td><td colspan="3">x 1.17</td></tr>
<tr><td>Restriction</td><td colspan="12">-</td></tr>
</table>

Gate Control (D5h)

D5h	Gate Control												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	1	1	0	1	0	1	0	1	D5h
1st parameter	1	#A	#B	X	0	0	0	ALL OFF	0	0	0	ALL ON	XXh
Description	Write #A="1" #B="↑" Read #A="↑" #B=" 1" & Insert dummy read This setting for gate test **ALLON** : All gate outputs are High. **ALLOFF** : All gate outputs are Low.												
Restriction	-												

VREF Control (D6h)

D6h	Vref Control												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	1	1	0	1	0	1	1	0	D6h
1st parameter	1	#A	#B	X	0	0	0	VREFT	0	0	0	VREFEN	XXh
2nd parameter	1	#A	#B	X	0	0	0	VREFVR	0	0	0	VREFDD	
Description	Write #A="1" #B="↑" Read #A="↑" #B=" 1" & Insert dummy read This setting for Vt Reference **VREFT** : Set. **VREFEN** : Set. **VREFVR** : Set. **VREFDD** : Set.												
Restriction	-												

Test Control 1(F0h)

F0h	Test Control 1												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	1	1	1	1	0	0	0	0	F0h
1st parameter	1	#A	#B	X	0	0	0	TDFN	0	0	TDLY[1]	TDLY[0]	XXh
2nd parameter	1	#A	#B	X	0	0	0	TOSC	0	0	TVCOM[1]	TVCOM[0]	XXh
3rd parameter	1	#A	#B	X	0	0	0	REGULPD	0	TSAP	0	TSHZ	XXh
4th parameter	1	#A	#B	X	0	0	0	TPATE	0	TPAT[2]	TPAT[1]	TPAT[0]	XXh
5th parameter	1	#A	#B	X	0	0	0	TSD_EN	0	0	TSD[1]	TSD[0]	XXh
6th parameter	1	#A	#B	X	0	LINEINV	0	TVON	0	HaltVreg	0	MultiVCOM	XXh
7th parameter	1	#A	#B	X	STBN	0	RDSM[1]	RDSM[0]	0	0	WRPW[1]	WRPW[0]	XXh
8th parameter	1	#A	#B	X	0	D_SHIZ	H_HIZ	L_HIZ	SBC	S_SCV	SWP	0	XXh

Description	Write #A=”1” #B=”↑” Read #A=”↑” #B=” 1” & Insert dummy read **TDFN** : **TDLY[1:0]** : **TOSC :** **TVCOM[1:0] :** **REGULPD :** **TSAP :** **TSHZ :** **TPATE :** **TPAT[2:0]:** **TSD_EN :** **TSD[1:0] :** **LINEINV :** **TVON :** **HaltVreg :** **MiltiVCOM :** **STBN :** **RDSM[1:0] :** **WRPW[1:0] :** **D_SHIZ :** **H_HIZ :** **L_HIZ :** **SBC :** **S_SCV :** **SWP :**
Restriction	-

Test Control 2(F1h)

F1h	Test Control 2												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	1	1	1	1	0	0	0	1	F1h
1st parameter	1	#A	#B	X	0	0	0	0	0	0	0	AUTO	XXh
2nd parameter	1	#A	#B	X	0	0	0	0	MEN4	MEN3	MEN2	MEN1	XXh
Description	Write #A="1" #B="↑" Read #A="↑" #B=" 1" & Insert dummy read This register for manual Power On sequence. **AUTO** : select Auto or Manual Power On sequence 0 – manual power on sequence 1 – Auto power on sequence **MEN1** : AVDD enable **MEN2** : VGH enable **MEN3** : VGL enable **MEN4** : VCL enable												
Restriction	-												

EPROM Control Setting 1(F2h)

F2h	EPROM Control Setting 1												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	1	1	1	1	0	0	1	0	F2h
1st parameter	1	#A	#B	X	PTM[1]	PTM[0]	0	0	PRD	PWE	VPP	PPROG	XXh
2nd parameter					APRG	0	0	0	0	0	PA[1]	PA[0]	
3rd parameter	1	#A	#B	X	PDIN[7]	PDIN[6]	PDIN[5]	PDIN[4]	PDIN[3]	PDIN[2]	PDIN[1]	PDIN[0]	XXh

Description

Write #A="1" #B="↑"
Read #A="↑" #B=" 1" & Insert dummy read

EPROM programming control. See "EPROM Control" section.

PTM[1:0] : Pins for enabling test mode

PRD : Pin for power-on rest.

PWE : Write enable.

VPP : Power switch control for the VPP pin of the embedded EPROM. When VPP = "1", t the internal VPP is set to 7.5V; otherwise it is set to 1.8V.

PPROG : Program mode enable.

APRG : Select the methoe of write operation
If APRG='1', write address is PA.
Else APRG='0', write address is auto select address.

PA[1:0] : address input. This selects one of four banks of the EPROM.

PA[1:0]	**Write Data Input**	**Write OTP Cell**
2'h0	PDIN[6:0]	Cell[6:0]
2'h1	PDIN[6:0]	Cell[14:8]
2'h2	PDIN[6:0]	Cell[22:16]
2'h3	PDIN[6:0]	Cell[30:24]

PDIN[7:0] : Data input. This corresponds to VCM[6:0] bits of B8h.

Restriction -

EPROM Control Setting 2(F3h)

<table>
<tr><td>F3h</td><td colspan="13">EPROM Control Setting 2</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>DB[17:8]</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td><td>Hex</td></tr>
<tr><td>command</td><td>0</td><td>1</td><td>↑</td><td>X</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>F3h</td></tr>
<tr><td>1st parameter</td><td>1</td><td>#A</td><td>#B</td><td>X</td><td>VCMSEL[1]</td><td>VCMSEL[0]</td><td>MSEL[1]</td><td>MSEL[0]</td><td>0</td><td>0</td><td>RA[1]</td><td>RA[0]</td><td>XXh</td></tr>
<tr><td>Description</td><td colspan="13">Write #A=”1” #B=”↑”
Read #A=”↑” #B=” 1” & Insert dummy read

VCMSEL[1:0] : With VCMSEL pin, sets VcomH level from either the register B8h or the EPROM

VCMSEL[1:0] | VcomH Level adjustment
2’h0 | VCM[6:0] of the register B8h
2’h1 | EPROM data at first if EPROM has data. Otherwise,VCM[6:0] of the register B8h
2’h2, 2’h3 | EPROM data selected by RA[1:0]

MSEL[1:0] : Select Eprom block

MSEL[1:0] | Eprom Block
2’h0 | VCOM eprom block
2’h1 | Device ID eprom block
2’h2 | Vt Rerecence eprom block
2’h3 | All disable

RA[1:0] : Read address input. This selects one of four banks of the EPROM</td></tr>
<tr><td>Restriction</td><td colspan="13">-</td></tr>
</table>

EPROM Control Setting 3(F4h)

F4h	EPROM Control Setting 3												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	1	1	1	1	0	1	0	0	F4h
Description	Write #A="1" #B="↑" Read #A="↑" #B=" 1" & Insert dummy read This command enable auto eprom write sequence If OTP_WP = 'hA5 (Eprom control setting 4, F5) and Eprom control setting (F4) enter, VCM and DID eprom block auto write. For detail, See "Eprom Auto Write sequence".												
Restriction	-												

EPROM Control Setting 4(F5h)

F5h	EPROM Control Setting 4												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	1	1	1	1	0	1	0	1	F5h
1st parameter	1	#A	#B	X	OTP_WP[7]	OTP_WP[6]	OTP_WP[5]	OTP_WP[4]	OTP_WP[3]	OTP_WP[2]	OTP_WP[1]	OTP_WP[0]	XXh
Description	Write #A="1" #B="↑" Read #A="↑" #B=" 1" & Insert dummy read **OTP_WP[7:0] :** This command is for otp auto write protection. When eprom control setting 3 enter : OTP_WP[7:0] = 'hA5 , Auto write start : OTP_WP[7:0] ≠ 'hA5 , no operation For detail, See "Eprom Auto Write sequence".												
Restriction	-												

EPROM Control Setting 5 (F6h)

F6h	EPROM Control Setting 5												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	1	1	1	1	0	1	1	0	F6h
1st parameter	1	#A	#B	X	OTP_WD [7]	OTP_WD [6]	OTP_WD [5]	OTP_WD [4]	OTP_WD [3]	OTP_WD [2]	OTP_WD [1]	OTP_WD [0]	XXh
2nd parameter	1	#A	#B	X	OTP_WD [15]	OTP_WD [14]	OTP_WD [13]	OTP_WD [12]	OTP_WD [11]	OTP_WD [10]	OTP_WD [9]	OTP_WD [8]	XXh
3rd parameter	1	#A	#B	X	OTP_WD [23]	OTP_WD [22]	OTP_WD [21]	OTP_WD [20]	OTP_WD [19]	OTP_WD [18]	OTP_WD [17]	OTP_WD [16]	XXh
4th parameter	1	#A	#B	X	OTP_WD [31]	OTP_WD [30]	OTP_WD [29]	OTP_WD [28]	OTP_WD [27]	OTP_WD [26]	OTP_WD [25]	OTP_WD [24]	XXh
Description	Write #A="1" #B="↑" Read #A="↑" #B=" 1" & Insert dummy read **OTP_WD[31:0] :** This command is Auto eprom write data. For detail, See "Eprom Auto Write sequence".												
Restriction	-												

EPROM Control Setting 6 (F7h)

F7h	EPROM Control Setting 6												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	1	1	1	1	0	1	1	1	F7h
1st parameter	1	#A	#B	X	0	0	0	0	0	0	0	OTP_DSEL	XXh
Description	Write #A="1" #B="↑" Read #A="↑" #B=" 1" & Insert dummy read **OTP_DSEL :** This command select Auto eprom write data When VCM block is enable.												
	OTP_DSEL	**Eprom VCM block auto write data**											
	0	OTP_WD[7:0] (eprom control setting 5, F6h)											
	1	{1'b0, VCM[6:0]} (power setting, BBh)											
Restriction	-												

EPROM Control Setting 7 (F8h)

F8h	EPROM Control Setting 7												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	1	1	1	1	1	0	0	0	F8h
1st parameter	1	#A	#B	X	0	0	0	TRSEL	0	0	0	RSEL	XXh
2nd parameter	1	#A	#B	X	0	0	0	REFTR[4]	REFTR[3]	REFTR[2]	REFTR[1]	REFTR[0]	XXh
3rd parameter	1	#A	#B	X	0	REFRS[6]	REFRS[5]	REFRS[4]	REFRS[3]	REFRS[2]	REFRS[1]	REFRS[0]	XXh

Description

Write #A="1" #B="↑"
Read #A="↑" #B=" 1" & Insert dummy read

This command select REFTR, REFRS value.

TRSEL : REFTR value select
RSEL : REFRS value select

REFTR[4:0] : Set
REFS[6:0] : Set

TRSEL	**REFTR value**
0	REFTR (eprom control setting 7, F8h)
1	If eprom VREF block was written, eprom data Else REFTR (eprom control setting 7, F8h)

RSEL	**REFRS value**
0	REFRS (eprom control setting 7, F8h)
1	If eprom VREF block was written, eprom data Else REFRS (eprom control setting 7, F8h)

Restriction -

EPROM Data Read 1(F9h)

F9h	EPROM Data Read 1												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	1	1	1	1	1	0	0	1	F9h
1st parameter	1	↑	1	X	PDOUT[7]	PDOUT[6]	PDOUT[5]	PDOUT[4]	PDOUT[3]	PDOUT[2]	PDOUT[1]	PDOUT[0]	XXh
Description	EPROM programming control. See “EPROM Control” section. **PDOUT[7:0] :** EPROM Read Data output.												
Restriction	-												

EPROM Data Read (FAh)

FAh	EPROM Data Read 2												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	1	1	1	1	1	0	1	0	FAh
1st parameter	1	↑	1	X	DID[7]	DID[6]	DID[5]	DID[4]	DID[3]	DID[2]	DID[1]	DID[0]	XXh
2nd prarmeter	1	↑	1	X	DID[15]	DID[14]	DID[13]	DID[12]	DID[11]	DID[10]	DID[9]	DID[8]	XXh
3rd parameter	1	↑	1	X	DID[23]	DID[22]	DID[21]	DID[20]	DID[19]	DID[18]	DID[17]	DID[16]	XXh
4th parameter	1	↑	1	X	DID[31]	DID[30]	DID[29]	DID[28]	DID[27]	DID[26]	DID[25]	DID[24]	XXh
Description	EPROM programming control. See “EPROM Control” section. **DID[31:0] :** EPROM Read Data output.												
Restriction	-												

EPROM Data Read (FBh)

FBh	EPROM Data Read 3												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
command	0	1	↑	X	1	1	1	1	1	0	1	1	FBh
1st parameter	1	↑	1	X	0	0	0	REFTR_OUT[4]	REFTR_OUT[3]	REFTR_OUT[2]	REFTR_OUT[1]	REFTR_OUT[0]	XXh
2nd prarmeter	1	↑	1	X	0	REFRS_OUT[6]	REFRS_OUT[5]	REFRS_OUT[4]	REFRS_OUT[3]	REFRS_OUT[2]	REFRS_OUT[1]	REFRS_OUT[0]	XXh
Description	EPROM programming control. See “EPROM Control” section. **REFTR_OUT[4:0] :** EPROM Read Data output. **REFRS_OUT[6:0] :** EPROM Read Data output.												
Restriction	-												

State Transition Diagram

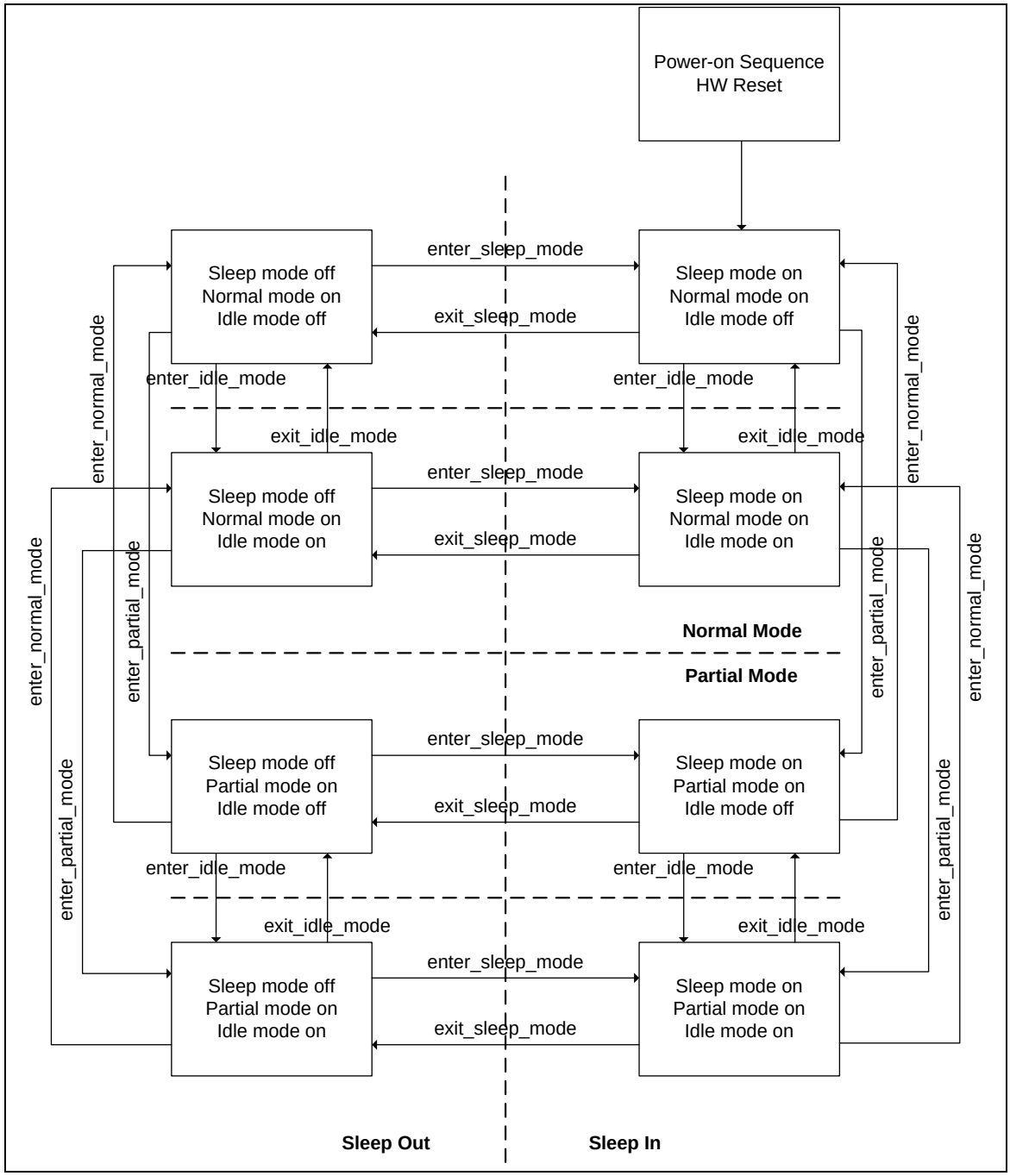


Figure 46

Reset Function

The LG4538 is initialized with a RESET input. During a reset period, the LG4538 is in a busy state and neither instruction nor access to the GRAM data from the MPU is accepted. The LG4538's internal power supply circuit unit is initialized also with a RESET input. The RESET period must be secured for at least 1ms. In case of power-on reset, wait until the RC oscillation frequency stabilizes (for 1 ms). During this period, neither access to the internal GRAM nor initial setting of instruction bits is accepted.

1. Initial state of instruction bits (default)
See the instruction list. The default value is shown in the parenthesis of each instruction bit cell.

2. RAM Data initialization
The RAM data is not automatically initialized with a RESET input and must be initialized by software in a display-off period .

3. Output pin initial state *See note

1. LCD driver S1~S720	: GND
G1~G320	: VGL (= GND)
2. VCOM	: GND
3. VCOMR	: Hi-Z
4. VCOMH	: Hi-Z
5. VCOML	: GND
6. GVDD	: Hi-Z
7. VCIOUT	: VCI
8. VLOUT1	: VCI
9. VLOUT2	: AVDD (= VCI)
10. VLOUT3	: GND
11. VLOUT4	: GND
12. VDD	: VDD
13. FMARK	: GND
14. SDO	: GND
15. Oscillator	: Oscillate

4. Initial state of input/output pins*See note

1. C11+	: VCI1
2. C11-	: GND
3. C12+	: VCI1
4. C12-	: GND
5. C13+	: VCI1
6. C13-	: GND
7. C21+	: AVDD (= VCI)
8. C21-	: GND
9. C22+	: AVDD (= VCI)
10. C22-	: GND

Note: The above-mentioned initial states of output and input pins are the ones when the LG4538's power supply circuit is connected as exemplified in "Wiring example".

5. Note on Reset function

(1) When a RESET input is entered into the LG4538 while it is in deep standby mode, the LG4538 starts up the inside logic regulator and makes a transition to the initial state. During this period, the interface pins may be under an unstable condition. For this reason, do not enter a RESET input in deep standby mode.

(2) When transferring instruction using either two or three transfer mode via 8-/9-/16-bit

interface, make sure to execute data transfer synchronization after executing a reset operation.

Frame Memory

Arrangement

The frame memory stores display pixels and consists of 1,382,400bits (240 x 320 x 18).

Address Mapping from Memory to Display

Normal Display On or Partial Mode On

In this mode, a content of the frame memory within an area where column pointer is 00h to EFh and page pointer is 00h to 13Fh is displayed.

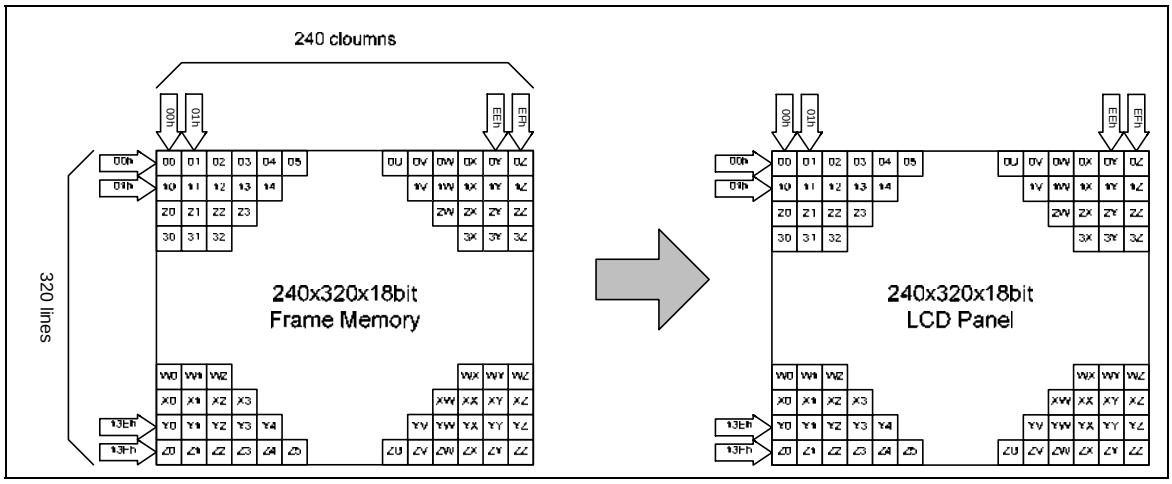


Figure 47

Host Processor to Memory Write/Read Direction

The data stream from host processor is as follows.

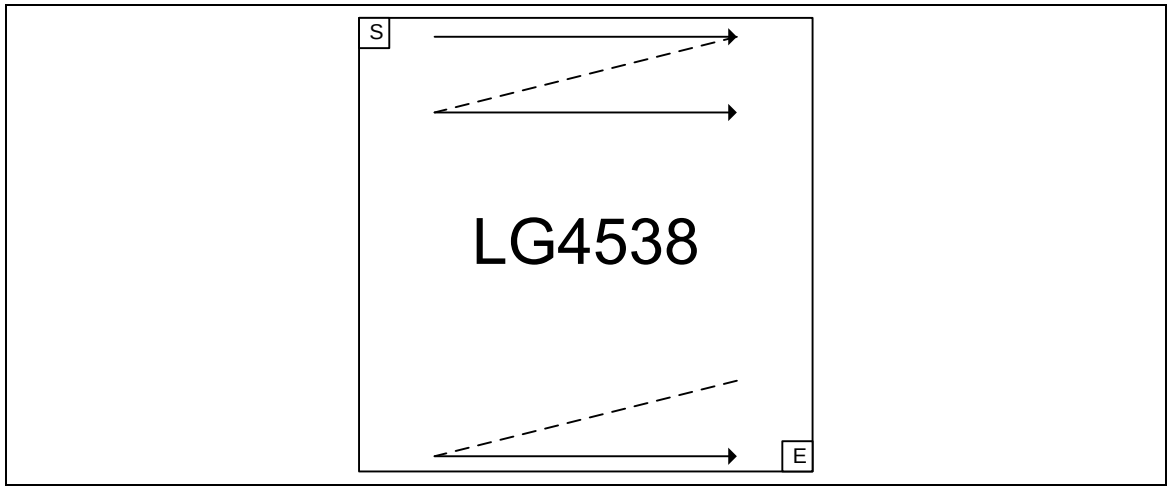


Figure 48

The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by “set_address_mode (36h)” command Bits B5, B6, B7 as described below.

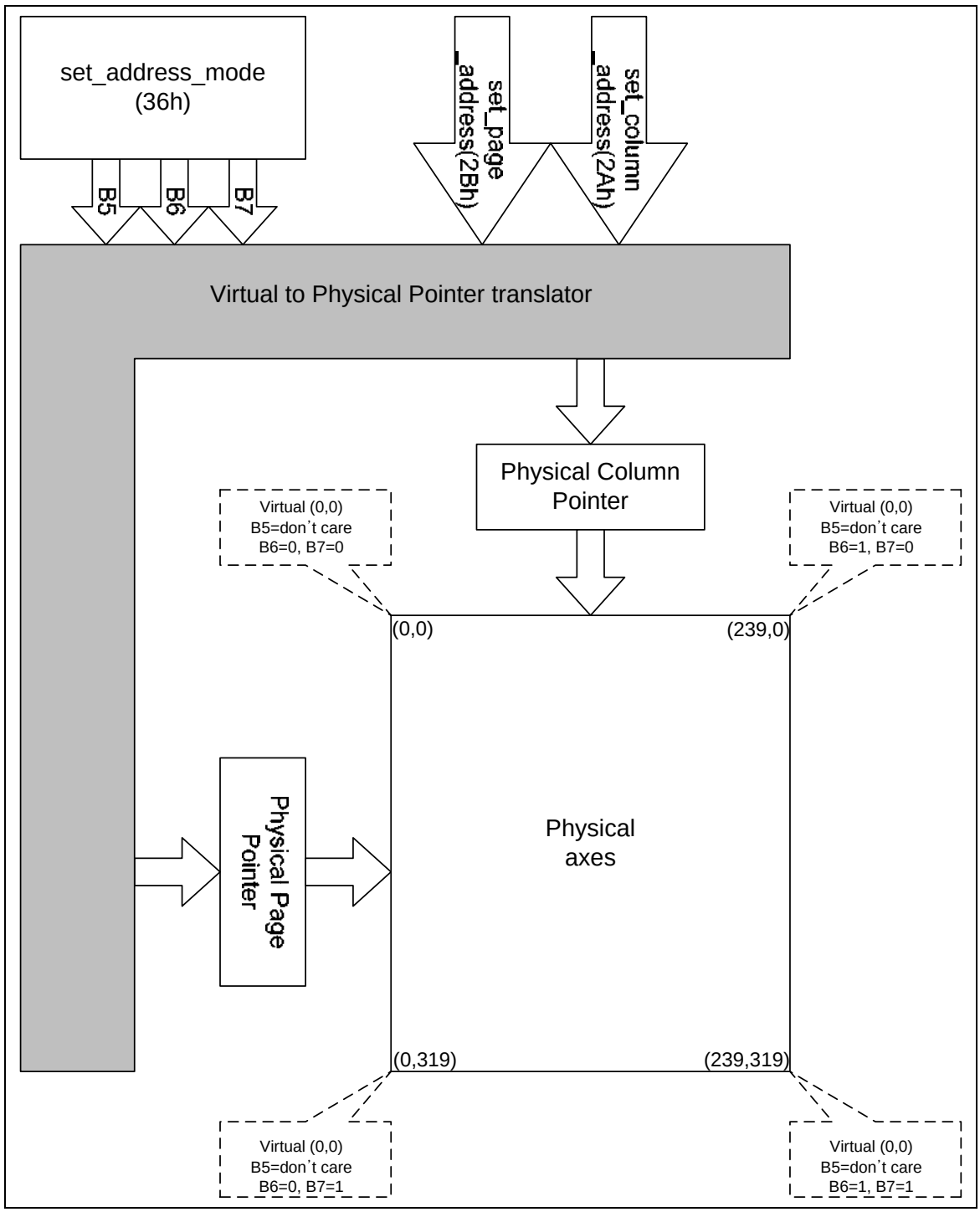


Figure 49

Table 19

B5	B6	B7	Column Address	Page Address
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (319-Physical Page Pointer)
0	1	0	Direct to (239-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (239-Physical Column Pointer)	Direct to (319-Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (319-Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (239-Physical Column Pointer)
1	1	1	Direct to (319-Physical Page Pointer)	Direct to (239-Physical Column Pointer)

For each image orientation, the controls on the column and page counters apply as below.

Note: Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by set_address_mode (36h) bits B7, B6 and B5. The write order for each pixel unit is as follows.

Table 20

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

Table 21

Codition	Column Counter	Page Counter	Notes
When write_memory_start (2Ch) /read_memory_start (2Eh) command is accepted.	Return to “Start Column”	Return to “Start Page”	
Complete Pixel Read/Write action	Increment by 1	No change	
The Column counter value is larger than that of “End column.”	Return to “Start Column”	Increment by 1	
The Column counter value is larger than that of “End column” and the Page counter value is larger than that of “End page”.	Stop	Stop	Entry Mode (B3h) WEMODE = 0
	Return to “Start Column”	Return to “Start Page”	Entry Mode (B3h) WEMODE = 1

One pixel unit represents 1 column and 1 page counter value on the Frame Memory. See the next page for the resultant image for each orientation setting.

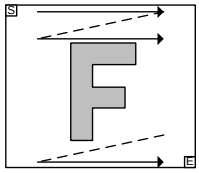
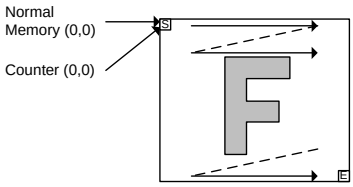
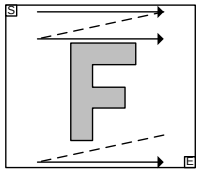
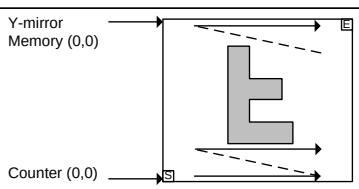
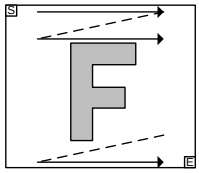
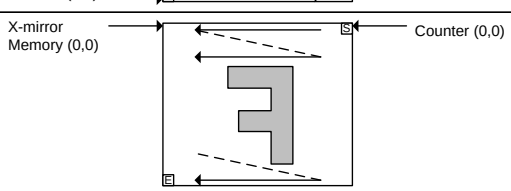
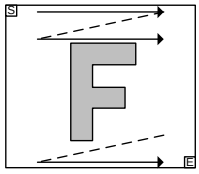
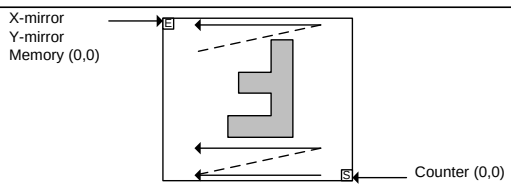
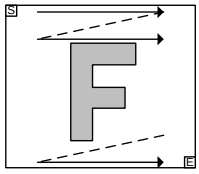
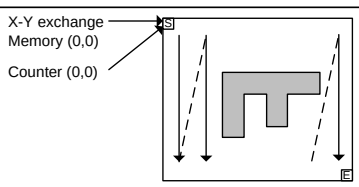
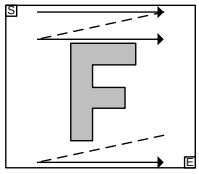
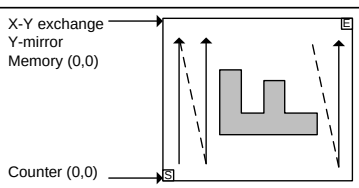
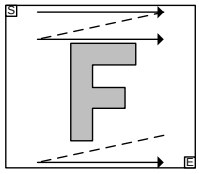
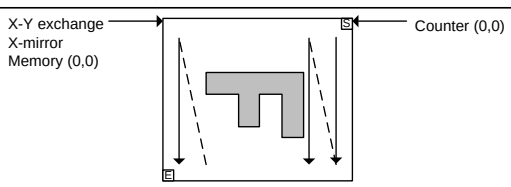
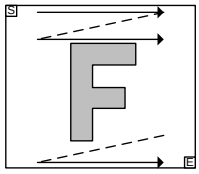
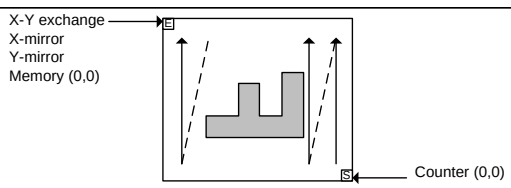
Display Data Direction	B5	B6	B7	Image In the Host	Image in Frame Memory
Normal	0	0	0		
Y-mirror	0	0	1		
X-mirror	0	1	0		
X-mirror Y-mirror	0	1	1		
X-Y exchange	1	0	0		
X-Y exchange Y-mirror	1	0	1		
X-Y exchange X-mirror	1	1	0		
X-Y exchange X-mirror Y-mirror	1	1	1		

Figure 50

Vertical Scroll Display Mode

The vertical scrolling display is specified by set_scroll_area instruction (33h) and set_scroll_start instruction (37h).

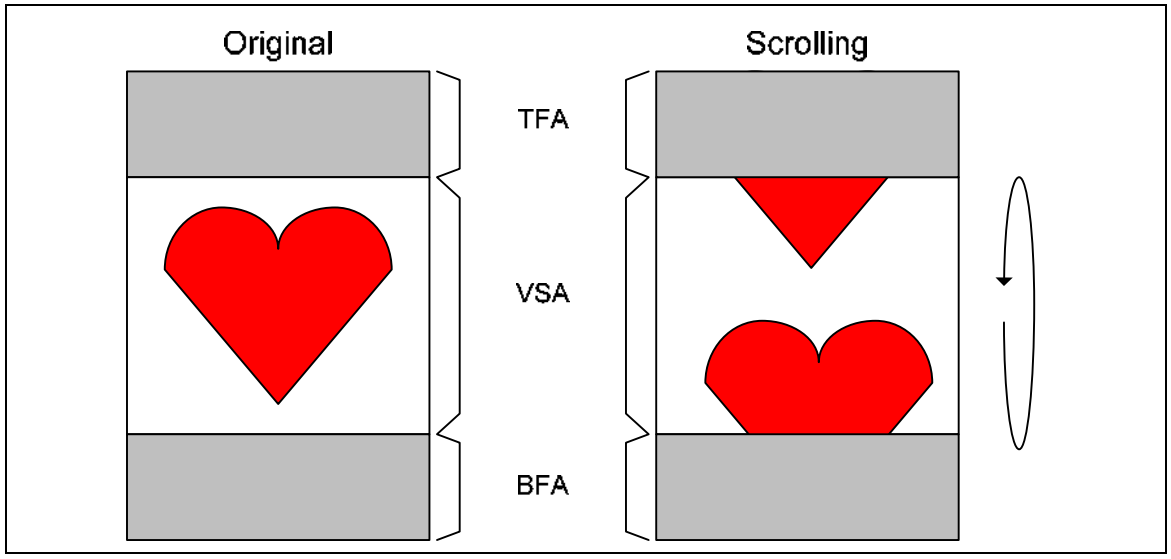


Figure 51 Vertical Scrolling

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA)=320. In this case, scrolling is applied as shown below.

Example (1) TFA=’2d’, VSA=’320d’, BFA=’0d’, VSP=’3d’ when set_address_mode B4=0

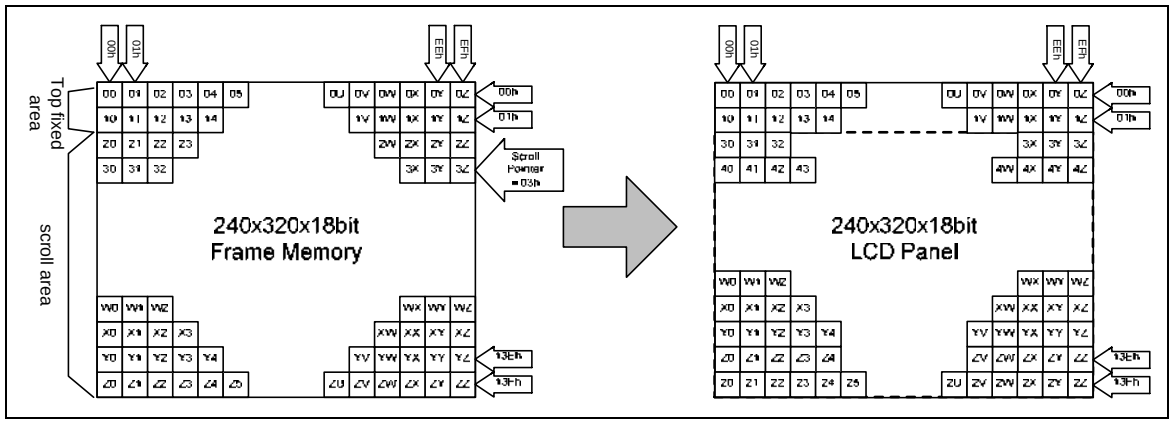


Figure 52

Example (2) TFA=’2d’, VSA=’316d’, BFA=’2d’, VSP=’3d’ when set_address_mode B4=0

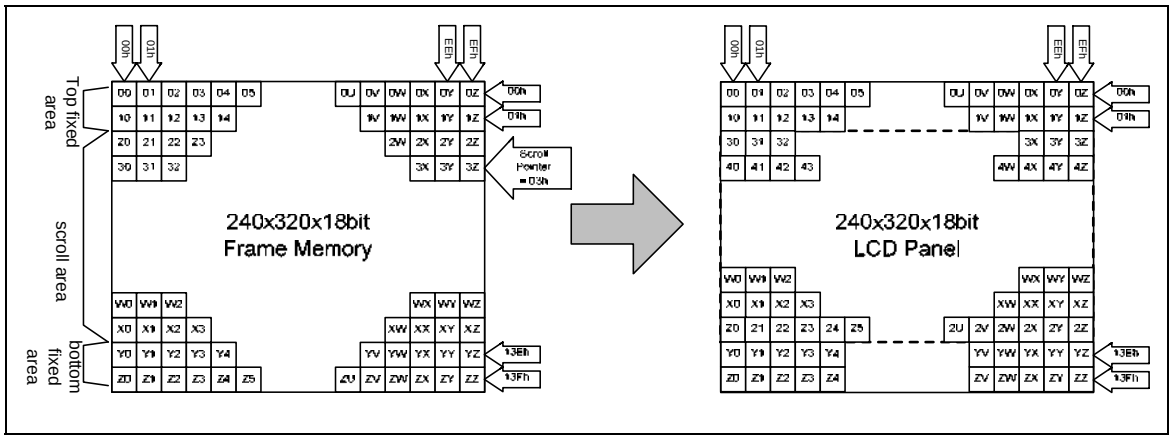


Figure 53

Example (3) TFA=’2d’, VSA=’316d’, BFA=’2d’, VSP=’5d’ when set_address_mode B4=0

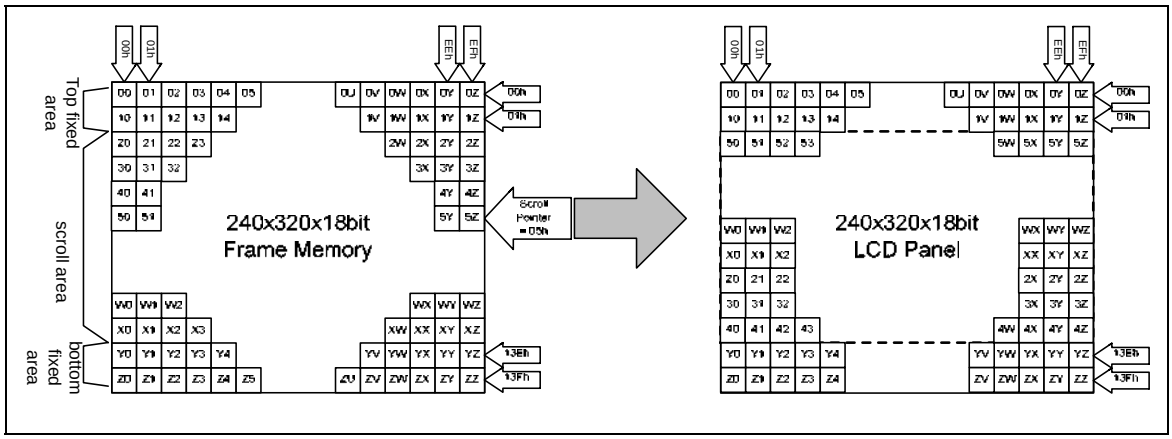


Figure 54

Dynamic Backlight Control Function

The LG4538 supports BLC (backlight control) function to control brightness of backlight and to process image dynamically. This function enables to reduce backlight power and minimize the effect of reduced power on the display image.

The display image is dynamically controlled by BLC function. The availability of this function ranges from moving picture such as TV image to still picture such as menu. The histogram of display data is analyzed by BLC function, according to the brightness range of backlight set by parameters. The brightness of backlight and image processing coefficient are calculated so that image data is optimized. Backlight power is reduced without changing display image.

TE Pin Output Signal

Tearing Effect Line signal can be output from TE pin as frame memory data transfer synchronous signals. TE signal is trigger for frame memory write operation to enable data transfer in synchronization with the scanning operation. Tearing Effect Output signal is turned on/off by set_tear_off (34h) and set_tear_on (35h) commands.

Table 22

TEON(35h)	TEM(35h's 1st parameter)	TE Pin Output
0	*	GND
1	0	TE (Mode 1)
1	1	TE (Mode 2)

The mode of TE signal is defined by D0 parameter (TEM) of set_tear_on (35h) command.

set_tear_on command (35h)

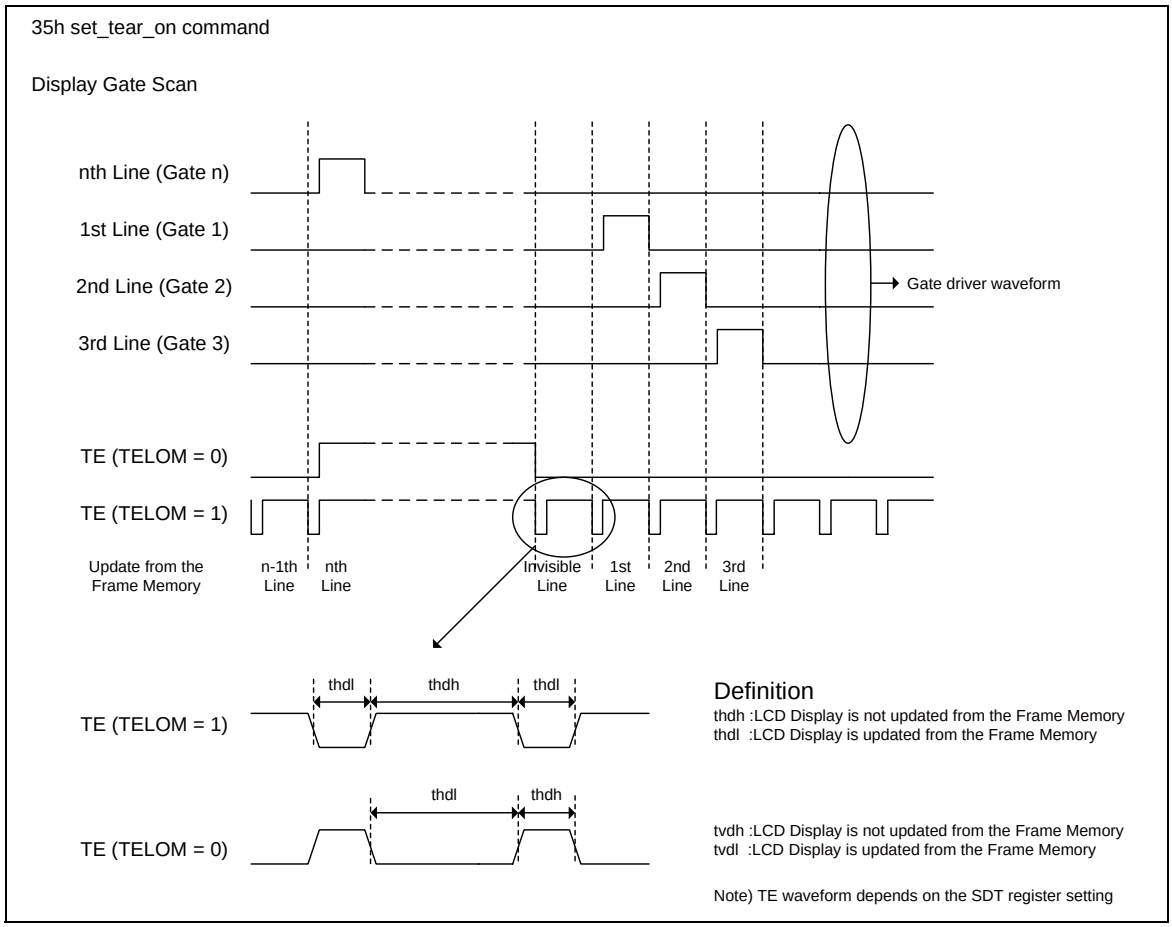
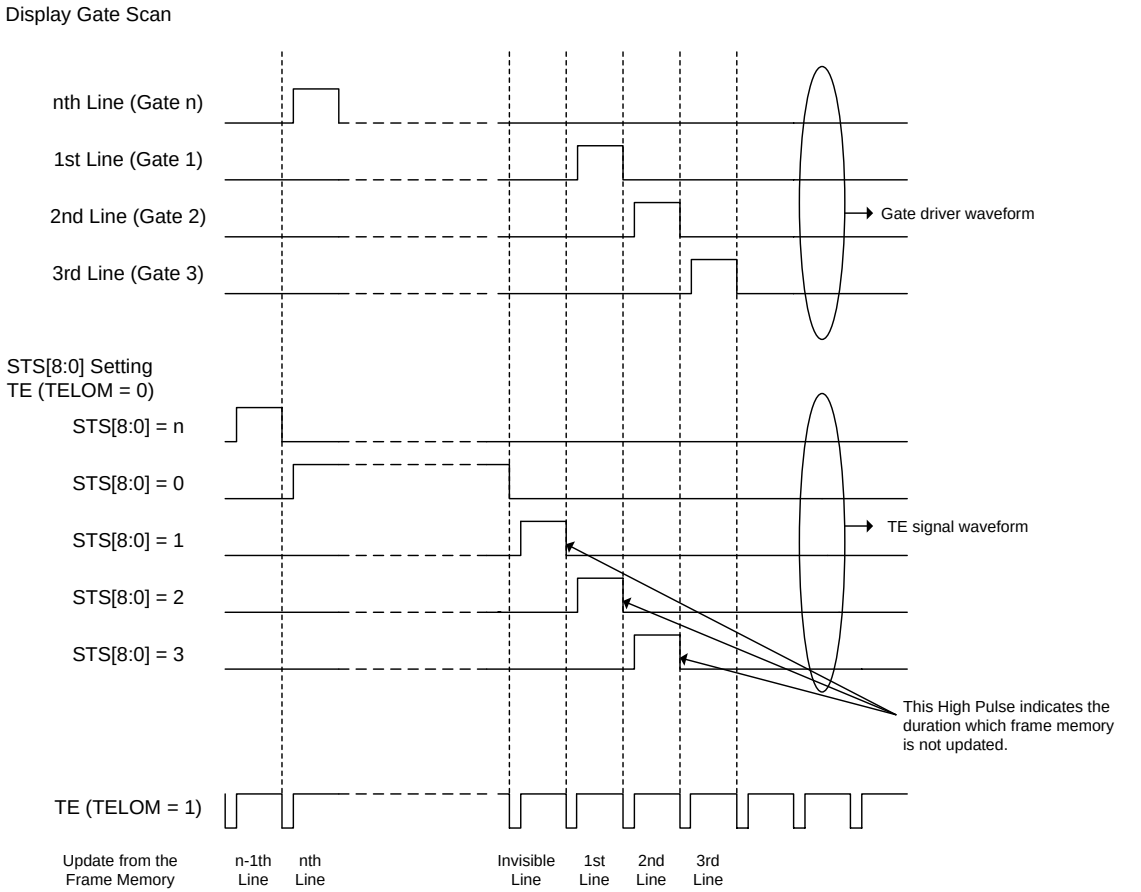


Figure 55

set_tear_scanline command (44h)



When STS[8:0] = 0, the waveform of TE is same as the one when 35h TELOM = 0.
When STS[8:0] is not equal 0, TE signal is shown above.

Restrictions
STA[8:0] <= (Number of lines (NL bits)) + 1

Figure 56

Display-Synchronous Data Transfer Using TE signal

The LG4538 enables data transfer in synchronization with the display scan by writing data to the internal frame memory using the TE signal as the trigger.

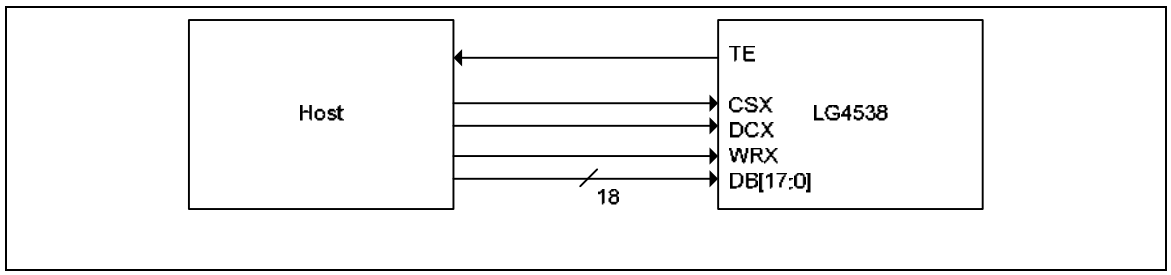


Figure 57 Interface Example for Display-Synchronous Data Transfer

By writing data to the internal Frame Memory at faster than calculated minimum speed, it becomes possible to rewrite the video image data without flickering the display and display video image via system interface. The display data is written in the Frame Memory so that the LG4538 rewrites the data only within the video image area and minimize the number of data transfer required to display video image.

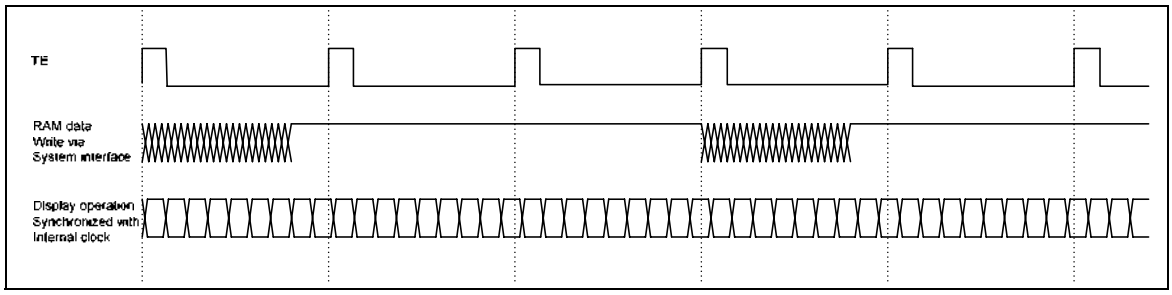


Figure 58 Video Image Data Write with TE

When transferring data using TE as the trigger, there are restrictions in setting the minimum Frame Memory data write speed and the minimum internal clock frequency, which must be more than the values calculated from the following formulas, respectively.

Internal clock frequency (fosc) [Hz]
= FrameFrequency x (DisplayLines(NL) + FrontPorch(FP) + BackPorch(BP)) x 64(clocks) x variance

$$RAMWriteSpeed > \frac{240 \times DisplayLines\ (NL)}{(\ (FP) + (BP) + DisplayLines\ (NL) - margins) \times DivisionRatio[DIV]\ \ Clocksper\ 1H[RTN] \times \frac{1}{fosc}}$$

Note: When frame memory write operation is not started right after the rising edge of TE, the time from the rising edge of TE until the start of frame memory write operation must also be taken into account.

An example of calculating the minimum frame memory writing speed and internal clock frequency for writing data in synchronization with display operation.

[Example]

Display size	240 RGB × 320 lines
Display lines	320 lines

Back/front porch 8/8 lines (BP = 8'h8/ FP = 8'h8)
set_tear_scanline (TEL) The end line of the display: 320th line
Frame frequency 60 Hz
Internal operation clock 3.25MHz x 1.07 = 3.48MHz
Division ratio of display operation clock 1/1
Clocks in 1 line period 120 clocks

Note: This example includes variances attributed to LSI production process and room temperature. Other possible causes of variances, such as voltage change, are not considered in this example. It is necessary to include a margin for these factors.

$$\textit{Frame memory Write speed(min.)} > \frac{240 \times 320}{(8 + 8 + 320 - 2)\ \textit{lines} \times 1 \times 120 \times \frac{1}{3480}} = 6.75\ MHz$$

Notes:
1. In this example, it is assumed that the LG4538 starts writing data in the frame memory on the rising edge of TE.
2. There must be at least a margin of 2 lines between the line to which the LG4538 has just written data and the line where the display operation on the LCD is performed.
3. TE signal may be set on any line.

In this example, the frame memory write operation at a speed of 6.75 MHz or more, which starts on the rising edge of TE, guarantees the completion of data write operation in a certain line address before the LG4538 starts the display operation of the data written in that line and can write video image data without causing flicker on the display.

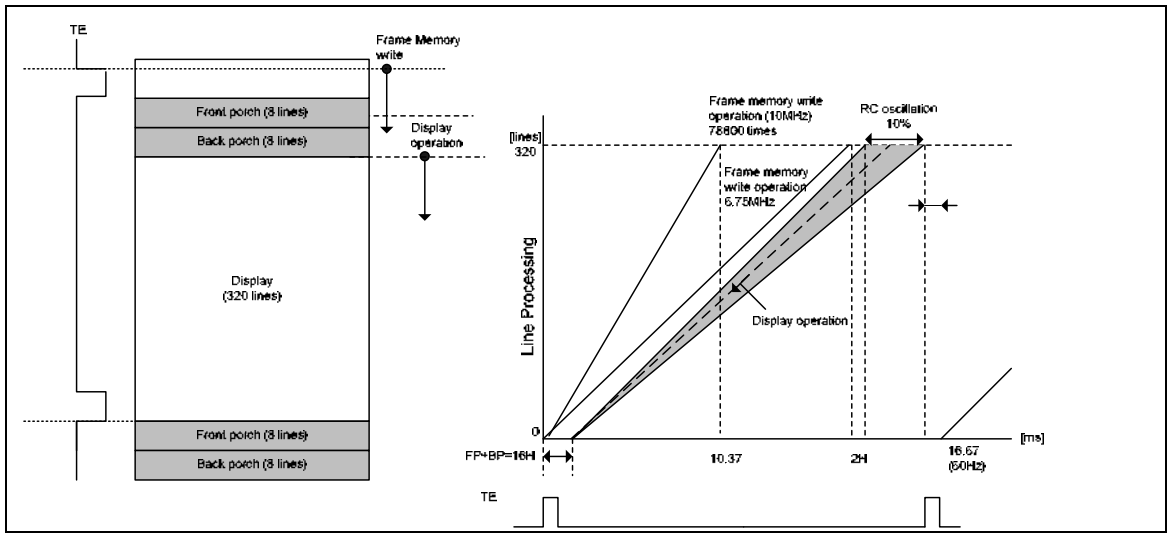


Figure 59

Scan Mode Setting

The LG4538 allows for changing the gate-line/gate driver assignment and the shift direction of gate line scan in the following 4 different ways by combination of SM and GS bit settings. These combinations allow various connections between the LG4538 and the LCD panel.

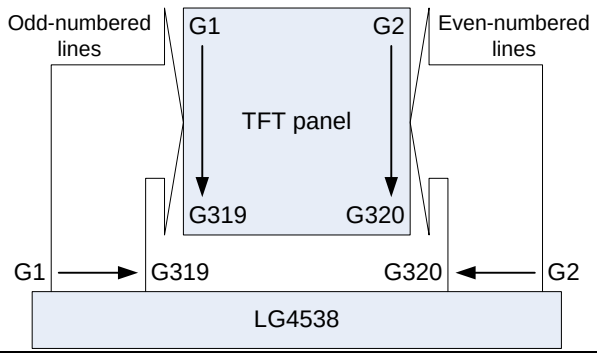
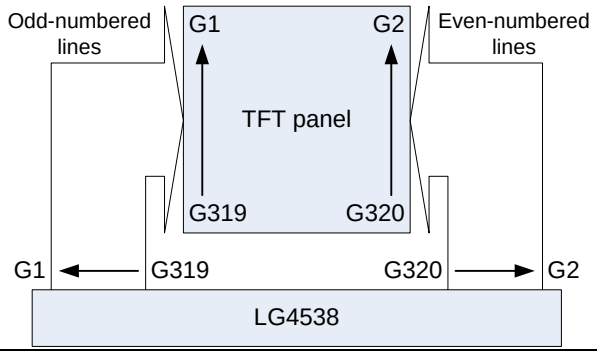
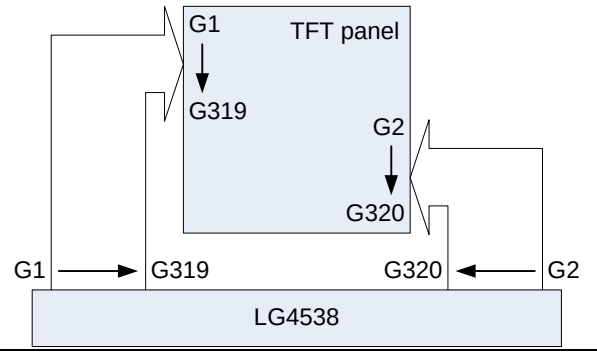
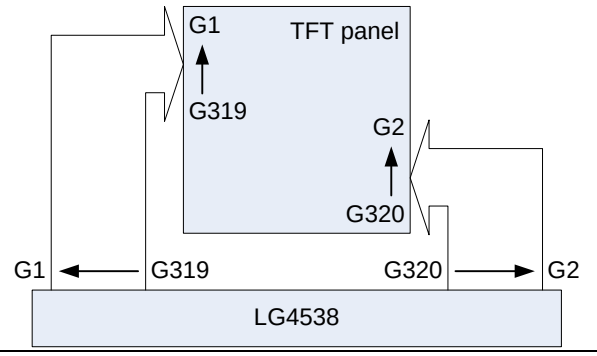
SM	GS	Scan direction	
0	0		G1, G2, G3, G4, …, G318, G319, G320
0	1		G320, G319, G318, …, G4, G3, G2, G1
1	0		G1, G3, G5, …, G317, G319, G2, G4, G6, …, G318, G320
1	1		G320, G318, G316, …, G6, G4, G2, G319, G317, G315, …, G5, G3, G1

Figure 60

Line Inversion AC Drive

The LG4538, in addition to the frame-inversion liquid crystal AC drive, supports the n-line inversion AC drive, in which the polarity of liquid crystal is inverted in units of n lines, where n takes a number from 1 to 64. The quality of display will be improved by using n-line inversion AC drive.
In determining n (the value set with the NW bits +1), which represents the number of lines that determines the timing of liquid crystal polarity inversion, check the quality of display on the liquid crystal panel in use. Note that setting a smaller number of lines will raise the frequency of liquid crystal polarity inversion and increase charging/discharging current on liquid crystal cells .

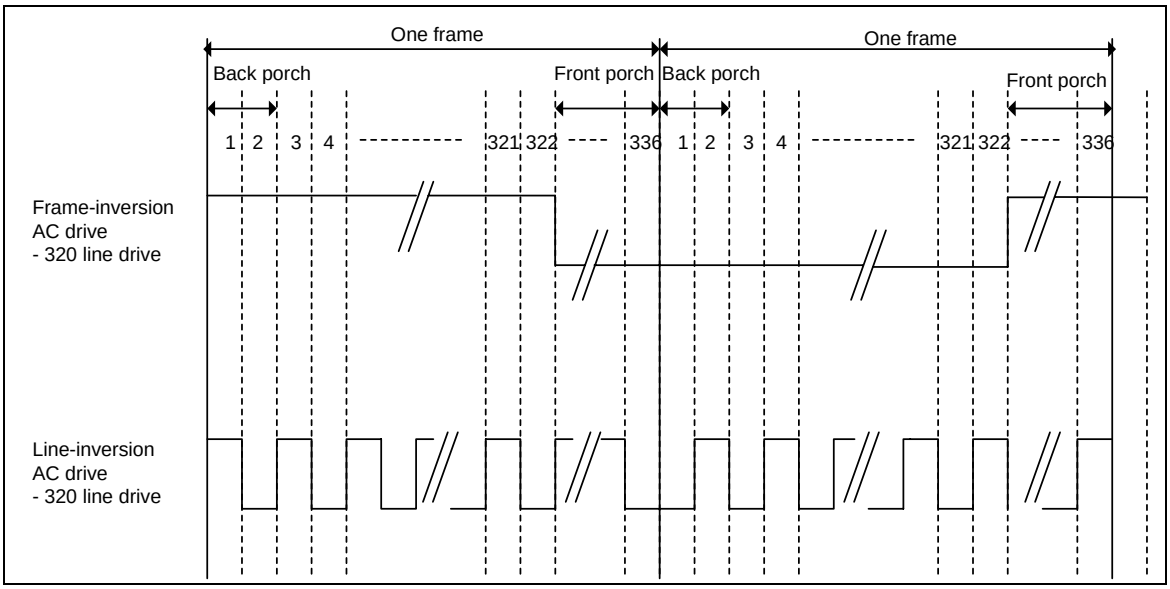


Figure 61 Example of Alternating Signals for n-line Inversion

Frame-Frequency Adjustment Function

The LG4538 supports a function to adjust frame frequency. The frame frequency for driving the LCD can be adjusted by setting the DIV, RTN bits without changing the oscillation frequency.

To switch frame frequencies according to whether displaying a moving picture or displaying a still picture, set a high oscillation frequency in advance. Then, set a low frame frequency to save power consumption when displaying a still picture. When displaying a moving picture, set the frequency high.

Relationship between the liquid crystal Drive Duty and the Frame Frequency

The relationship between the liquid crystal drive duty and the frame frequency is calculated from the following equation. The frame frequency can be adjusted by setting the 1H period adjustment (RTN) bit and the operation clock division (DIV) bit.

Equation for calculating frame frequency

$$Frame\ Frequency = \frac{Fosc}{Number\ Of\ Clocks\ Per\ Line \times Division\ Ratio \times (Line + FP + BP)}$$

Fosc	: RC oscillation frequency
Number of Clocks per line	: RTN bit
Division Ratio	: DIV bit
Line	: number of lines to drive the LCD (NL bit)
FP	: Number of lines for front porch
BP	: Number of lines for back porch

Example of Calculation : when maximum frame frequency = 70Hz

Number of lines : 320 lines
1H period : 120 Clock cycles (RTN[7:0] = “01111000”)
Division ratio of operating clock : 1/1
Front porch : 2 lines
Back porch : 14 lines

Fosc = 60 (Hz) x 120 (clocks) x 1/1 x (320 + 2 + 14) (Lines) = 2.4192(MHz)

In this case, the RC oscillation frequency is to set to 2.4192MHz. Adjust the value of the external resistor connected to the RC oscillator so that RC oscillation frequency becomes 2.4192MHz.

Backlight Control Function

CABC : Content Adaptive Brightness Control

The LG4538 supports “Content Adaptive Brightness Control” function which can be used to reduce the power consumption of the luminance source. Content adaptation means that content gray scale can be increased while simultaneously lowering brightness of the backlight to achieve same perceived brightness. The adjusted gray scale and thus the power consumption reduced depend on the content of the image.

Figure 32 shows that how the CABC algorithm works. The CABC block accumulates the gray scales for each pixels of the image and thus CABC block comes to know the histograms about the gray scales of the image. Next, CABC block modify the original image data to have more widely spreaded shape while it makes the back light luminance lower so that the image luminance perceived by human becomes almost the same.

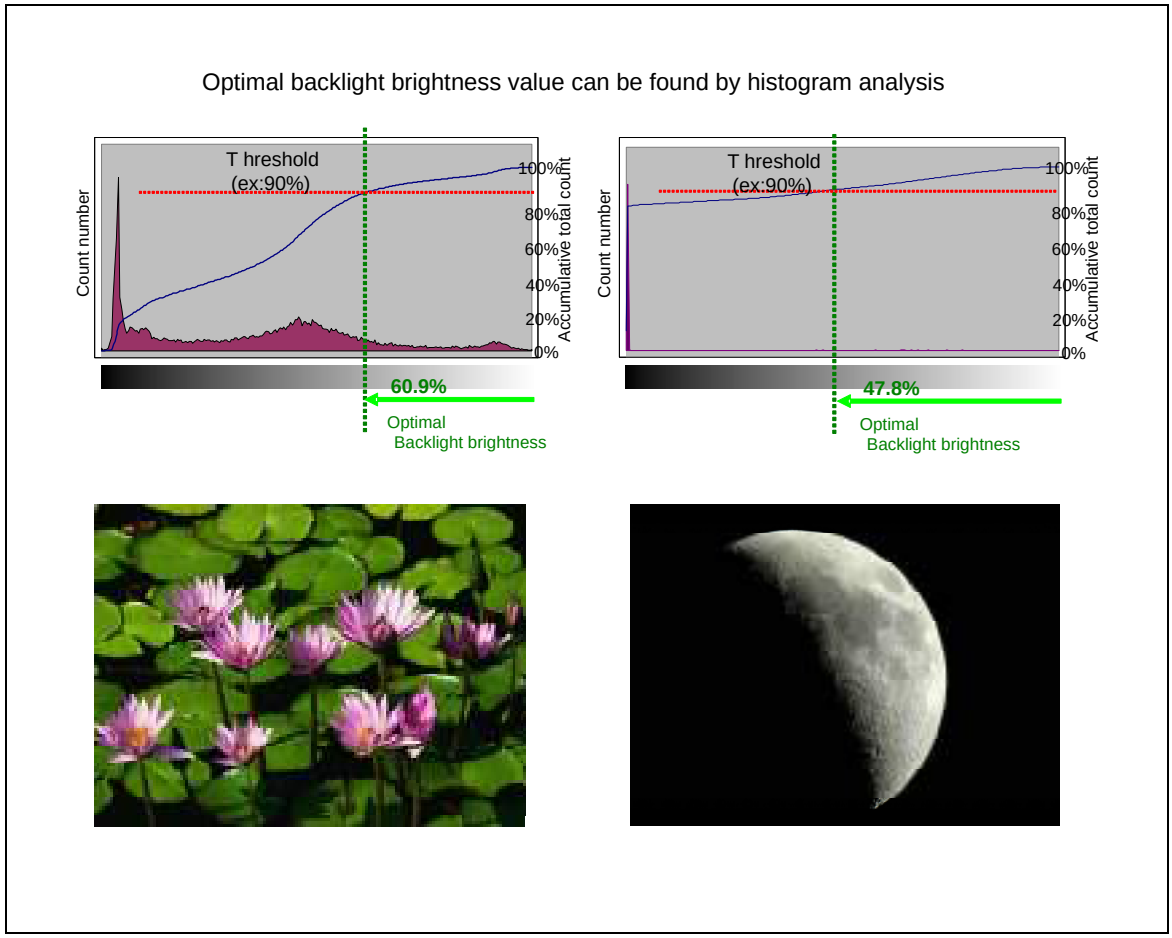


Figure 62 Content Adaptive Brightness Control algorithm

Module Architecture for CABC

Interface should be supported for the following module architectures. Hardware configuration has to be optimized for each architecture.
Architecture I is recommended module architecture. Architecture II is an option for the solutions of the future issues. Implementation should be taken into account in the interface point of view.

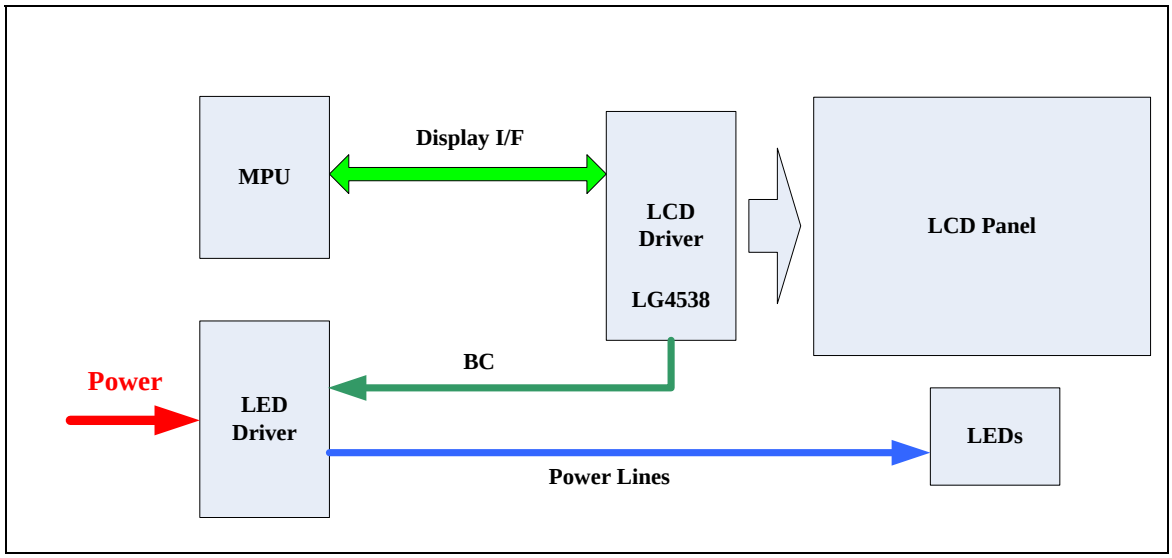


Figure 63 Architecture 1 for CABC

Architecture 1
LED driver is not integrated into display module. LED driving circuit for display backlight is located on the main PCB and it is controlled by the LG4538 through PWM control signal. Bit BL of “Write CTRL Display(53h)” is set to “1”. Brightness for the display is controlled by BC signal.

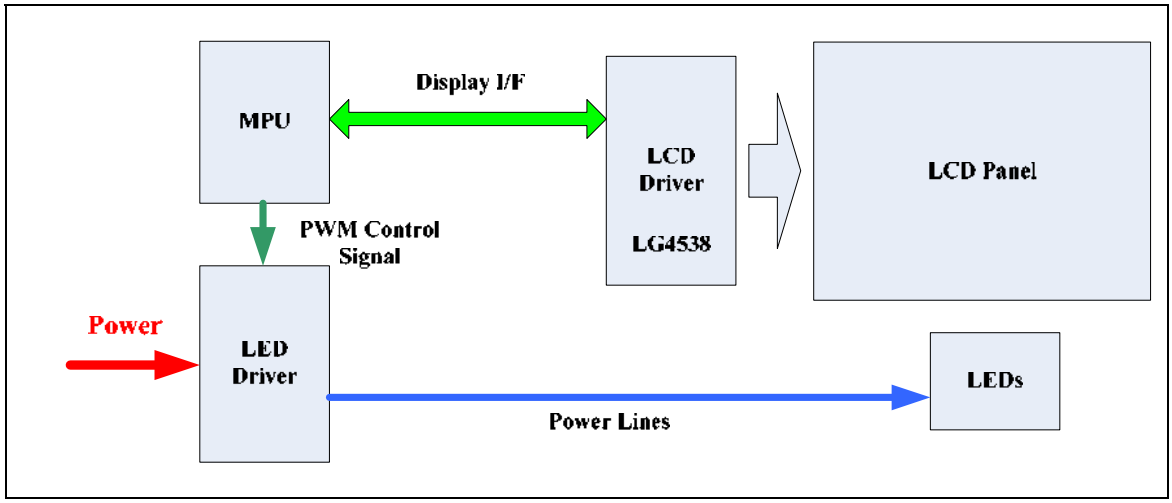


Figure 64 Architecture 2 for CABC

Architecture 2
LED driver is not integrated into display module. LED driving circuit for display backlight is located on the main PCB and it is controlled by the MPU. Bit BL of “Write CTRL Display(53h)” is set to “0”. Brightness data for the display is read with “Read Display Brightness Value (52h)”.
Read commands, “Read Display Brightness Value (52h)”, should be synchronized with Vsync. Display Brightness can be synchronized with CABC function when it read the brightness register with “Read

Dsiaplay Brightness Value (52h)” just after Vsync.

Definition of brightness control bit for each architecture is as follows.

Bit BL of WRCTRLD (53h)

	Architecture I	Architecture II
BL	1	0

Brightness Control Block and CABC Block

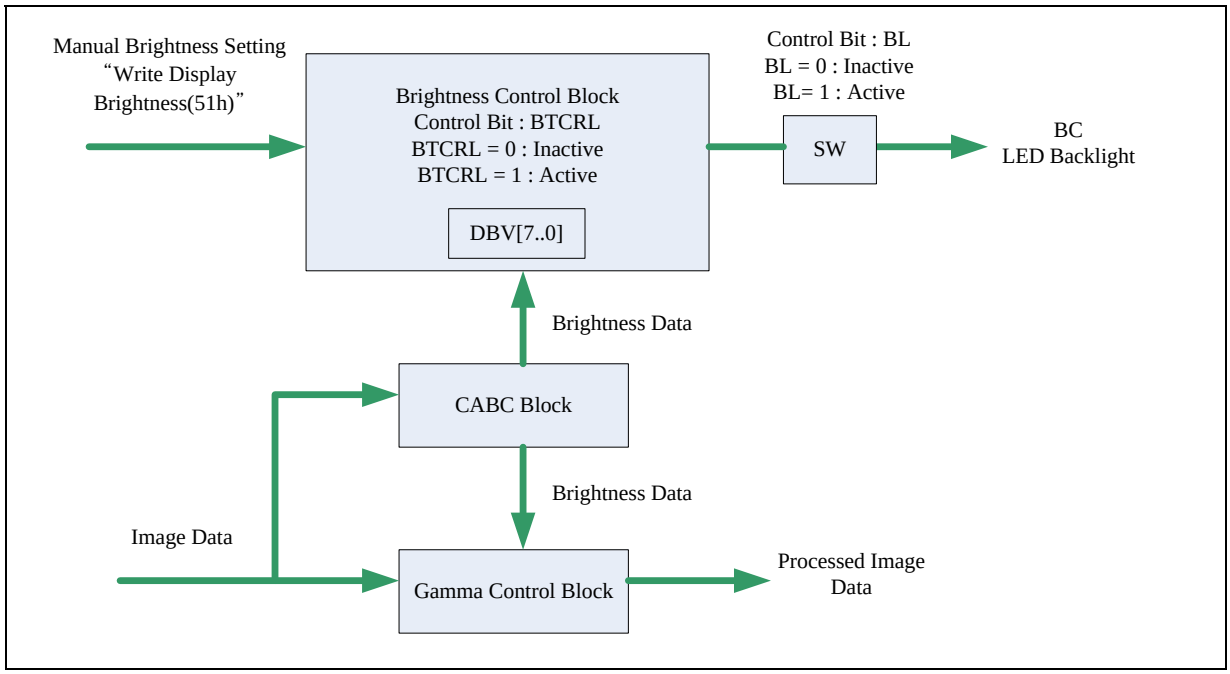


Figure 65 Block Diagram for Brightness Control Block and CABC Block

Brightness Control with CABC and LABC*

Brightness control block is used to control the display brightness as follows:

There is a resister, WRDISBV: 8 bit, for display brightness of manual brightness setting and CABC in the display module. There is a PWM output signal, BC line, to control the LED driver IC in order to control display brightness.

The brightness control block can be used in manual brightness mode and CABC mode, see “Write CTRL Display (53h)” and “Write Content Adaptive Brightness Control (55h)”.

The user can adjust brightness, see “Write Display Brightness (51h) ” for the display.

“Write Display Brightness(51h)” register also be used for the LABC(Luminance Adaptive Brightness Control). In this case, the host adjusts the value of the register according to the sensed environmetal luminance.

Output brightness level calculates with the following formula.

*Display Output Brightness = Manual brightness setting(BRT) * CABC brightness ratio.*

CABC function is automatically reduced backlight brightness based on image contents. In the case of the combination with the LABC or manual brightness setting, display brightness is too dark. It must affect to image quality degradation. CABC minimum brightness setting is to avoid too much brightness reduction.

When CABC is active, CABC can not reduce the display brightness to less than CABC minimum brightness setting. Image processing function is worked as normal, even if the brightness can not be changed.

This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal.

When display brightness is turned off (BCTRL=0 of "Write CTRL Display (53h)"), CABC minimum brightness setting is ignored. "Read CABC minimum brightness (5Fh)" always read the setting value of "Write CABC minimum brightness (5Eh)".

	WRCABC(55h)	Function	RDCABCMB(5Fh)	Image
CABC Off	00b	Disable	WRCABCMB(5Eh)	Original
CABC On	01b /10b /11b	Enable	WRCABCMB(5Eh)	CABC modified

Below drawing is for the explanation of the CABC minimum brightness setting.

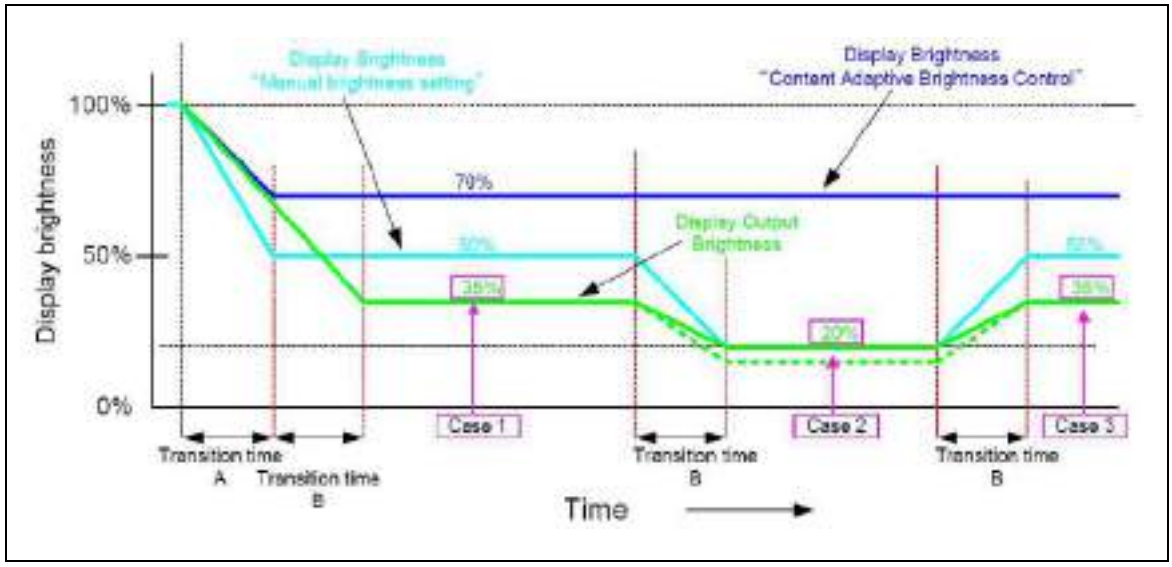


Figure 66 Cotrolled Display Brightness by LABC and CABC Algorithm

CABC minimum brightness value = 51 (33h: 20% display brightness)

	Display Brightness [manual setting]	Brightness Ratio[CABC]	Calculation result of the display brightness formula	Display Output Brightness	Image
Case 1	50%	70%	35%	35%	CABC modified
Case 2	20%	70%	14%	20%	CABC modified
Case 3	50%	70%	35%	35%	CABC modified

At the case 2, the calculation result of the display brightness is 14%. CABC minimum brightness value is set to 20% brightness. Actual display brightness is 20% as the CABC minimum brightness setting.

*LABC : Luminance Adaptive Brightness Control

EPROM Write Sequence

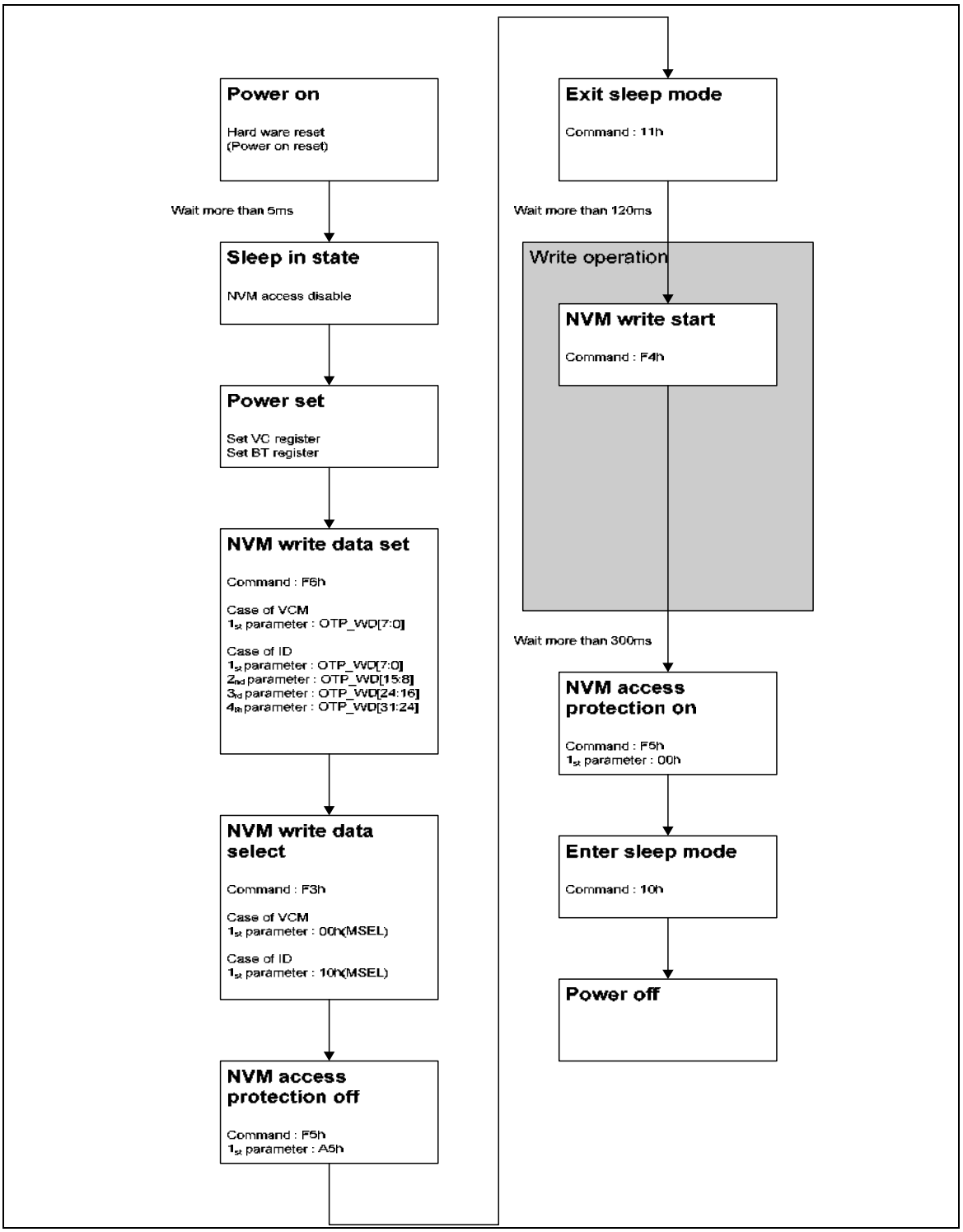


Figure 67 Example of OTP_DSEL = 0

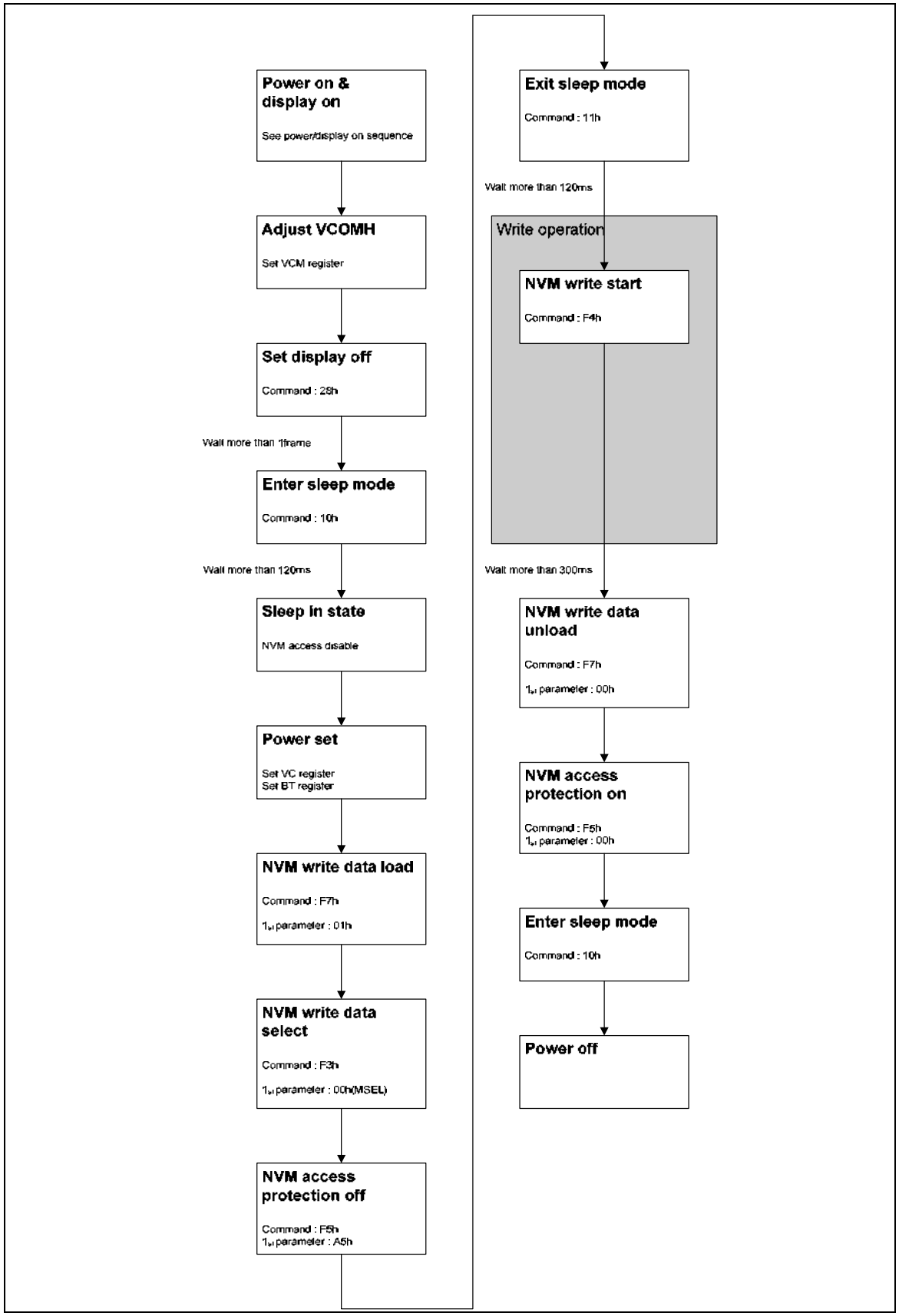


Figure 68 Example of OTP_DSEL = 1

Liquid crystal panel interface timing

The relationships between RGB interface signals and liquid crystal panel control signals in internal operation and RGB interface operations are as follows.

Liquid crystal Panel Interface Timing in Internal clock operation

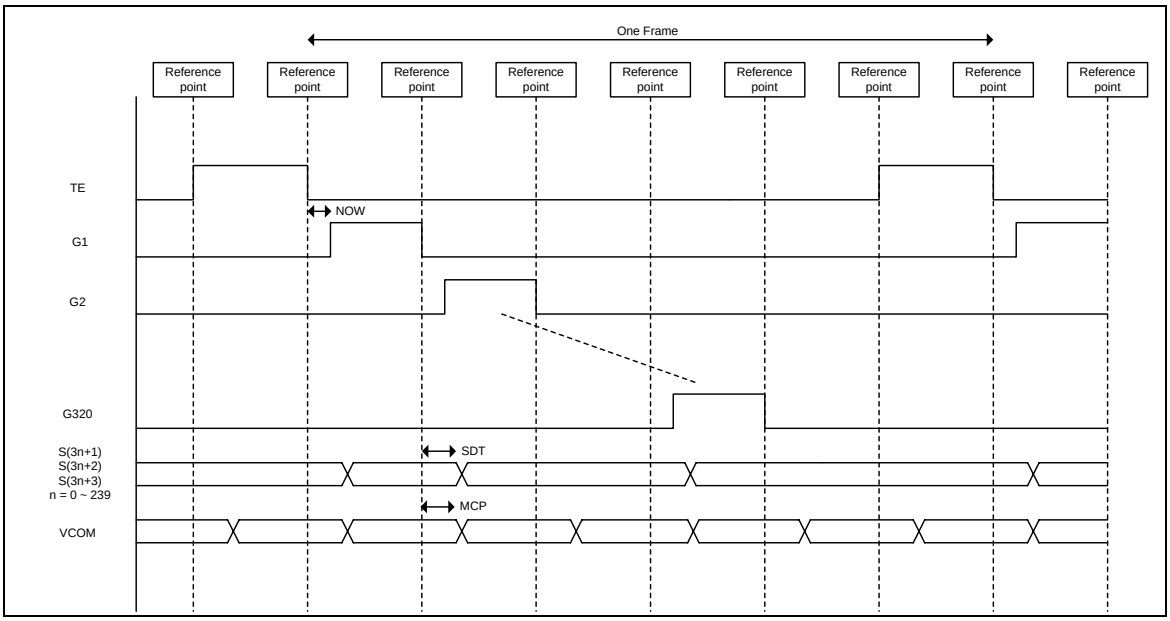


Figure 69

Liquid crystal Panel Interface Timing in DPI Operation

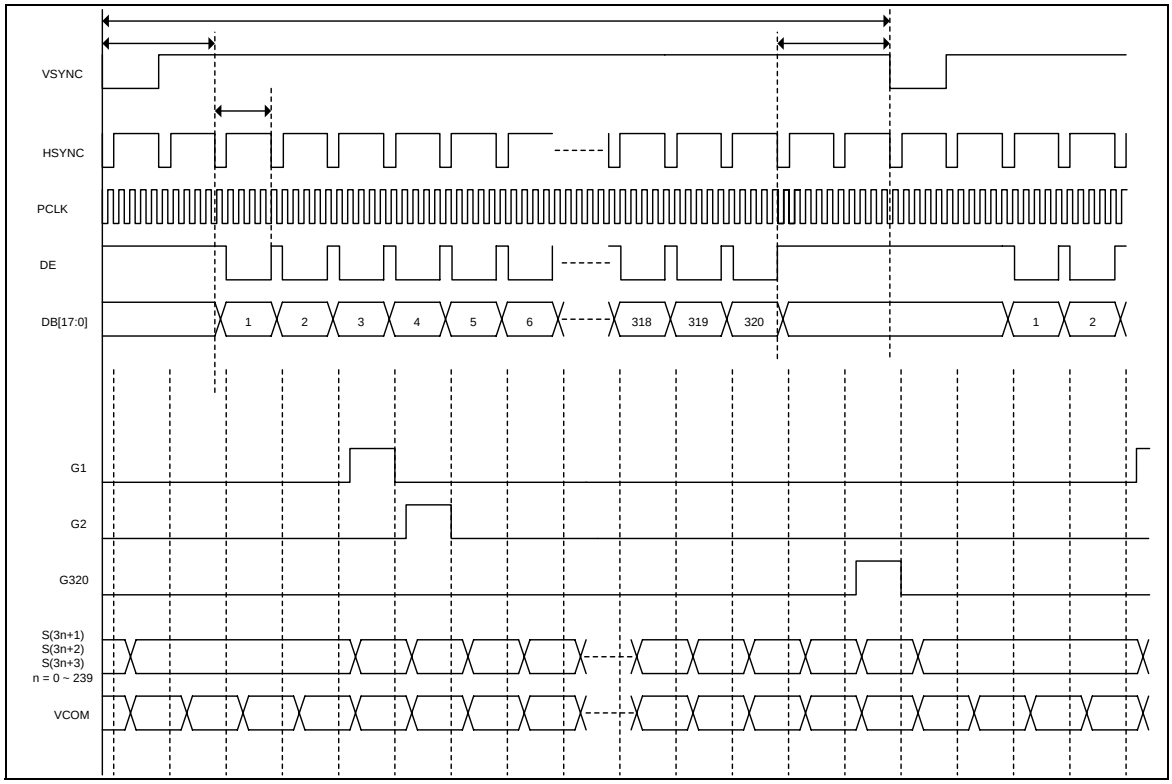

VSYNC
HSYNC
PCLK
DE
DB[17:0]
1
2
3
4
5
6
318
319
320
1
2
G1
G2
G320
S(3n+1)
S(3n+2)
S(3n+3)
n = 0 ~ 239
VCOM

Figure 70

γ-Correction Function

The LG4538 has the γ-correction function to display in 262,144 colors simultaneously. The γ-correction is performed with 3 groups of registers determining eight reference grayscale levels, which are gradient adjustment, amplitude adjustment and fine-adjustment registers. Each register groups further consists of register groups of positive and negative polarities. Each register group is set independently to other register groups, making the LG4538 available with liquid crystal panels of various characteristics.

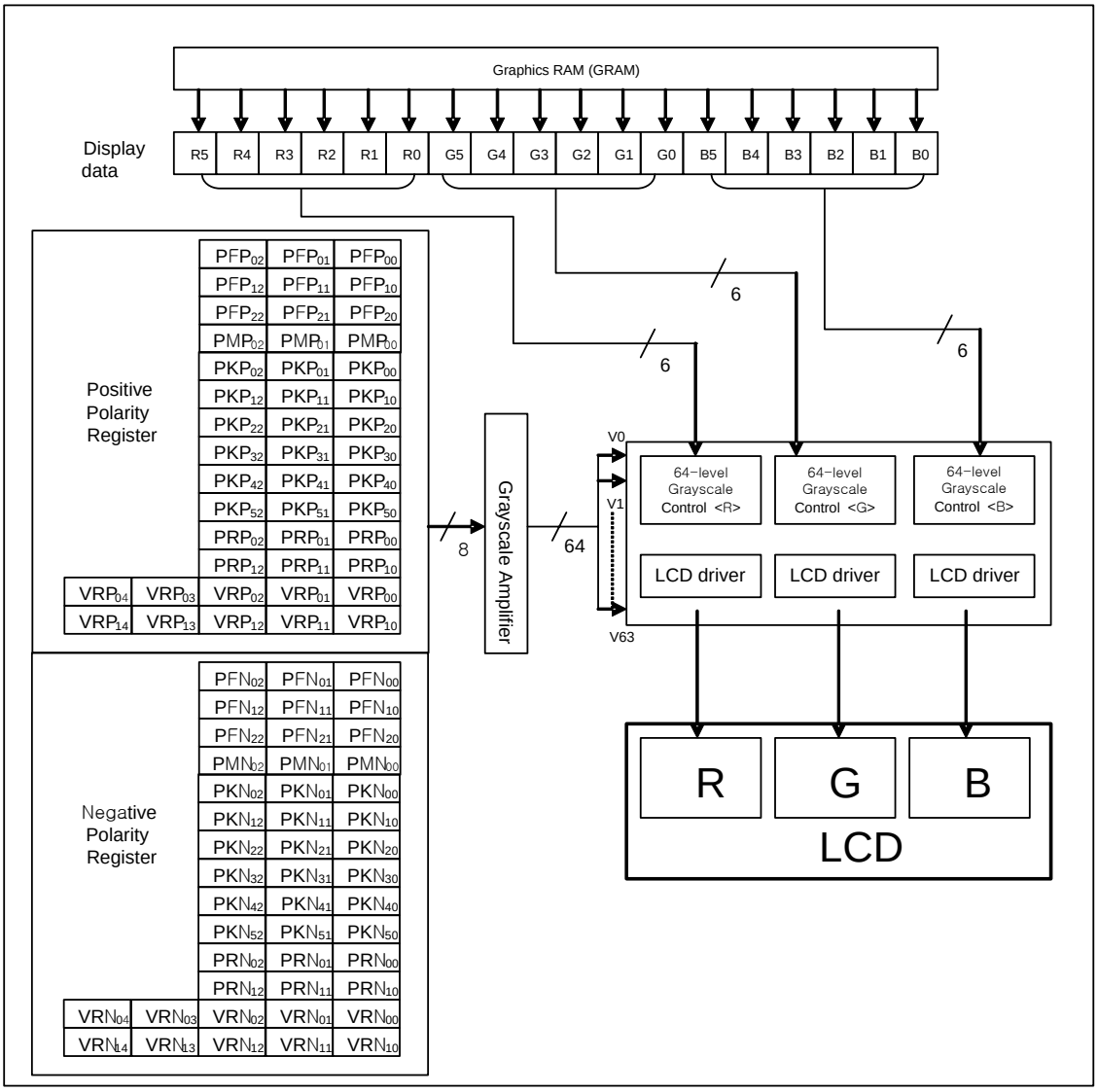


Figure 71 Grayscale control

Grayscale Amplifier Unit Configuration

The following figure illustrates the grayscale amplifier unit of the LG4538.

To generate 64 grayscale voltages (V0 to V63), the LG4538 first generates eight reference grayscale voltages (VINP0-7/VINN0-7). The grayscale amplifier unit then divides eight reference grayscale voltages with the ladder resistors incorporated therein.

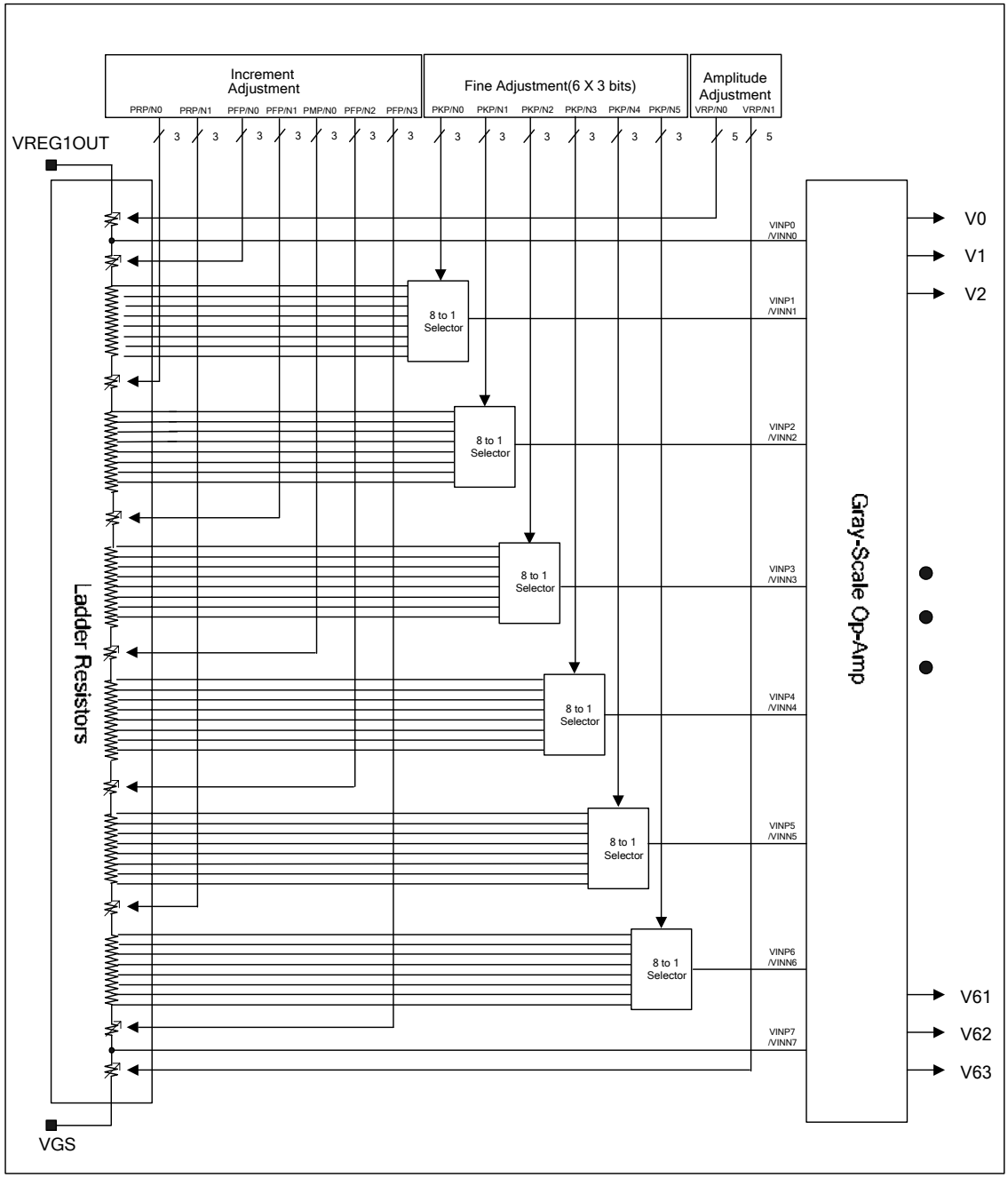


Figure 72 Grayscale amplifier unit

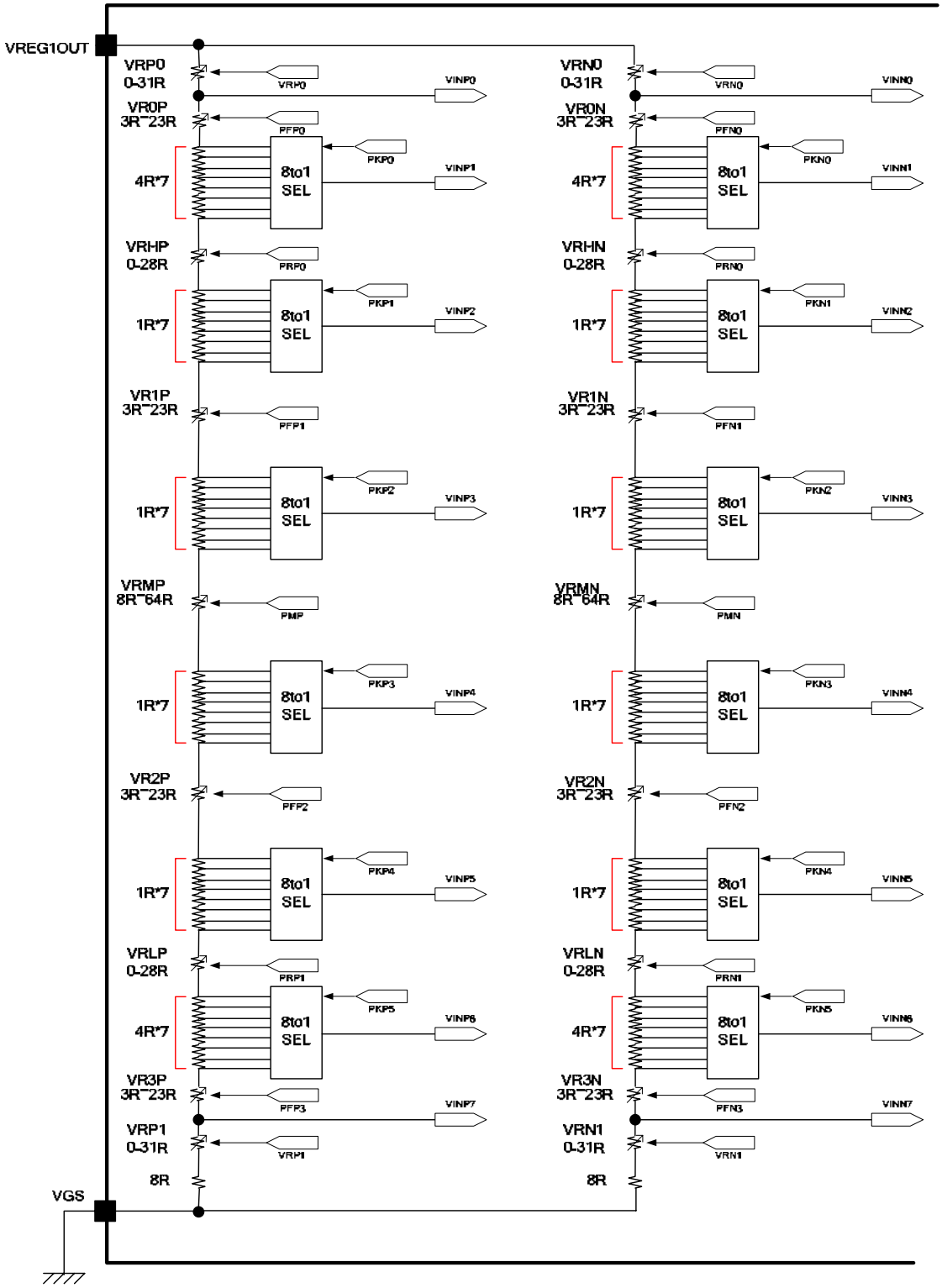


Figure 73 Ladder resistor units and 8-to-1 selectors

γ-Correction Register

The γ-correction registers of the LG4538 consist of gradient adjustment, amplitude adjustment, and fine adjustment registers, each of which has registers of positive and negative polarities. Each different register group can be set independently to others, enabling adjustment of grayscale voltage levels in relation to grayscales set optimally for γ-characteristics of a liquid crystal panel. These γ-correction register settings and the reference levels of the 64 grayscales to which the three kinds of adjustments are made (bold lines in the following figure) are common to all RGB dots.

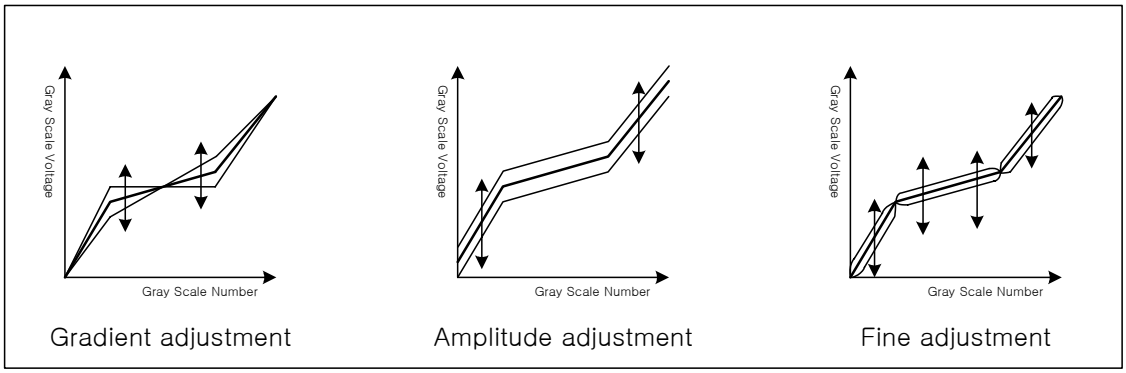


Figure 74

1. Gradient adjustment registers
The gradient adjustment registers are used to adjust the gradient of the curve representing the relationship between the grayscale and the grayscale voltage level around middle grayscales without changing the dynamic range. To adjust the gradient, the resistance values of grayscale reference voltage generating variable resistors (VRHP(N)/VRLP(N)) in the middle of the ladder resistor unit are adjusted. The registers consist of positive and negative polarity registers, allowing asymmetric drive.

2. Amplitude adjustment registers
The amplitude adjustment registers are used to adjust the amplitude of grayscale voltages. To adjust the amplitude, the resistance values of the grayscale voltage generating variable resistors (VRP(N)1/0) at the top and bottom of the ladder resistor unit are adjusted. Same with the gradient registers, the amplitude adjustment registers consist of positive and negative polarity registers.

3. Fine adjustment registers
The fine adjustment registers are used to fine-adjust grayscale voltage levels. To fine-adjust grayscale voltage levels, fine adjustment registers adjust the reference voltage levels, 8 levels for each register generated from the ladder resistor unit, in respective 8-to-1 selectors. Same with other registers, the fine adjustment registers consist of positive and negative polarity registers.

Table 23 List of registers

Register Groups	Positive Polarity	Negative Polarity	Description
Gradient adjustment	PRP0[2:0]	PRN0[2:0]	Variable resistor VRHP(N)
	PRP1[2:0]	PRN1[2:0]	Variable resistor VRHP(N)
	PFP0[2:0]	PFN0[2:0]	Variable resistor VR0P(N)
	PFP1[2:0]	PFN1[2:0]	Variable resistor VR1P(N)
	PFP2[2:0]	PFN2[2:0]	Variable resistor VR2P(N)
	PFP3[2:0]	PFN3[2:0]	Variable resistor VR3P(N)
	PMP[2:0]	PMN[2:0]	Variable resistor VRMP(N)

Amplitude adjustment	VRP0[4:0]	VRN0[4:0]	Variable resistor VRP(N)0
	VRP1[4:0]	VRN1[4:0]	Variable resistor VRP(N)1
Fine adjustment	PKP0[2:0]	PKN0[2:0]	8-to-1 selector (voltage level of grayscale 1)
	PKP1[2:0]	PKN1[2:0]	8-to-1 selector (voltage level of grayscale 8)
	PKP2[2:0]	PKN2[2:0]	8-to-1 selector (voltage level of grayscale 20)
	PKP3[2:0]	PKN3[2:0]	8-to-1 selector (voltage level of grayscale 43)
	PKP4[2:0]	PKN4[2:0]	8-to-1 selector (voltage level of grayscale 53)
	PKP5[2:0]	PKN5[2:0]	8-to-1 selector (voltage level of grayscale 62)

Ladder Resistors and 8-to-1 Selector

Block Configuration

The reference voltage generating unit as illustrated in figure 66 consists of two ladder resistor units including variable resistors and 8-to-1 selectors. Each 8-to-1 selector selects one of the 8 voltage levels generated from the ladder resistor unit to output as a grayscale reference voltage. Both variable resistors and 8-to-1 selectors are controlled according to the γ-correction registers. This unit has pins to connect a volume resistor externally to compensate differences in various characteristics of panels.

Variable Resistors

The LG4538 uses variable resistors of the following three purposes: gradient adjustment (VRHP(N)/VRLP(N)/VR0~4P(N)/VRMP(N)) and amplitude adjustment (VRP(N)0~1). The resistance values of these variable resistors are set by gradient adjustment registers and amplitude adjustment registers as follows.

Table 24 Gradient adjustment

Contents of register PRP(N)0/1[2:0]	**Resistance VRHP(N) VRLP(N)**	**Contents of register PFP(N)0/1/2/3[2:0]**	**Resistance VR0/1P(N) VR2/3P(N)**	**Contents of register PMP(N)[2:0]**	**Resistance VRMP(N)**
000	0R	000	3R	000	8R
001	4R	001	5R	001	16R
010	8R	010	9R	010	24R
011	12R	011	11R	011	32R
100	16R	100	15R	100	40R
101	20R	101	17R	101	48R
110	24R	110	21R	110	56R
111	28R	111	23R	111	64R

.

Table 25 Amplitude adjustment

Contents of register VRP(N)0[4:0]	**Resistance VRP(N)0 VRP(N)1**
00000	0R
00001	1R
00010	2R
:	:
:	:

11101	29R
11110	30R
11111	31R

8-to-1 Selectors

The 8-to-1 selector selects one of eight voltage levels generated from the ladder resistor unit according to the fine adjustment register, and output the selected voltage level as a reference grayscale voltage (VINP(N)1~ VINP(N 6). The table below shows the setting in the fine adjustment register and the selected voltage levels for respective reference grayscale voltages

Table 26 Fine adjustment registers and selected voltage

PKP(N)[2:0]	**Selected Voltage**					
	VINP(N)1	**VINP(N)2**	**VINP(N)3**	**VINP(N)4**	**VINP(N)5**	**VINP(N)6**
3'h0	KVP(N)1	KVP(N)9	KVP(N)17	KVP(N)25	KVP(N)33	KVP(N)41
3'h1	KVP(N)2	KVP(N)10	KVP(N)18	KVP(N)26	KVP(N)34	KVP(N)42
3'h2	KVP(N)3	KVP(N)11	KVP(N)19	KVP(N)27	KVP(N)35	KVP(N)43
3'h3	KVP(N)4	KVP(N)12	KVP(N)20	KVP(N)28	KVP(N)36	KVP(N)44
3'h4	KVP(N)5	KVP(N)13	KVP(N)21	KVP(N)29	KVP(N)37	KVP(N)45
3'h5	KVP(N)6	KVP(N)14	KVP(N)22	KVP(N)30	KVP(N)38	KVP(N)46
3'h6	KVP(N)7	KVP(N)15	KVP(N)23	KVP(N)31	KVP(N)39	KVP(N)47
3'h7	KVP(N)8	KVP(N)16	KVP(N)24	KVP(N)32	KVP(N)40	KVP(N)48

The grayscale voltage levels for V0~V63 grayscales are calculated from the following formula.

Table 27 Formula for calculating voltage (1)

Pin	**Formula**	**Fine adjustment register value**	**Reference voltage**
KVP0	GVDD - ΔV x VRP0/SUMRP	-	VINP0
KVP1	GVDD - ΔV x (VRP0+VR0P+0R)/SUMRP	PKP0= 3'h0	VINP1
KVP2	GVDD - ΔV x (VRP0+VR0P+4R)/SUMRP	PKP0= 3'h1	
KVP3	GVDD - ΔV x (VRP0+VR0P+8R)/SUMRP	PKP0= 3'h2	
KVP4	GVDD - ΔV x (VRP0+VR0P+12R)/SUMRP	PKP0= 3'h3	
KVP5	GVDD - ΔV x (VRP0+VR0P+16R)/SUMRP	PKP0= 3'h4	
KVP6	GVDD - ΔV x (VRP0+VR0P+20R)/SUMRP	PKP0= 3'h5	
KVP7	GVDD - ΔV x (VRP0+VR0P+24R)/SUMRP	PKP0= 3'h6	
KVP8	GVDD - ΔV x (VRP0+VR0P+28R)/SUMRP	PKP0= 3'h7	
KVP9	GVDD - ΔV x (VRP0+VR0P+28R+VRHP)/SUMRP	PKP1= 3'h0	VINP2
KVP10	GVDD - ΔV x (VRP0+VR0P+29R+VRHP)/SUMRP	PKP1= 3'h1	
KVP11	GVDD - ΔV x (VRP0+VR0P+30R+VRHP)/SUMRP	PKP1= 3'h2	
KVP12	GVDD - ΔV x (VRP0+VR0P+31R+VRHP)/SUMRP	PKP1= 3'h3	
KVP13	GVDD - ΔV x (VRP0+VR0P+32R+VRHP)/SUMRP	PKP1= 3'h4	

KVP14	GVDD - ΔV x (VRP0+VR0P+33R+VRHP)/SUMRP	PKP1= 3'h5	
KVP15	GVDD - ΔV x (VRP0+VR0P+34R+VRHP)/SUMRP	PKP1= 3'h6	
KVP16	GVDD - ΔV x (VRP0+VR0P+35R+VRHP)/SUMRP	PKP1= 3'h7	
KVP17	GVDD - ΔV x (VRP0+VR0/1P+35R+VRHP)/SUMRP	PKP2= 3'h0	
KVP18	GVDD - ΔV x (VRP0+VR0/1P+36R+VRHP)/SUMRP	PKP2= 3'h1	
KVP19	GVDD - ΔV x (VRP0+VR0/1P+37R+VRHP)/SUMRP	PKP2= 3'h2	
KVP20	GVDD - ΔV x (VRP0+VR0/1P+38R+VRHP)/SUMRP	PKP2= 3'h3	VINP3
KVP21	GVDD - ΔV x (VRP0+VR0/1P+39R+VRHP)/SUMRP	PKP2= 3'h4	
KVP22	GVDD - ΔV x (VRP0+VR0/1P+40R+VRHP)/SUMRP	PKP2= 3'h5	
KVP23	GVDD - ΔV x (VRP0+VR0/1P+41R+VRHP)/SUMRP	PKP2= 3'h6	
KVP24	GVDD - ΔV x (VRP0+VR0/1P+42R+VRHP)/SUMRP	PKP2= 3'h7	
KVP25	GVDD - ΔV x (VRP0+VR0/1P+42R+VRHP +VRMP)/SUMRP	PKP3= 3'h0	
KVP26	GVDD - ΔV x (VRP0+VR0/1P+43R+VRHP +VRMP)/SUMRP	PKP3= 3'h1	
KVP27	GVDD - ΔV x (VRP0+VR0/1P+44R+VRHP +VRMP)/SUMRP	PKP3= 3'h2	
KVP28	GVDD - ΔV x (VRP0+VR0/1P+45R+VRHP +VRMP)/SUMRP	PKP3= 3'h3	
KVP29	GVDD - ΔV x (VRP0+VR0/1P+46R+VRHP +VRMP)/SUMRP	PKP3= 3'h4	VINP4
KVP30	GVDD - ΔV x (VRP0+VR0/1P+47R+VRHP +VRMP)/SUMRP	PKP3= 3'h5	
KVP31	GVDD - ΔV x (VRP0+VR0/1P+48R+VRHP +VRMP)/SUMRP	PKP3= 3'h6	
KVP32	GVDD - ΔV x (VRP0+VR0/1P+49R+VRHP +VRMP)/SUMRP	PKP3= 3'h7	
KVP33	GVDD - ΔV x (VRP0+VR0/1/2P+49R+VRHP +VRMP)/SUMRP	PKP4= 3'h0	
KVP34	GVDD - ΔV x (VRP0+VR0/1/2P+50R+VRHP +VRMP)/SUMRP	PKP4= 3'h1	
KVP35	GVDD - ΔV x (VRP0+VR0/1/2P+51R+VRHP +VRMP)/SUMRP	PKP4= 3'h2	
KVP36	GVDD - ΔV x (VRP0+VR0/1/2P+52R+VRHP +VRMP)/SUMRP	PKP4= 3'h3	
KVP37	GVDD - ΔV x (VRP0+VR0/1/2P+53R+VRHP +VRMP)/SUMRP	PKP4= 3'h4	VINP5
KVP38	GVDD - ΔV x (VRP0+VR0/1/2P+54+VRHP +VRMP)/SUMRP	PKP4= 3'h5	
KVP39	GVDD - ΔV x (VRP0+VR0/1/2P+55R+VRHP +VRMP)/SUMRP	PKP4= 3'h6	
KVP40	GVDD - ΔV x (VRP0+VR0/1/2P+56R+VRHP +VRMP)/SUMRP	PKP4= 3'h7	
KVP41	GVDD - ΔV x (VRP0+VR0/1/2P+56R+VRHP +VRMP+VRLP)/SUMRP	PKP5= 3'h0	
KVP42	GVDD - ΔV x (VRP0+VR0/1/2P+60R+VRHP +VRMP+VRLP)/SUMRP	PKP5= 3'h1	
KVP43	GVDD - ΔV x (VRP0+VR0/1/2P+64R+VRHP +VRMP+VRLP)/SUMRP	PKP5= 3'h2	
KVP44	GVDD - ΔV x (VRP0+VR0/1/2P+68R+VRHP +VRMP+VRLP)/SUMRP	PKP5= 3'h3	
KVP45	GVDD - ΔV x (VRP0+VR0/1/2P+72R+VRHP +VRMP+VRLP)/SUMRP	PKP5= 3'h4	VINP6
KVP46	GVDD - ΔV x (VRP0+VR0/1/2P+76R+VRHP+VRMP +VRLP)/SUMRP	PKP5= 3'h5	
KVP47	GVDD - ΔV x (VRP0+VR0/1/2P+80R+VRHP+VRMP +VRLP)/SUMRP	PKP5= 3'h6	
KVP48	GVDD - ΔV x (VRP0+VR0/1/2P+84R+VRHP+VRMP +VRLP)/SUMRP	PKP5= 3'h7	
KVP49	GVDD - ΔV x (VRP0+VR0/1/2/3P+84R+VRHP+VRMP +VRLP)/SUMRP	-	VINP7

SUMRP: Sum of positive ladder resistors = 92R+VRHP+VRLP+VRP0+VRP1+VR0P+VR1P+VR2P +VR3P+VRMP

ΔV : Difference in electrical potential between GVDD and VGS

Table 28 Formula for calculating voltage (2)

Grayscale voltage	Formula
V0	VINP0
V1	VINP1
V2	VINP2+(VINP1-VINP2) x (30/48)
V3	VINP2+(VINP1-VINP2) x (23/48)
V4	VINP2+(VINP1-VINP2) x (16/48)
V5	VINP2+(VINP1-VINP2) x (12/48)
V6	VINP2+(VINP1-VINP2) x (8/48)
V7	VINP2+(VINP1-VINP2) x (4/48)
V8	VINP2
V9	VINP3+(VINP2-VINP3) x (22/24)
V10	VINP3+(VINP2-VINP3) x (20/24)
V11	VINP3+(VINP2-VINP3) x (18/24)
V12	VINP3+(VINP2-VINP3) x (16/24)
V13	VINP3+(VINP2-VINP3) x (14/24)
V14	VINP3+(VINP2-VINP3) x (12/24)
V15	VINP3+(VINP2-VINP3) x (10/24)
V16	VINP3+(VINP2-VINP3) x (8/24)
V17	VINP3+(VINP2-VINP3) x (6/24)
V18	VINP3+(VINP2-VINP3) x (4/24)
V19	VINP3+(VINP2-VINP3) x (2/24)
V20	VINP3
V21	VINP4+(VINP3-VINP4) x (22/23)
V22	VINP4+(VINP3-VINP4) x (21/23)
V23	VINP4+(VINP3-VINP4) x (20/23)
V24	VINP4+(VINP3-VINP4) x (19/23)
V25	VINP4+(VINP3-VINP4) x (18/23)
V26	VINP4+(VINP3-VINP4) x (17/23)
V27	VINP4+(VINP3-VINP4) x (16/23)
V28	VINP4+(VINP3-VINP4) x (15/23)
V29	VINP4+(VINP3-VINP4) x (14/23)
V30	VINP4+(VINP3-VINP4) x (13/23)
V31	VINP4+(VINP3-VINP4) x (12/23)

Grayscale voltage	Formula
V32	VINP4+(VINP3-VINP4) x (11/23)
V33	VINP4+(VINP3-VINP4) x (10/23)
V34	VINP4+(VINP3-VINP4) x (9/23)
V35	VINP4+(VINP3-VINP4) x (8/23)
V36	VINP4+(VINP3-VINP4) x (7/23)
V37	VINP4+(VINP3-VINP4) x (6/23)
V38	VINP4+(VINP3-VINP4) x (5/23)
V39	VINP4+(VINP3-VINP4) x (4/23)
V40	VINP4+(VINP3-VINP4) x (3/23)
V41	VINP4+(VINP3-VINP4) x (2/23)
V42	VINP4+(VINP3-VINP4) x (1/23)
V43	VINP4
V44	VINP5+(VINP4-VINP5) x (22/24)
V45	VINP5+(VINP4-VINP5) x (20/24)
V46	VINP5+(VINP4-VINP5) x (18/24)
V47	VINP5+(VINP4-VINP5) x (16/24)
V48	VINP5+(VINP4-VINP5) x (14/24)
V49	VINP5+(VINP4-VINP5) x (12/24)
V50	VINP5+(VINP4-VINP5) x (10/24)
V51	VINP5+(VINP4-VINP5) x (8/24)
V52	VINP5+(VINP4-VINP5) x (6/24)
V53	VINP5+(VINP4-VINP5) x (4/24)
V54	VINP5+(VINP4-VINP5) x (2/24)
V55	VINP5
V56	VINP6+(VINP5-VINP6) x (44/48)
V57	VINP6+(VINP5-VINP6) x (40/48)
V58	VINP6+(VINP5-VINP6) x (36/48)
V59	VINP6+(VINP5-VINP6) x (32/48)
V60	VINP6+(VINP5-VINP6) x (25/48)
V61	VINP6+(VINP5-VINP6) x (18/48)
V62	VINP6
V63	VINP7

Note: Make sure AVDD-V0 > 0.5V

Relationship between RAM Data and Voltage Output Levels
The relationship between RAM data and source output voltage levels is as follows.

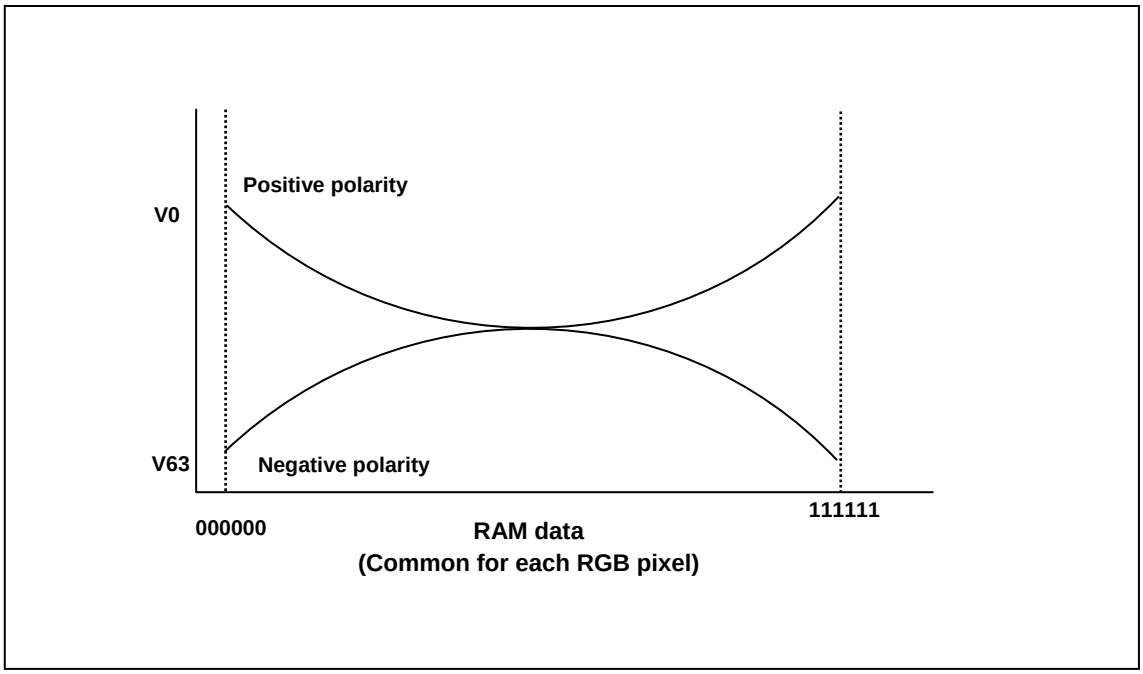


Figure 75 RAM data and the output voltage (REV = "1")

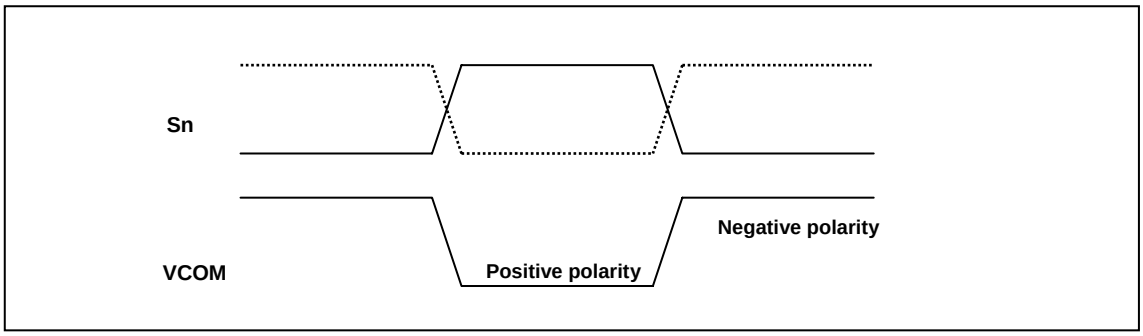


Figure 76 Source output and VCOM

8-Color Display Mode

The LG4538 has a function to display in 8colors. In 8-color mode, available grayscale levels are V0 and V63, and the power supplies of other grayscales (V1 to V62) are halted to reduce power consumption.

In 8-color display mode, the MSBs of the respective dot data (R5, G5, B5) are written to the rest of the dot data in order to display in 8 colors without rewriting the RAM data.

The γ- correction registers, PKP0-PKP5 and PKN0-PKN5, are disabled in 8-color display mode.

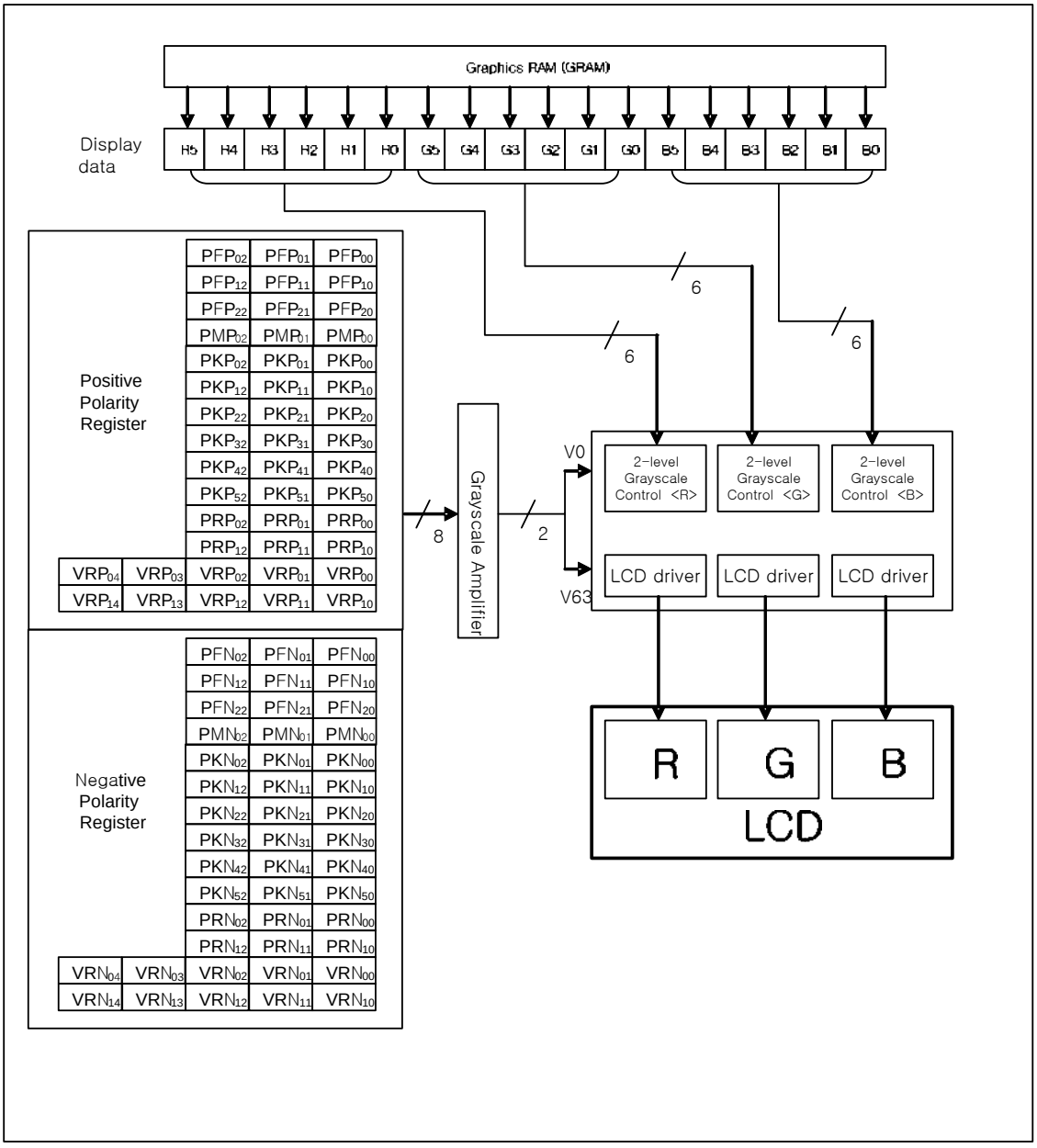


Figure 77 8-color display mode

Power-supply Generating Circuit

The following figures show the configurations of liquid crystal drive voltage generating circuit of the LG4538.

Power supply circuit connection example 1 (VCI1 ≠ VCI)

In the following example, the VCIOUT level is adjusted internally with the VCIOUT output circuit.

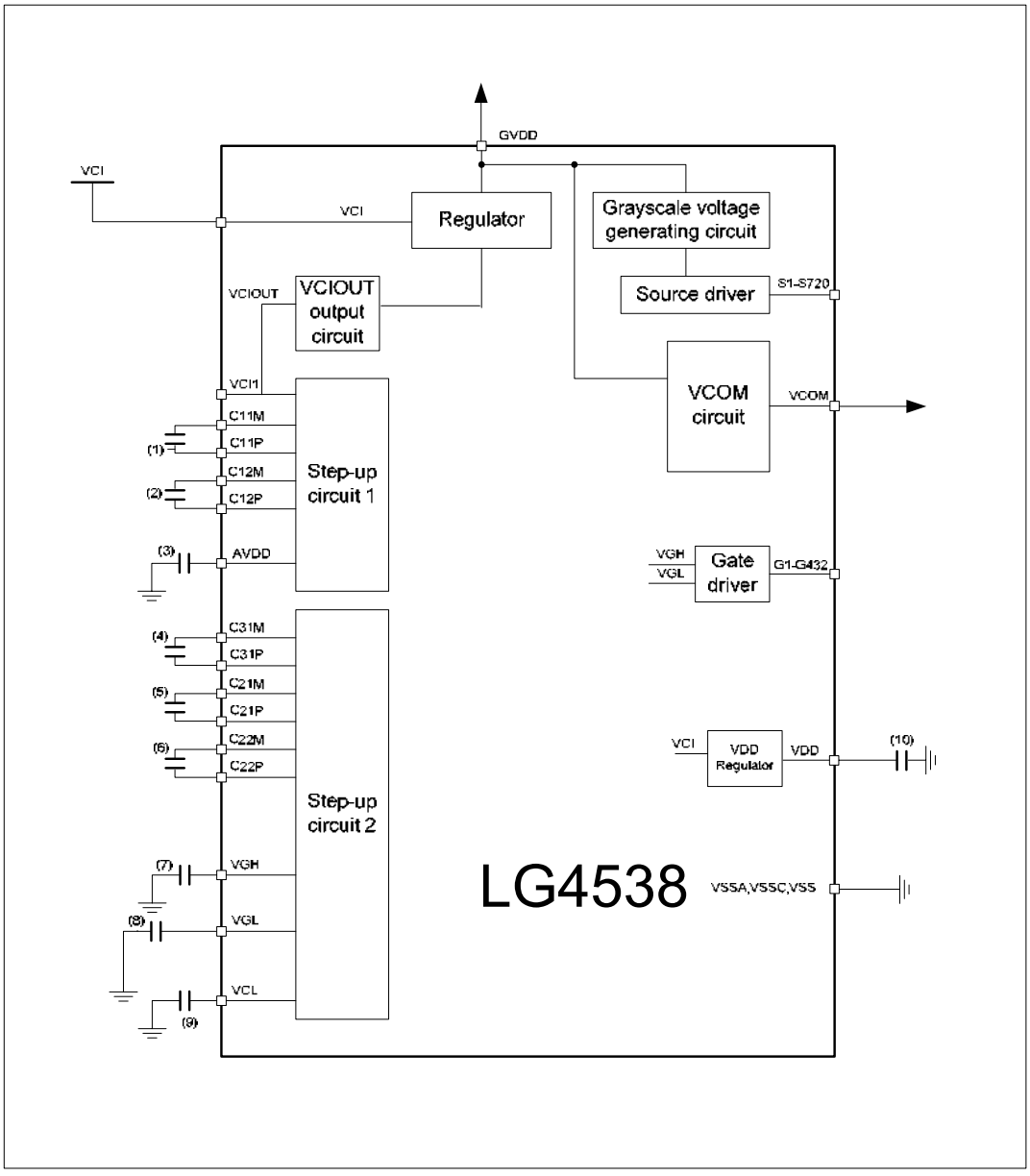


Figure 78

Note: The wiring resistance between the schottky diode and GND/VGL must be 10-Ohm or less.

Power supply circuit connection example2 (VCI1 = VCI direct input)

In the following example, the electrical VCI is directly applied to VCI1. In this case, the VCIOUT level cannot be adjusted internally but step-up operation becomes more effective

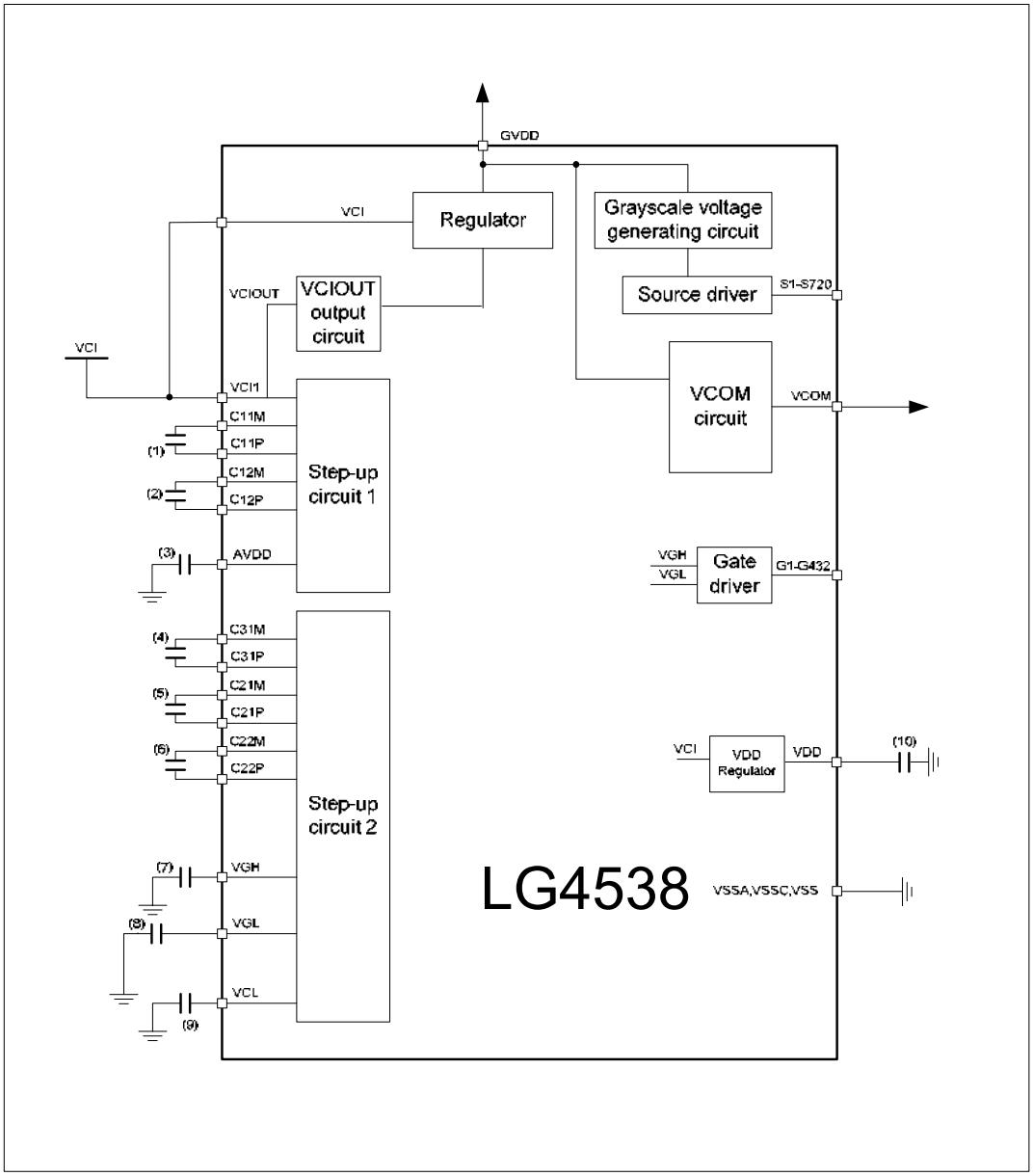


Figure 79

Note: 1. The wiring resistance between the schottky diode and GND/VGL must be 10-Ohm or less.
2. When directly applying the VCI level to VCI1, set VC=3'h0.

Specifications of Power-supply Circuit External Elements

The specifications of external elements connected to the power-supply circuit of the LG4538 are as follows.

Table 29 Capacitor

Capacitance	Voltage proof	Pin Connection
1uF (B characteristics)	6V	(1) C11N/P, (2) C12N/P, (3)AVDD, (4) C31M/P, (9) VCL, (10) VDD
	10V	(5) C21M/P, (6) C22M/P
	25V	(7) VGH, (8) VGL

Notes: 1. Check with the LC module.
2. The numbers in the parentheses corresponds to the numbers of the elements in Figure 78, Figure 79.

Application of Power-supply Circuit

T.B.D.

Figure 80

Voltage Setting Pattern Diagram

The pattern diagram of voltage setting and waveforms of the liquid crystal application voltages are as follows.

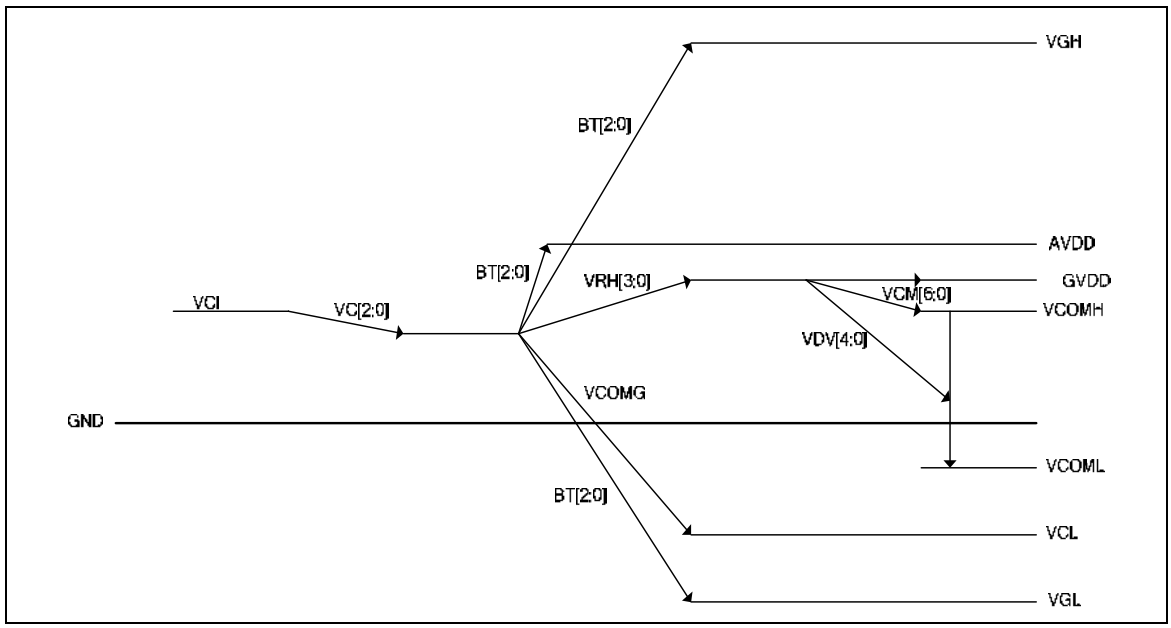


Figure 81 Pattern Diagram for Voltage Setting

Note Output voltages of AVDD, VGH, VGL, and VCL drop from setting voltage(idea voltage) depending on the current consumption at output. (AVDD – GVDD) > 0.5V is the relation to the actual voltage. When using the voltage in the large current consumption at the fast VCOM2 cycle(such as line-by-line inversion), check the voltage value

Absolute Maximum Ratings

Table 30

Item	Symbol	Unit	value	Notes
Power supply voltage (1)	VDD3 – VSS	V	-0.3 ~ +4.5	1, 2
Power supply voltage (2)	VCI – VSS	V	-0.3 ~ +4.5	1, 3
Power supply voltage (3)	AVDD – VSS	V	-0.3 ~ +8.0	1, 4
Power supply voltage (4)	VSS – VCL	V	-0.3 ~ +4.5	1, 5
Power supply voltage (5)	VCI –VCL	V	-0.3 ~ +8.0	1, 6
Power supply voltage (6)	VSS – VGL	V	-0.3 ~ +18	1, 7
Power supply voltage (7)	VGH – VGL	V	-0.3 ~ +30	1, 8
Input voltage	Vt	V	-0.3~VDD3+0.3	1
Operating temperature	Topr	˚C	-40 ~ +85	1, 9
Storage temperature	Tstg	˚C	-55 ~ +125	1

Note 1) If used beyond the absolute maximum ratings, the LSI may permanently be damaged. It is strongly recommended to use the LSI at a condition within the electrical characteristics for normal operation. Exposure to a condition not within the electrical characteristics may affect device reliability.
Note 2) Make sure (High) VDD3 ≥ VSS (Low).
Note 3) Make sure (High) VCI ≥ VSS (Low).
Note 4) Make sure (High) AVDD ≥ VSS (Low).
Note 5) Make sure (High) VSS ≥ VCL (Low).
Note 6) Make sure (High) VCI ≥ VCL (Low).
Note 7) Make sure (High) VSS ≥ VGL (Low).
Note 8) Make sure (High) VGH ≥ VGL (Low).
Note 9) The DC/AC characteristics of die and wafer products is guaranteed at 85 ℃.

Electrical Characteristics

DC Characteristics

Table 31

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Notes
Input high-level voltage	VIH	V	VDD3 = 1.65 ~ 3.3V	0.8VDD3		VDD3	2,3
Input low-level voltage	VIL	V	VDD3 = 1.65 ~ 3.3V	0		0.2VDD3	2,3
Output high-level voltage (1) (DB17-0, SDO, FMARK)	VOH	V	VDD3 = 1.65 ~ 3.3V IOH = 0.1mA	0.8VDD3			2
Output lowlevel voltage (1) (DB17-0, SDO, FMARK)	VOL	V	VDD3 = 1.65~ 3.3V IOL = 0.1mA			0.2VDD3	2
I/O leakage current	I_{li}	µA	Vin = 0 ~ VDD3	-1		1	4
Current consumption : Deep standby mode	I_{ST}	µA	VDD3 = VCI = 2.8V , Ta ≈ 25°C		1	10	5

DBI Type A Timing Characteristics (18/16-Bit Bus)

Table 32 See Figure 78 (Condition: VDD3 = 1.65 to 3.30V, VCI = 2.50 to 3.30V)

Item			Symbol	Unit	Min.	Typ.	Max.
Bus Cycle time		Write	tCYCE	ns	TBD	-	-
		Read	tCYCE	ns	TBD	-	-
Write “Low” level pulse width Read “Low” level pulse width		Write	PWEL	ns	TBD	-	-
		Read	PWEL	ns	TBD	-	-
Write “High” level pulse width Read “High” level pulse width		Write	PWEH	ns	TBD	-	-
		Read	PWEH	ns	TBD	-	-
Write/Read rise/fall time			tEr, tEf	ns	-	-	TBD
Setup time	Write (RS, RW to E)		tASE	ns	TBD	-	-
	Read (RS, RW to E)				TBD	-	-
Address hold time			tAHE	ns	TBD	-	-
Write data setup time			tDSWE	ns	TBD	-	-
Write data hold time			tHE	ns	TBD	-	-
Read data delay time			tDDRE	ns	-	-	TBD
Read data hold time			tDHRE	ns	TBD	-	-

DBI Type A Timing Characteristics (9/8-Bit Bus)

Table 33 See Figure 78 (Condition: VDD3 = 1.65 to 3.30V, VCI = 2.50 to 3.30V)

Item			Symbol	Unit	Min.	Typ.	Max.
Bus Cycle time		Write	tCYCE	ns	TBD	-	-
		Read	tCYCE	ns	TBD	-	-
Write “Low” level pulse width Read “Low” level pulse width		Write	PWEL	ns	TBD	-	-
		Read	PWEL	ns	TBD	-	-
Write “High” level pulse width Read “High” level pulse width		Write	PWEH	ns	TBD	-	-
		Read	PWEH	ns	TBD	-	-
Write/Read rise/fall time			tEr, tEf	ns	-	-	TBD
Setup time	Write (RS, RW to E)		tASE	ns	TBD	-	-
	Read (RS, RW to E)				TBD	-	-
Address hold time			tAHE	ns	TBD	-	-
Write data setup time			tDSWE	ns	TBD	-	-
Write data hold time			tHE	ns	TBD	-	-
Read data delay time			tDDRE	ns	-	-	TBD
Read data hold time			tDHRE	ns	TBD	-	-

DBI Type B Timing Characteristics (18/16-Bit Bus)

Table 34 See Figure 78 (Condition: VDD3 = 1.65 to 3.30V, VCI = 2.50 to 3.30V)

Item			Symbol	Unit	Min.	Typ.	Max.
Bus Cycle time		Write	tCYCW	ns	TBD	-	-
		Read	tCYCR	ns	TBD	-	-
Write “Low” level pulse width Read “Low” level pulse width		Write	PWLW	ns	TBD	-	-
		Read	PWLR	ns	TBD	-	-
Write “High” level pulse width Read “High” level pulse width		Write	PWHW	ns	TBD	-	-
		Read	PWHR	ns	TBD	-	-
Write/Read rise/fall time			tWRr,tWRF	ns		-	TBD
Setup time	Write (DCX to CSB/ WRB)		tAS	ns	TBD	-	-
	Read (DCX to CSB/ RDB)				TBD	-	-
Address hold time			tAH	ns	TBD	-	-
Write data setup time			tDSW	ns	TBD	-	-
Write data hold time			tH	ns	TBD	-	-
Read data delay time			tDDR	ns	-	-	TBD
Read data hold time			tDHR	ns	TBD	-	-

DBI Type B Timing Characteristics (8/9-Bit Bus)

Table 35 See Figure 78 (Condition: VDD3 = 1.65 to 3.30V, VCI = 2.50 to 3.30V)

Item			Symbol	Unit	Min.	Typ.	Max.
Bus Cycle time		Write	tCYCW	ns	TBD	-	-
		Read	tCYCR	ns	TBD	-	-
Write “Low” level pulse width		Write	PWLW	ns	TBD	-	-
Read “Low” level pulse width		Read	PWLR	ns	TBD	-	-
Write “High” level pulse width		Write	PWHW	ns	TBD	-	-
Read “High” level pulse width		Read	PWHR	ns	TBD	-	-
Write/Read rise/fall time			tWRr,tWRF	ns	-	-	TBD
Setup time	Write (RS to CSB/ WRB)		tAS	ns	TBD	-	-
	Read (RS to CSB/ RDB)				TBD	-	-
Address hold time			tAH	ns	TBD	-	-
Write data setup time			tDSW	ns	TBD	-	-
Write data hold time			tH	ns	TBD	-	-
Read data delay time			tDDR	ns	-	-	TBD
Read data hold time			tDHR	ns	TBD	-	-

Serial Peripheral Interface Timing Characteristics

Table 36 See Figure 79 (Condition: VDD3 = 1.65 to 3.30V, VCI = 2.50 to 3.30V)

Item		Symbol	Unit	Min.	Typ.	Max.
Serial clock cycle time	Write (received)	tSCYC	ns	TBD	-	-
	Read (transmitted)	tSCYC	ns	TBD	-	-
Serial clock “High” level pulse width	Write (received)	tSCH	ns	TBD	-	-
	Read (transmitted)	tSCH	ns	TBD	-	-
Serial clock “Low” level pulse width	Write (received)	tSCL	ns	TBD	-	-
	Read (transmitted)	tSCL	ns	TBD	-	-
Serial clock rise/fall time		tscr,tscf	ns	-	-	TBD
Chip select setup time		tCSU	ns	TBD	-	-
Chip select hold time		tCH	ns	TBD	-	-
Serial input data setup time		tSISU	ns	TBD	-	-
Serial input data hold time		tSIH	ns	TBD	-	-
Serial output data delay time		tSOD	ns	-	-	TBD
Serial output data hold time		tSOH	ns	TBD	-	-

DPI Timing Characteristics

Table 37 See Figure 80 (18/16-bit I/F, VDD3 = 1.65 to 3.30V, VCI = 2.50 to 3.30V)

Item	Symbol	Unit	Min.	Typ.	Max.
VSYNC/HSYNC setup time	tSYNCS	ns	TBD	-	-
ENABLE setup time	tENS	ns	TBD	-	-
ENABLE hold time	tENH	ns	TBD	-	-
DOTCLK “Low” level pulse width	PWDL	ns	TBD	-	-
DOTCLK “High” level pulse width	PWDH	ns	TBD	-	-
DOTCLK cycle time	tCYCD	ns	TBD	-	-
Data setup time	tPDS	ns	TBD	-	-
Data hold time	tPDH	ns	TBD	-	-
DOTCLK, VSYNC, HSYNC rise/fall time	trgbr, trgbf	ns	-	-	TBD

Reset Timing Characteristics

Table 38 See Figure 81 & Figure 82 (Condition: VDD3 = 1.65 to 3.30V, VCI = 2.50 to 3.30V)

Item	Symbol	Unit	Min	Typ	Max
Reset wait time	**tRW**	**ms**	1	-	-
Reset “Low” level width	**tRES**	**ms**	1	-	-
Reset rise time	**trRES**	**us**	-	-	10
Reset time	**tRT**	**ms**	-	-	10

Oscillator Clock Characteristics

Table 39 (Condition: VDD3=VCI=2.8V, Ta=25°C, R15h=16’h6030, R9Ah=16’h0013

Item	Symbol	Unit	Min	Typ	Max
Oscillator Frequency	fosc	MHz	TBD	TBD	TBD

Notes to Electrical Characteristics

1. The DC/AC electrical characteristics of bare die and wafer products are guaranteed at 85°C.
2. The following are the configurations of I pin, I/O pin, and O pin.

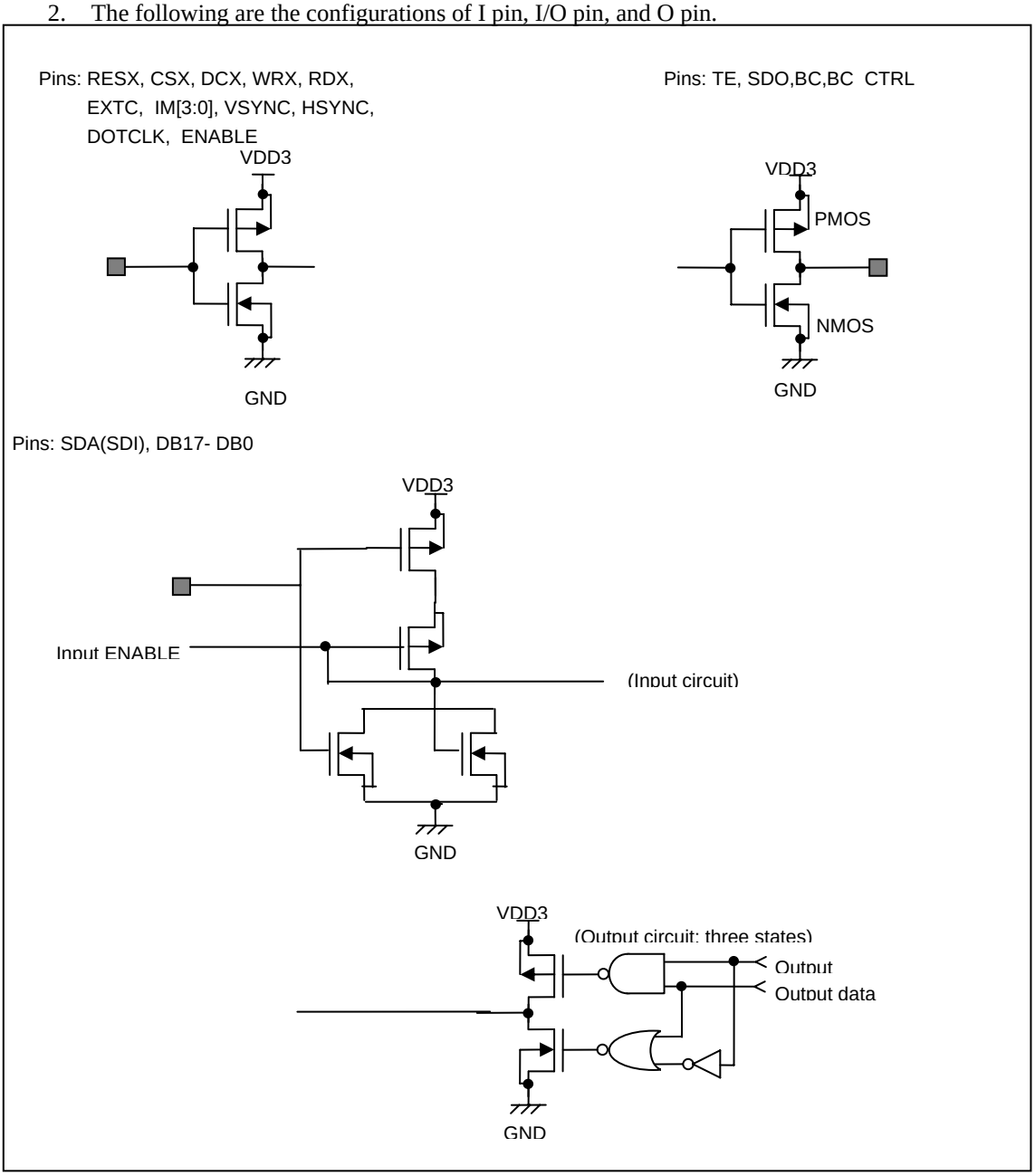
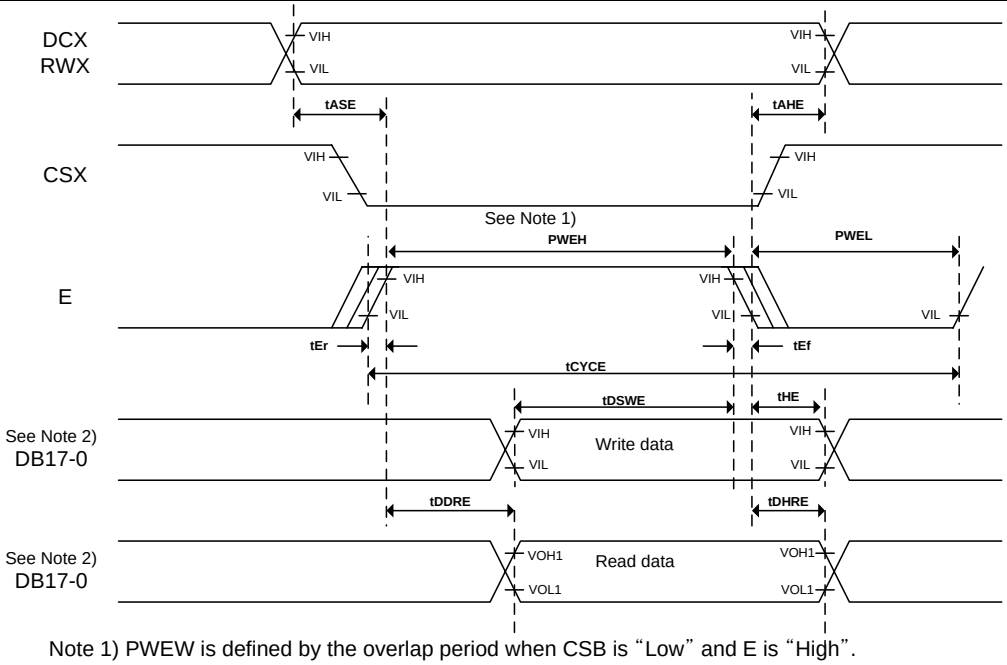


Figure 82

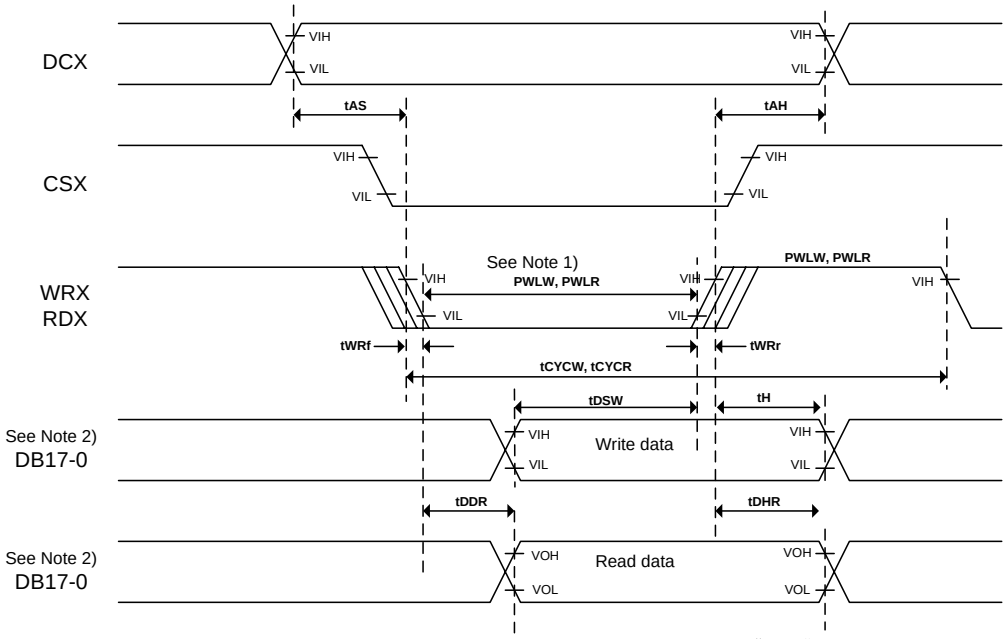
3. The TEST1 pin must be grounded (GND). The IM[3:0] pins must be fixed at either GND or the VDD3 level.
4. This excludes currents though the output drive MOS.
5. This excludes currents flowing through input/output units. Be sure that input levels are fixed to prevent increase in the transient current in input units when a CMOS input level takes medium range. While not accessing via interface pins, current consumption will not change whether the CSB pin is set to “High” or “Low”.

Timing characteristic diagram



Note 1) PWEW is defined by the overlap period when CSB is "Low" and E is "High".
Note 2) Unused DB pins must be fixed at "IOVCC" or "GND".

Figure 83 DBI Type A interface operation



Note 1) PWLW and PWLR are defined by the overlap period when CSX is "Low" and WRX or RDX is "Low".
Note 2) Unused DB pins must be fixed at "IOVCC" or "GND".

Figure 84 DBI Type B interface operation

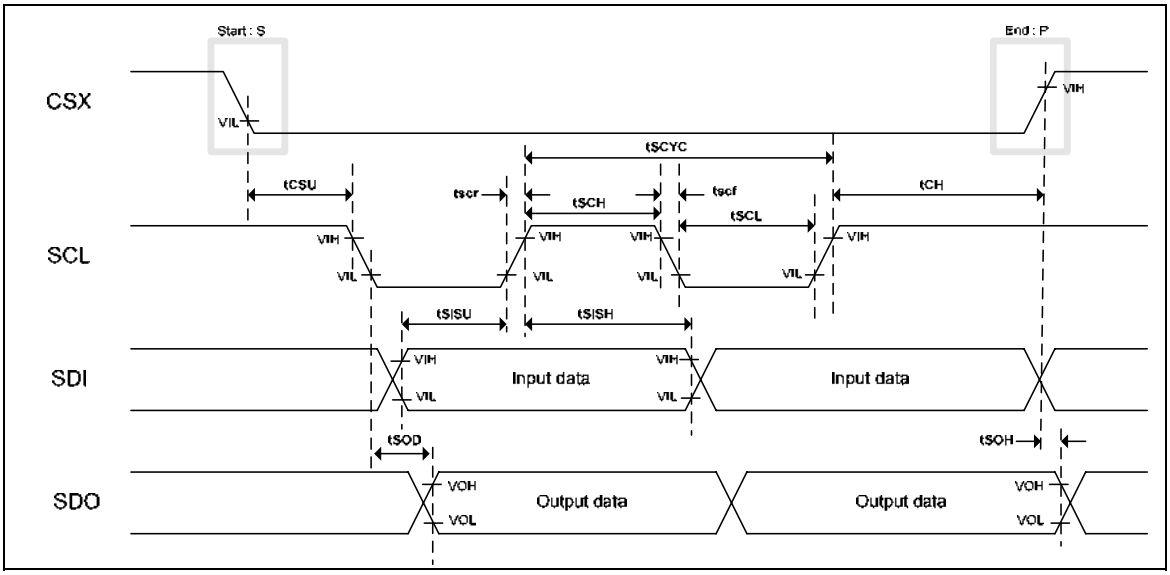


Figure 85 Serial Peripheral Interface operation

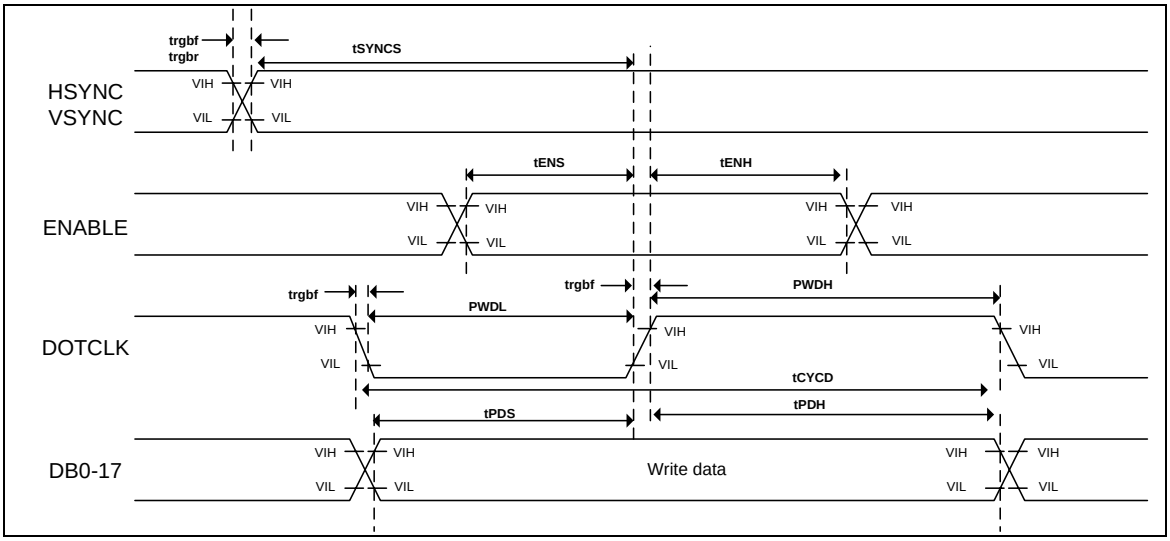


Figure 86 DPI operation

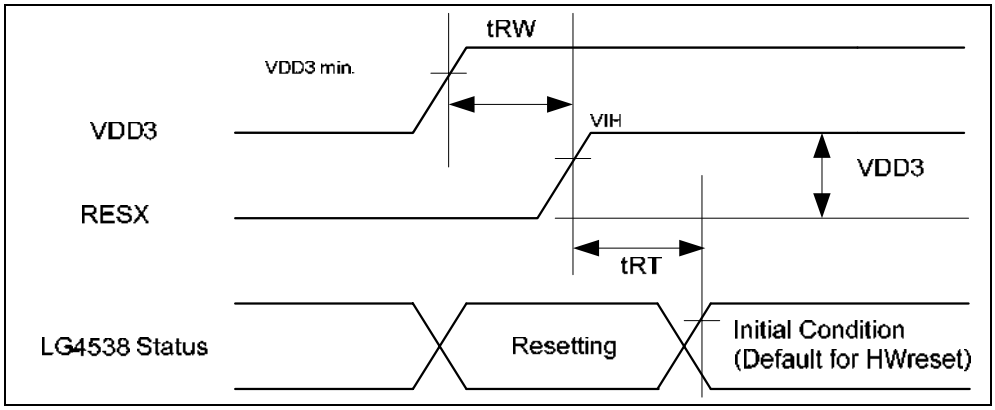


Figure 87 Reset timing when power supply is input

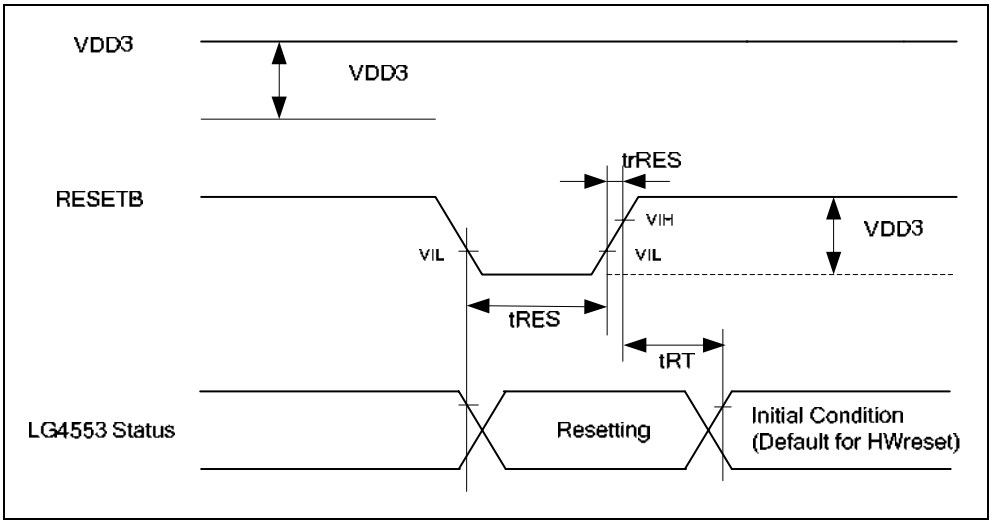


Figure 88 Reset timing during normal operation

Revision History

Ver.	Date	Revision Description	Revised by
0.01	2009.06.23	Preliminary release	S.H. Koh
0.02	2009.07.14	Revised Pad & Bump information : p11~21	H.C.Kim