Specification

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Controlled by DCC

Copy List

Code Name	100	200	300	400	500	600	700
Dept.	HR	S/M	MFG	R&D	CH	QRA	MIS
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文件變更履歷頁

Document Change History

版次 Rev.	變更項次 Change Items#	變更內容簡述 Change Description	變更依據 文件號碼 ECN #	撰寫者 Writer	生效日期 Eff. Date
P001	-	● New Release	E03120001	Plato	03/02/2012
P002	P10	Corrected Interface mode	E03120008	Plato	03/12/2012
P003	P4	Align Key Location modifed IC thickness	E04120004	Plato	04/25/2012
	P3	Removed VR/VRS/IRS			
	P8	PS Pin define			
	P9	Add V0I Pin define			
	P7	CL must fix to VSS1 or VDD1 when CLS is “H”			
	P11	SPI4 interface define			
	P13	Add IIC interface detail description			
	P19	Modify RAM address			
	P22	Add note about AX/AY			
	P23	Add description for SLP			
	P25	Modify DUTY description			
	P26	Modify read status command			
	P27	Modify read flow diagram			
	P31	Delete redundant Frame Rate compensation description			
	P49~53	Modify Application diagram			

接續頁 CONTINUATION --- ■ 是 YES; □ V 否 NO

版次 Rev.	變更項次 Change Items#	變更內容簡述 Change Description	變更依據 文件號碼 ECN #	撰寫者 Writer	生效日期 Eff. Date
P003	P28-P28	Add Frame control	E04120004	Plato	06/25/2012
	P31	Add MX description		Plato	06/25/2012
	P32	Add V0 calculation		Plato	06/25/2012
	P34	Add Frame frequency compensation note		Plato	06/25/2012
P004	P40	Add command Map_mode description	E071200008	Plato	07/25/2012
P005	P51~55	REFERENCE APPLICATIONS	E081200003	Plato	08/24/2012
	P56	ITO CONNECTION			
001	P45	DC CHARACTERISTICS	E03130002	Plato	03/07/2013
	P46	Dynamic Current Consumption			
	P46	Static Current Consumption			
		Remove “Preliminary “			
002	P20	Modify ADC value Modify SEG direction	E05130008	Michael	2013/5/29
	P26	Modify RESET value			
	P36	Add CTOFT value table			
	P42	Add C* value			
	P51~P55	Remove “2.2uf or above”			
	P20~P35	Remove temperature sensor items			
	P21~P35	Updated the command description sequence			
	P41	Updated the system cycle time and pulse width			

版次 Rev.	變更項次 Change Items#	變更內容簡述 Change Description			
003	P36~P38	Add Power On/Off Sequence	E08130007	Michael	2013/08/09
004	P48	Add IIC interface AC characteristics	E04160003	Michael	2016/04/21
005	P2 & P42	Change Operation temperature range (Topr) from-30℃ to -40 ℃ & from 80 ℃ to 85 ℃	E03170005	Michael	2017/03/09
006	P16	Change Read Mode flag to “1”	E06170008	Michael	2017/06/23
007	P49	Updated “Reset Input Timing”	E11190004	Michael	2019/11/11
008	P9,10,48	Add Serial interface selection instructions	E05200006	Sky	2020/05/29

接續頁 CONTINUATION --- ☐ 是 YES; ■ 否 NO

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INTRODUCTION

The IST3931 is a single chip driver & controller LSI for graphic dot-matrix liquid crystal display systems. This chip can be connected directly to a microprocessor, accepts serial or 8-bit parallel display data from the microprocessor, stores the display data in an on-chip display data RAM of 65 x 132 bits and generates a liquid crystal display drive signal independent of the microprocessor. It provides a high-flexible display section due to 1-to-1 correspondence between on-chip display data RAM bits and LCD panel pixels. It contains 65 common driver circuits and 132 segment driver circuits, so that a single chip can drive a 65 x 132 dot display.

This chip is able to minimize power consumption because it performs display data RAM read / write operation with no external operation clock. In addition, because it contains power supply circuits necessary to drive liquid crystal, which is a display clock oscillator circuit, high performance voltage converter circuit, high-accuracy voltage regulator circuit, low power consumption voltage divider resistors and OP-Amps for liquid crystal driver power voltage, it is possible to make the lowest power consumption display system with the fewest components for high performance portable systems.

FEATURES

Power Supply

- Logic Power VDD1 –GROUND = 2.4V ~ 3.6V
- Analog Power VDD2/VDD3/VDD4 –GROUND = 2.4V ~ 3.6V
- LCD Driving V0 – GROUND = 13.5V (Max)

Display Driver Output Circuits

- 65 common outputs / 132 segment outputs
- Display Duty = 1/1~ 1/65
- Applicable Bias: 1/6 ~ 1/11

On-chip Display Data RAM

- RAM size : 65x132 = 8,580 bits

Built-in Analog Circuit

- Reduced external parts (1~5 capacitors only, depending on panel loading)
- On-chip oscillator circuit for display clock (external clock can also be used)
- High performance voltage converter (with booster ratios x5)
- High accuracy reference voltage generator
- Electronic contrast control (256 steps)
- Embedded V0 Voltage regulator
- High performance voltage follower (V1 ~ V4 voltage generator with output buffer)
- Temperature compensation on frame frequency and V0 voltage

Microprocessor Interface

- High-speed 8080/6800-series 8-bit parallel bi-directional interface
- Serial 3/4 line Write/Read interface
- IIC Write/Read interface

Various Function Set

- Display On/Off control
- Set display starting line,
- Set row/column address
- Software reset
- Read Status
- Reverse display
- Select Bias
- Set Duty
- COM/SEG output direction control
- Display power control
- LCD Contrast (V0) control
- MTP(Multi-Times-Programming) Contrast adjust

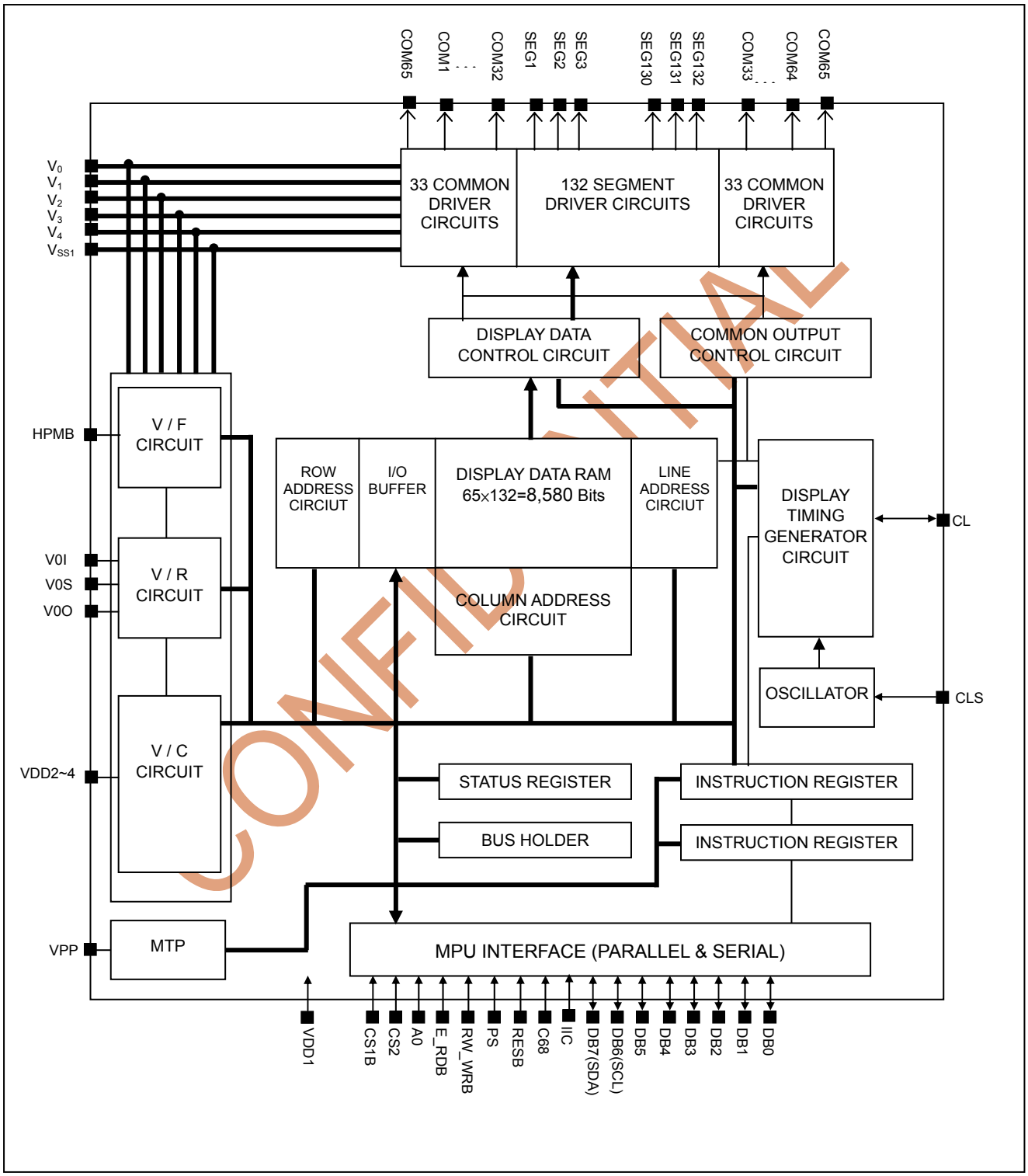
Operating Temperatures

- Wide range of operating temperatures from -40℃ to 85℃

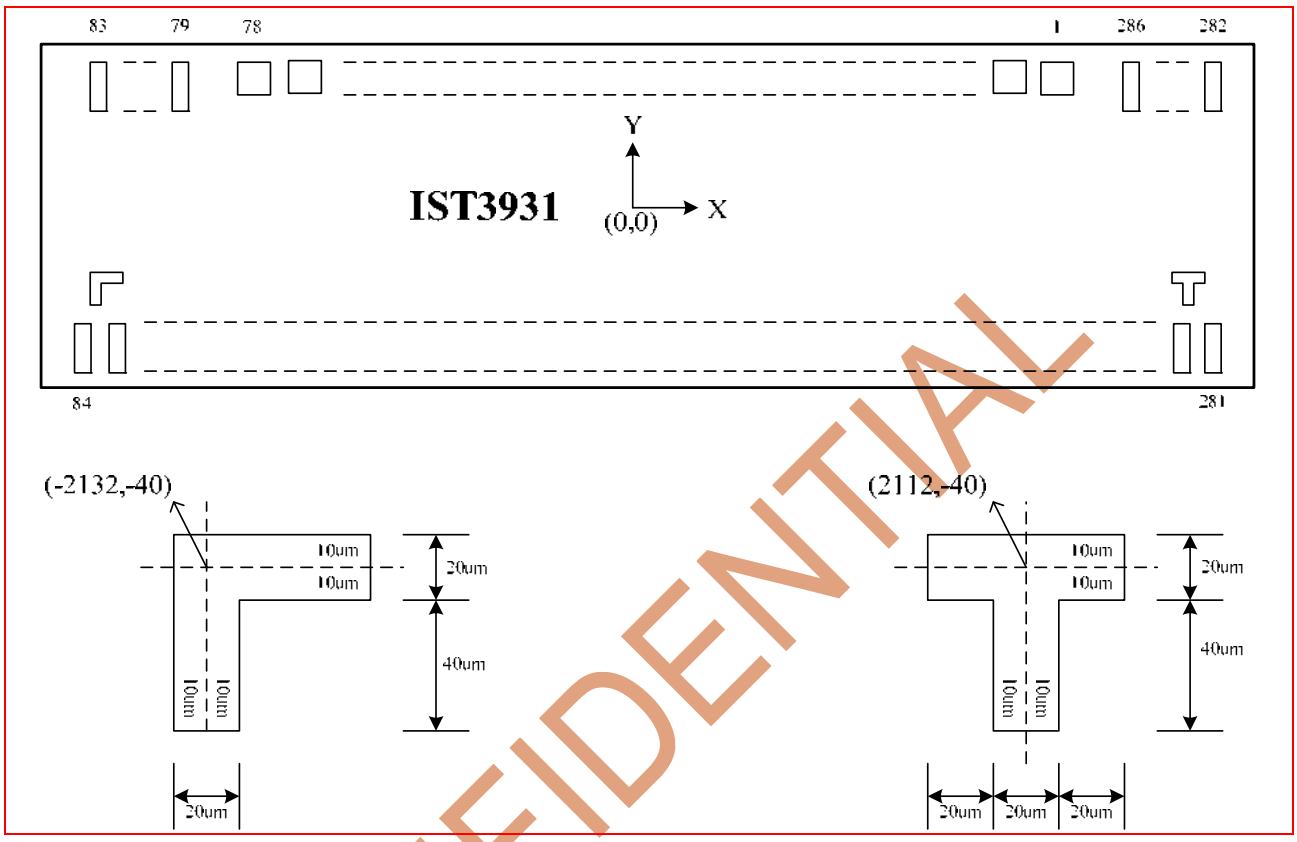
Package Type

- COG(Gold-bumped bared chip)

BLOCK DIAGRAM



PAD CONFIGURATION



Chip Size	4431 um x 600 um	
Bump Pitch	22um (min)	
Bump Spacing	12um (min)	
Bump Size(X*Y)	32 x 50 um2	Pad No = 1 ~78
	10 x 150 um2	Pad No =79 ~ 286
Bump Height	12um (Typ)	
Chip Thickness	300um (Typ)	

PAD CENTER COORDINATES

Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)
1	NC	1925	263	51	VSS1	-575	263	101	COM<27>	-1793	-214
2	NC	1875	263	52	VSS1	-625	263	102	COM<25>	-1771	-214
3	NC	1825	263	53	VSS4	-675	263	103	COM<23>	-1749	-214
4	NC	1775	263	54	VSS4	-725	263	104	COM<21>	-1727	-214
5	NC	1725	263	55	VSS2	-775	263	105	COM<19>	-1705	-214
6	NC	1675	263	56	VSS2	-825	263	106	COM<17>	-1683	-214
7	VPP	1625	263	57	VSS2	-875	263	107	COM<15>	-1661	-214
8	VPP	1575	263	58	VSS2	-925	263	108	COM<13>	-1639	-214
9	VSS1	1525	263	59	V4	-975	263	109	COM<11>	-1617	-214
10	VDD1	1475	263	60	V3	-1025	263	110	COM<9>	-1595	-214
11	CS1B	1425	263	61	V2	-1075	263	111	COM<7>	-1573	-214
12	CS2	1375	263	62	V1	-1125	263	112	COM<5>	-1551	-214
13	RESB	1325	263	63	V0S	-1175	263	113	COM<3>	-1529	-214
14	A0	1275	263	64	V0S	-1225	263	114	COM<1>	-1507	-214
15	VSS1	1225	263	65	V0I	-1275	263	115	NC	-1485	-214
16	VDD1	1175	263	66	V0I	-1325	263	116	NC	-1463	-214
17	WRB	1125	263	67	V0I	-1375	263	117	SEG<132>	-1441	-214
18	RDB	1075	263	68	V0I	-1425	263	118	SEG<131>	-1419	-214
19	VSS1	1025	263	69	V0O	-1475	263	119	SEG<130>	-1397	-214
20	VDD1	975	263	70	V0O	-1525	263	120	SEG<129>	-1375	-214
21	DB<0>	925	263	71	V0O	-1575	263	121	SEG<128>	-1353	-214
22	DB<1>	875	263	72	V0O	-1625	263	122	SEG<127>	-1331	-214
23	DB<2>	825	263	73	NC	-1675	263	123	SEG<126>	-1309	-214
24	DB<3>	775	263	74	NC	-1725	263	124	SEG<125>	-1287	-214
25	DB<4>	725	263	75	NC	-1775	263	125	SEG<124>	-1265	-214
26	DB<5>	675	263	76	NC	-1825	263	126	SEG<123>	-1243	-214
27	DB<6>	625	263	77	NC	-1875	263	127	SEG<122>	-1221	-214
28	DB<7>	575	263	78	NC	-1925	263	128	SEG<121>	-1199	-214
29	VSS1	525	263	79	NC	-2079	214	129	SEG<120>	-1177	-214
30	VDD1	475	263	80	COM<65>	-2101	214	130	SEG<119>	-1155	-214
31	C68	425	263	81	COM<63>	-2123	214	131	SEG<118>	-1133	-214
32	PS	375	263	82	COM<61>	-2145	214	132	SEG<117>	-1111	-214
33	IIC	325	263	83	NC	-2167	214	133	SEG<116>	-1089	-214
34	CLS	275	263	84	NC	-2167	-214	134	SEG<115>	-1067	-214
35	CL	225	263	85	COM<59>	-2145	-214	135	SEG<114>	-1045	-214
36	TEST3	175	263	86	COM<57>	-2123	-214	136	SEG<113>	-1023	-214
37	HPMB	125	263	87	COM<55>	-2101	-214	137	SEG<112>	-1001	-214
38	VDD1	75	263	88	COM<53>	-2079	-214	138	SEG<111>	-979	-214
39	VDD1	25	263	89	COM<51>	-2057	-214	139	SEG<110>	-957	-214
40	VDD4	-25	263	90	COM<49>	-2035	-214	140	SEG<109>	-935	-214
41	VDD4	-75	263	91	COM<47>	-2013	-214	141	SEG<108>	-913	-214
42	VDD3	-125	263	92	COM<45>	-1991	-214	142	SEG<107>	-891	-214
43	VDD3	-175	263	93	COM<43>	-1969	-214	143	SEG<106>	-869	-214
44	VDD2	-225	263	94	COM<41>	-1947	-214	144	SEG<105>	-847	-214
45	VDD2	-275	263	95	COM<39>	-1925	-214	145	SEG<104>	-825	-214
46	VDD2	-325	263	96	COM<37>	-1903	-214	146	SEG<103>	-803	-214
47	VDD2	-375	263	97	COM<35>	-1881	-214	147	SEG<102>	-781	-214
48	TEST1	-425	263	98	COM<33>	-1859	-214	148	SEG<101>	-759	-214
49	TEST2	-475	263	99	COM<31>	-1837	-214	149	SEG<100>	-737	-214
50	VOP	-525	263	100	COM<29>	-1815	-214	150	SEG<99>	-715	-214

Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)
151	SEG<98>	-693	-214	201	SEG<48>	407	-214	251	COM<2>	1507	-214
152	SEG<97>	-671	-214	202	SEG<47>	429	-214	252	COM<4>	1529	-214
153	SEG<96>	-649	-214	203	SEG<46>	451	-214	253	COM<6>	1551	-214
154	SEG<95>	-627	-214	204	SEG<45>	473	-214	254	COM<8>	1573	-214
155	SEG<94>	-605	-214	205	SEG<44>	495	-214	255	COM<10>	1595	-214
156	SEG<93>	-583	-214	206	SEG<43>	517	-214	256	COM<12>	1617	-214
157	SEG<92>	-561	-214	207	SEG<42>	539	-214	257	COM<14>	1639	-214
158	SEG<91>	-539	-214	208	SEG<41>	561	-214	258	COM<16>	1661	-214
159	SEG<90>	-517	-214	209	SEG<40>	583	-214	259	COM<18>	1683	-214
160	SEG<89>	-495	-214	210	SEG<39>	605	-214	260	COM<20>	1705	-214
161	SEG<88>	-473	-214	211	SEG<38>	627	-214	261	COM<22>	1727	-214
162	SEG<87>	-451	-214	212	SEG<37>	649	-214	262	COM<24>	1749	-214
163	SEG<86>	-429	-214	213	SEG<36>	671	-214	263	COM<26>	1771	-214
164	SEG<85>	-407	-214	214	SEG<35>	693	-214	264	COM<28>	1793	-214
165	SEG<84>	-385	-214	215	SEG<34>	715	-214	265	COM<30>	1815	-214
166	SEG<83>	-363	-214	216	SEG<33>	737	-214	266	COM<32>	1837	-214
167	SEG<82>	-341	-214	217	SEG<32>	759	-214	267	COM<34>	1859	-214
168	SEG<81>	-319	-214	218	SEG<31>	781	-214	268	COM<36>	1881	-214
169	SEG<80>	-297	-214	219	SEG<30>	803	-214	269	COM<38>	1903	-214
170	SEG<79>	-275	-214	220	SEG<29>	825	-214	270	COM<40>	1925	-214
171	SEG<78>	-253	-214	221	SEG<28>	847	-214	271	COM<42>	1947	-214
172	SEG<77>	-231	-214	222	SEG<27>	869	-214	272	COM<44>	1969	-214
173	SEG<76>	-209	-214	223	SEG<26>	891	-214	273	COM<46>	1991	-214
174	SEG<75>	-187	-214	224	SEG<25>	913	-214	274	COM<48>	2013	-214
175	SEG<74>	-165	-214	225	SEG<24>	935	-214	275	COM<50>	2035	-214
176	SEG<73>	-143	-214	226	SEG<23>	957	-214	276	COM<52>	2057	-214
177	SEG<72>	-121	-214	227	SEG<22>	979	-214	277	COM<54>	2079	-214
178	SEG<71>	-99	-214	228	SEG<21>	1001	-214	278	COM<56>	2101	-214
179	SEG<70>	-77	-214	229	SEG<20>	1023	-214	279	COM<58>	2123	-214
180	SEG<69>	-55	-214	230	SEG<19>	1045	-214	280	COM<60>	2145	-214
181	SEG<68>	-33	-214	231	SEG<18>	1067	-214	281	NC	2167	-214
182	SEG<67>	-11	-214	232	SEG<17>	1089	-214	282	NC	2167	214
183	SEG<66>	11	-214	233	SEG<16>	1111	-214	283	COM<62>	2145	214
184	SEG<65>	33	-214	234	SEG<15>	1133	-214	284	COM<64>	2123	214
185	SEG<64>	55	-214	235	SEG<14>	1155	-214	285	COM<65>	2101	214
186	SEG<63>	77	-214	236	SEG<13>	1177	-214	286	NC	2079	214
187	SEG<62>	99	-214	237	SEG<12>	1199	-214	(END)	----	----	----
188	SEG<61>	121	-214	238	SEG<11>	1221	-214				
189	SEG<60>	143	-214	239	SEG<10>	1243	-214				
190	SEG<59>	165	-214	240	SEG<9>	1265	-214				
191	SEG<58>	187	-214	241	SEG<8>	1287	-214				
192	SEG<57>	209	-214	242	SEG<7>	1309	-214				
193	SEG<56>	231	-214	243	SEG<6>	1331	-214				
194	SEG<55>	253	-214	244	SEG<5>	1353	-214				
195	SEG<54>	275	-214	245	SEG<4>	1375	-214				
196	SEG<53>	297	-214	246	SEG<3>	1397	-214				
197	SEG<52>	319	-214	247	SEG<2>	1419	-214				
198	SEG<51>	341	-214	248	SEG<1>	1441	-214				
199	SEG<50>	363	-214	249	NC	1463	-214				
200	SEG<49>	385	-214	250	NC	1485	-214				

PAD DESCRIPTION

Power Supply

Name	I/O	Description
VDD1	Power Supply	Logic power supply The input voltage range is 2.4V ≤ VDD1 ≤ 3.6V
VDD2	Power Supply	DCDC Power source The input voltage range is 2.4V ≤ VDD2 ≤ 3.6V
VDD3	Power Supply	OSC Power source The input voltage range is 2.4V ≤ VDD3 ≤ 3.6V
VDD4	Power Supply	Analog power supply The input voltage range is 2.4V ≤ VDD4 ≤ 3.6V
VSS1	Power Supply	Logic Ground
VSS2	Power Supply	DCDC Ground
VSS4	Power Supply	Analog Ground
VPP	Power Supply	MTP (Multi-Times-Program) power source. Just keep open when not in MTP programming section
V0 V1 V2 V3 V4	I/O	LCD driver supply voltages The voltage determined by LCD pixel is impedance-converted by an operational amplifier for application. Voltages should have the following relationship; V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS1/VSS2/VSS4=GROUND When the internal power circuit is active, these voltages are generated as following as following table according to the state of LCD bias.

LCD bias	V1	V2	V3	V4
1/11 bias	(10/11) x V0	(9/11) x V0	(2/11) x V0	(1/11) x V0
1/10 bias	(9/10) x V0	(8/10) x V0	(2/10) x V0	(1/10) x V0
1/9 bias	(8/9) x V0	(7/9) x V0	(2/9) x V0	(1/9) x V0
1/8 bias	(7/8) x V0	(6/8) x V0	(2/8) x V0	(1/8) x V0
1/7 bias	(6/7) x V0	(5/7) x V0	(2/7) x V0	(1/7) x V0
1/6 bias	(5/6) x V0	(4/6) x V0	(2/6) x V0	(1/6) x V0

System Control

Name	I/O	Description
CLS	I	Built-in oscillator circuit enable / disable select pin - CLS = “H” : enable (this pin is used together with digital command) - CLS = “L” : disable (external display clock input through CL pin)
CL	I/O	External clock input pin, It must fix to VSS1 or VDD1 when CLS is “H”
HPMB	I	Power circuit driving ability control - HPMB = “H” : Normal mode - HPMB = “L” : High power mode

Micro-Controller Interface

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>RESB</td><td>I</td><td>Hardware Reset input pin
When RESB is “L”, initialization is executed.</td></tr>
<tr><td>PS</td><td>I</td><td>Parallel / serial data input select input, and IIC must set to “H”
<table>
<tr><th>PS</th><th>Interface mode</th><th>Chip select</th><th>Data / instruction</th><th>Data</th><th>Read / Write</th><th>Serial clock</th></tr>
<tr><td>H</td><td>Parallel</td><td>CS1B, CS2</td><td>A0</td><td>DB0 to DB7</td><td>E_RDB RW_WRB</td><td>--</td></tr>
<tr><td>L</td><td>Spi3/spi4</td><td>CS1B, CS2</td><td>-</td><td>SDA (DB7)</td><td>Write/Read</td><td>SCL (DB6)</td></tr>
</table>
<NOTE> In serial mode, DB0 to DB5 and E_RDB and RW_WRB must be fixed to either “H” or “L”. It also define as ID0 when IIC interface (IIC=”L”) is use.</td></tr>
<tr><td>C68</td><td>I</td><td>Microprocessor Interface Select input pin in parallel mode(when IIC=”H”,PS=”H”)
- C68 = “H” : 6800-series MPU interface
- C68 = “L” : 8080-series MPU interface
It also define as ID1 when IIC interface(IIC=”L”) is use</td></tr>
<tr><td>CS1B
CS2</td><td>I</td><td>Chip select input pins
Data / instruction I/O is enabled only when CS1B is “L” and CS2 is “H”. when chip select is non-active, DB0 to DB7 may be high impedance.</td></tr>
<tr><td>IIC</td><td>I</td><td>IIC mode selection pin. IIC mode is enabled when IIC is “L”, CS1B must fix at “L”, and it disabled when IIC is “H”</td></tr>
<tr><td>A0</td><td>I</td><td>Register select input pin
- A0 = “H” : DB0 to DB7 are display data
- A0 = “L” : DB0 to DB7 are control data</td></tr>
<tr><td>RW_WRB</td><td>I</td><td>Read / Write execution control pin
<table>
<tr><th>C68</th><th>MPU Type</th><th>RW_WRB</th><th>Description</th></tr>
<tr><td>H</td><td>6800-series</td><td>RW</td><td>Read / Write control input pin
- RW = “H” : read
- RW = “L” : write</td></tr>
<tr><td>L</td><td>8080-series</td><td>/WRB</td><td>Write enable clock input pin
The data on DB0 to DB7 are latched at the rising edge of the /WRB signal.</td></tr>
</table></td></tr>
<tr><td>E_RDB</td><td>I</td><td>Read / Write execution control pin
<table>
<tr><th>C68</th><th>MPU Type</th><th>E_RDB</th><th>Description</th></tr>
<tr><td>H</td><td>6800-series</td><td>E</td><td>Read / Write control input pin
- RW = “H” : When E is “H”, DB0 to DB7 are in an output status.
- RW = “L”: The data on DB0 to DB7 are latched at the falling edge the E signal.</td></tr>
<tr><td>L</td><td>8080-series</td><td>/RDB</td><td>Read enable clock input pin
When / RDB is “L”, DB0 to DB7 are in an output status.</td></tr>
</table></td></tr>
<tr><td>DB0
to
DB7</td><td>I/O</td><td>8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus. When the serial interface selected (PS = “L”);
- DB0 to DB5 : high impedance
- DB6 : serial input clock (SCL)
- DB7 : serial input data (SDA)
When chip select is not active, DB0 to DB7 may be high impedance.</td></tr>
<tr><td>VOP</td><td>I/O</td><td>Test pin, must keep them open</td></tr>
</table>

V0I	I	V0I is the power of COM and SEG driver
V0S	I	V0S is the sensor of the V0 generator
V0O	O	V0O is the output of V0 generator
TEST1~2	I/O	Test pins, must keep them open
TEST3	I	Test pin, let it “L” when not be used

LCD Driver Outputs

<table>
<tr><th>Name</th><th>I/O</th><th colspan="4">Description</th></tr>
<tr><td rowspan="8">SEG1 ~
SEG132</td><td rowspan="8">O</td><td colspan="4">LCD segment driver outputs
The display data and the FR signal control the output voltage of segment driver.</td></tr>
<tr><td rowspan="2">Display data</td><td rowspan="2">M</td><td colspan="2">Segment driver output voltage</td></tr>
<tr><td>Normal display</td><td>Reverse display</td></tr>
<tr><td>H</td><td>H</td><td>V0</td><td>V2</td></tr>
<tr><td>H</td><td>L</td><td>GROUND</td><td>V3</td></tr>
<tr><td>L</td><td>H</td><td>V2</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V3</td><td>GROUND</td></tr>
<tr><td colspan="2">Power save mode</td><td>GROUND</td><td>GROUND</td></tr>
<tr><td rowspan="6">COM1 ~
COM65</td><td rowspan="6">O</td><td colspan="4">LCD common driver outputs
The internal scanning data and the FR signal control the output voltage of segment driver.</td></tr>
<tr><td>Scan data</td><td>M</td><td colspan="2">Common driver output voltage</td></tr>
<tr><td>H</td><td>H</td><td colspan="2">GROUND</td></tr>
<tr><td>H</td><td>L</td><td colspan="2">V0</td></tr>
<tr><td>L</td><td>H</td><td colspan="2">V1</td></tr>
<tr><td>L</td><td>L</td><td colspan="2">V4</td></tr>
<tr><td colspan="2">Power save mode</td><td colspan="2">GROUND</td></tr>
</table>

I/O PIN ITO Resister Limitation

PIN Name	ITO Resister
VDD1, VDD3,VDD4,VSS1, VSS4,V0O,V0I	<200Ω
VDD2, VSS2,	<100Ω
V0,V1,V2,V3,V4,V0S	<300Ω
CS1B,CS2,RW_WRB,E_RDB,A0,DB0~DB7	<1KΩ
DB6(SCL) and DB7(SDA) for IIC interface	< 500Ω
RESB	<10KΩ
CL,C68,PS,HPMB,CLS,TEST3,IIC,VOP	No Limitation
TEST1, TEST2	Floating
VPP	<200Ω

FUNCTIONAL DESCRIPTION

Microprocessor Interface

Chip select control

There are CS1B and CS2 pins for chip selection. The IST3931 can interface with an MPU only when CS1B is "L" and CS2 is "H". When these pins are set to any other combination, A0, E_RDB, and RW_WRB inputs are disabled and DB0 to DB7 are high impedance. In case of serial interface, the internal shift registers and the counter are reset.

MPU Interface types

IST3931 has five types of MPU interface, which are three serial and two parallel interfaces. This parallel or serial interface is determined by IIC , PS , C68 pin as shown below.

IIC	PS	C68	Type	Interface mode
H	H	H	Parallel	6800-series MPU mode
H	H	L	Parallel	8080-series MPU mod
H	L	H	Serial	3-Line SPI Serial-mode (*2)
H	L	L	Serial	4-Line SPI Serial-mode (*2)
L	ID1(*1)	ID0(*1)	Serial	IIC Serial-mode (*2)

NOTE:
*1) PS/C68 is use as ID1/ID0, IIC host can use ID1/ID0 to select difference IIC device.

*2) For serial Interface, If the serial data(SDA) and serial clock (SCL) pins will be shared with other devices, SPI3 or SPI4 is recommended. If IIC interface is required, there are some application notices that should be regarded. Please contact our FAE member for further information.

Parallel Interface (IIC="H" PS = "H")

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by C68. The type of data transfer is determined by signals at A0, E_RDB and RW_WRB as shown below.

C68	CS1B	CS2	A0	E_RDB	RW_WRB	DB0 to DB7	MPU bus
H	CS1B	CS2	A0	E	RW	DB0 to DB7	6800-series
L	CS1B	CS2	A0	/RDB	/WRB	DB0 to DB7	8080-series

Common	6800-series		8080-series		Description
A0	E_RDB (E)	RW_WRB (RW)	E_RDB (/RDB)	RW_WRB (/WRB)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register (instruction)

Serial Interface (IIC="H" PS = "L")

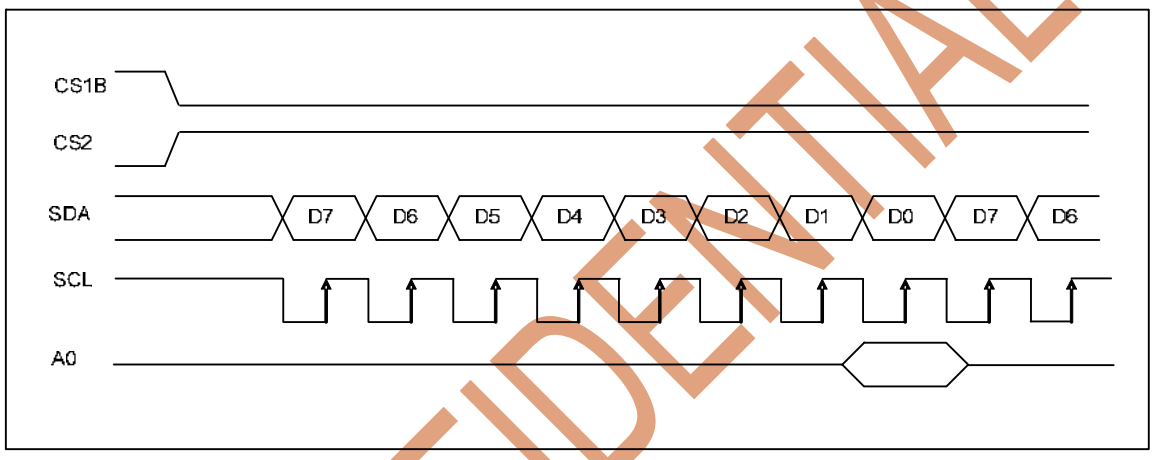
When IIC = "H" PS = "L", the IST3931 is configured as Serial interface(4-line or 3-line), the serial data can be input through DB7 (SDA) and serial clock can be input through DB6 (SCL).

When the chip is not selected, the shift register & serial data counter will be reset and SDA & SCL will also be disabled internally.

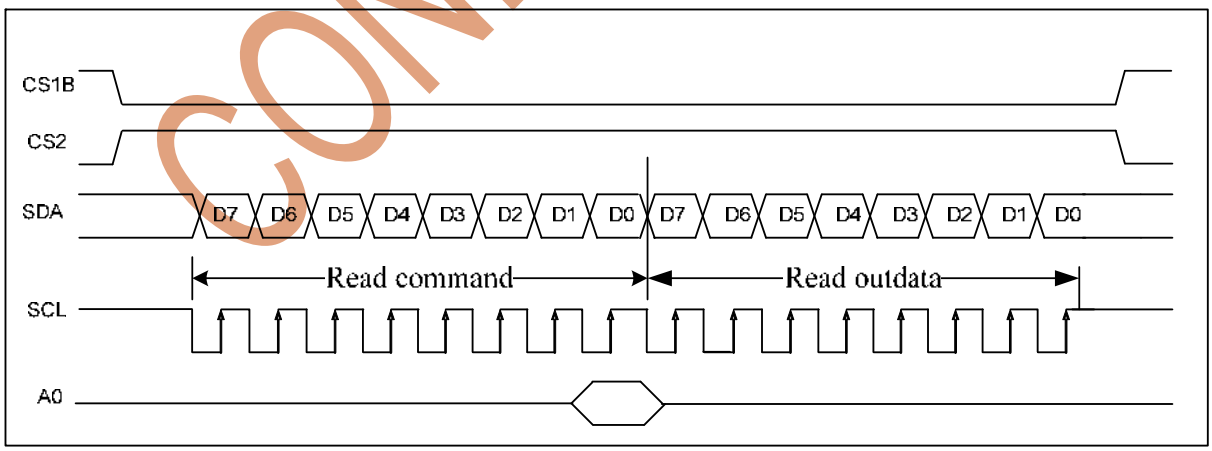
4-Line Serial Interface (IIC="H" PS = "L" C68="L")

When the chip is selected (CS1B="L", CS2="H"), the serial data can be shifted in sequentially at the rising edge of SCL and transferred to 8-bit parallel data internally; at the eighth SCL rising edge, A0 will also be sampled to decide these 8-bit data is interpreted as command or display data.

4-Line Serial Interface Timing



Write operation of 4-Line SPI

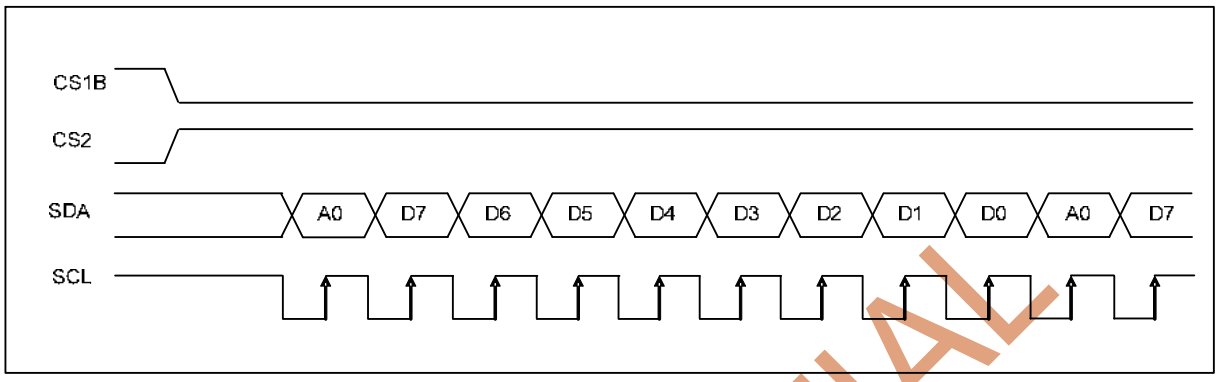


Read operation of 4-Line SPI

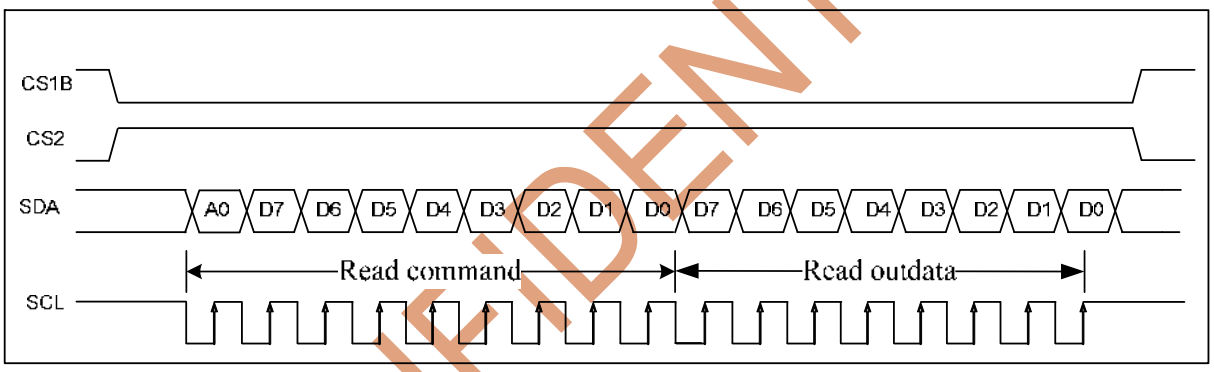
3-Line Serial Interface (IIC="H" PS = "L" C68="H")

In 3-Line interface, A0 signal is not available and the 1st output of SDA will be treated as A0 flag.

3-Line Serial Interface Timing



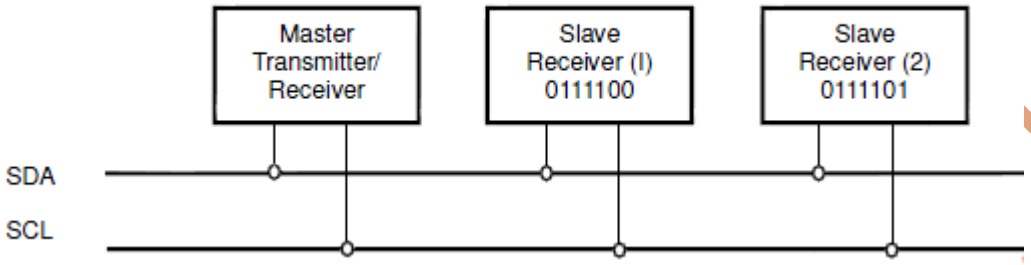
Write operation of 3-Line SPI



Read operation of 3-Line SPI

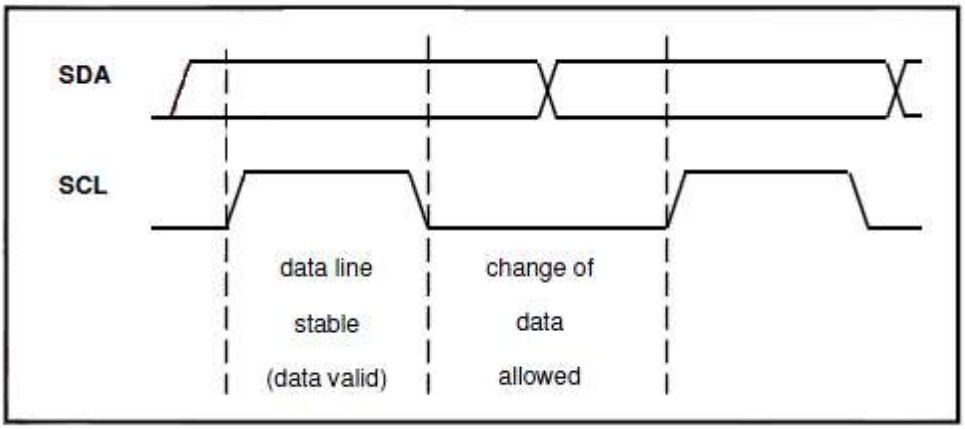
IIC Interface

As 80/68-sreies or 4-line serial interface, The IST3931 also supports standard IIC interface for command & display data communication. The IIC interface is a bi-directional, two-line serial interface, the two lines are a Serial Data line(SDA) and a Serial Clock line(SCL), both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.



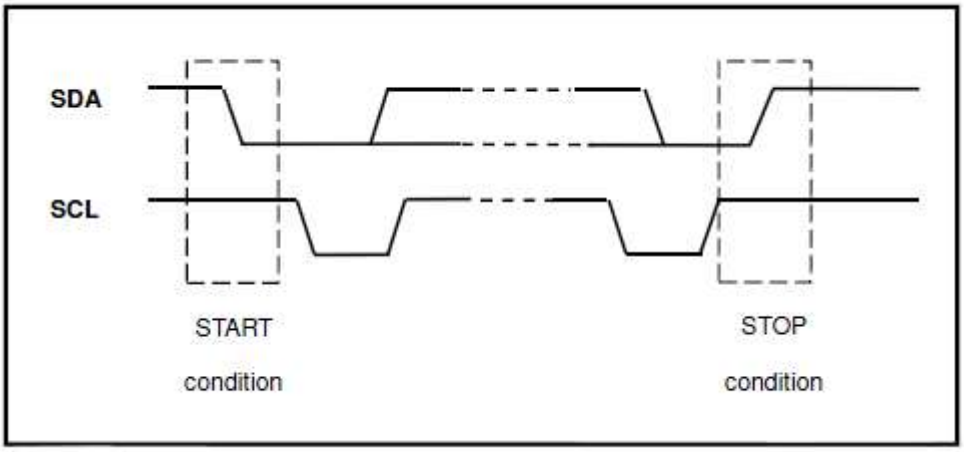
Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse , because changes in the data line at this time will be interpreted as a control signal



START and STOP Conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).



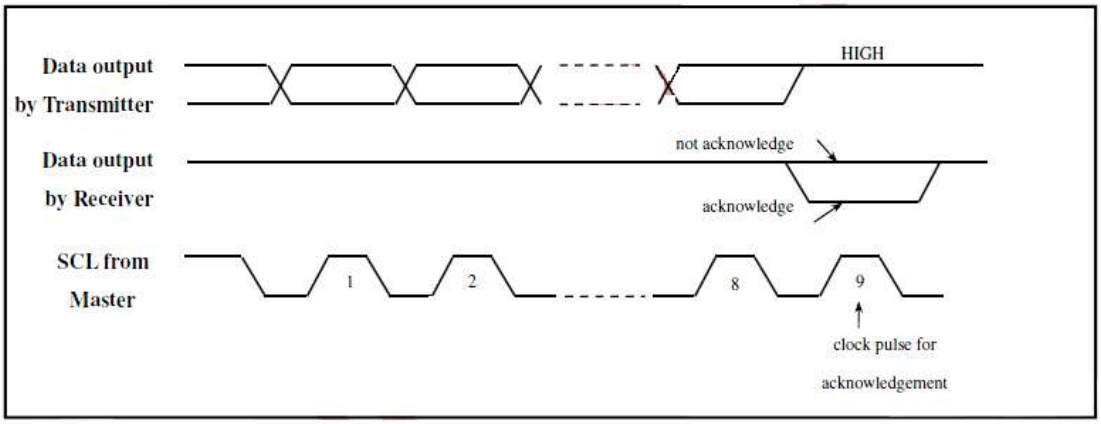
ACKNOWLEDGE

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter(to release the SDA control and waiting for receiver's acknowledgement), during which time the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. A master receiver must also generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledge must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).

A master receiver must signal and end-of-data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.



IIC Interface Protocol

The IIC transmitting is initiated with a START condition (S) from the IIC–bus Master and followed by a slave address. Two 7-bit slave address (0111100, 0111101, 0111110, 0111111) are reserved for the IST3931. The least significant bit of the slave address (ID) is configured by C68 and PS pin to decide is the slave address is 0111100 (C68=0/PS=0) or 0111101 (C68=0/PS=1) or 0111110(C68=1/PS=0) or 0111111(C68=1/PS=1). The 8th bit follows the previous 7-bit address is the data direction bit (R/W) -- '0' indicates Master data transmission (WRITE), '1' indicates Master data request (READ).

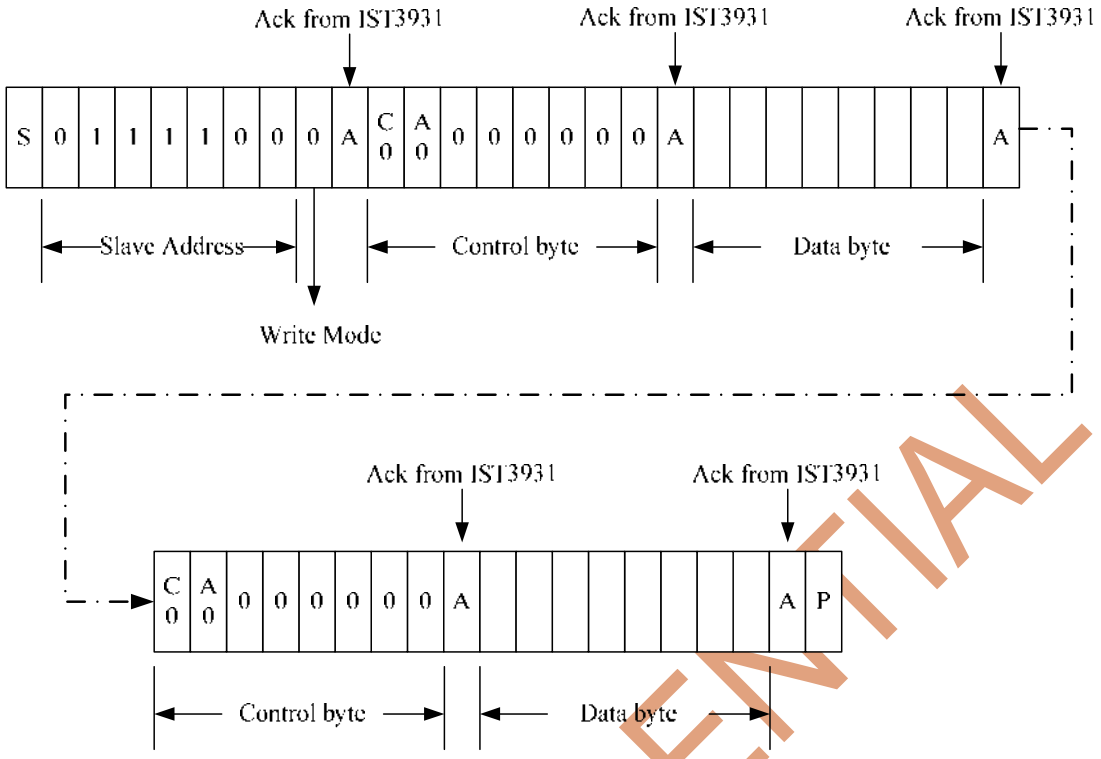
WRITE Mode (Master transmits data to Slave, R/W=0)

Write mode includes Slave address byte, control byte & data byte. After acknowledgement, one or more command words follow which define the status of the addressed slaves. A command word consists of a control byte, which defines C0 and A0, and a data byte. The control and data bytes are also acknowledged by all addressed slaves on the bus.

The C0 bit indicates the continuation of the command, please just set C0=1 during the whole Write transmitting period. The A0 bit decides the interpretation of the data byte. If A0 bit is 0, the data byte will be interpreted as command index, if A0 bit is 1, the data byte will be interpreted as command data.

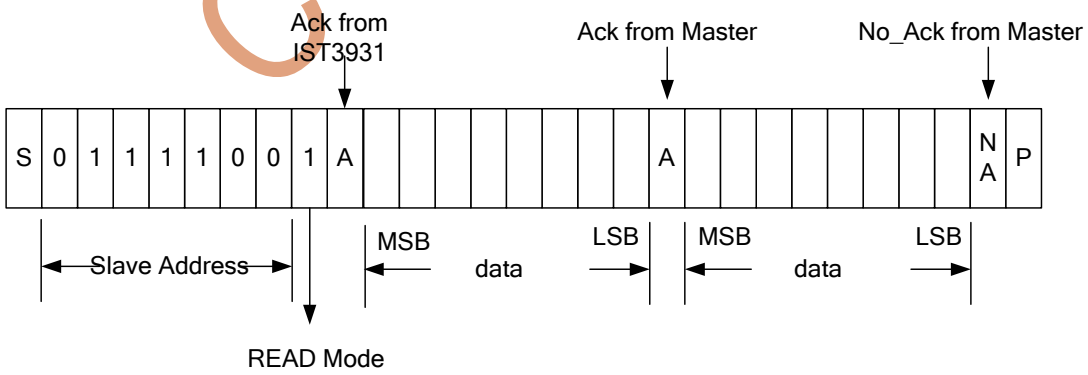
A data transfer is always terminated by a STOP condition (P)generated by the master. However, if master still wishes to communicate on the bus, it can generate a repeated START condition and address another slave without first generating a STOP condition.

WRITE Mode



READ Mode (Master requests data from Slave, R/W=1)

At the moment of the first acknowledge, the Master-transmitter becomes a Master-receiver and the Slave-receiver becomes a Slave transmitter. The first acknowledge is still generated by the slave, but the following data bytes' acknowledgement are generated by Master. The STOP and Re-START conditions are generated by Master. If Master wants to stop the data request, after the last data byte has been received, send a Non-Acknowledge condition (keep SDA at HIGH) and trigger a STOP condition.



Busy Flag

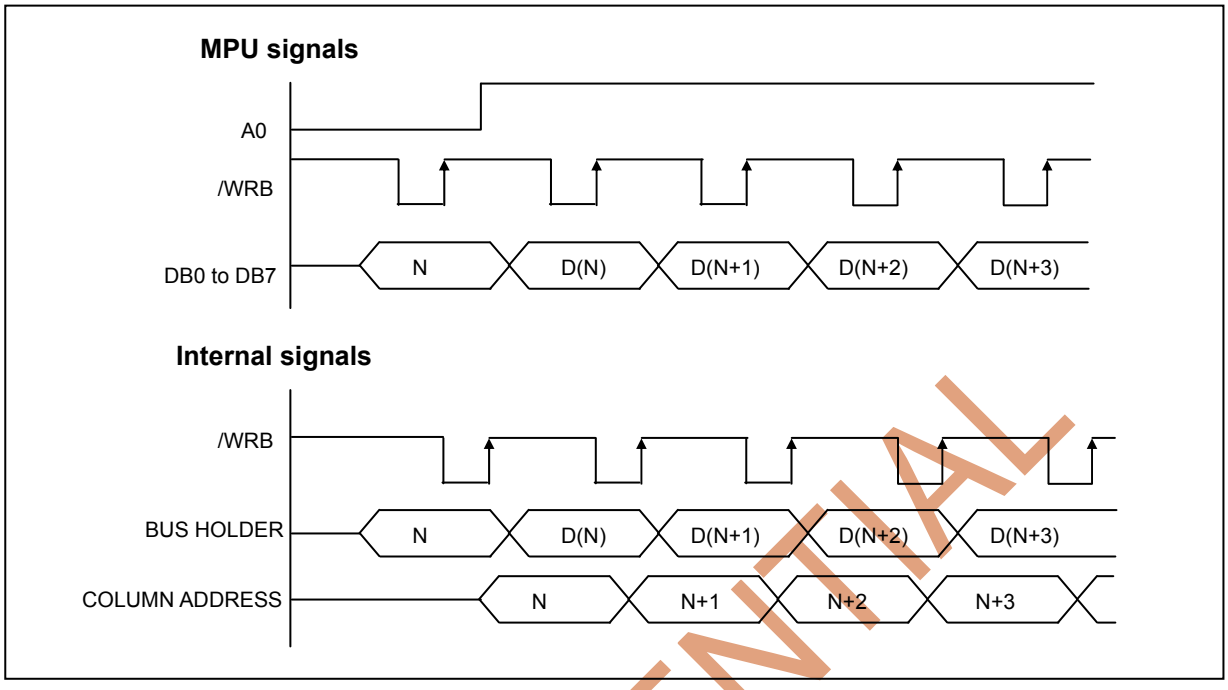
The Busy Flag indicates whether the IST3931 is still during operation or not. When DB7 is “H” in read status operation, this device is in busy status and will accept only read status instruction. If the write cycle time is correct, the microprocessor needs not to check this flag before each instruction to improve the operation efficiency.

Data Transfer

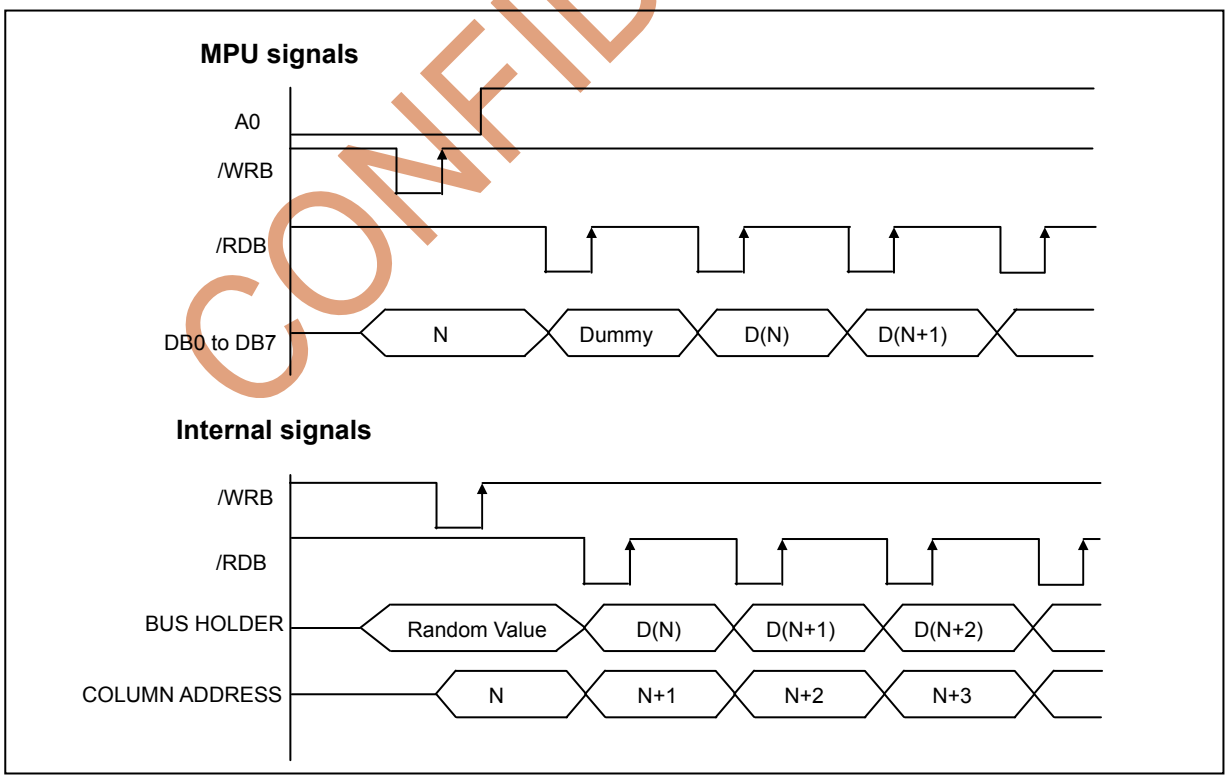
The IST3931 has a I/O bus holder stage to temporary storage the data received from MPU or on-chip RAM data requesting from MPU to read.

When user wants to read out the on-chip RAM data, after setting the address, a “dummy read” cycle must be inserted first to clean out the data stored in the output bus holder, so please just skip this dummy read data and the target RAM data can be read out from the second read cycle.

Write Timing



Read Timing



Display RAM Address Mapping

The IST3931 embedded a one-on-one bit-pixel mapping display RAM to storage the display image data. The RAM size is 65(row) x 132(column) bits. Each pixel can be selected when the row and column addresses are specified. Data is read from or written to by 8-bit width through DB0 to DB7. The display data & LCD display mapping is illustrated as below.

The display RAM is designed with two ports, so when display is turned on, the internal LCD display operation and MPU display RAM access is independent and will not affect each other

ADC=0	AX		00H								01H								02H	…		…	10H								11H							
	Data		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D7	…	D0	…	D7	D6	D5	D4	x	x	x	x	x	x	x	x	x	x	x	x
SHL=0	SHL=1	AY	seg1	seg2	seg3	seg4	seg5	seg6	seg7	seg8	seg9	seg10	seg11	seg12	seg13	seg14	seg15	seg16	seg17	…	seg24	…	Seg129	Seg130	Seg131	Seg132	X	X	X	X	X	X	X	X	X	X	X	X
COM1	COM65	00H	Address 0000H								Address 0001H								0002H	…		…	0010H								0011H							
COM2	COM64	01H	Address 0100H								Address 0101H								0102H	…		…	0110H								0111H							
COM3	COM63	02H	Address 0200H								Address 0201H								0202H	…		…	0210H								0211H							
COM4	COM62	03H	Address 0300H								Address 0301H								0302H	…		…	0310H								0311H							
COM5	COM61	04H	Address 0400H								Address 0401H								0402H	…		…	0410H								0411H							
…	…	…	…								…								…	…		…	……								……							
COM62	COM4	3DH	Address 3D00H								Address 3D01H								3D02H	…		…	3D10H								3D11H							
COM63	COM3	3EH	Address 3E00H								Address 3E01H								3E02H	…		…	3E10H								3E11H							
COM64	COM2	3FH	Address 3F00H								Address 3F01H								3F02H	…		…	3F10H								3F11H							
COM65	COM1	40H	Address 4000H								Address 4001H								4002H	…		…	4010H								4011H							
SHL=0	SHL=1	AY	X	X	X	X	X	X	X	X	X	X	X	X	seg1	seg2	seg3	seg4	Seg5	…	Seg6	…	Seg117	Seg118	Seg119	Seg120	Seg121	Seg122	Seg123	Seg124	Seg125	Seg126	Seg127	Seg128	Seg129	Seg130	Seg131	Seg132
ADC=1	AX		11H								10H								0FH	…		…	01H								00H							
	Data		X	X	X	X	X	X	X	X	X	X	X	X	D4	D5	D6	D7	D0	…	D7	…	D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7

Reset Initialization

The IST3931 provides both hardware (H/W) reset and software (S/W) reset function. When the RESB is setting to “L”, the H/W reset will be activated, or user can use S/W reset instruction to initialize the internal registers’ configurations, but the H/W reset and S/W reset covered range is different, please check the table listed as below.

The default H/W reset initializing settings are listed as below:

No.	Register	Description
1.	DON=0	Display OFF
2.	REV=0	Reverse display OFF
3.	ADC=1	SEG output direction SEG132 → SEG1
4.	SHL=0	COM output direction COM1 → COM65
5.	(internal status)	Serial interface internal register data clear
6.	BS=0	LCD bias
7.	EON=0	Entire display OFF
8.	AY=0	Row address
9.	AX=0	Column address
10.	(internal status)	SEG/COM output GROUND level
11.	RMW=0	Read-Modify-Write OFF
12.	ST=0	Display start line address = 0
13.	CT=0000_0000	Electronic volume register

★ For S/W reset , only the 1 ~ 12 items above will be reinitialized.

When doing the H/W reset (RESB = “L”), the V0 will also discharge to GROUND level internally, so when using external LCD power sources, please input these power sources only when the H/W reset process has been finished (RESB is backing to “H”) .

Command Table

* : Don't care

NO.	INSTRUCTION	A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
1	Set AY(2B)	0	0	0	0	0	0	AY3	AY2	AY1	AY0	Set column address LSB
		0	0	0	0	0	1	*	AY6	AY5	AY4	Set column address MSB
2	Power Control	0	0	0	0	1	0	1	1	VC	VF	Power control
3	Select LCD Bias	0	0	0	0	1	1	0	BS2	BS1	BS0	Set LCD bias
4	Sleep Mode	0	0	0	0	1	1	1	0	0	SLP	Power save mode 1:sleep
5	OSC Control	0	0	0	0	1	1	1	0	1	OSCOFF	0: OSC on; 1:OSC off
6	Display On/Off	0	0	0	0	1	1	1	1	0	DON	Turn on/off LCD 0:off;1:on
7	Set Starting Line(2B)	0	0	0	1	0	0	ST3	ST2	ST1	ST0	Set starting line -LSB
		0	0	0	1	0	1	*	ST6	ST5	ST4	Set starting line -MSB
8	Driver Display Control	0	0	0	1	1	0	SHL	ADC	EON	REV	Driver display control
9	S/W reset	0	0	0	1	1	1	0	1	1	0	Soft reset
10	Set Duty(2B)	0	0	1	0	0	1	DUTY3	DUTY2	DUTY1	DUTY0	Set duty-LSB
		0	0	1	0	1	0	*	DUTY6	DUTY5	DUTY4	Set duty-MSB
11	Set AX Address	0	0	1	1	0	AX4	AX3	AX2	AX1	AX0	Set AX address
12	Read Status	0	1	BUSY	ADC	DONB	RESB	0	0	0	0	Read the internal status
13	SPI3&SPI4 Read Status Command	0	0	0	1	1	1	1	0	0	0	SPI3&SPI4&IIC read status command
14	Write Display Data	1	0	Write Data								Write data into display RAM
15	Read Display Data	1	1	Read Data								Read data from display RAM
16	SPI3&SPI4 Read Ram Command	0	0	0	1	1	1	0	1	1	1	SPI3&SPI4 read ram data command
17	Reference Voltage Select(2B)	0	0	1	0	1	1	0	0	0	1	Set reference voltage mode
				CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0	
18	Frame Control (3B)	0	0	1	0	1	1	0	0	1	0	Set frame control
				LN7	LN6	LN5	LN4	LN3	LN2	LN1	LN0	
				LN15	LN14	LN13	LN12	LN11	LN10	LN9	LN8	
19	NOP	0	0	1	1	1	0	0	0	1	1	No operation (dummy command)
20	MTP command entry	0	0	1	0	0	0	0	0	0	0	MTP command entry
21	MTP CT Offset enable select	0	0	0	0	0	1	1	0	CTOFTE	0	MTP CT offset enable select
22	MTP Program Enable	0	0	1	1	1	0	1	1	0	0	Programming enable
23	MTP Program Start	0	0	0	0	1	0	0	0	0	0	Programming start

24	MTP CT Offset (2B)	0	0	0	0	1	0	0	1	1	0	CT offset (2B)
				*	*	*	CTOFT 4	CTOFT 3	CTOFT 2	CTOFT 1	CTOFT 0	
25	MTP Manually ADR	0	0	1	0	1	0	0	0	1	0	MTP manually ADR
				*	ADR[6]	ADR[5]	ADR[4]	ADR[3]	ADR[2]	ADR[1]	ADR[0]	
26	Command Register Read Enable	0	0	1	0	0	0	1	1	0	0	Command register read enable
27	IST Command Entry	0	0	1	0	0	0	1	0	0	0	IST command entry, for some hardware operation configuration, it need repeat 4 times to enter
28	COM Mapping	0	0	0	1	1	0	0	0	0	MAP_ MODE	Set com pad map sequence
29	Exit Entry	0	0	1	1	1	0	0	0	1	1	Exit to normal command access

COMMAND DESCRIPTION

1. Set AY (ROW) Address

Set the AY address of display data RAM for MPU Write/Read access. After setting the AY (row) and/or AX (column) address, user can write/read the internal display RAM consecutively. When the AX (Column) address auto-incremented at the end, the AY address will auto-incremented by +1.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	AY3	AY2	AY1	AY0
0	0	0	0	0	1	*	AY6	AY5	AY4

Note: Avoid setting AX before AY

2. Power Control

Internal Power supply circuits On/Off control. For details please refer to the “Power Supply Circuits” section.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	1	1	VC	VF

3. Select LCD Bias

Selects LCD bias ratio of the voltage required for driving the LCD.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	0	BS2	BS1	BS0

4. Sleep Mode

Sleep mode only happen at SLP=1, It’ll stop all the operations in this chip, as long as there are no accesses from the MPU, the power consumption is close to the static leakage current.

set SLP=0 to exit sleep mode

The internal status during sleep mode is as below:

a) The oscillator circuit and the LCD power supply circuit are turned off.

b) All liquid crystal drive circuits are stop, all the LCD driving outputs (SEGx/COMx) output GROUND level.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	0	0	SLP

5. OSC Control

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	0	1	OSCOFF

The oscillator circuit will be turned off when OSCOFF set “H”

6. Display ON / OFF

LCD display ON / OFF select

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	1	0	DON

DON = 1 Display ON
DON = 0 Display OFF

7. Set Starting Line

Set the starting line address for the first common output.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	ST3	ST2	ST1	ST0
0	0	0	1	0	1	*	ST6	ST5	ST4

ST6	ST5	ST4	ST3	ST2	ST1	ST0	Line address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
…	…	…	…	…	…	…	…
1	0	0	0	0	0	0	64

8. Driver display control

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	0	SHL	ADC	EON	REV

SHL: Select (Common Output Mode Select)

SHL = 0: COM1 → COM_N
SHL = 1: COM_N → COM1

N define as duty setting, reference as “SET DUTY”.

ADC:
Defines the relationship between RAM column address and segment driver. The detailed mapping please referred to the “Display RAM Address Mapping” chapter.

ADC = 0: SEG1 → SEG132
ADC = 1: SEG132 → SEG1

EON:

Forces the whole LCD points to be turned on regardless of the contents of the display data RAM. This instruction will not change the original display RAM data and has higher priority than the reverse display ON / OFF instruction.

EON = 0: Normal display
EON = 1: Entire display ON

REV:

Reverse the lit and unlit display relation between RAM bit data and LCD cell. This setting will not change the original display RAM data.

REV	RAM bit data = "1"	RAM bit data = "0"
0	LCD pixel will accumulated ON voltage	LCD pixel will accumulated OFF voltage
1	LCD pixel will accumulated OFF voltage	LCD pixel will accumulated ON voltage

9. S/W Reset

This instruction will activate the internal S/W reset operation. The covered ranged is different with H/W reset, for details please refer to the "Reset Initialization" section.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	1	0	1	1	0

10. Set Duty

This instruction will activate the internal S/W reset operation. The covered ranged is different with H/W reset, for details please refer to the "Reset Initialization" section.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	DUTY3	DUTY2	DUTY1	DUTY0
0	0	1	0	1	0	*	DUTY6	DUTY5	DUTY4

DUTY6	DUTY5	DUTY4	DUTY3	DUTY2	DUTY1	DUTY0	Duty Ratio
0	0	0	0	0	0	0	reserve
0	0	0	0	0	0	1	1/1
…	…	…	…	…	…	…	…
1	0	0	0	0	0	0	1/64
1	0	0	0	0	0	1	1/65

After setting DUTY, Com1~COM_N is select, N=DUTY[6:0].

11. Set AX Address

Sets the Column Address of display data RAM for MPU Write/Read access. After setting the row and/or Column address, user can write/read the internal display RAM consecutively. The Column address will auto-incremented by +1 .

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	AX4	AX3	AX2	AX1	AX0

12. Read Status

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BUSY	ADC	ON/OFF	RESB	0	0	0	0

Flag	Description
BUSY	BUSY = 1 : The chip is still under processing, including reset initialization BUSY = 0 : The chip is free to accept MPU commands
ADC	ADC = 1 : SEG direction is SEG132 → SEG1 ADC = 0 : SEG direction is SEG1 → SEG132
DISPLAY ON/OFF	ON/OFF = 1 : Display is turned off ON/OFF = 0 : Display is turned on * The polarity is reversed with DON command !
RESET	RESET = 0 : The chip is doing the H/W or S/W reset RESET = 1 : The chip is not doing the reset operation

13. SPI3 & SPI4 read status command

Indicate the internal status. When use SPI3, SPI4 or IIC interface, it must send the command 78H before read operation.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	1	1	1	0	0	0

Only use in SPI3, SPI4 or IIC interface

14. Write Display Data

8-bit display data can be written to the display RAM location specified by the column address and row address by this instruction. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed rows.

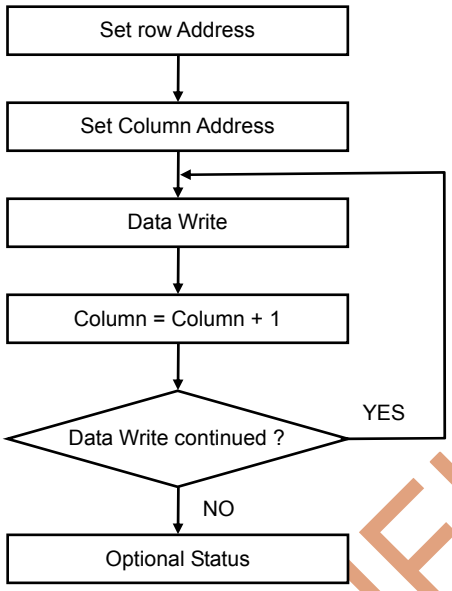
A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	Write data							

15. Read Display Data

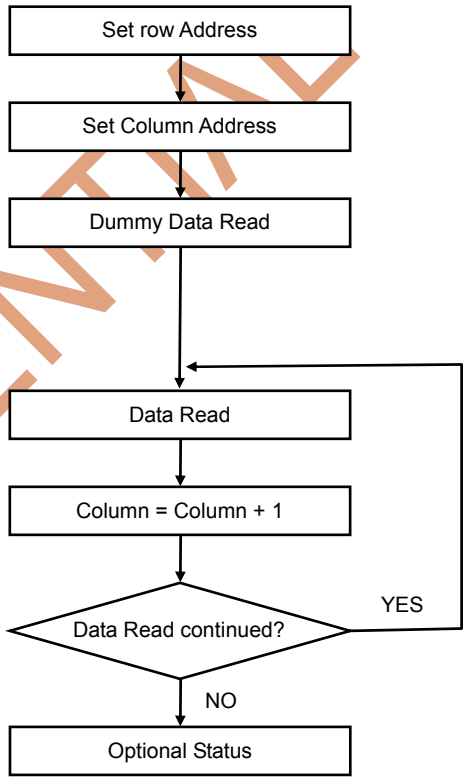
8-bit display data RAM specified by the column address and row address can be read by this instruction. As the column address is increased by 1 automatically after each this instruction, the microprocessor can continuously can continuously read data from the addressed row. A dummy read is required after specified the target column and/or row address.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Read data							

Display RAM Write Sequence



Display RAM Read Sequence



16. SPI3 & SPI4 read ram command

When use SPI3, SPI4 or IIC interface, it must send the command 77H before read operation.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	1	0	1	1	1

Only use in SPI3, SPI4 or IIC interface

17. **Reference Voltage Select (double byte command)**

The Reference voltage select instruction consists of 2-byte command. The 1st instruction sets reference voltage mode and the 2nd one is the contents of reference voltage register. These two instructions must be executed adjacently or the following commands sequence will be misinterpreted and lead to unexpected results.

The 1st instruction : Set Reference Voltage Select Mode

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	0	0	0	1

The 2nd instruction : Set Reference Voltage Register

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0

CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0	Reference voltage Parameter (α)	V0	Contrast
0	0	0	0	0	0	0	0	0（default）	Minimum	Low
0	0	0	0	0	0	0	1	1		
:	:	:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	0	0	128	:	:
:	:	:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	0	254		
1	1	1	1	1	1	1	1	255	Maximum	High

V0 calculation:

*V0= [0.7+CT*0.005]/Bias at 24 ^{0}C if the MTP is Pre-programmed*
*or V0= [0.7+ (CT+CTOFT)*0.005]/Bias（if using the MTP Programmed）*

<Example>

*CT =3CH , Bias=1/9, then V0=(0.7+60*0.005)/(1/9)=9.0V*

18. Frame Control (Three bytes command)

The Frame Control instruction consists by three commands. The 1st instruction sets Frame Control mode, the 2nd and 3rd command set the Frame frequency DIV number

The 1st instruction: sets Frame Control mode

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	0	0	1	0

The 2nd and 3rd instruction :

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	LN7	LN6	LN5	LN4	LN3	LN2	LN1	LN0
0	0	LN15	LN14	LN13	LN12	LN11	LN10	LN9	LN8

LN15~0: DIV number by inside oscillator (3MHZ)

Row frequency = $3X10^6$/ (LN15~0+1) Frame frequency = **Row frequency / DUTY6~0 (at 25 ^{0}C)**

19. NOP

No-Operation command (dummy command).

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	1

MTP Command Table

INSTRUCTION	A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
MTP CT Offset enable select	0	0	0	0	0	1	1	0	CTOFTE	0
Programming Start	0	0	0	0	1	0	0	0	0	0
CT offset (2B)	0	0	0	0	1	0	0	1	1	0
			*	*	*	CTOFT4	CTOFT3	CTOFT2	CTOFT1	CTOFT0
MTP Manually ADR	0	0	1	0	1	0	0	0	1	0
			*	ADR[6]	ADR[5]	ADR[4]	ADR[3]	ADR[2]	ADR[1]	ADR[0]
Command register read enable	0	0	1	0	0	0	1	1	0	0
Programming Enable	0	0	1	1	1	0	1	1	0	0

CTOFT[4:0]	STEP
0x00	0
0x01	+1
. .	. .
0x0F	+15
0X10	-16
0X11	-15
. .	. .
0X1F	-1

20. MTP Command Entry (80h, repeat 4 times)

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	0

IST3931 embedded MTP (Multi-Time-Programming) memories for users to store individual settings by modules to keep a consistent display quality. User can use 80h command to enter the MTP command mode and then the following commands will be interpreted as MTP commands (listed as above). After the MTP commands' setting have been finished, use NOP (E3h) command can leave the MTP command section and then back to the normal command section.

After entered the MTP command section, user can first use the provided MTP adjustable parameters to preview the adjusted display results, after the display quality has been satisfied, then set the enable select bit and use MTP Program Enable (ECH) and MTP Program Start (20H) command to start programming all the ready registered settings into MTP memory cells at the same time. After the MTP programming has been be finished, the programmed MTP values will be automatically reloaded.

21. MTP CT Offset enable select

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	1	0	CTOFTE	0

CTOFTE=0,disable; CTOFTE=1,enable.

22. MTP Program Enable

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	1	0	0

23. MTP Program Start

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	0	0	0	0

Once execute MTP Program Enable (ECH) command and MTP Program Start (20H) the MTP programming section is enabled and waiting for the MTP Program Start command to automatically starts the whole MTP programming section.

24. MTP CT Offset

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	0	1	1	0
		*	*	*	CTOFT4	CTOFT3	CTOFT2	CTOFT1	CTOFT0

25. MTP Manually ADR

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	1	0
		*	ADR[6]	ADR[5]	ADR[4]	ADR[3]	ADR[2]	ADR[1]	ADR[0]

When ADR[6:0] = 0X1E, the read out data is CTOFT.

26. Command Register Read Enable

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	1	1	0	0

MTP Write Flow

The suggested MTP write flow is listed as below: (Where the VPP Pin supplied 7.0v.)

MTP Write Flow

Step	A0	RW	Command	Description
0	--	--	(Initial)	■ Set Display ON, Power Configuration, Contrast (SV), … etc.
1^{step1}	0	0	80h	■ Enter MTP command mode
1^{step2}	0	0	80h	■ Enter MTP command mode
1^{step3}	0	0	80h	■ Enter MTP command mode
1^{step4}	0	0	80h	■ Enter MTP command mode
2^{A1}	0	0	CTOFT	■ MTP CTOFT adjust (1Fh~00h) if doing the SV offset adjust
3	0	0	MTP Enable Select	■ Set Enable bit for CTOFTE ..and so on
4	0	0	ECh	■ MTP Program enable
5	0	0	20h	■ MTP Program Start
6	0	0	(Waiting)	■ MTP programming section, idle about 10ms to wait the MTP programming section finished
7	0	0	E3h	■ Use NOP command to release MTP command mode
8	--	--	(Initial)	■ Set Display ON, Power Configuration, Contrast (SV), … etc.

Annotation -

A1: maybe need some iteration to get the best display result.

MTP Read Flow

The MTP memory cells data can be read back through parallel interfaces. The suggested MTP read flow is listed as below: (Where the VPP Pin keeps Floating.)

MTP Read Flow

Step	A0	RW	Command	Description
1^{step1}	0	0	80h	■ Enter MTP command mode
1^{step2}	0	0	80h	■ Enter MTP command mode
1^{step3}	0	0	80h	■ Enter MTP command mode
1^{step4}	0	0	80h	■ Enter MTP command mode
2	0	0	Set MTP Address	■ Set MTP read address (MTPRA=1EH)*
3	0	0	8ch	■ Enter Read mode
4	0	1	Read operation	■ Read data from MTP
5	0	0	E3h	■ Use NOP command to release MTP command mode

*Note:1EH store the value of CTOFT.

27. IST Command Entry

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	1	0	0	0

IST command entry, for some hardware operation configuration, it need repeat 4 times to enter

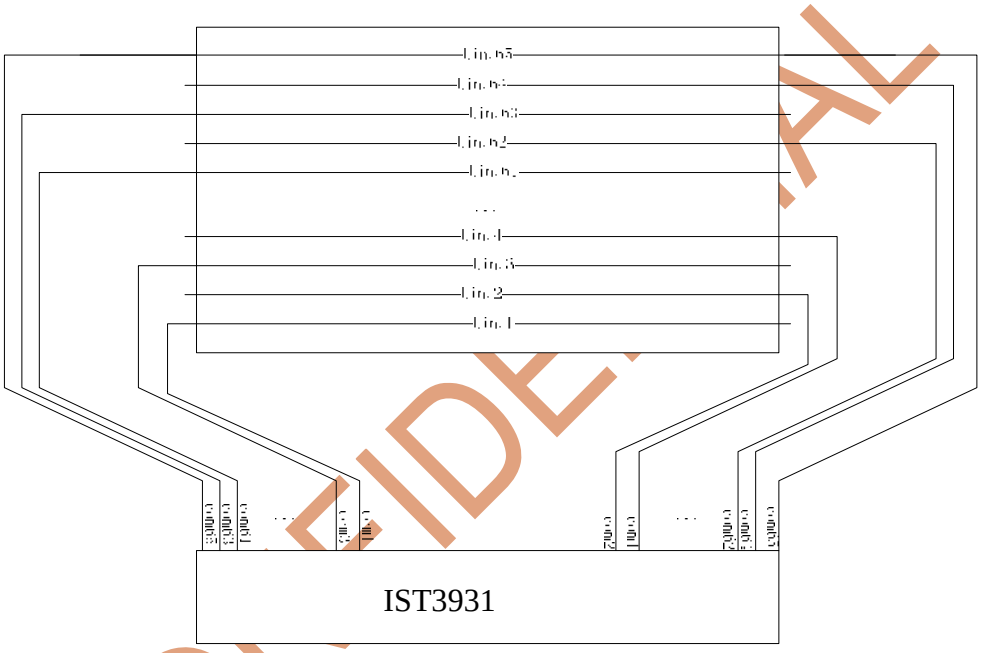
28. COM Mapping

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	0	0	0	0	MAP_MODE

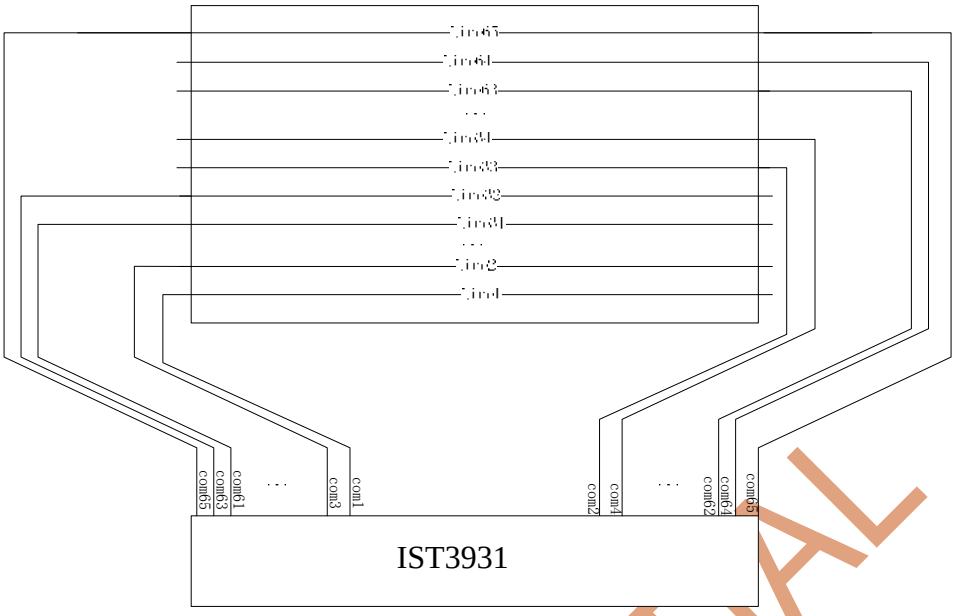
Set com pad map sequence

*MAP_MODE default is 1.

MAP_MODE=0, COM65~1 and panel mapping show as next figure:



MAP_MODE=1, COM65~1 and panel mapping show as next figure:



29. Exit Entry

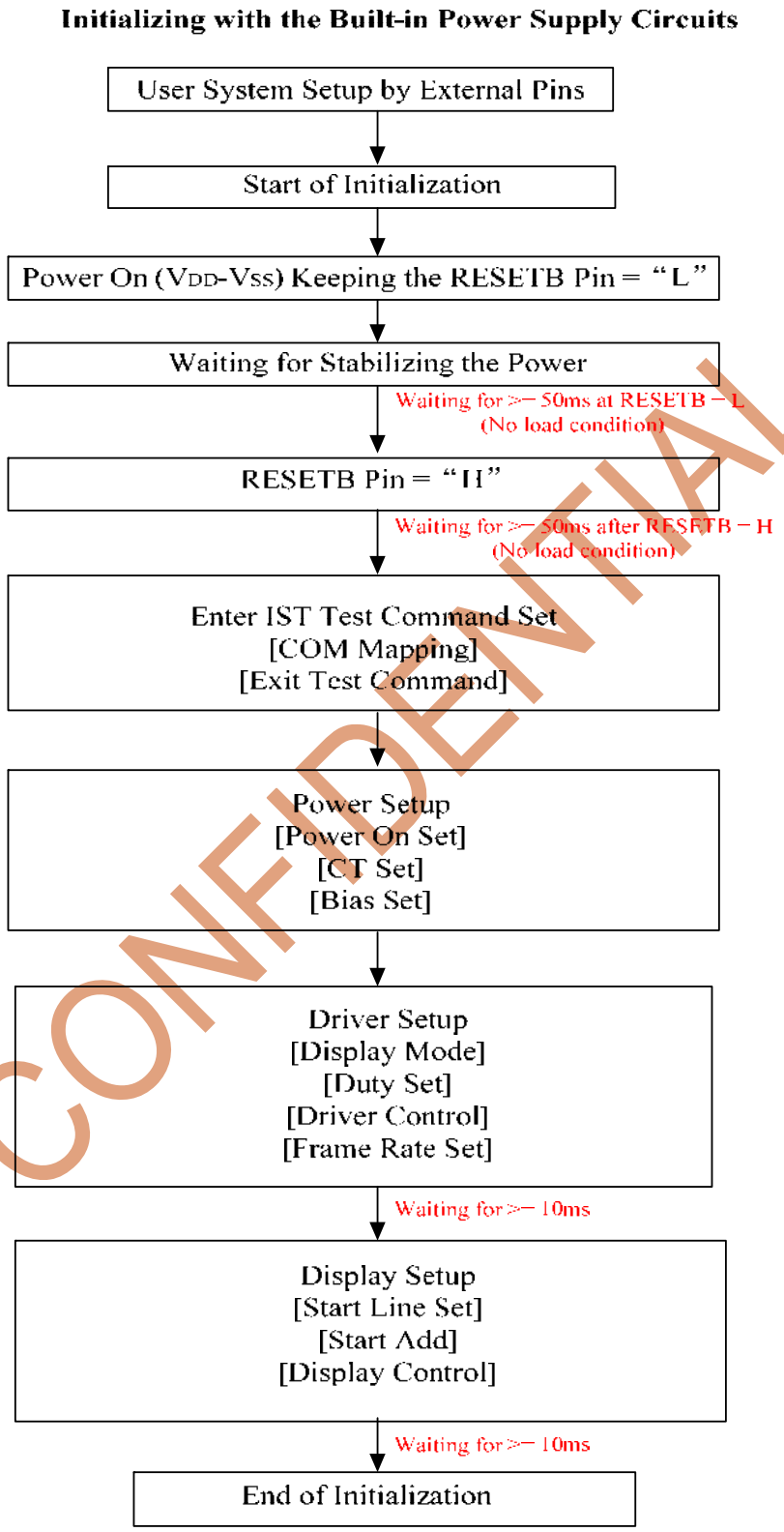
A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	1

Exit to normal command access

IST command write Flow

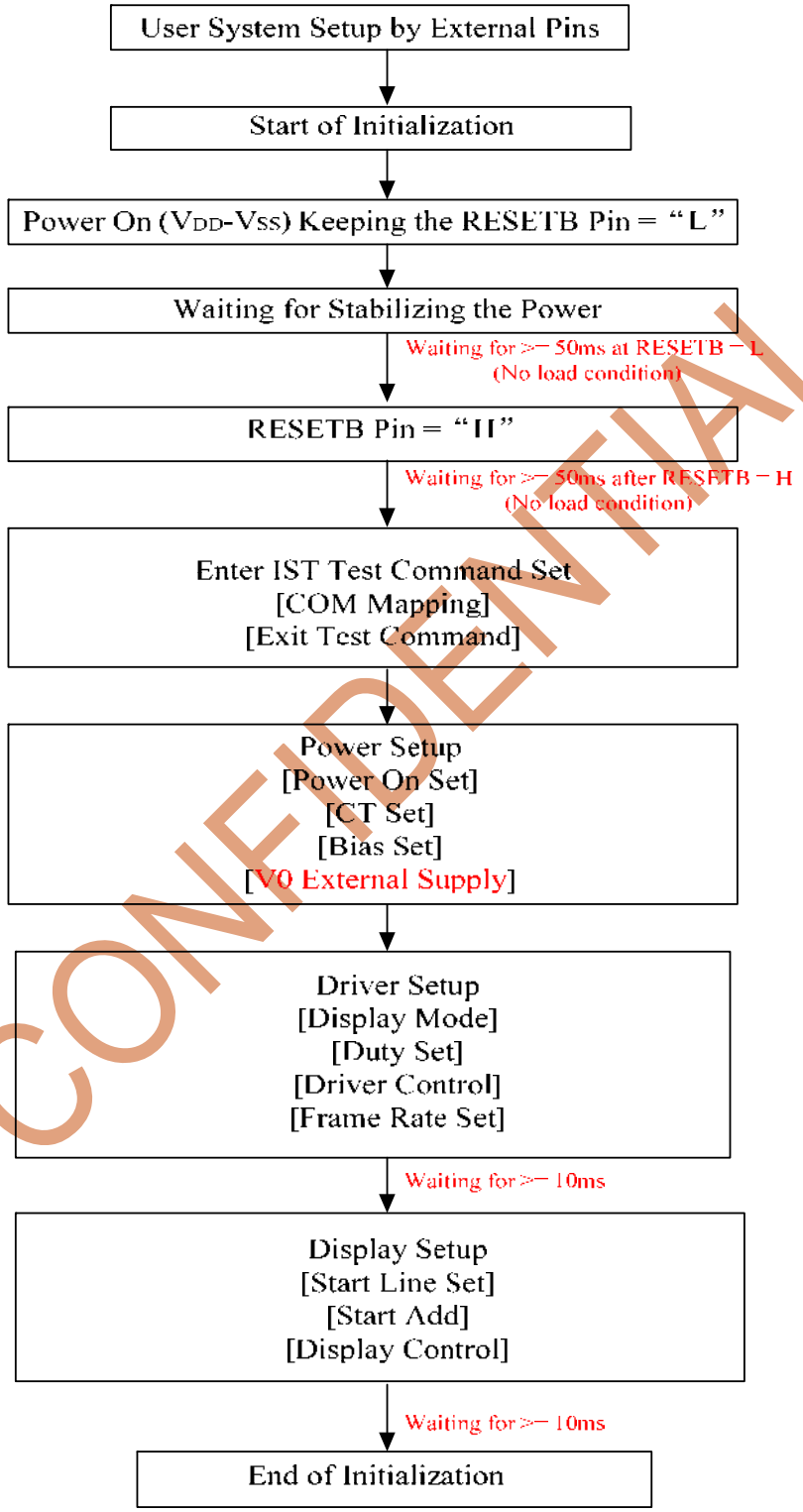
Step	A0	RW	Command	Description
1^{step1}	0	0	88h	■ Enter IST command mode
1^{step2}	0	0	88h	■ Enter IST command mode
1^{step3}	0	0	88h	■ Enter IST command mode
1^{step4}	0	0	88h	■ Enter IST command mode
2	0	0	Set set MAP_MODE	■ Set set MAP_MODE
3	0	0	E3h	■ Use NOP command to release IST command mode

Power On Sequence (1)

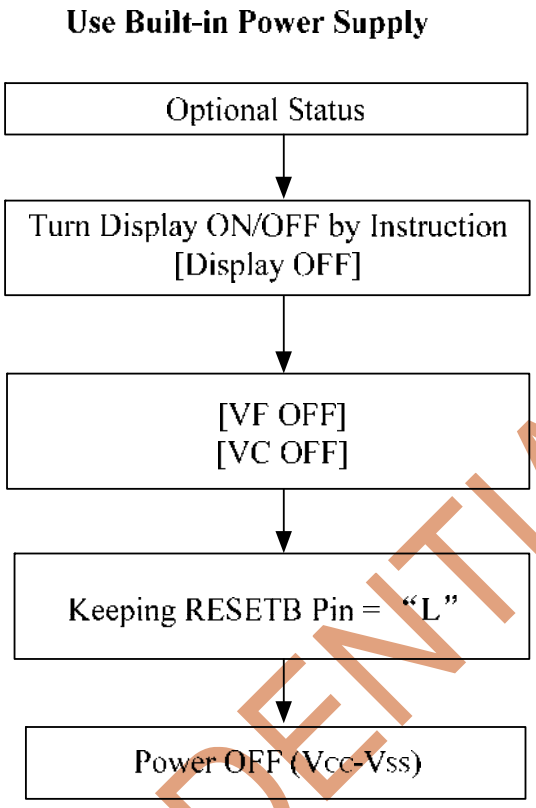


Power On Sequence (2)

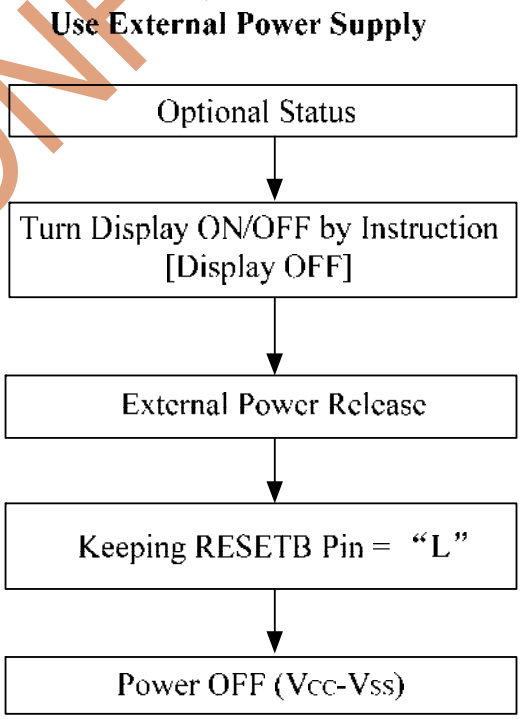
Initializing with the External Power Supply Circuits



Power Off Sequence (1)



Power Off Sequence (2)



Power Supply Circuits

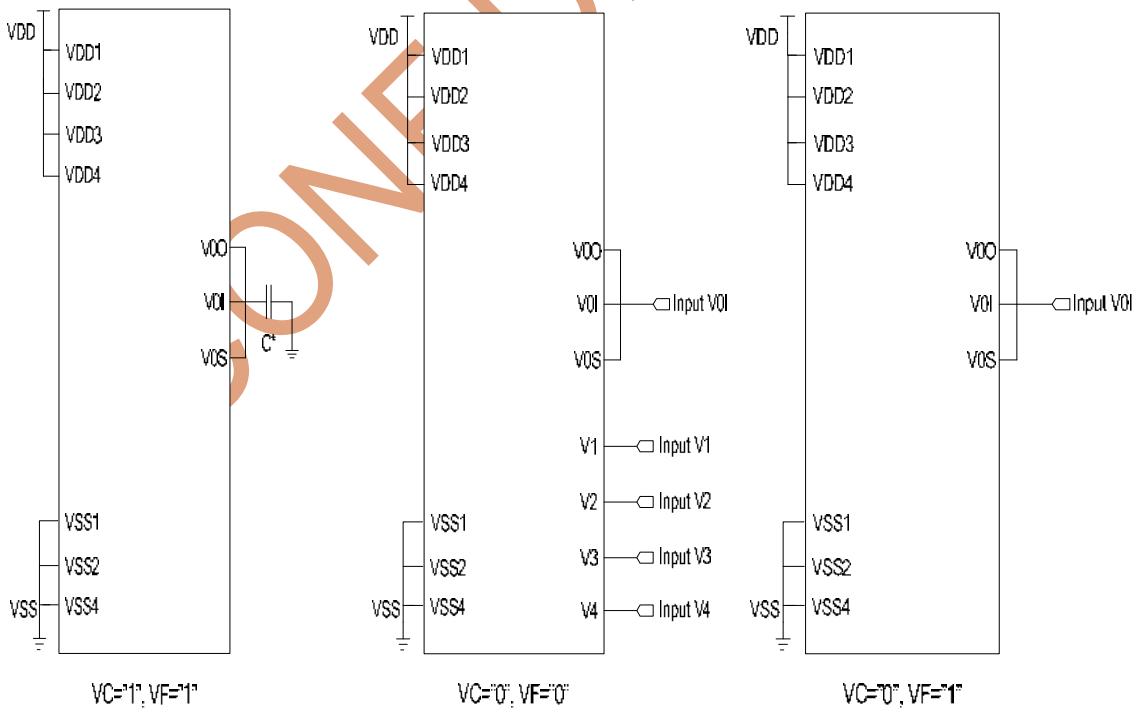
The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are two modules, voltage converter circuits (VC) and voltage follower circuits (VF). They are valid only in master operation and controlled by power control instruction. The possible LCD power supply configurations are listed as below.

Power Supply Configurations

Power Configuration	Instruction (VC VF)	VC circuits	VF circuits	V0O V0I V0S*1	V1 to V4
Internal power supply circuits are used	(1 1)	ON	ON	Open*1	Open*2
Only the voltage follower circuits are used	(0 1)	OFF	ON	External input	Open*2
Only the external power supply circuits are used	(0 0)	OFF	OFF	External input	External input

<Note>

* 1 V0O, V0I and V0S are short together by ITO. When VC="1", connect external stabilizing capacitors to GROUND.



C*=0.01~4.7uF

Voltage Follower Circuits

The Voltage Follower circuits resistively divide the liquid crystal operating voltage (V0) into four voltage levels (V1, V2, V3 and V4) and these voltage levels will be buffered output to serve as the LCD driving power sources.

BS<2>	BS<1>	BS<0>	Bias	V1	V2	V3	V4
1	0	1	1/11	10/11 x V0	9/11 x V0	2/11 x V0	1/11 x V0
0	0	1	1/10	9/10 x V0	8/10 x V0	2/10 x V0	1/10 x V0
0	0	0	1/9*	8/9 x V0*	7/9 x V0*	2/9 x V0*	1/9 x V0*
0	1	0	1/8	7/8 x V0	6/8 x V0	2/8 x V0	1/8 x V0
0	1	1	1/7	6/7 x V0	5/7 x V0	2/7 x V0	1/7 x V0
1	0	0	1/6	5/6 x V0	4/6 x V0	2/6 x V0	1/6 x V0

* Default Value

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply voltage range	VDD1/VDD2/VDD3/VDD4	-0.3 ~ 7	V
	V0	-0.3 ~ 13.5	V
Supply voltage range	V1/V2/V3/V4	-0.3 ~ V0	V
Input voltage range	V_{IN}	-0.3 to V_{DD1} + 0.3	V
Operating temperature range	T_{OPR}	-40 to +85	℃
Storage temperature range (Bare chip)	T_{STR}	-55 to +125	℃

NOTES:

1. VDD1/VDD2/VDD3/VDD4 and V0 are based on VSS1/VSS2/VSS4 = 0V
2. The Voltage levels relation V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥VSS1/VSS2/VSS4 = 0V must always be satisfied.
3. If supply voltage exceeds the absolute maximum range, this LSI may be damaged permanently.

DC CHARACTERISTICS

(Ta = -30 to 80℃)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Operating Voltage(1)		VDD1		2.4	-	3.6	V	VDD1 *1
Operating Voltage(2)		VDD2~4		2.4	-	3.6	V	VDD2~4 *9
Operating Voltage(3)		V0O/V0I/ V0S		4.0	-	13.5	V	V0O/V0I/ V0S *2
Input voltage	High	V_{IH}		0.8*V_{DD1}	-	V_{DD1}	V	*3
	Low	V_{IL}		V_{SS1}	-	0.2*V_{DD1}		
Output voltage	High	V_{OH}	I_{OH} = -0.5mA	0.8*V_{DD1}	-	V_{DD1}	V	*4
	Low	V_{OL}	I_{OL} = 0.5mA	V_{SS1}	-	0.2*V_{DD1}		
Input leakage current		I_{IL}	V_{IN} = V_{DD1} or V_{SS1}	-1.0	-	+1.0	μA	*5
Output leakage current		I_{OL}	V_{IN} = V_{DD1} or V_{SS1}	-3.0	-	+3.0	μA	*6
LCD driver ON Resistance		R_{ON}	Ta = 25℃, V0 = 13V	-	2.0	3.0	kΩ	SEGn COMn *7
Oscillator frequency (internal)		F_{OSC}	Ta = 25℃	2.8	3.0	3.2	MHz	
Oscillator frequency (External)		F_{CL}	Ta = 25℃	2.8	3.0	3.2	MHz	CL
MTP programming voltage		VPP	No loading	6.8	7.0	7.2	V	VPP
		IPP				3	mA	
LCD operation Voltage		V0	Ta = 25℃ , CT=3C, BoosterX5, BAIS=1/9 VDD1=VDD2=VDD4=3.3V	8.9	9	9.1	V	V0

Dynamic Current Consumption

(Ta = 25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Dynamic current consumption	I_{DYN}	VDD2=VDD1= 3.3V X5 Boost V0 – GROUND = 9.0V Display ON (HPMB=1, Checker pattern)	-	300	400	μA	*8 $I_{VDD1+VDD2+VDD3+VDD4}$

Static Current Consumption

(Ta =25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Sleep mode current	I_{SLP}	Sleep mode, VDD1=VDD2~VDD4=3.3V	-	1	5	μA	$I_{VDD1+VDD2+VDD3+VDD4}$

NOTE

*1. Although the wide range of DC operating voltages is guaranteed, but if the voltage fluctuation is too large during MPU accessing, the performance can't be guaranteed.

*2. In case of external power supply is applied.

*3. CS1B, CS2, A0, DB0~ DB7, E_RDB, RW_WRB, RESB, C68, PS, CLS, CL, pins.

*4. DB0 ~ DB7

*5. CS1B, CS2, A0, DB [7:0], E_RDB, RW_WRB, RESB, C68, PS, CLS, CL pins.

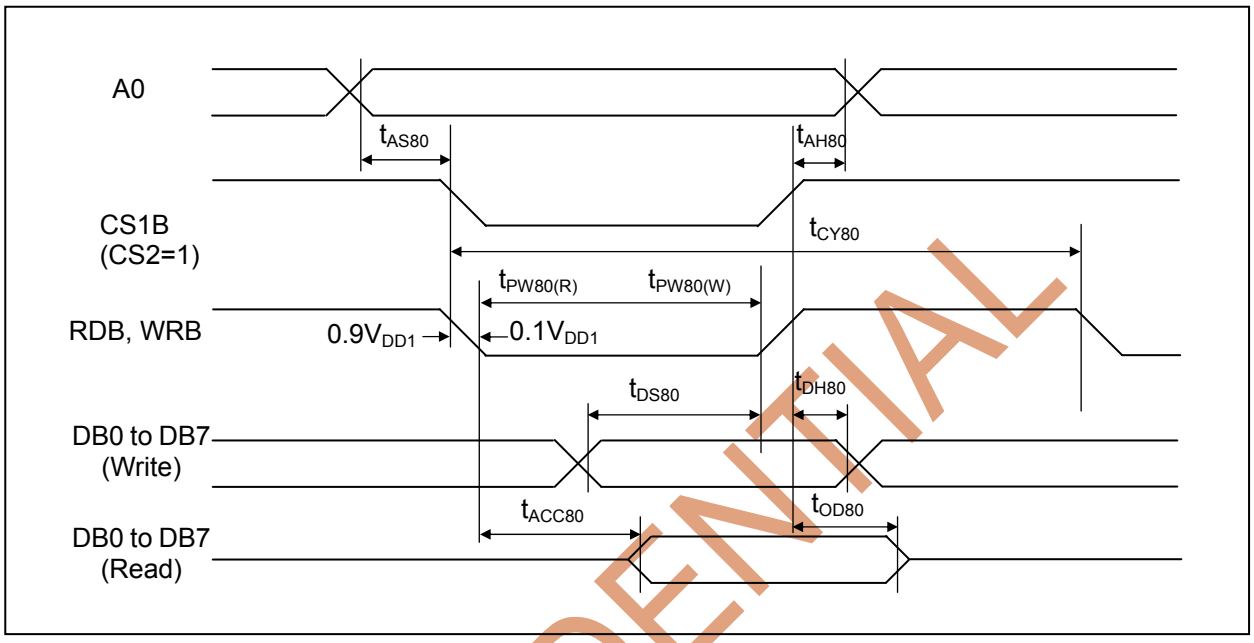
*6. Applies when the DB0 ~ DB7pins are in high impedance.

*7. Resistance value when 0.1mA is applied during the ON status of the output pin SEGn or COMn.
RON= ΔV / 0.1 [KΩ] (ΔV: voltage change when 0.1mA is applied in the ON status.)

*8. Applies to the case where the on-chip oscillation circuit is used and no access is made from the MPU & the LCD outputs (COMx, SEGx) are just floating, without any loading

AC CHARACTERISTICS

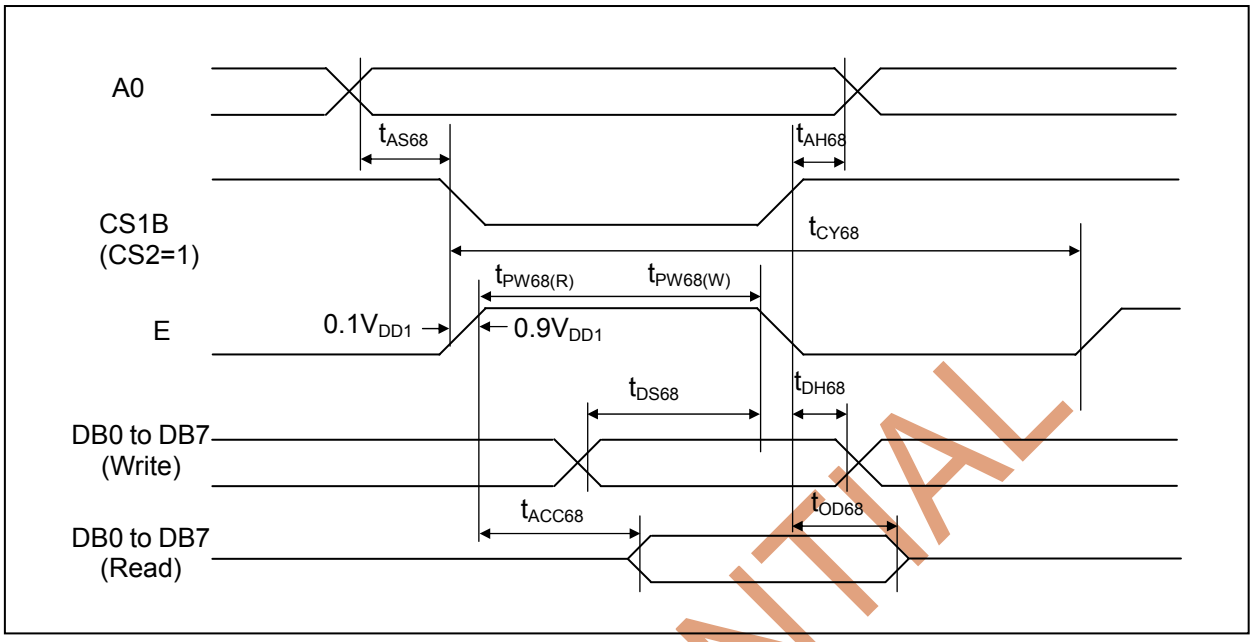
Read / Write Characteristics (8080-series MPU)



(V**DD1** = 2.4 ~ 3.6V, Ta = -30~80°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	A0	**tAS80** **tAH80**	0 0	-	-	ns	
System cycle time		tcy80(W)	300	-	-	ns	
		tcy80(R)	500	-	-	ns	
Pulse width (WRB)	RW_WRB	tpw80(W)	150	-	-	ns	
Pulse width (RDB)	E_RDB	tpw80(R)	250	-	-	ns	
Data setup time Data hold time	DB7 to DB0	tds80 tdh80	60 0	-	-	ns	
Read access time Output disable time		tacc80 tod80	140 -	-	- 10	ns	(No load)

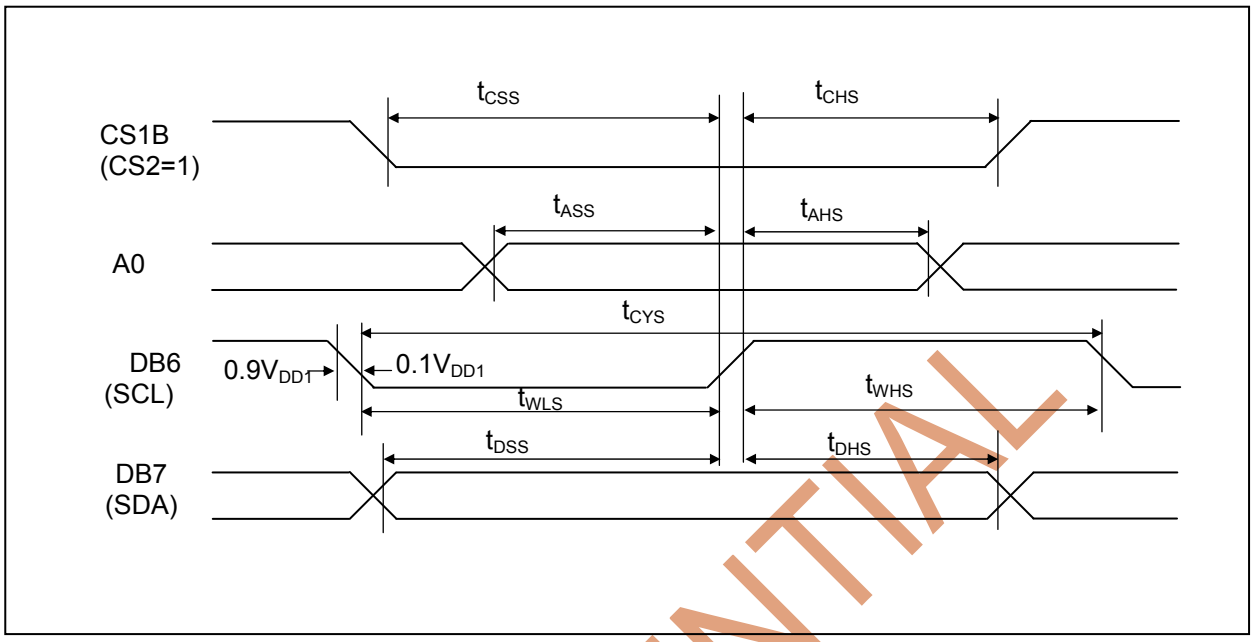
Read / Write Characteristics (6800-series Microprocessor)



(V_{DD1} = 2.4 ~ 3.6V, Ta = -30~80℃)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	A0	t_{AS68} t_{AH68}	0 0	-	-	ns	
System cycle time	RW_WRB E_RDB DB7 to DB0	$t_{CY68(W)}$	300	-	-	ns	
		$t_{CY68(R)}$	500	-	-	ns	
Pulse width (E)		t_{PW68}(W)	150	-	-	ns	
Pulse width (E)		t_{PW68}(R)	250	-	-	ns	
Data setup time Data hold time		t_{DS68} t_{DH68}	60 0	-	-	ns	
Read access time Output disable time		t_{ACC68} t_{OD68}	140 -	-	- 10	ns	(No load)

Serial Interface Characteristics(SPI Interface)

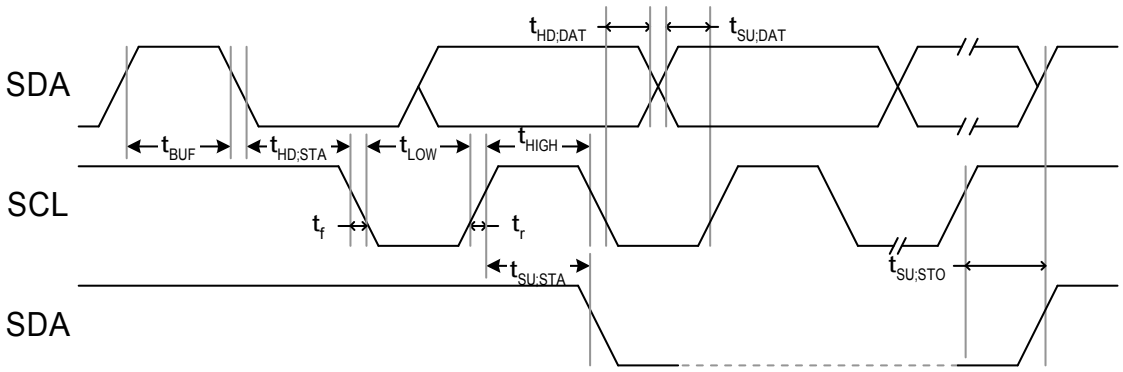


(V_{DD1} = 2.4 ~ 3.6V, Ta = -30~80℃)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle SCL high pulse width SCL low pulse width	DB6 (SCL)	t_{CYS} t_{WHS} t_{WLS}	200 90 90	- - -	- - -	ns	
Address setup time Address hold time	A0	t_{ASS} t_{AHS}	45 45	- -	- -	ns	
Data setup time Data hold time	DB7 (SDA)	t_{DSS} t_{DHS}	45 45	- -	- -	ns	
CS1B setup time CS1B hold time	CS1B	t_{CSS} t_{CHS}	90 90	- -	- -	ns	

Note: All signal Rising time and falling Time <15ns

Serial Interface Characteristics(IIC Interface)

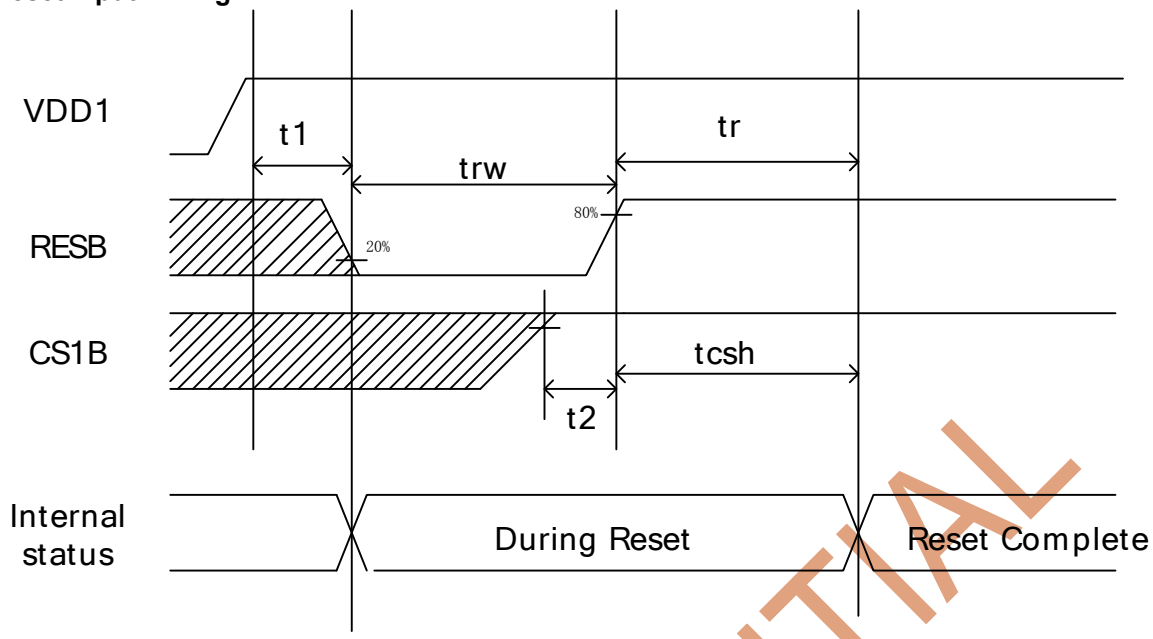


(V_{DD1} = 2.4 ~ 3.6V, Ta = -30~80℃)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
SCL clock frequency	SCL	fSCL	-	-	400	KHz	
SCL clock low period		tLOW	1	-	-	us	
SCL clock high period		tHIGH	0.4	-	-	us	
Data set-up time	SDA	tSU;Data	0.5	-	-	us	
Data hold time		tHD;Data	0.25	-	-	us	
Setup time for a repeated START condition	SDA	tSU;STA	0.6	-	-	us	
Start condition hold time		tHD;STA	1.4	-	-	us	
Setup time for STOP condition		tSU;STO	0.7	-	-	us	
Bus free time between a STOP and START		tBUF	0.8	-	-	us	

Note:
*1) All signal Rising time and falling Time <15ns
*2) It is recommended to use 4.7KΩ for the pull-up resistors of SCL and SDA. The actual resistance value should be adjusted according to the characteristics of the real system.

Reset Input Timing



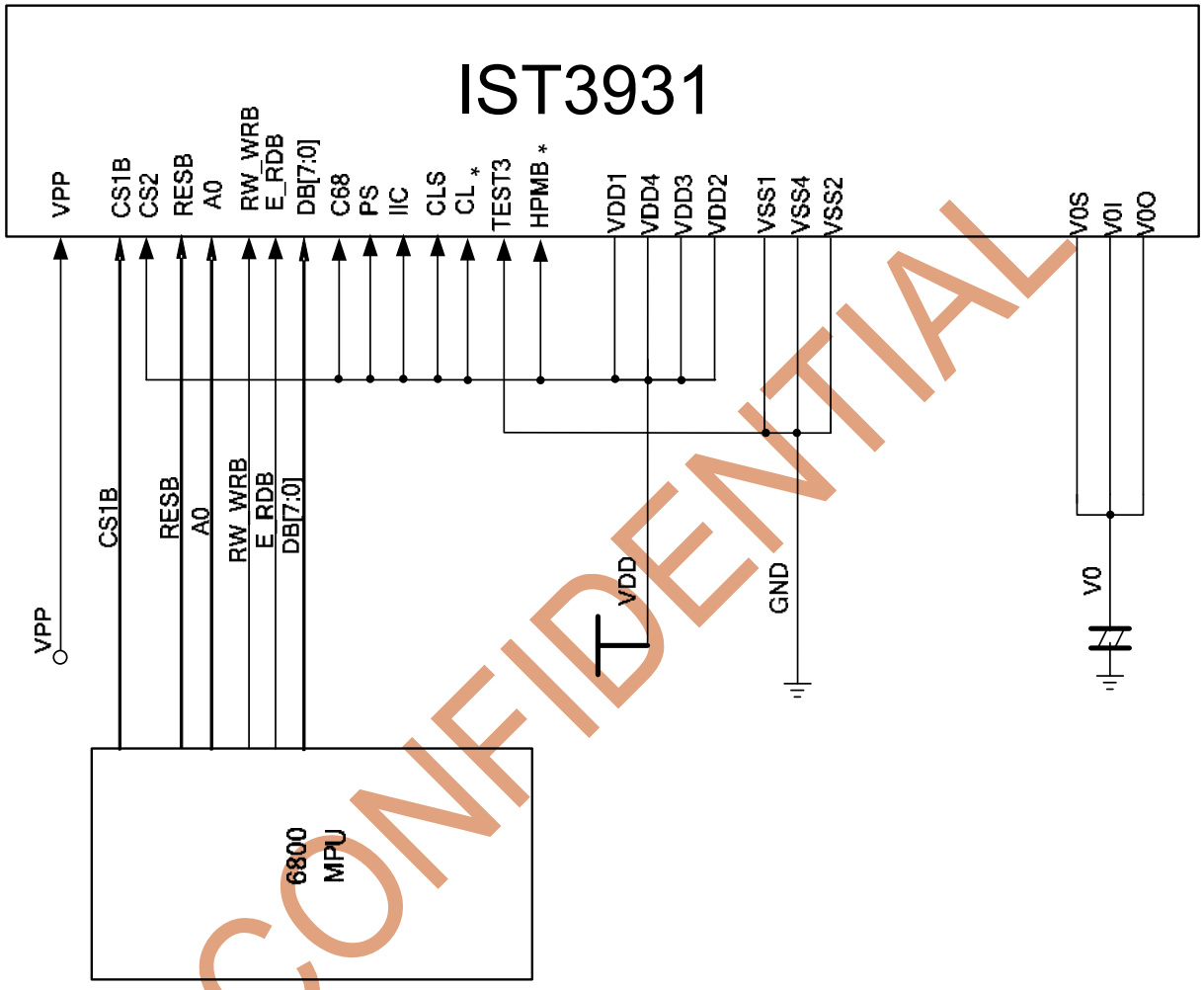
(V**DD1** = 2.4V ~ 3.6V, Ta = -30~80℃)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Reset low pulse width	RESB	t**RW**	50	-	-	us	
Reset time	-	t**R**	50	-		us	
Reset after VDD stable	RESB	t1	0	-	-	us	
CS1B to RESB pull High	CS1B	t2	0			us	
CS1B hold	CS1B	tcsh	50			us	

REFERENCE APPLICATIONS

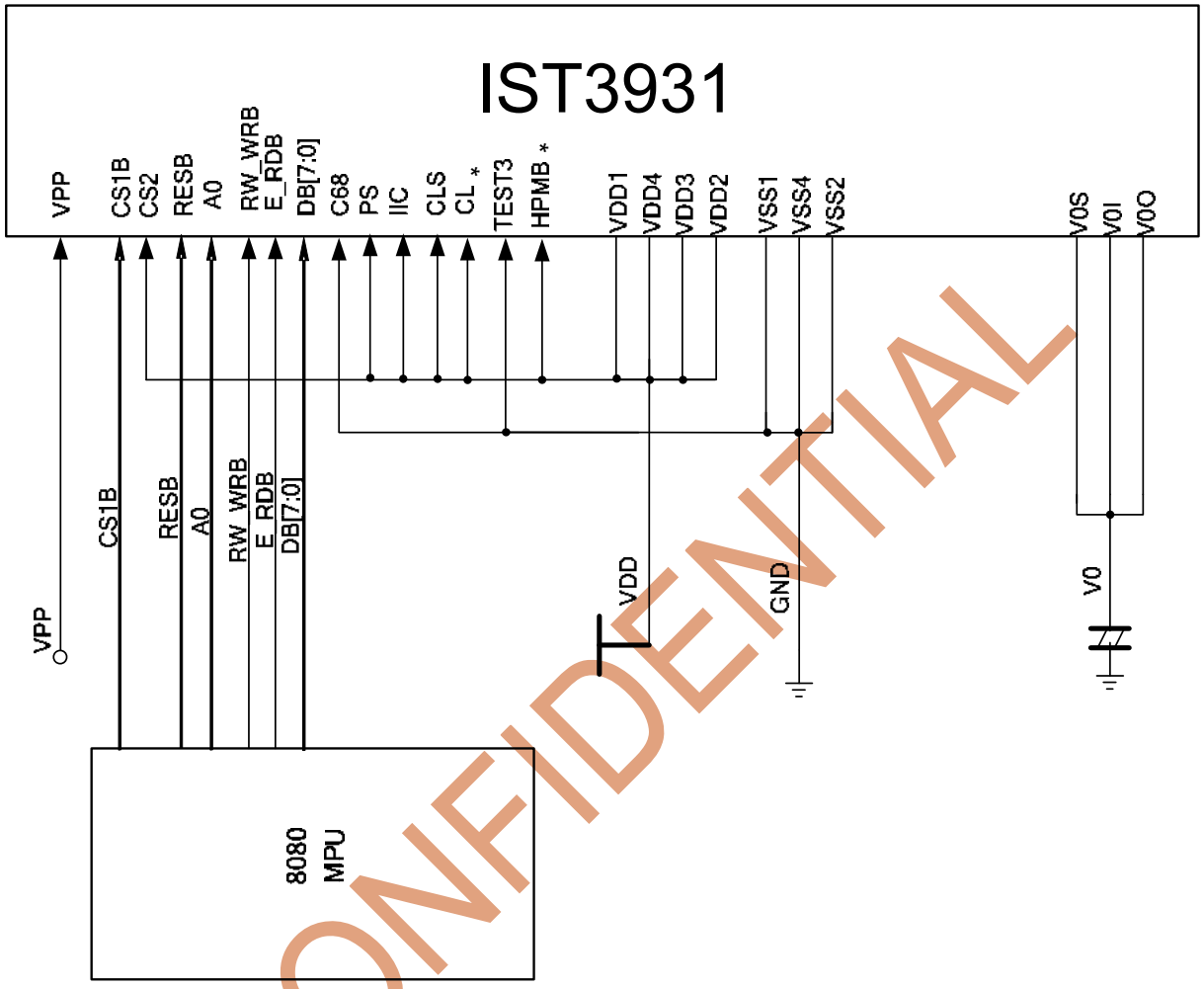
MPU Interface

In Case of Interfacing with 6800-series (PS = "H", C68 = "H" , IIC=H)



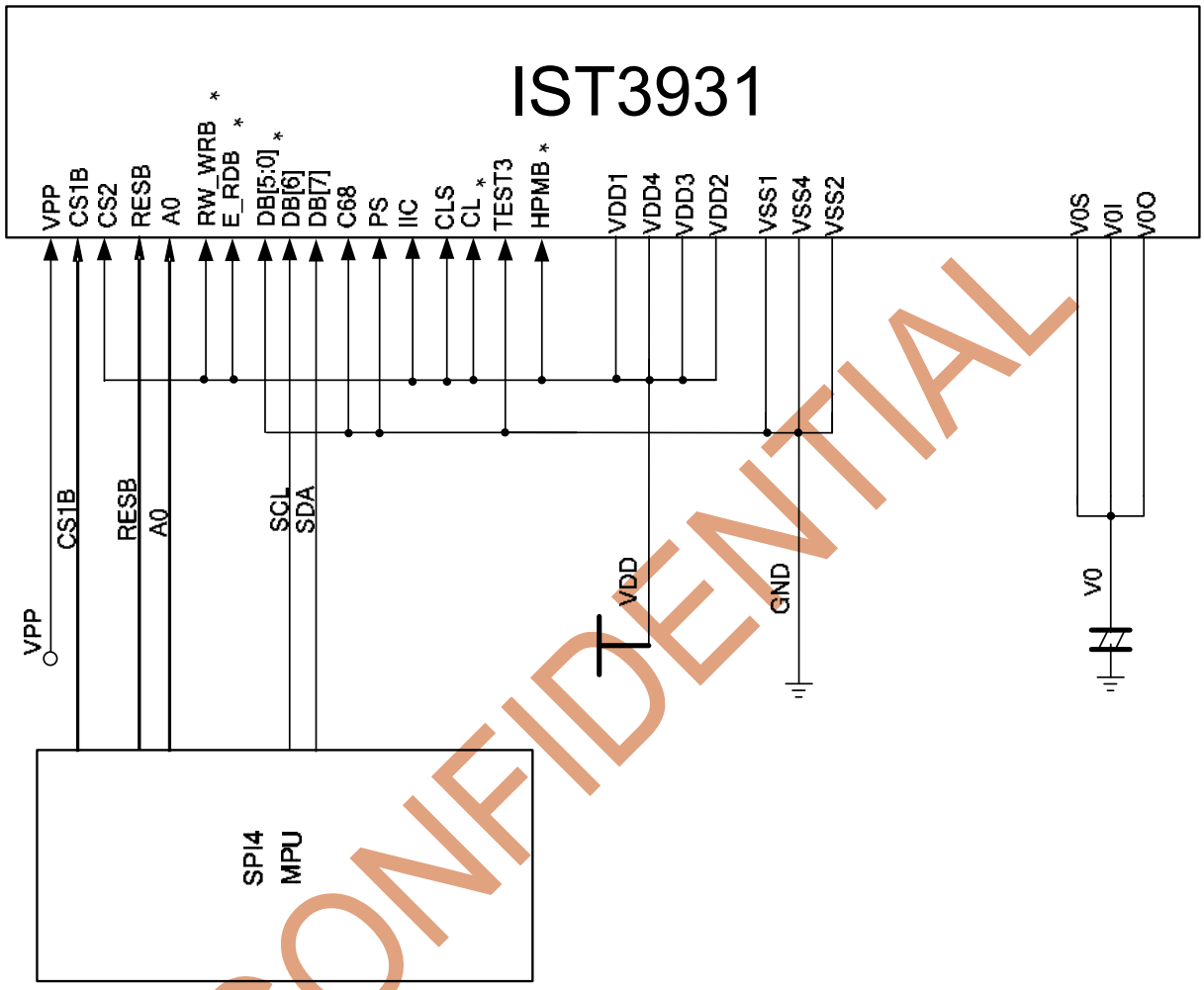
*: No use pin must fix to VSS1 or VDD1

In Case of Interfacing with 8080-series (PS = "H", C68 = "L" , IIC=H)



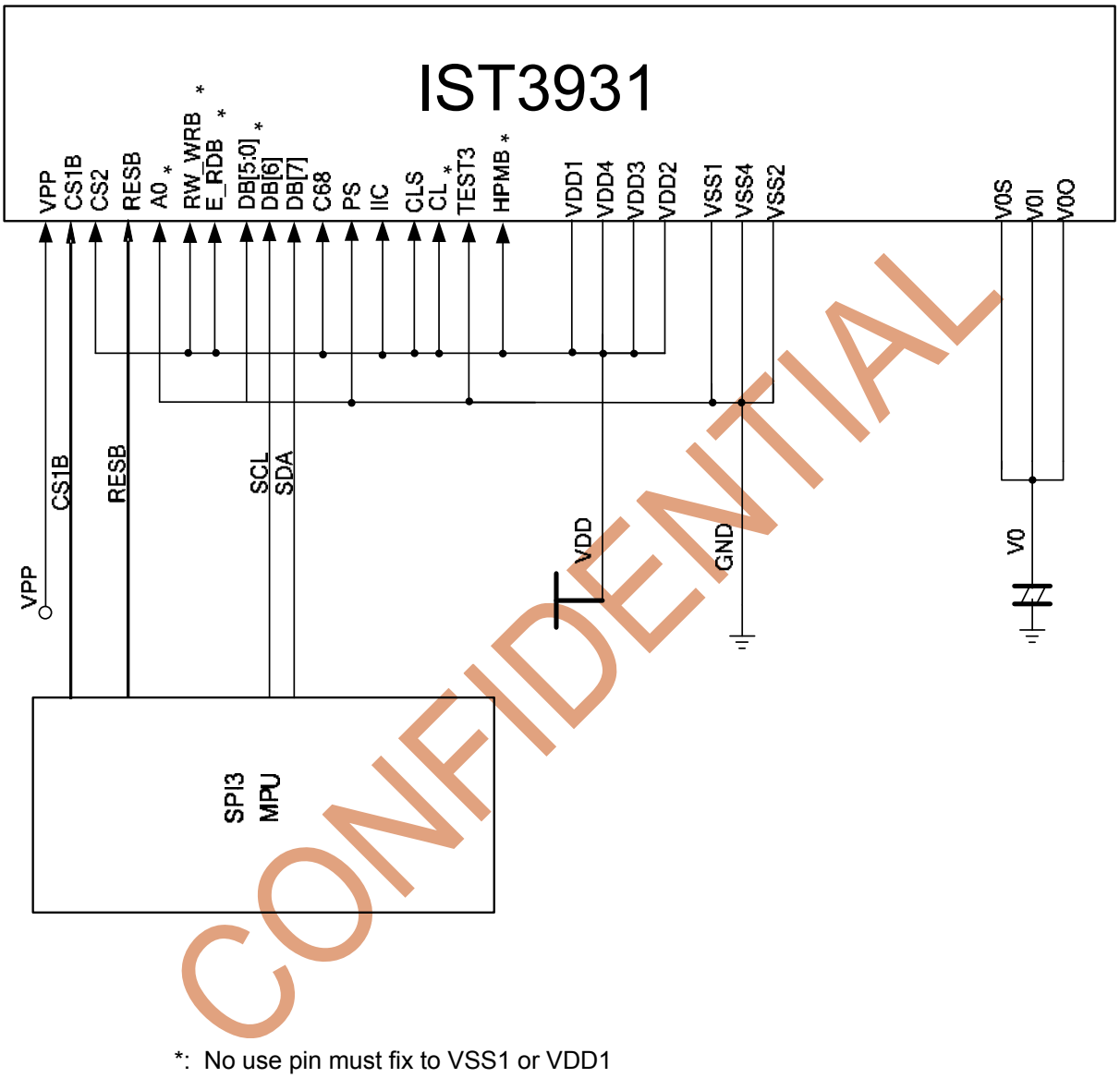
*: No use pin must fix to VSS1 or VDD1

In Case of Serial Interface 4 (PS = "L", C68 = "L", IIC=H)



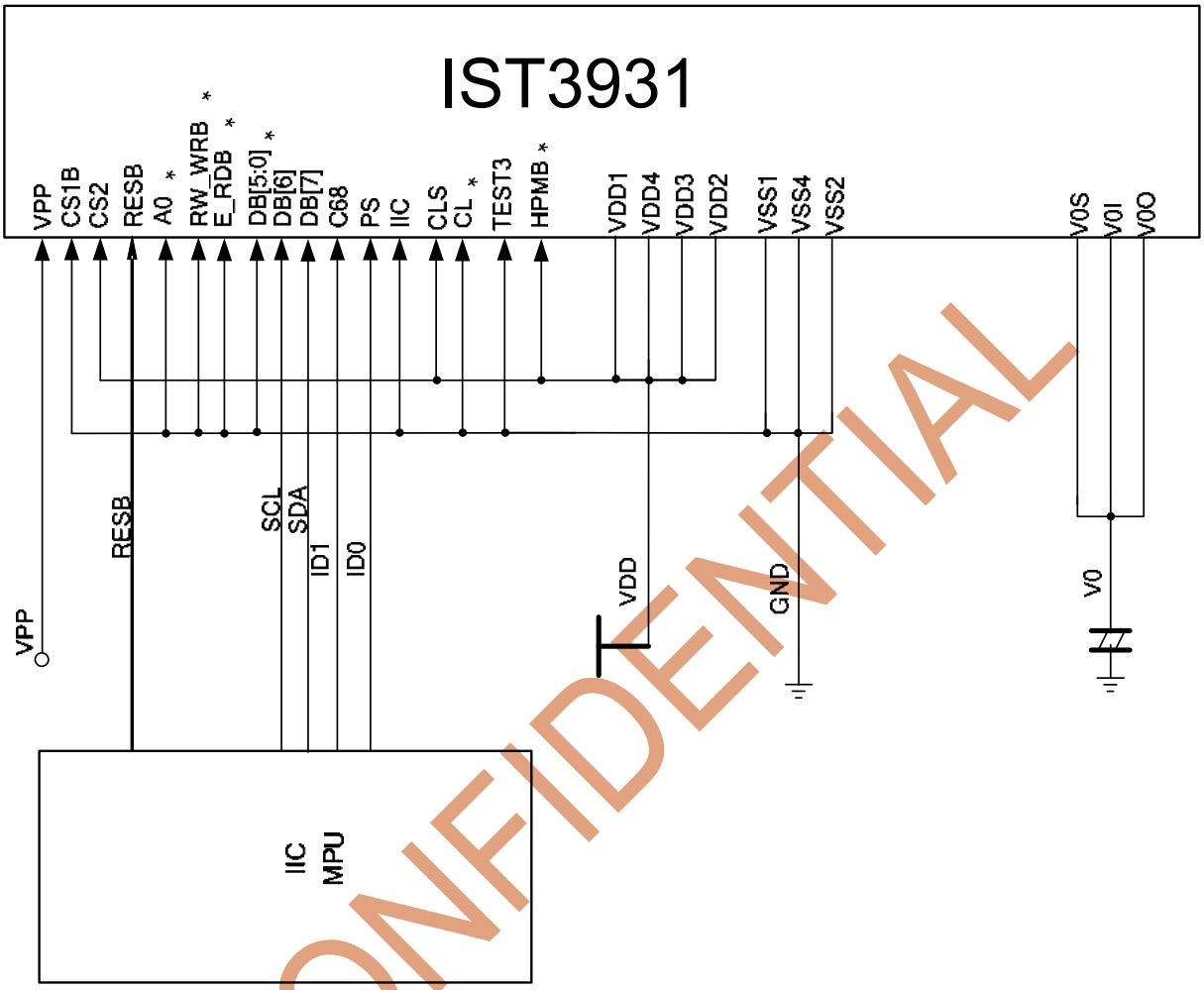
*: No use pin must fix to VSS1 or VDD1

In Case of Serial Interface 3 (PS = "L", C68 = "H" , IIC=H)



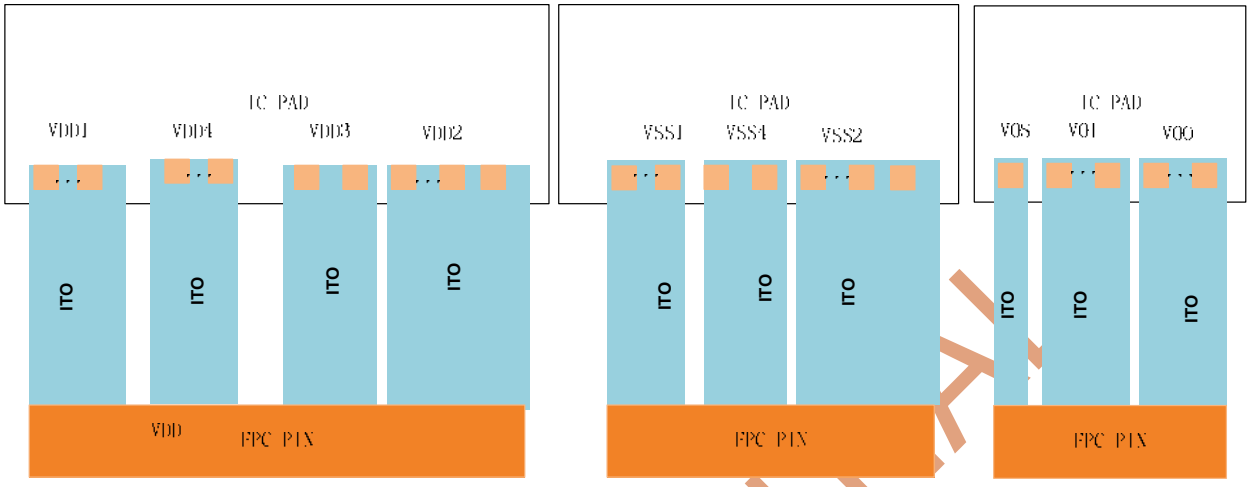
*: No use pin must fix to VSS1 or VDD1

In Case of IIC (PS = "X", C68 = "X", IIC=L)



*: No use pin must fix to VSS1 or VDD1

ITO CONNECTION



CAUTIONS:

1.This Specification will be subjected to modify without notice.

2.Precutions on Light:

Characteristics of semiconductor devices can be changed when exposed to light as described in the operational principles of solar batteries. Exposing this IC to light ,therefore ,can potentially lead to its malfunctioning.

2.1Care must be exercised in designing the operation system and mounting the IC so that it may not be exposed light during operation .

2.2Care must be exercised in designing the inspection process and handling the IC so that it may not be exposed to light during the process.

2.3The IC must be shielded from light in the front, back and side faces.

3.ESD control and prevention:

3.1Humidity Control:30~70% relative humidity is recommended.

3.2To reduce the risk of ESD, all equipment at the wok surface should be properly grounded and all sources of static fields removed.(Example: Station ionizers).

3.3Grounding all personnel who come in contact with parts will eliminate a possible source of ESD. (Example: Wrist straps remove charge from the body and constitute a central part of ESD control).

4.Storage Conditions:

Before open package	After open package
Temp.=25±5℃ Humidity:50~70% Less than 1 Years	Temp.=25±5℃ Humidity:50~70% Less than 3 Months