

 Integrated Solutions Technology, Inc.	Title IST3040 Specification 40X4 Mono STN-LCD Driver	文件編號 DOC#	版次 Rev
		IST-RD-0046	004
			生效日期 Effective Date : 07/31/2007

<h1>Specification</h1>			
Written by Department	Written by / Date	Approved by QRA Manager	Issued by D.C.C.
Research & Development	Sam Ho 07/31/2007	Bonnie Lee 07/31/2007	Allan Huang 07/31/2007

Controlled by DCC

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Code Name	100	200	300	400	500	600	700
Dept.	HR	S/M	MFG	R&D	CH	QRA	MIS
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文件變更履歷頁

Document Change History

版次 Rev.	變更項次 Change Items#	變更內容簡述 Change Description	變更依據文件號碼 ECN #	生效日期 Eff. Date
001	--	New Release	E06060008	06/07/2006
002	1.Block map 2.DC Characteristic	1.Add the INH input port 2.Update Vdd & Vlcd power consumption for "TBD" in SPEC Rev.001	E07060012	2006/7/25
003	Operating voltage	1.Change low operation voltage from 3.0 to 5.0 at Page 1. 2.Change operating voltage(1) from 3.6 to 5.0 at page 8.	E10060001	2006/10/02
004	Feature	1.Wide operation voltage 2.4V~5.0V(MAX) 2.IST3040 I/O PIN ITO Resister Limitation	E07070011	07/31/2007



IST3040 40X4 LCD Segment/Common Driver

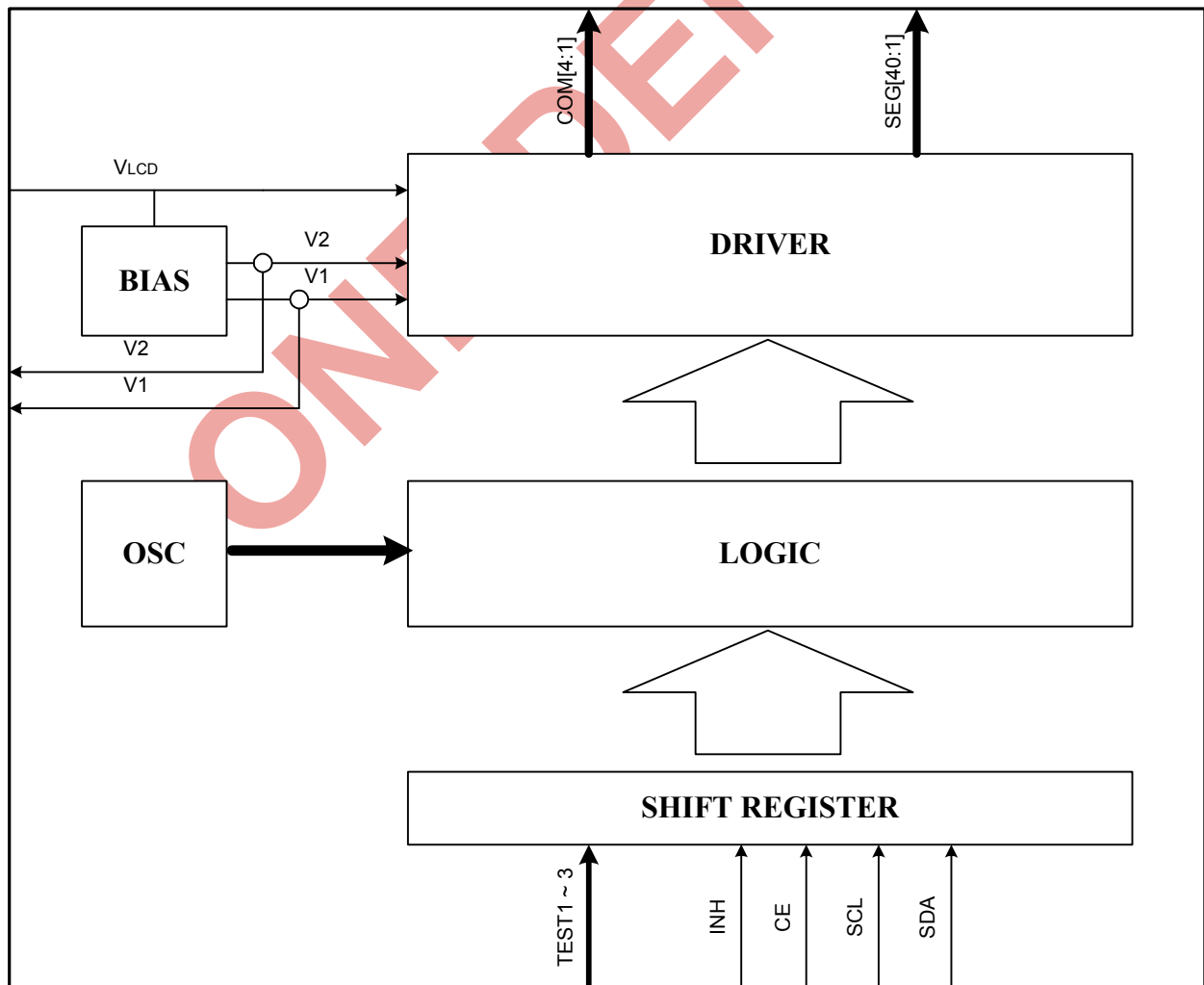
Introduction:

IST3040 is the LCD driver with 1/4 duty. IST3040 incorporate 4 common output circuits and 40 segment output circuits, it can drive a 160 dots display panel. The display data is serial in at maximum 2MHz clock.

Feature:

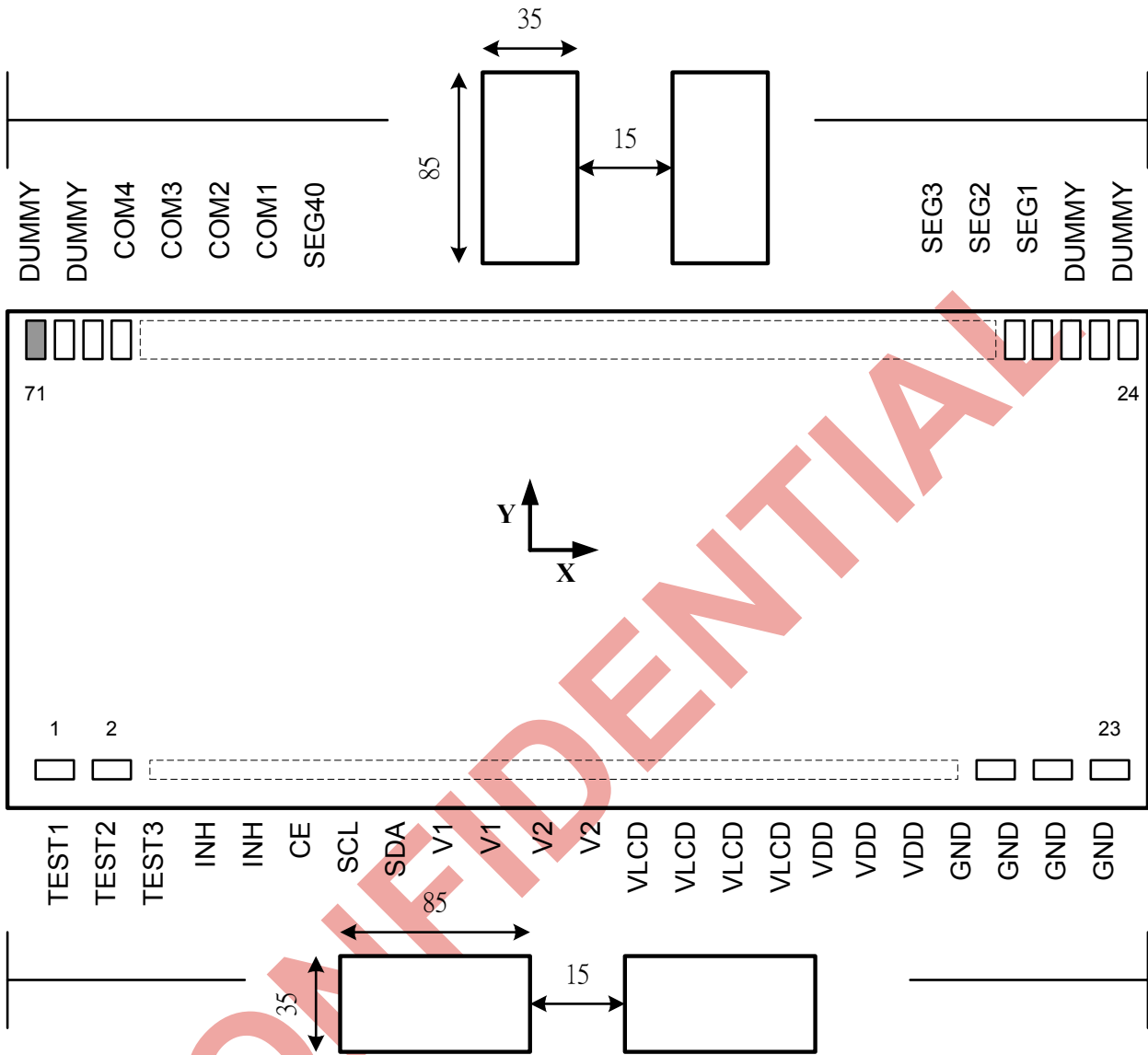
- Duty: 1/4(160 segment), BIAS: 1/3
- Serial data input (serial clock 2MHz MAX)
- Display on display off switch function
- Wide operation voltage 2.4V~5.0V(MAX)
- Liquid crystal drive voltage 6.0V(MAX)

Block map:





Pad location:



Item	Pad Info.	Dimension (um)	
		X	Y
Chip size	Total 71 pins	2515	1114
Bumped pad size	I/O Pad 1~23	85	35
	Output Pad 26~69	35	85
	Dummy Pad 24~25, 70~71	35	85

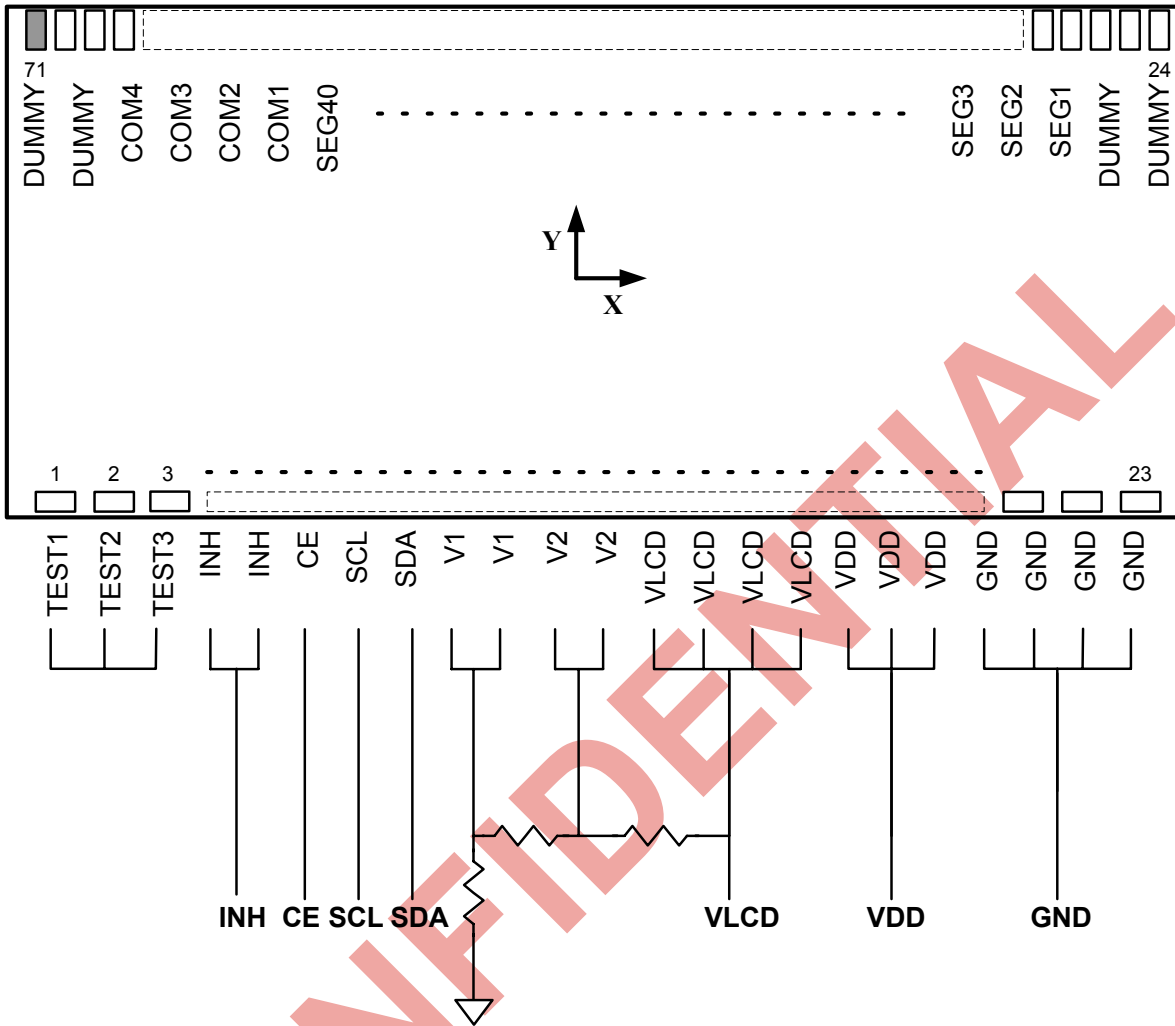


PAD COORDINATE

No	Pad Name	X	Y	No	Pad Name	X	Y
1	TEST1	-1100	-424.1	51	SEG<26>	-175	449.5
2	TEST2	-1000	-424.1	52	SEG<27>	-225	449.5
3	TEST3	-900	-424.1	53	SEG<28>	-275	449.5
4	INH	-800	-424.1	54	SEG<29>	-325	449.5
5	INH	-700	-424.1	55	SEG<30>	-375	449.5
6	CE	-600	-424.1	56	SEG<31>	-425	449.5
7	SCL	-500	-424.1	57	SEG<32>	-475	449.5
8	SDA	-400	-424.1	58	SEG<33>	-525	449.5
9	V1	-300	-424.1	59	SEG<34>	-575	449.5
10	V1	-200	-424.1	60	SEG<35>	-625	449.5
11	V2	-100	-424.1	61	SEG<36>	-675	449.5
12	V2	0	-424.1	62	SEG<37>	-725	449.5
13	V0	100	-424.1	63	SEG<38>	-775	449.5
14	V0	200	-424.1	64	SEG<39>	-825	449.5
15	V0	300	-424.1	65	SEG<40>	-875	449.5
16	V0	400	-424.1	66	COM<1>	-925	449.5
17	VDD	500	-424.1	67	COM<2>	-975	449.5
18	VDD	600	-424.1	68	COM<3>	-1025	449.5
19	VDD	700	-424.1	69	COM<4>	-1075	449.5
20	GND	800	-424.1	70	DUMMY	-1125	449.5
21	GND	900	-424.1	71	DUMMY	-1175	449.5
22	GND	1000	-424.1				
23	GND	1100	-424.1				
24	DUMMY	1175	449.5				
25	DUMMY	1125	449.5				
26	SEG<1>	1075	449.5				
27	SEG<2>	1025	449.5				
28	SEG<3>	975	449.5				
29	SEG<4>	925	449.5				
30	SEG<5>	875	449.5				
31	SEG<6>	825	449.5				
32	SEG<7>	775	449.5				
33	SEG<8>	725	449.5				
34	SEG<9>	675	449.5				
35	SEG<10>	625	449.5				
36	SEG<11>	575	449.5				
37	SEG<12>	525	449.5				
38	SEG<13>	475	449.5				
39	SEG<14>	425	449.5				
40	SEG<15>	375	449.5				
41	SEG<16>	325	449.5				
42	SEG<17>	275	449.5				
43	SEG<18>	225	449.5				
44	SEG<19>	175	449.5				
45	SEG<20>	125	449.5				
46	SEG<21>	75	449.5				
47	SEG<22>	25	449.5				
48	SEG<23>	-25	449.5				
49	SEG<24>	-75	449.5				
50	SEG<25>	-125	449.5				



APPLICATION NOTE:





PIN DISCRPTION:

Pin number	Pin name	Description
1~3	TEST1 ~ TEST3	For test usage, this three pins have to be short together.
4~5	INH	Display control pin: “ High ”: Display off “ Low ”: Display on
6	CE	Check enable input pin: “ High ”: Display data input enable “ Low ”: Display data input disable
7	SCL	Shift clock input pin: SDA input data read in at the rise edge of SCL
8	SDA	LCD data input pin: LCD display data read in at the rise edge of SCL
9~10	V1	BIAS pin
11~12	V2	BIAS pin
13~16	V _{LCD}	LCD driver supply voltage
17~19	V _{DD}	Power supply
20~23	GND	Ground
26~65	SEG ₁ ~ SEG ₄₀	LCD segment driver outputs
66~69	COM ₁ ~ COM ₄	LCD comment driver outputs

IST3040 I/O PIN ITO Resister Limitation

PIN Name	ITO Resister
GND, V _{DD} , V _{LCD} , V1, V2	< 200Ω
INH, CE, SCL, SDA	< 1KΩ

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FUNCTIONAL DESCRIPTION:

I .BIAS block :

Provide the voltage source of common and segment driver

II .Shift register :

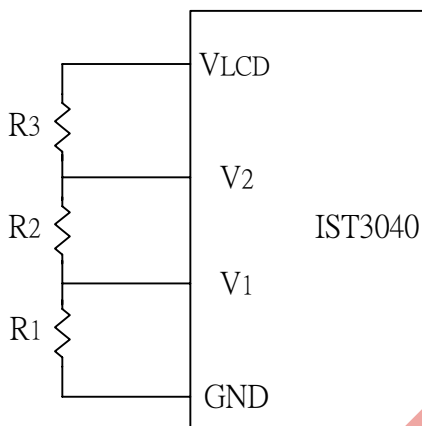
The display data is store in 160bit shift register. When CE is “HIGH” display data will be read in the shift register at the rise edge of SCL. The shift register is in the LOGIC block.

III.Driver block :

The driver block provide the COM₁~COM₄ and SEG₁~SEG₄₀ waveform to drive the LCD panel.

IV.External BIAS circuit :

The V1 V2 of IST3040 can connect to the external resistors, with the external resistors the drive current will be increased.

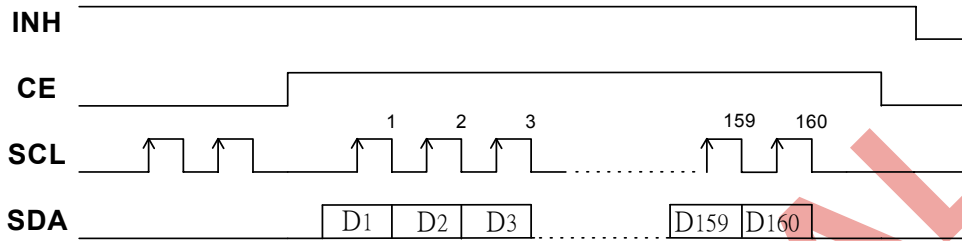


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V. Display data format and the relationship between display data and output pin :

When the CE in the “HIGH” level the SDA can transform the display data to the internal shift register at the rise edge of SCL. When the CE in the “LOW” level the display data in the shift register will be fixed even if the SCL is vibrating.



Display data waveform

Display data (D ₁ ~D ₁₆₀)	Segment output
HIGH	Display on
LOW	Display off

Relationship between display data and segment

Segment pin	Display data	Common pin			
		COM ₁	COM ₂	COM ₃	COM ₄
SEG ₁	D1 D2 D3 D4	○	○	○	○
SEG ₂	D5 D6 D7 D8	○	○	○	○
⋮	⋮	⋮	⋮	⋮	⋮
SEG ₃₉	D53 D154 D155 D156	○	○	○	○
SEG ₄₀	D157 D158 D159 D160	○	○	○	○

Relationship between the shift register and COM/SEG pin



ABSOLUTE MAXIMUM RATINGS:

(Ta=25°C)

Parameter	Symbol	Rating
Supply voltage range	V_{DD}	-0.3V ~ +7.0V
	V_{LCD}	-0.3V ~ +7.0V
	V_{1}, V_{2}	-0.3V ~ +7.0V
Input voltage range	V_{IN}	-0.3V ~ V_{DD}
Operation temperature	T_{opr}	-20°C ~ +75°C
Storage temperature	T_{stg}	-55°C ~ +125°C

Notes:

1. V_{DD} and V_{LCD} are based on GND = 0V
2. Voltages $V_0 \geq V_2 \geq V_1 \geq V_{SS}$ must always be satisfied.
3. If supply voltage exceeds its absolute maximum range, this LSI may be damaged permanently. It is desirable to use this LSI under electrical characteristic conditions during general operation. Otherwise, this LSI may malfunction or reduced LSI reliability may result.
4. Please insert the capacitance between V_{DD} - V_{SS} and V_{LCD} - V_{SS} if the more stable operation is needed.

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DC CHARACTERISTIC:

(Ta = 25°C, V_{SS} = 0V, V_{DD} = 3.0V, V_{LCD} = 6.0V)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Notes
Operating voltage(1)	Suggested	V _{DD}		2.4	3.0	5.0	V	
	Receivable	V _{DD}		2.4	3.0	5.5	V	
Operating voltage(2)		V _{LCD}		2.0	-	6.0	V	
		V ₂		V ₁	2/3V _{LCD}	V _{LCD}	V	
		V ₁		0.7	1/3V _{LCD}	V ₂	V	
Input voltage	High	V _{IH}	CE, SCL, SDA, INH	0.7V _{DD}	-	V _{DD}	V	
	Low	V _{IL}	CE, SCL, SDA, INH	V _{SS}	-	0.3V _{DD}	V	
Output voltage	High	V _{OH}		V _{LCD} -0.6	-	V _{LCD}	V	
	Low	V _{OL}		V _{SS}	-	V _{SS} +0.6	V	
LCD driver ON Resistance		R _{ON}	V _{ds} = 0.1v I _{ds} = 0.09mA			1.1	KΩ	
V _{DD} power consumption		I _{DD}	V _{DD} =3.0V V _{LCD} =Open		15	25	μA	*1
V _{LCD} power consumption		I _{LCD}	V _{DD} =3.0V V _{LCD} =6.0V		18	28	μA	*2

*1.CE, SCL , SDA short to Vss and INH short to Vdd.

*2. CE, SCL , SDA and INH short to Vss.

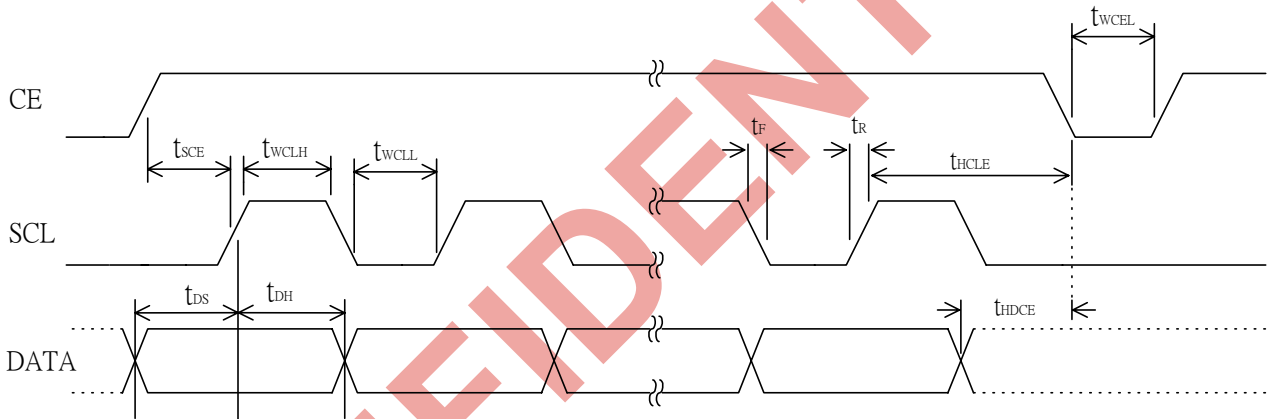
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AC CHARACTERISTIC:

(Ta = 25°C, VSS = 0V, VDD = 3.0V, VLCD = 6.0V)

Item	Symbol	Pin	Min.	Typ.	Max.	Unit
“Low” level pulse time	t _{WCLL}	SCL	0.25	-----	-----	μ S
“High” level pulse time	t _{WCLH}	SCL	0.25	-----	-----	μ S
SCL rise time, fall time	t _r , t _f	SCL	-----	-----	50	nS
Setup time	t _{DS}	SCL, SDA	0.25	-----	-----	μ S
Hold time	t _{DH}	SCL	0.25	-----	-----	μ S
CE setup time	t _{SCE}	CE, SDA	1.25	-----	-----	μ S
CE hold time	t _{HCLE}	SCL, CE	1.25	-----	-----	μ S
CE “Low” level pulse time	t _{WCEL}	CE	4.00	-----	-----	μ S
Frame rate	f _O	COM ₁₋₄ , SEG ₁₋₄₀	45	70	-----	Hz



Input data timing



LCD DRIVE WAVEFORM (DUTY : 1/4 , BIAS : 1/3):

