Specification

Written by Department	Written by / Date	Approved by QRA Manager	Issued by D.C.C.
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Controlled by DCC

Copy List

Code Name	100	200	300	400	500	600	700
Dept.	HR	S/M	MFG	R&D	CH	QRA	MIS
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文件變更履歷頁
Document Change History

版次 Rev.	變更項次 Change Items#	變更內容簡述 Change Description	變更依據文件號碼 ECN #	撰寫者 Writer	生效日期 Eff. Date
001	--	New Release	E07070009	Quin	07/27/2007
002	PAD configuration	Update Alignment mark location	E09070001	Quin	09/07/2007
	DC spec	Correct DC specification			
	Command description	Correct Software reset covered ranges			
003	System Control	H L H:1/19 → 1/17	E09070003	Quin	09/11/2007
	Read Status	ADC = 0: SEG direction is SEG0 → SEG131			
	SHL Select	SHL = 0 : COM0 → COM63 SHL = 1 : COM63 → COM0			
	MPU Interface	Interfacing with 8080-series (PS = "H", C68 = "L")			
004	Typing error correction	P33. α define correction P5.Pin naming consistency correction P18.COM output channels correction P27.Status description correction P29.Duty 1/1 Bias setting correction	E11070006	Quin	11/07/2007
	VDD/VDD2 DC range modify	P2/21/40. VDD/VDD2 Max DC range changed from 3.3V →3.6V			
	Miss spec patching	P8. HPMB pin define P35. Booster ratio command P10. I/O pin ITO resistor correction			
	Add "OTP Programming Control" Section	P37~38 New OTP Programming Control Section			
005	Pin name modify	SEL3~1→DUTY2~0 ， WRB→RW_WRB ， RDB→E_RDB ， TESTx→TEST1~6	E01080009	Quin	01/31/2008
		Block diagram modify, add VPP pin and OTP			

		block			
006	System Control	HPMB : I/O to I	E04080003	Quin	04/22/2008
	Line Address Circuit	Remove starting line function			
	Power Supply Circuits	Add external vout & v0~v4 input circuit drawing			
	Voltage Converter Circuits	Add v0 to v4 capactitor to vss circuit drawing			
	OTP PROGRAMMING CONTROL	Add OTP programming control			
	Dynamic Current Consumption	Add dynamic cruuent consumption for typical			
	LCD Driver Outputs	coms0/s1 to coms1/s2			
007	ITO connection example	Correct ITO connection example	E05080012	Quin	05/29/2008
	OTP write follow	Correct OTP write follow			
	PAD CENTER COORDINATES	Pin 84 TEST6 to GNDDNY			
008	Micro-Controller Interface	DB0 to DB5 and E_RDB and RW_WRB must be fixed to either “H” or “L”	E07080002	Quin	07/02/2008
	ABSOLUTE MAXIMUM RATINGS	VDD/VDD2 change from 0.3~5.0→-0.3~3.6V			
		V0,Vout change from 0.3~13.5→-0.3~13.5			
		V1/V2/V3/V4 change from 0.3~V0→-0.3~V0			
009	I/O PIN ITO Resister Limitation	Add “VPP<500Ω”	E08080002	Quin	08/04/2008
	Power Save (Compound Instruction)	Correct Power Save (Compound Instruction)			
	ABSOLUTE				

	MAXIMUM RATINGS	Add ” Input voltage range=-0.3 to VDD + 0.3”			
	DC CHARACTERISTICS	Correct Reference voltage :Max:2.07 min:2.13			
		Add “OTP programming voltage”			
	Dynamic Current Consumption	Correct IDD1 MAX=120, IDD2 MAX=250			
010	Line Address Circuit	Add starting line function for (F version)	E10080001	Quin	10/06/2008
011	Absolute Maximum ratings	Correct Supply voltage range	E11080002	Quin	11/07/2008
012	Chip Thickness	Chip Thickness correction	E11080011	Quin	11/20/2008
013	PAGE37~42 PAGE44~52 PAGE16	Update OTP programming flow Correct AC/DC spec. Correct Starting line illustration drawing	E02090001	Quin	02/04/2009
014	Page 44~49	Update AC/DC SPEC	E03090006	Quin	03/24/2009
	Page 41	Modify OTP Write Flow			
015	Page 18	Duty17: COM56 →/← COM63	E05090003	Quin	05/08/2009
	Page 21	The VDD2 = 2.4V ~ 3.6V, but the boost ratio configuration and that the boosted output VOUT level should not exceed 13.5V.			
	Page 22	Correct “Voltage Regulator Circuits”			
	Page 49	Correct “Reset Input Timing”			
016	Chip Thickness	Chip Thickness correction	E06090019	Quin	06/19/2009

接續頁 CONTINUATION --- ☐ 是 YES; ☒ 否 NO

INTRODUCTION

The IST3004 is a single chip driver & controller LSI for graphic dot-matrix liquid crystal display systems. This chip can be connected directly to a microprocessor, accepts serial or 8-bit parallel display data from the microprocessor, stores the display data in an on-chip display data RAM of 65 x 132 bits and generates a liquid crystal display drive signal independent of the microprocessor. It provides a high-flexible display section due to 1-to-1 correspondence between on-chip display data RAM bits and LCD panel pixels. It contains 65 common driver circuits and 132 segment driver circuits, so that a single chip can drive a 65 x 132 dot display.

This chip is able to minimize power consumption because it performs display data RAM read / write operation with no external operation clock. In addition, because it contains power supply circuits necessary to drive liquid crystal, which is a display clock oscillator circuit, high performance voltage converter circuit, high-accuracy voltage regulator circuit, low power consumption voltage divider resistors and OP-Amps for liquid crystal driver power voltage, it is possible to make the lowest power consumption display system with the fewest components for high performance portable systems.

FEATURES

Display Driver Output Circuits

- 65 common outputs / 132 segment outputs

Power Supply

- Logic Power VDD – VSS = 2.4V ~ 3.6V
- Analog Power VDD2 – VSS = 2.4V ~ 3.6V
- LCD Driving V0 – VSS = 13.5V (Max)

On-chip Display Data RAM

- RAM size : 65 x 132 = 8,580 bits

Applicable Duty Ratios

- Duty = 1/65 → Applicable Bias = 1/7 or 1/9
- Duty = 1/55 → Applicable Bias = 1/6 or 1/8
- Duty = 1/53 → Applicable Bias = 1/6 or 1/8
- Duty = 1/49 → Applicable Bias = 1/6 or 1/8
- Duty = 1/33 → Applicable Bias = 1/5 or 1/6
- Duty = 1/17 → Applicable Bias = 1/4 or 1/5
- Duty = 1/9 → Applicable Bias = 1/4 or 1/5
- Duty = 1/1 → Applicable Bias = 1/4 or 1/5

Built-in Analog Circuit

- On-chip oscillator circuit for display clock (external clock can also be used
- High performance voltage converter (with booster ratios x2/x3/x4/x5/x6)
- High accuracy reference voltage generator (Temperature coefficient = -0.05%)
- Electronic contrast control (64 steps)
- Embedded V0 Voltage regulator resistors
- High performance voltage follower (V1 ~ V4 voltage generator with output buffer)

Microprocessor Interface

- High-speed 8-bit parallel bi-directional interface with 6800-series or 8080-series
- Serial interface (only write operation) available

Various Function Set

- Display ON / OFF, set initial display line, set page address, set column address, read status, write / read display data, select segment driver output, reverse display ON / OFF, entire display ON / OFF, select LCD bias, set/reset modify-read, select common driver output, control display power circuit, select internal regulator resistor ratio for V0 voltage regulation, electronic volume, static indicator setting.
- OTP(One-Time-Programming) Contrast adjust is available

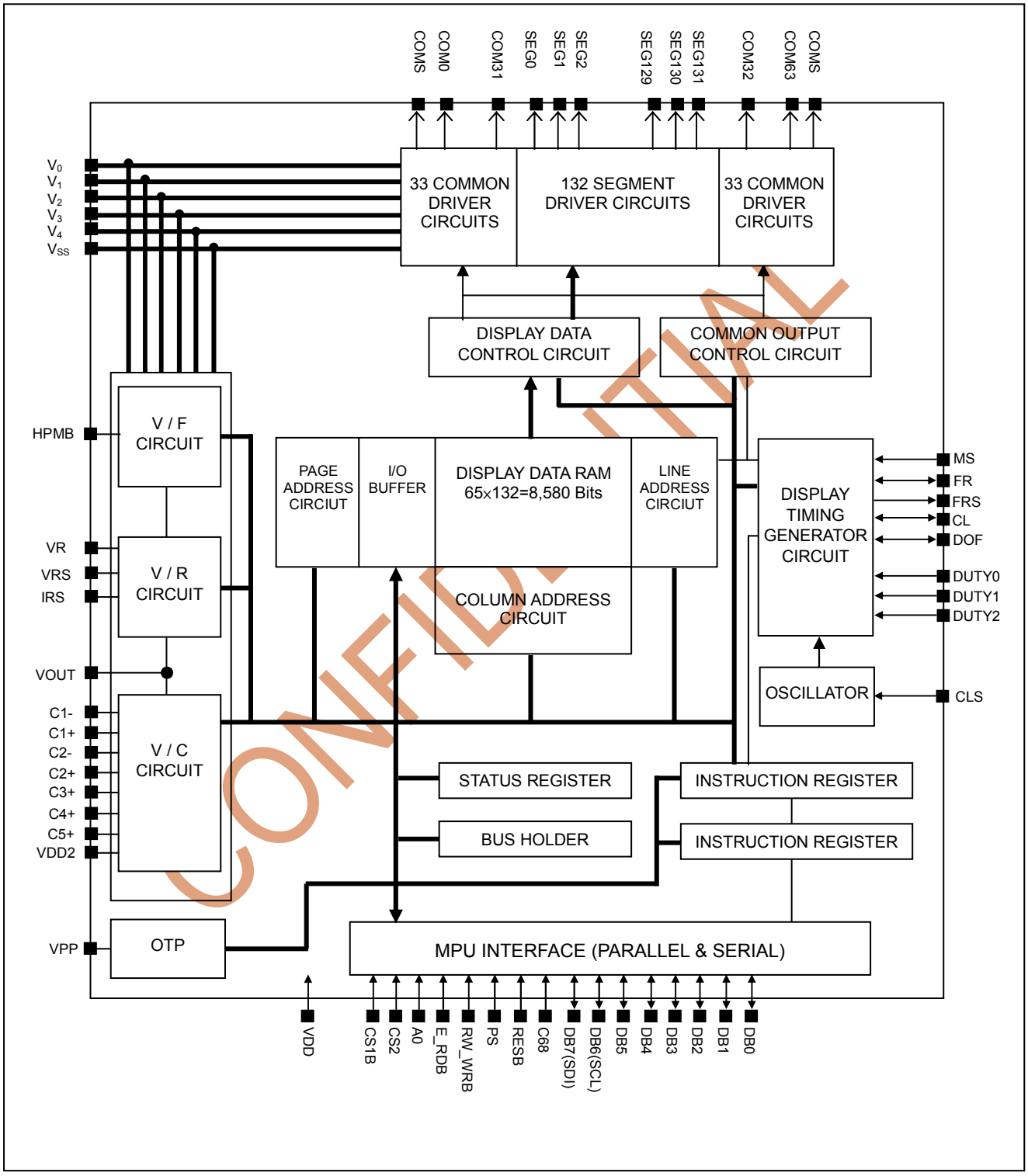
Operating Temperatures

- Wide range of operating temperatures from -30 to 80

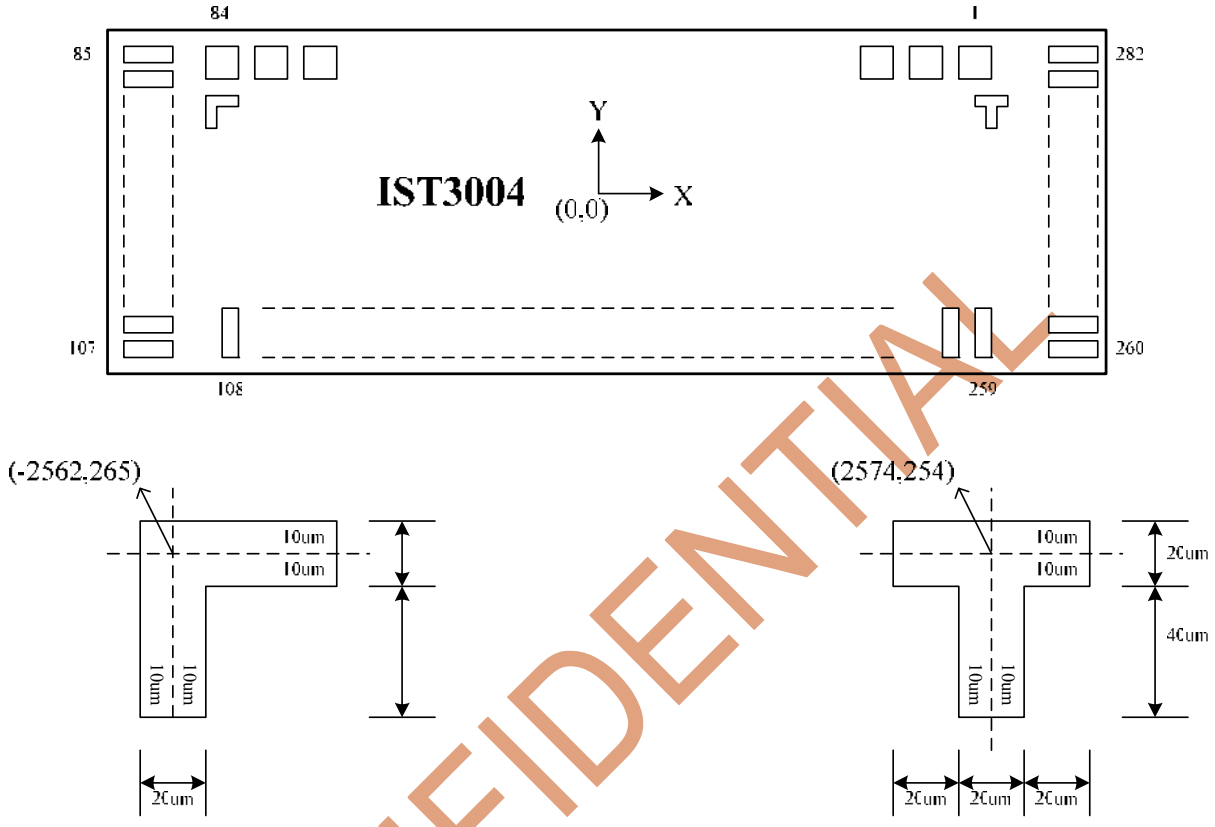
Package Type

- COG(Gold-bumped bared chip)

BLOCK DIAGRAM



PAD CONFIGURATION



Chip Size	5900 um x 1000 um	
Bump Pitch	34um (min)	
Bump Spacing	17um (min)	
Bump Size(X*Y)	42 x 54 um2	Pad No = 1 ~ 84
	118 x 17 um	Pad No = 85 ~ 107, 260 ~ 282
	17 x 118 um	Pad No = 108 ~ 259
Bump Height	15um (Typ)	
Chip Thickness	480um (Typ)	

PAD CENTER COORDINATES

Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)
1	FRS	2575	392	51	VRS	-468	392	101	COM<15>	-2810	-171
2	FR	2515	392	52	VDD2	-542	392	102	COM<14>	-2810	-205
3	CL	2455	392	53	VDD	-602	392	103	COM<13>	-2810	-239
4	DOF	2395	392	54	V4	-676	392	104	COM<12>	-2810	-273
5	VSS	2335	392	55	V4	-736	392	105	COM<11>	-2810	-307
6	CS1B	2275	392	56	V3	-796	392	106	COM<10>	-2810	-341
7	CS2	2215	392	57	V3	-856	392	107	COM<9>	-2810	-375
8	VDD	2155	392	58	V2	-916	392	108	COM<8>	-2573	-360
9	RESB	2095	392	59	V2	-976	392	109	COM<7>	-2539	-360
10	A0	2035	392	60	V1	-1036	392	110	COM<6>	-2505	-360
11	VSS	1975	392	61	V1	-1096	392	111	COM<5>	-2471	-360
12	RW_WRB	1915	392	62	V0	-1156	392	112	COM<4>	-2437	-360
13	E_RDB	1855	392	63	V0	-1216	392	113	COM<3>	-2403	-360
14	VDD	1795	392	64	VR	-1276	392	114	COM<2>	-2369	-360
15	DB<0>	1735	392	65	VR	-1336	392	115	COM<1>	-2335	-360
16	DB<1>	1675	392	66	VDD	-1410	392	116	COM<0>	-2301	-360
17	DB<2>	1615	392	67	VDD2	-1470	392	117	COMS2	-2267	-360
18	DB<3>	1555	392	68	TEST1	-1537	392	118	SEG<0>	-2227	-360
19	DB<4>	1495	392	69	TEST2	-1611	392	119	SEG<1>	-2193	-360
20	DB<5>	1435	392	70	TEST3	-1685	392	120	SEG<2>	-2159	-360
21	DB<6>	1375	392	71	TEST4	-1759	392	121	SEG<3>	-2125	-360
22	DB<7>	1315	392	72	TEST5	-1833	392	122	SEG<4>	-2091	-360
23	VDD	1255	392	73	VPP	-1907	392	123	SEG<5>	-2057	-360
24	VDD2	1195	392	74	VDD	-1974	392	124	SEG<6>	-2023	-360
25	VDD2	1135	392	75	MS	-2034	392	125	SEG<7>	-1989	-360
26	VSS	1075	392	76	CLS	-2094	392	126	SEG<8>	-1955	-360
27	VSS	1015	392	77	C68	-2154	392	127	SEG<9>	-1921	-360
28	VSS	955	392	78	PS	-2214	392	128	SEG<10>	-1887	-360
29	VSS	895	392	79	HPMB	-2274	392	129	SEG<11>	-1853	-360
30	VOUT	821	392	80	IRS	-2334	392	130	SEG<12>	-1819	-360
31	VOUT	761	392	81	DUTY0	-2394	392	131	SEG<13>	-1785	-360
32	C5+	701	392	82	DUTY1	-2454	392	132	SEG<14>	-1751	-360
33	C5+	641	392	83	DUTY2	-2514	392	133	SEG<15>	-1717	-360
34	C1-	581	392	84	GNDDMY	-2574	392	134	SEG<16>	-1683	-360
35	C1-	521	392	85	COM<31>	-2810	373	135	SEG<17>	-1649	-360
36	C3+	461	392	86	COM<30>	-2810	339	136	SEG<18>	-1615	-360
37	C3+	401	392	87	COM<29>	-2810	305	137	SEG<19>	-1581	-360
38	C1-	341	392	88	COM<28>	-2810	271	138	SEG<20>	-1547	-360
39	C1-	281	392	89	COM<27>	-2810	237	139	SEG<21>	-1513	-360
40	C1+	221	392	90	COM<26>	-2810	203	140	SEG<22>	-1479	-360
41	C1+	161	392	91	COM<25>	-2810	169	141	SEG<23>	-1445	-360
42	C2+	101	392	92	COM<24>	-2810	135	142	SEG<24>	-1411	-360
43	C2+	41	392	93	COM<23>	-2810	101	143	SEG<25>	-1377	-360
44	C2-	-19	392	94	COM<22>	-2810	67	144	SEG<26>	-1343	-360
45	C2-	-79	392	95	COM<21>	-2810	33	145	SEG<27>	-1309	-360
46	C4+	-139	392	96	COM<20>	-2810	-1	146	SEG<28>	-1275	-360
47	C4+	-199	392	97	COM<19>	-2810	-35	147	SEG<29>	-1241	-360
48	VSS	-273	392	98	COM<18>	-2810	-69	148	SEG<30>	-1207	-360
49	VSS	-333	392	99	COM<17>	-2810	-103	149	SEG<31>	-1173	-360
50	VRS	-408	392	100	COM<16>	-2810	-137	150	SEG<32>	-1139	-360

Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)
151	SEG<33>	-1105	-360	201	SEG<83>	595	-360	251	COM<33>	2301	-360
152	SEG<34>	-1071	-360	202	SEG<84>	629	-360	252	COM<34>	2335	-360
153	SEG<35>	-1037	-360	203	SEG<85>	663	-360	253	COM<35>	2369	-360
154	SEG<36>	-1003	-360	204	SEG<86>	697	-360	254	COM<36>	2403	-360
155	SEG<37>	-969	-360	205	SEG<87>	731	-360	255	COM<37>	2437	-360
156	SEG<38>	-935	-360	206	SEG<88>	765	-360	256	COM<38>	2471	-360
157	SEG<39>	-901	-360	207	SEG<89>	799	-360	257	COM<39>	2505	-360
158	SEG<40>	-867	-360	208	SEG<90>	833	-360	258	COM<40>	2539	-360
159	SEG<41>	-833	-360	209	SEG<91>	867	-360	259	COM<41>	2573	-360
160	SEG<42>	-799	-360	210	SEG<92>	901	-360	260	COM<42>	2810	-375
161	SEG<43>	-765	-360	211	SEG<93>	935	-360	261	COM<43>	2810	-341
162	SEG<44>	-731	-360	212	SEG<94>	969	-360	262	COM<44>	2810	-307
163	SEG<45>	-697	-360	213	SEG<95>	1003	-360	263	COM<45>	2810	-273
164	SEG<46>	-663	-360	214	SEG<96>	1037	-360	264	COM<46>	2810	-239
165	SEG<47>	-629	-360	215	SEG<97>	1071	-360	265	COM<47>	2810	-205
166	SEG<48>	-595	-360	216	SEG<98>	1105	-360	266	COM<48>	2810	-171
167	SEG<49>	-561	-360	217	SEG<99>	1139	-360	267	COM<49>	2810	-137
168	SEG<50>	-527	-360	218	SEG<100>	1173	-360	268	COM<50>	2810	-103
169	SEG<51>	-493	-360	219	SEG<101>	1207	-360	269	COM<51>	2810	-69
170	SEG<52>	-459	-360	220	SEG<102>	1241	-360	270	COM<52>	2810	-35
171	SEG<53>	-425	-360	221	SEG<103>	1275	-360	271	COM<53>	2810	-1
172	SEG<54>	-391	-360	222	SEG<104>	1309	-360	272	COM<54>	2810	33
173	SEG<55>	-357	-360	223	SEG<105>	1343	-360	273	COM<55>	2810	67
174	SEG<56>	-323	-360	224	SEG<106>	1377	-360	274	COM<56>	2810	101
175	SEG<57>	-289	-360	225	SEG<107>	1411	-360	275	COM<57>	2810	135
176	SEG<58>	-255	-360	226	SEG<108>	1445	-360	276	COM<58>	2810	169
177	SEG<59>	-221	-360	227	SEG<109>	1479	-360	277	COM<59>	2810	203
178	SEG<60>	-187	-360	228	SEG<110>	1513	-360	278	COM<60>	2810	237
179	SEG<61>	-153	-360	229	SEG<111>	1547	-360	279	COM<61>	2810	271
180	SEG<62>	-119	-360	230	SEG<112>	1581	-360	280	COM<62>	2810	305
181	SEG<63>	-85	-360	231	SEG<113>	1615	-360	281	COM<63>	2810	339
182	SEG<64>	-51	-360	232	SEG<114>	1649	-360	282	COMS1	2810	373
183	SEG<65>	-17	-360	233	SEG<115>	1683	-360	(END)	----	----	----
184	SEG<66>	17	-360	234	SEG<116>	1717	-360				
185	SEG<67>	51	-360	235	SEG<117>	1751	-360				
186	SEG<68>	85	-360	236	SEG<118>	1785	-360				
187	SEG<69>	119	-360	237	SEG<119>	1819	-360				
188	SEG<70>	153	-360	238	SEG<120>	1853	-360				
189	SEG<71>	187	-360	239	SEG<121>	1887	-360				
190	SEG<72>	221	-360	240	SEG<122>	1921	-360				
191	SEG<73>	255	-360	241	SEG<123>	1955	-360				
192	SEG<74>	289	-360	242	SEG<124>	1989	-360				
193	SEG<75>	323	-360	243	SEG<125>	2023	-360				
194	SEG<76>	357	-360	244	SEG<126>	2057	-360				
195	SEG<77>	391	-360	245	SEG<127>	2091	-360				
196	SEG<78>	425	-360	246	SEG<128>	2125	-360				
197	SEG<79>	459	-360	247	SEG<129>	2159	-360				
198	SEG<80>	493	-360	248	SEG<130>	2193	-360				
199	SEG<81>	527	-360	249	SEG<131>	2227	-360				
200	SEG<82>	561	-360	250	COM<32>	2267	-360				

PAD DESCRIPTION

Power Supply

Name	I/O	Description
VDD	Power Supply	Logic power supply The input voltage range is 2.4V ≤ VDD ≤ 3.6V
VDD2	Power Supply	Analog power supply The input voltage range is 2.4V ≤ VDD2 ≤ 3.6V
VSS	Power Supply	Ground
VPP	Power Supply	OTP (One-Time-Program) power source. Just keep open when not in OTP programming section
V0 V1 V2 V3 V4	I/O	LCD driver supply voltages The voltage determined by LCD pixel is impedance-converted by an operational amplifier for application. Voltages should have the following relationship; V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS When the internal power circuit is active, these voltages are generated as following as following table according to the state of LCD bias.

LCD bias	V1	V2	V3	V4
1/9 bias	(8/9) x V0	(7/9) x V0	(2/9) x V0	(1/9) x V0
1/8 bias	(7/8) x V0	(6/8) x V0	(2/8) x V0	(1/8) x V0
1/7 bias	(6/7) x V0	(5/7) x V0	(2/7) x V0	(1/7) x V0
1/6 bias	(5/6) x V0	(4/6) x V0	(2/6) x V0	(1/6) x V0
1/5 bias	(4/5) x V0	(3/5) x V0	(2/5) x V0	(1/5) x V0
1/4 bias	(3/4) x V0	(2/4) x V0	(2/4) x V0	(1/4) x V0

LCD Power Supply

Name	I/O	Description
C1-	O	Capacitor 1 negative connection pin for voltage converter
C1+	O	Capacitor 1 positive connection pin for voltage converter
C2-	O	Capacitor 2 negative connection pin for voltage converter
C2+	O	Capacitor 2 positive connection pin for voltage converter
C3+	O	Capacitor 3 positive connection pin for voltage converter
C4+	O	Capacitor 4 positive connection pin for voltage converter
C5+	O	Capacitor 5 positive connection pin for voltage converter
VOUT	I/O	Voltage converter output when the internal DC/DC converter is used If the panel loading too large for the internal DC/DC voltage converter to afford, user can disable internal Voltage Converter circuit & input external power through this pin to drive the remaining Power block (Voltage Regulator & Voltage Follower)
VRS	I/O	Test pin, please just keep this pin open
IRS	I	Voltage regulator internal/external resistor source select IRS = ”L” → Use external resistor source through VR terminal IRS = ”H” → Use internal resistor source
VR	O	Voltage regulator terminal When IRS = ”L”, the Voltage Regulator resistor will be decided by the external resistors connected between V0/VR & VR/VSS When IRS = “H”, please just keep this pin open

System Control

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>MS</td><td>I</td><td>MS = “H” : master mode, this pin must tied to “H” level
<table>
<tr><td>MS</td><td>CLS</td><td>OSC Circuit</td><td>Power Circuit</td><td>CL</td><td>FR</td><td>FRS</td><td>DOF</td></tr>
<tr><td>“H”</td><td>“H”
“L”</td><td>Enabled
Disabled</td><td>(by command)</td><td>Output
Input</td><td>Output
Output</td><td>Output
Output</td><td>Output
Output</td></tr>
<tr><td>“L”</td><td colspan="7">(MS = “L” is prohibited)</td></tr>
</table></td></tr>
<tr><td>CLS</td><td>I</td><td>Built-in oscillator circuit enable / disable select pin
- CLS = “H” : enable
- CLS = “L” : disable (external display clock input through CL pin)</td></tr>
<tr><td>CL</td><td>I/O</td><td>Display clock input / output pin</td></tr>
<tr><td>FR</td><td>I/O</td><td>Test pin, must keep open</td></tr>
<tr><td>FRS</td><td>O</td><td>Static driver output pin
This pin is used together with the FR pin.</td></tr>
<tr><td>DOF</td><td>I/O</td><td>Test pin, must keep open</td></tr>
<tr><td>HPMB</td><td>I</td><td>Power circuit driving ability control
- HPMB = “H” : Normal mode
- HPMB = “L” : High power mode</td></tr>
<tr><td>DUTY2
DUTY1
DUTY0</td><td>I</td><td>The LCD driver duty ratio & Bias selectable range listed on the following table
<table>
<tr><td>DUTY2</td><td>DUTY1</td><td>DUTY0</td><td>Duty ratio</td><td>Bias</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>1/65</td><td>1/9 or 1/7</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>1/49</td><td>1/8 or 1/6</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>1/33</td><td>1/6 or 1/5</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>1/55</td><td>1/8 or 1/6</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>1/53</td><td>1/8 or 1/6</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>1/17</td><td>1/5 or 1/4</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>1/9</td><td>1/5 or 1/4</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>1/1</td><td>1/5 or 1/4</td></tr>
</table></td></tr>
</table>

Micro-Controller Interface

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>RESB</td><td>I</td><td>Hardware Reset input pin
When RESB is “L”, initialization is executed.</td></tr>
<tr><td>PS</td><td>I</td><td>Parallel / serial data input select input
<table>
<tr><th>PS</th><th>Interface mode</th><th>Chip select</th><th>Data / instruction</th><th>Data</th><th>Read / Write</th><th>Serial clock</th></tr>
<tr><td>H</td><td>Parallel</td><td>CS1B, CS2</td><td>A0</td><td>DB0 to DB7</td><td>E_RDB RW_WRB</td><td>--</td></tr>
<tr><td>L</td><td>Serial</td><td>CS1B, CS2</td><td>A0</td><td>SDI (DB7)</td><td>Write only</td><td>SCL (DB6)</td></tr>
</table>
<NOTE> In serial mode, it is impossible to read data from the on-chip RAM. And DB0 to DB5 and E_RDB and RW_WRB must be fixed to either “H” or “L”.</td></tr>
<tr><td>C68</td><td>I</td><td>Microprocessor Interface Select input pin in parallel mode
- C68 = “H” : 6800-series MPU interface
- C68 = “L” : 8080-series MPU interface</td></tr>
<tr><td>CS1B
CS2</td><td>I</td><td>Chip select input pins
Data / instruction I/O is enabled only when CS1B is “L” and CS2 is “H”. when chip select is non-active, DB0 to DB7 may be high impedance.</td></tr>
<tr><td>A0</td><td>I</td><td>Register select input pin
- A0 = “H” : DB0 to DB7 are display data
- A0 = “L” : DB0 to DB7 are control data</td></tr>
<tr><td>RW_WRB</td><td>I</td><td>Read / Write execution control pin
<table>
<tr><th>C68</th><th>MPU Type</th><th>RW_WRB</th><th>Description</th></tr>
<tr><td>H</td><td>6800-series</td><td>RW</td><td>Read / Write control input pin
- RW = “H” : read
- RW = “L” : write</td></tr>
<tr><td>L</td><td>8080-series</td><td>/WRB</td><td>Write enable clock input pin
The data on DB0 to DB7 are latched at the rising edge of the /WRB signal.</td></tr>
</table></td></tr>
<tr><td>E_RDB</td><td>I</td><td>Read / Write execution control pin
<table>
<tr><th>C68</th><th>MPU Type</th><th>E_RDB</th><th>Description</th></tr>
<tr><td>H</td><td>6800-series</td><td>E</td><td>Read / Write control input pin
- RW = “H” : When E is “H”, DB0 to DB7 are in an output status.
- RW = “L” : The data on DB0 to DB7 are latched at the falling edge the E signal.</td></tr>
<tr><td>L</td><td>8080-series</td><td>/RDB</td><td>Read enable clock input pin
When / RDB is “L”, DB0 to DB7 are in an output status.</td></tr>
</table></td></tr>
<tr><td>DB0
to
DB7</td><td>I/O</td><td>8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus. When the serial interface selected (PS = “L”);
- DB0 to DB5 : high impedance
- DB6 : serial input clock (SCL)
- DB7 : serial input data (SDI)
When chip select is not active, DB0 to DB7 may be high impedance.</td></tr>
<tr><td>TEST1~5</td><td>I/O</td><td>Test pins, must keep them open</td></tr>
</table>

LCD Driver Outputs

<table>
<tr><th>Name</th><th>I/O</th><th colspan="4">Description</th></tr>
<tr><td rowspan="8">SEG0 ~
SEG131</td><td rowspan="8">O</td><td colspan="4">LCD segment driver outputs
The display data and the FR signal control the output voltage of segment driver.</td></tr>
<tr><td colspan="2" rowspan="2">Display data</td><td colspan="2" rowspan="2">FR</td><td colspan="2">Segment driver output voltage</td></tr>
<tr><td>Normal display</td><td>Reverse display</td></tr>
<tr><td colspan="2">H</td><td colspan="2">H</td><td>V0</td><td>V2</td></tr>
<tr><td colspan="2">H</td><td colspan="2">L</td><td>Vss</td><td>V3</td></tr>
<tr><td colspan="2">L</td><td colspan="2">H</td><td>V2</td><td>V0</td></tr>
<tr><td colspan="2">L</td><td colspan="2">L</td><td>V3</td><td>Vss</td></tr>
<tr><td colspan="4">Power save mode</td><td>Vss</td><td>Vss</td></tr>
<tr><td colspan="4"></td></tr>
<tr><td rowspan="6">COM0 ~
COM63</td><td rowspan="6">O</td><td colspan="4">LCD common driver outputs
The internal scanning data and the FR signal control the output voltage of segment driver.</td></tr>
<tr><td colspan="2">Scan data</td><td colspan="2">FR</td><td colspan="2">Common driver output voltage</td></tr>
<tr><td colspan="2">H</td><td colspan="2">H</td><td colspan="2">Vss</td></tr>
<tr><td colspan="2">H</td><td colspan="2">L</td><td colspan="2">V0</td></tr>
<tr><td colspan="2">L</td><td colspan="2">H</td><td colspan="2">V1</td></tr>
<tr><td colspan="2">L</td><td colspan="2">L</td><td colspan="2">V4</td></tr>
<tr><td colspan="4">Power save mode</td><td colspan="2">Vss</td></tr>
<tr><td>COMS1
COMS2</td><td>O</td><td colspan="4">Common output for the icons
These two pins output the same signal, When not be used, these pins should be left Open.</td></tr>
</table>

I/O PIN ITO Resister Limitation

PIN Name	ITO Resister
VDD,VDD2,VSS,VOUT,VR	<200Ω
V0,V1,V2,V3,V4,C1+/- ~C5+	<300Ω
CS1B,CS2,RW_WRB,E_RDB,A0,DB0~DB7	<1KΩ
RESB	<10KΩ
FR,CL,FRS,DOF,C68,PS,MS,HPMB,DUTY0~2,CLS,IRS	No Limitation
VRS,TESTx	Floating
VPP	<500Ω

FUNCTIONAL DESCRIPTION

Microprocessor Interface

Chip select control

There are CS1B and CS2 pins for chip selection. The IST3004 can interface with an MPU only when CS1B is "L" and CS2 is "H". When these pins are set to any other combination,
A0, E_RDB, and RW_WRB inputs are disabled and DB0 to DB7 are high impedance. In case of serial interface, the internal shift registers and the counter are reset.

MPU Interface types

IST3004 has three types of MPU interface, which are one serial and two parallel interfaces. This parallel or serial interface is determined by PS pin as shown below.

PS	Type	CS1B	CS2	C68	Interface mode
H	Parallel	CS1B	CS2	H	6800-series MPU mode
				L	8080-series MPU mode
L	Serial	CS1B	CS2	*×	Serial-mode

*× : Don't care

Parallel Interface (PS = "H")

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by C68. The type of data transfer is determined by signals at A0, E_RDB and RW_WRB as shown below.

C68	CS1B	CS2	A0	E_RDB	RW_WRB	DB0 to DB7	MPU bus
H	CS1B	CS2	A0	E	RW	DB0 to DB7	6800-series
L	CS1B	CS2	A0	/RDB	/WRB	DB0 to DB7	8080-series

Common	6800-series		8080-series		Description
A0	E_RDB (E)	RW_WRB (RW)	E_RDB (/RDB)	RW_WRB (/WRB)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register (instruction)

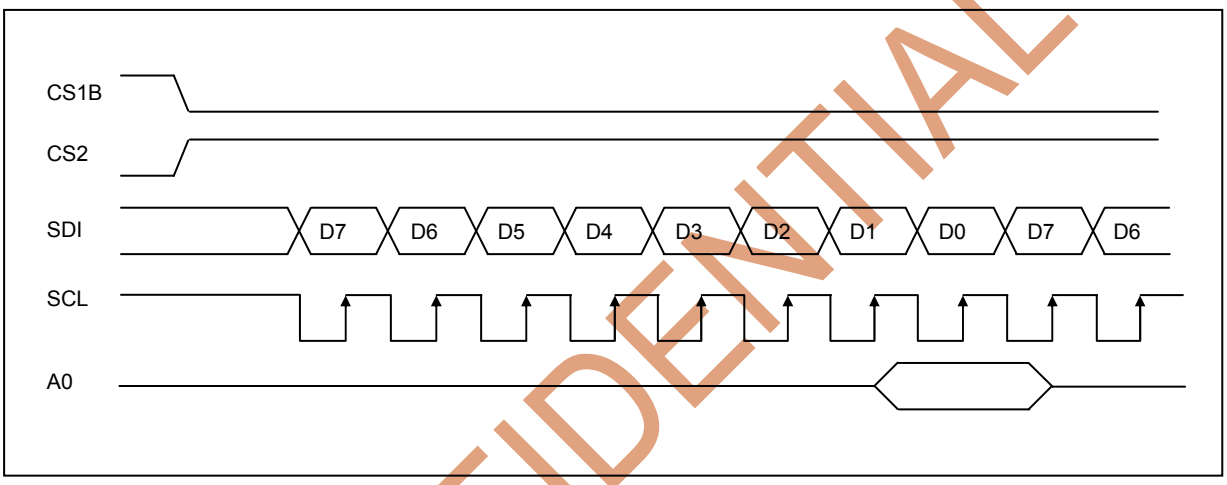
Serial Interface (PS = "L")

When PS = "L", the IST3004 is configured as Serial interface, the serial data can be input through DB7 (SDI) and serial clock can be input through DB6 (SCL).

When the chip is selected (CS1B="L", CS2="H"), the serial data can be shifted in sequentially at the rising edge of SCL and transferred to 8-bit parallel data internally; at the eighth SCL rising edge, A0 will also be sampled to decide these 8-bit data is interpreted as command or display data.

When the chip is not selected, the shift register & serial data counter will be reset and SDI & SCL will also be disabled internally.

Serial Interface Timing



Busy Flag

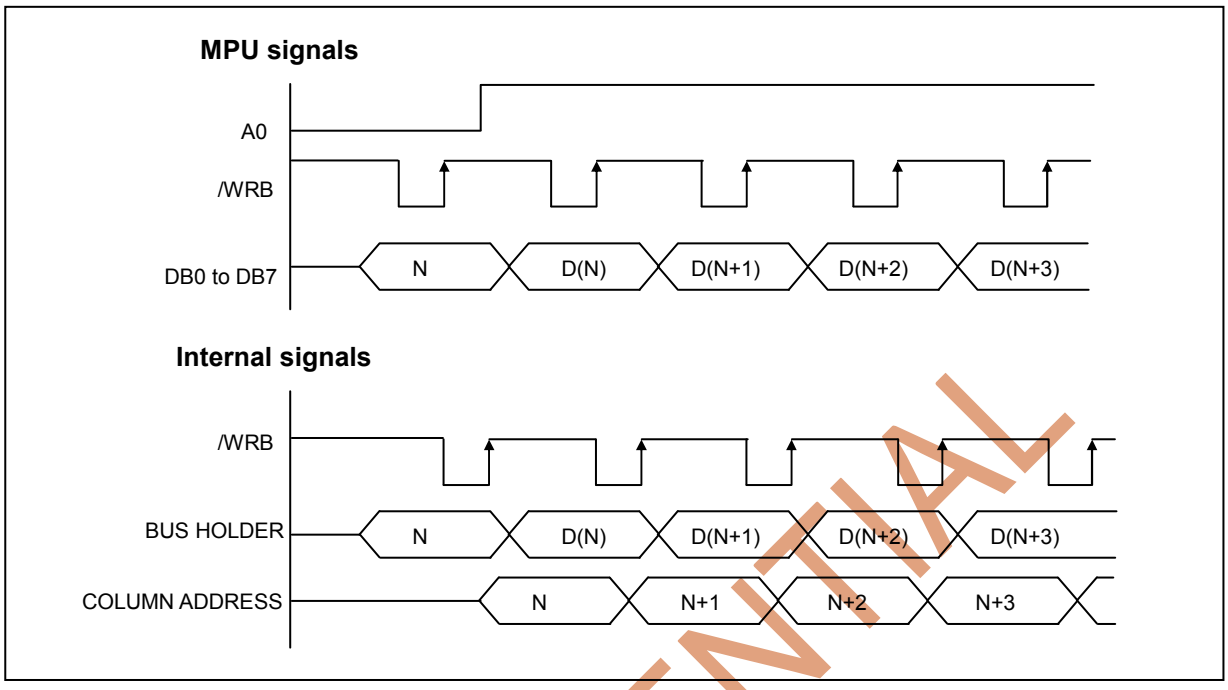
The Busy Flag indicates whether the IST3004 is still during operation or not. When DB7 is "H" in read status operation, this device is in busy status and will accept only read status instruction. If the write cycle time is correct, the microprocessor needs not to check this flag before each instruction to improve the operation efficiency.

Data Transfer

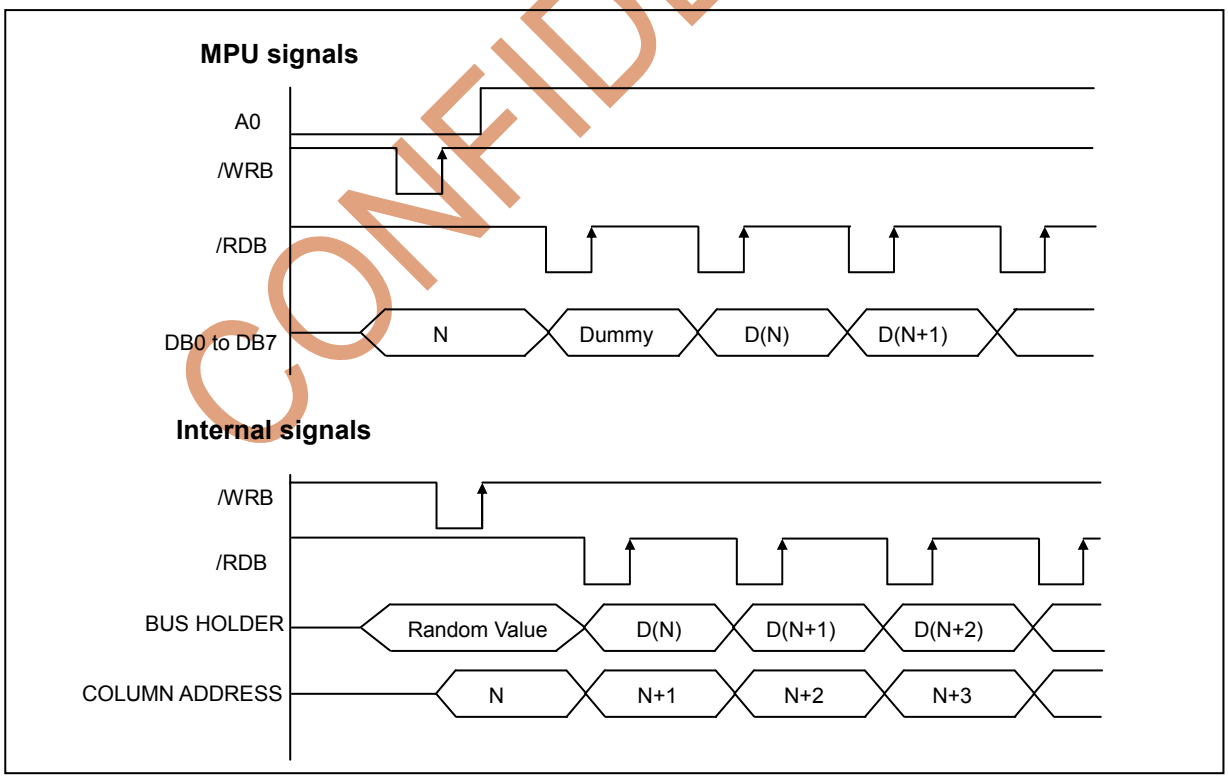
The IST3004 has a I/O bus holder stage to temporary storage the data received from MPU or on-chip RAM data requesting from MPU to read.

When user wants to read out the on-chip RAM data, after setting the address, a "dummy read" cycle must be inserted first to clean out the data stored in the output bus holder, so please just skip this dummy read data and the target RAM data can be read out from the second read cycle.

Write Timing



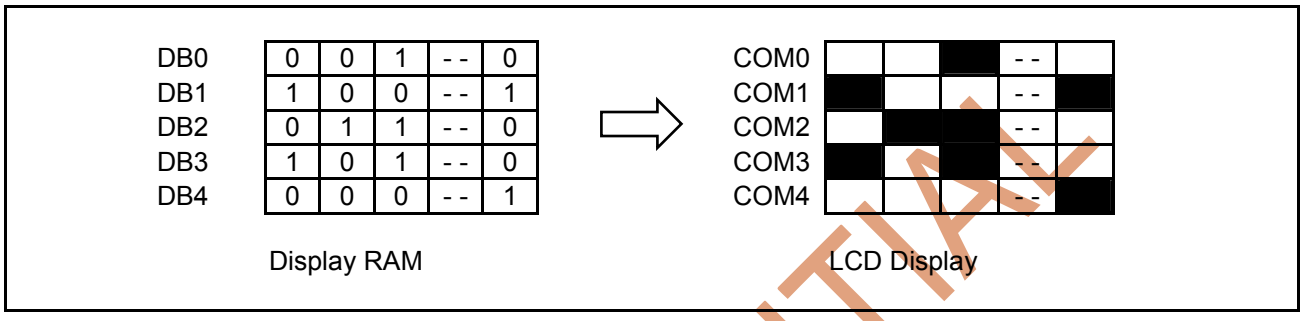
Read Timing



Display RAM

The IST3004 embedded a one-on-one bit-pixel mapping display RAM to storage the display image data. The RAM size is 65(row) x 132(column) bits. Each pixel can be selected when the page and column addresses are specified. The 65 rows are divided into 8 pages of 8 lines and the 9th page with a single line (DB0 only). Data is read from or written to by 8-bit width through DB0 to DB7. The display data & LCD display mapping is illustrated as below.

The display RAM is designed with two ports, so when display is turned on, the internal LCD display operation and MPU display RAM access is independent and will not affect each other



Page Address Circuit

This circuit will generate the Page Address of display RAM. It incorporates 4-bit Page Address register changed by only the “Set Page” instruction. Page Address 8 is a special RAM area for the icons and display data DB0 is only valid. When Page Address is above 8, the RAM access is invalid.

Line Address Circuit

This circuit generates the Line address for the display RAM corresponding to the first line (COM0) of the display. Therefore, by setting starting line address repeatedly, it is possible to realize the screen scrolling without changing the contents of on-chip RAM.

Column Address Circuit

Column Address circuit has 8-bit preset counter that provides column address to the Display RAM. When set Column Address MSB / LSB instruction is issued, 8-bit [Y7:Y0] Column address is updated.

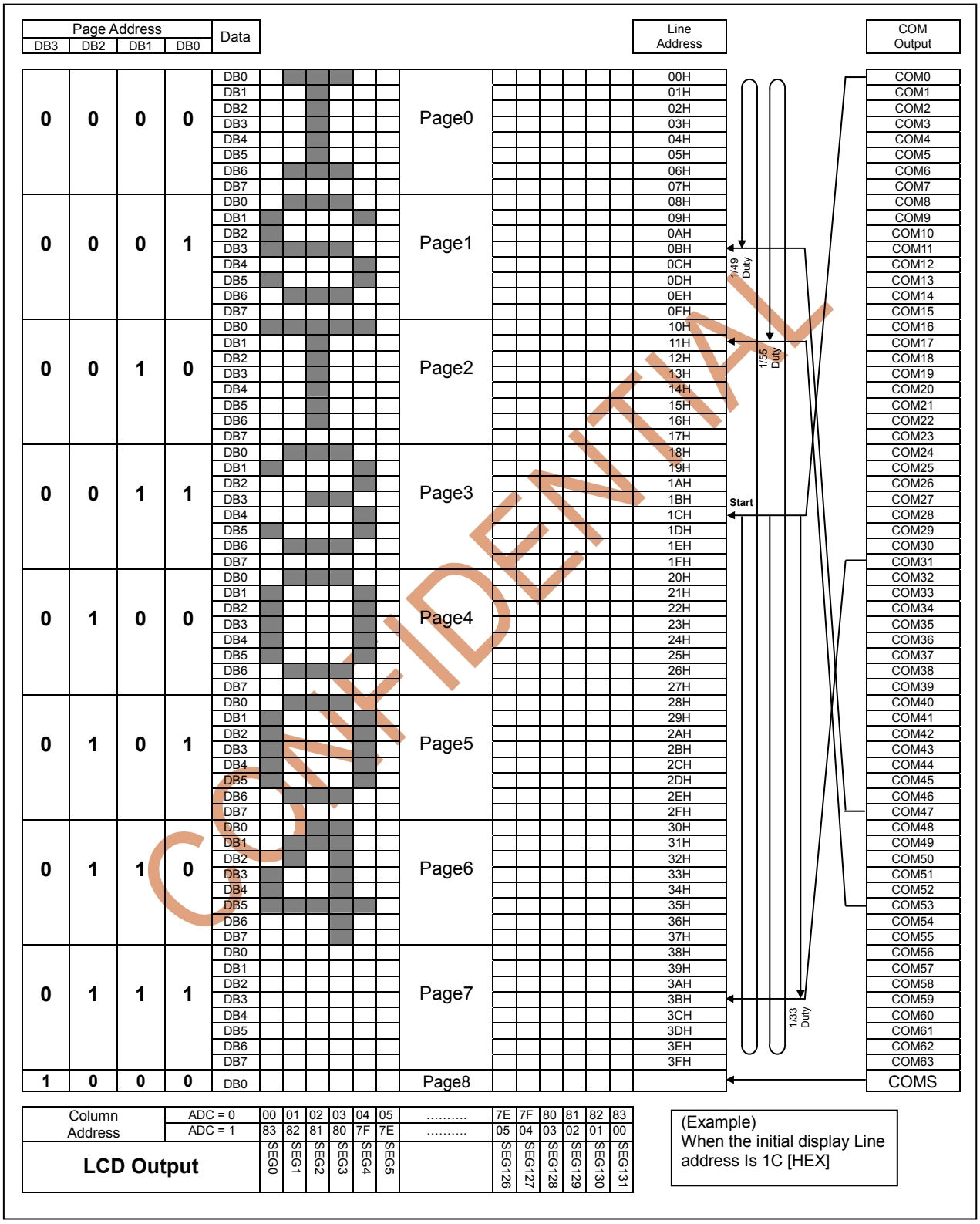
The specified column address is increased by one (+1) for each display RAM read or write instruction, so MPU can access the display RAM data continuously after setting the starting Column address. However, the address increment will stop at 83H. Because only the Column address will auto-increment, when the Page address need to be changed, the Page and Column address have to be set up again.

ADC select instruction makes it possible to invert the relationship between the Column Address and the segment outputs. It is necessary to rewrite the display RAM data after change the ADC setting.

The Relationship between the Column Address and the Segment Outputs

SEG output	SEG 0	SEG 1	SEG 2	SEG 3	… …	SEG 128	SEG 129	SEG 130	SEG 131
Column address[Y7:Y0]	00H	01H	02H	03H	… …	80H	81H	82H	83H
Display data	1	0	1	0		1	1	0	0
LCD panel display (ADC = 0)	■		■			■	■		
	↑								↑
	↓								↓
LCD panel display (ADC = 1)			■	… …			■		■

Display RAM Address Mapping



LCD Display circuits

Oscillator

The IST3004 includes an on-chip RC-type oscillator circuit. This oscillator signal is used in the voltage converter and display timing generation circuit. The oscillator circuit is only enabled when MS = “H” and CLS = “H”. When on-chip oscillator is not used, CLS pin must be “L” condition and the external clock source must be input through CL pin.

Display Timing Generator Circuit

This circuit generates the control signals used for LCD display. The display clock source is from internal oscillation circuit or externally input through CL. It supports the LCD polarity inversion by frame or by lines. The COM/SEG AC timing (polarity inverted by frame) is illustrated as below.

AC Driving Waveform Illustration

Common Output Control Circuit

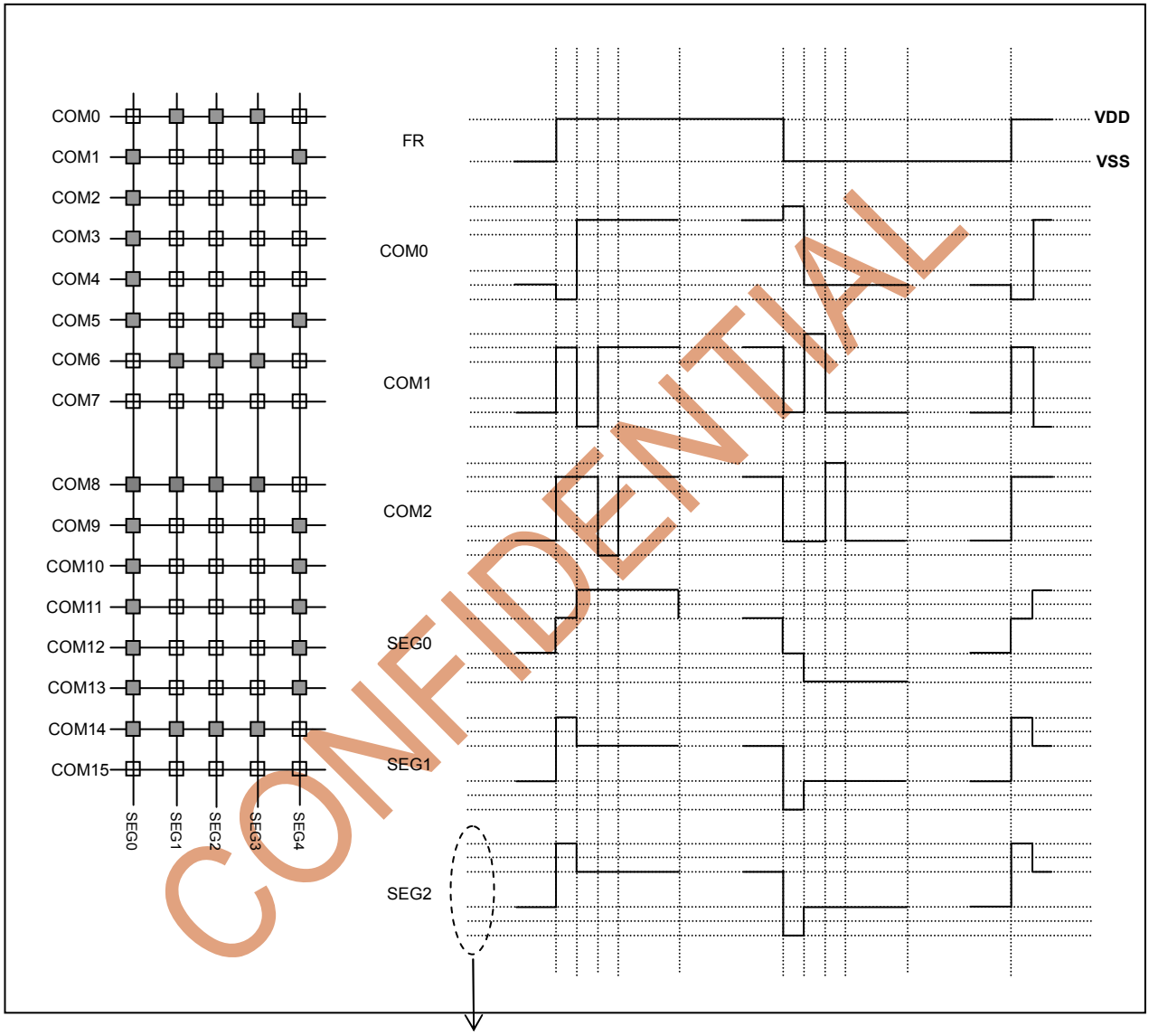
This circuit controls the Common scan direction and the duty selection. SHL instruction specifies the scanning direction of the common output pins. For example, when the duty is setting as 1/33 and SHL = "L", the Common scan sequence is from COM0 → COM15, then directly jumped to COM48 → COM63 → COMS, the unused COM pins (in this case when duty = 1/33, the unused COM pins are COM16 ~ COM47) must keep open. When Duty = 1/1, only the COMS will be activate.

Relationship between Duty Ratio and Common Output

		COM output channels												
Duty	SHL	[0:3]	[4:7]	[8:15]	[16:23]	[24:25]	[26]	[27:36]	[37]	[38:39]	[40:47]	[48:55]	[56:59]	[60:63]	COMS
1/1	0														COMS
	1														COMS
1/9	0	COM0 → COM3	→											COM60 → COM63	COMS
	1	COM0 ← COM3	←											COM60 ← COM63	COMS
1/17	0	COM0 → COM7		→									COM56 → COM63		COMS
	1	COM0 ← COM7		←									COM56 ← COM63		COMS
1/33	0	COM0 → COM15			→							COM48 → COM63			COMS
	1	COM0 ← COM15			←							COM48 ← COM63			COMS
1/49	0	COM0 → COM23				→					COM40 → COM63				COMS
	1	COM0 ← COM23				←					COM40 ← COM63				COMS
1/53	0	COM0 → COM25					→			COM38 → COM63					COMS
	1	COM0 ← COM25					←			COM38 ← COM63					COMS
1/55	0	COM0 → COM26						→		COM37 → COM63					COMS
	1	COM0 ← COM26						←		COM37 ← COM63					COMS
1/65	0	COM0 → COM63													COMS
	1	COM0 ← COM63													COMS

LCD Driving Circuits

This LCD driving circuit is configured by 66-channel (including 2 COMS channels) common driver and 132-channel segment driver. This LCD driving voltage depends on the combination of display data and FR signal.



- Total 6 driving voltages → V0 , V1 , V2 , V3 , V4 , VSS
- V0 ≧ V1 ≧ V2 ≧ V3 ≧ V4 ≧ VSS

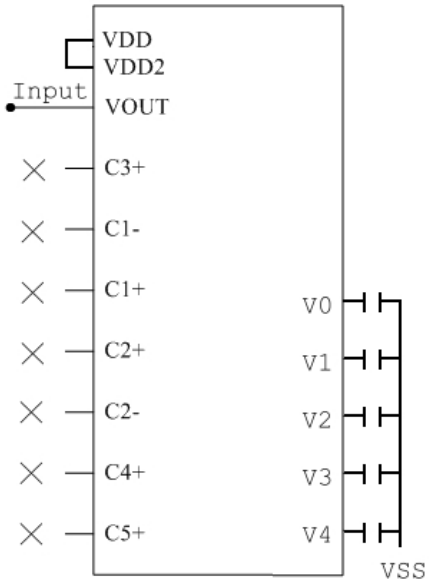
Power Supply Circuits

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits(VC), voltage regulator circuits(VR), and voltage follower circuits(VF). They are valid only in master operation and controlled by power control instruction. The possible LCD power supply configurations are listed as below.

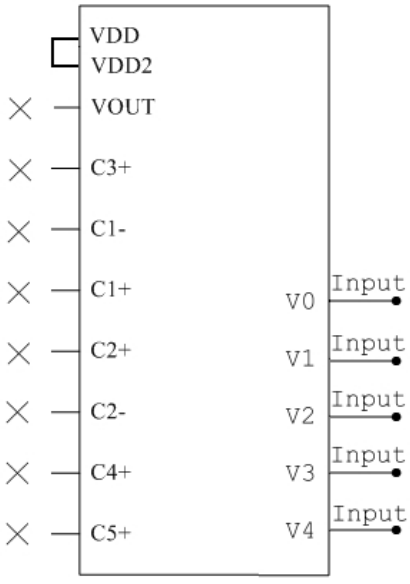
Power Supply Configurations

Power Configuration	Instruction (VC VR VF)	VC circuits	VR circuits	VF circuits	VOUT	V0	V1 to V4
Only the internal power supply circuits are used	(1 1 1)	ON	ON	ON	Open (*1)	Open (*1)	Open (*1)
Only the voltage regulator circuits and voltage follower circuits are used	(0 1 1)	OFF	ON	ON	External input	Open (*2)	Open (*2)
Only the external power supply circuits are used	(0 0 0)	OFF	OFF	OFF	Open	External input	External input

<Note>
*1. Vout, V0, V1~V4 have to connect external stabilizing capacitors to VSS individually.
*2. V0, V1~V4 have to connect external stabilizing capacitors to VSS individually



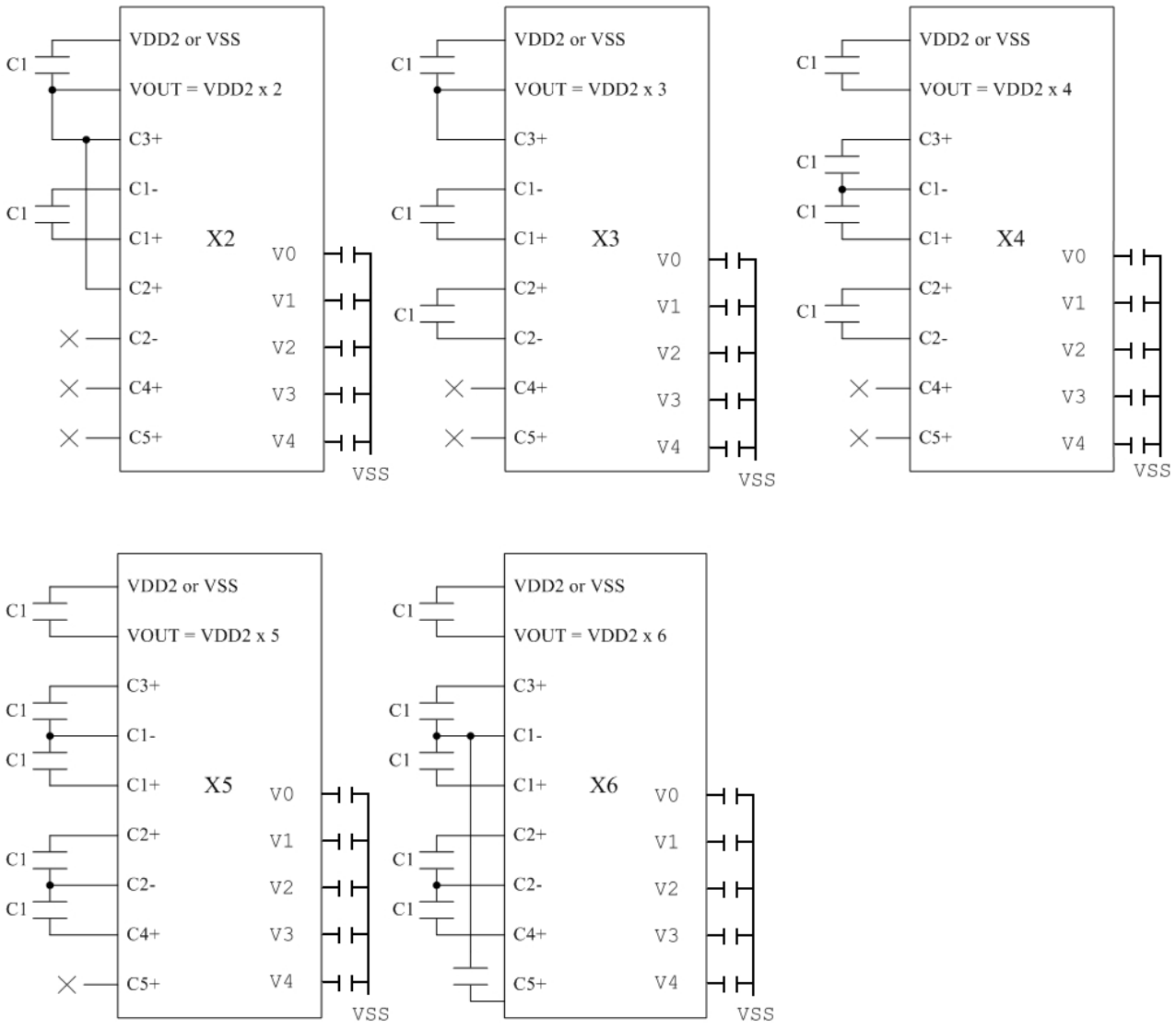
VC=0,VF=VR=1



VC=VF=VR=0

Voltage Converter Circuits

These circuits boost up the electric potential between VDD2 and VSS and the boost ratios are configurable between x2/x3/x4/x5/x6 times through the external booster capacitors' configurations, which are illustrated as below.



<Note>
*1. The Booster capacitor c1 = 1uF ~ 4.7uF
*2 The VDD2 = 2.4V ~ 3.6V, but the boost ratio configuration and that the boosted output VOUT level should not exceed 13.5V.

Voltage Regulator Circuits

The Voltage Regulator circuits generate the liquid crystal operating voltage (V0). The regulator resistors (Rb,Ra) can be selected to use internal or external by IRS pin, when use external resistors (IRS="L"), user can connect the Rb & Ra through VR terminal.

The V0 equation is listed as below

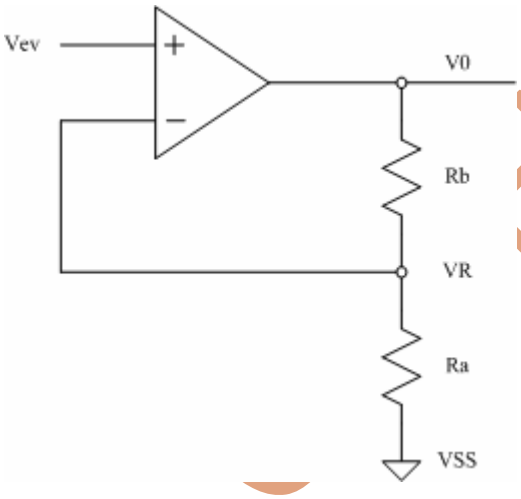
$$V0 = (1 + \frac{Rb}{Ra}) * (Vev) \quad (V)$$

$$= (1 + \frac{Rb}{Ra}) * (\frac{(162 - \alpha)}{162} * Vref) \quad [\, Vref = 2.1V,\ Temp.\ Coefficient = -0.05\%/℃ \,]$$

When using internal regulator resistors, the Rb/Ra ratio can be selected by instruction from 3.0 ~ 6.5 and the Contrast adjust scale (**α**) is 64-step adjustable from 0 ~ 63.

For example, when the temp. = 25℃ and using internal regulator resistors, the (1+Rb/Ra) ratio is setting to 6.0, Contrast scale **α** is setting to 30 (SV = 63-30 = 33) , then the target V0 = 6* 2.1* (162-30)/162 = 10.27V

When using external regulator resistors, the Rb/Ra ratio is decided by external resistors. For example, if Rb=1200KΩ, Ra=250 KΩ, temp. = 25℃, the Contrast adjust scale (**α**) setting is 32, then the target V0 = (1+1100/250)*2.1*(162-32)/162 = 9.77V



Voltage Follower Circuits

The Voltage Follower circuits resistively divide the liquid crystal operating voltage (V0) into four voltage levels (V1, V2, V3 and V4) and these voltage levels will be buffered output to serve as the LCD driving power sources.

Duty	DUTY2	DUTY1	DUTY0	BS	Bias	V1	V2	V3	V4
1/65	L	L	L	0	1/9	8/9 x V0	7/9 x V0	2/9 x V0	1/9 x V0
1/65	L	L	L	1	1/7	6/7 x V0	5/7 x V0	2/7 x V0	1/7 x V0
1/49	L	L	H	0	1/8	7/8 x V0	6/8 x V0	2/8 x V0	1/8 x V0
1/49	L	L	H	1	1/6	5/6 x V0	4/6 x V0	2/6 x V0	1/6 x V0
1/33	L	H	L	0	1/6	5/6 x V0	4/6 x V0	2/6 x V0	1/6 x V0
1/33	L	H	L	1	1/5	4/5 x V0	3/5 x V0	2/5 x V0	1/5 x V0
1/55	L	H	H	0	1/8	7/8 x V0	6/8 x V0	2/8 x V0	1/8 x V0
1/55	L	H	H	1	1/6	5/6 x V0	4/6 x V0	2/6 x V0	1/6 x V0
1/53	H	L	L	0	1/8	7/8 x V0	6/8 x V0	2/8 x V0	1/8 x V0
1/53	H	L	L	1	1/6	5/6 x V0	4/6 x V0	2/6 x V0	1/6 x V0
1/17	H	L	H	0	1/5	4/5 x V0	3/5 x V0	2/5 x V0	1/5 x V0
1/17	H	L	H	1	1/4	3/4 x V0	2/4 x V0	2/4 x V0	1/4 x V0
1/9	H	H	L	0	1/5	4/5 x V0	3/5 x V0	2/5 x V0	1/5 x V0
1/9	H	H	L	1	1/4	3/4 x V0	2/4 x V0	2/4 x V0	1/4 x V0
1/1	H	H	H	0	1/5	4/5 x V0	3/5 x V0	2/5 x V0	1/5 x V0
1/1	H	H	H	1	1/4	3/4 x V0	2/4 x V0	2/4 x V0	1/4 x V0

Reset Initialization

The IST3004 provides both hardware (H/W) reset and software (S/W) reset function. When the RESB is setting to “L”, the H/W reset will be activated, or user can use S/W reset instruction to initialize the internal registers’ configurations, but the H/W reset and S/W reset covered range is different, please check the table listed as below.

The default H/W reset initializing settings are listed as below:

No.	Register	Description
1.	DON=0	Display OFF
2.	REV=0	Reverse display OFF
3.	ADC=0	SEG output direction SEG0 → SEG131
4.	VC/VR/VF = 0/0/0	Internal Power circuits turned off
5.	(internal status)	Serial interface internal register data clear
6.	BS=0	LCD bias
7.	EON=0	Entire display OFF
8.	(internal status)	Power saving clear
9.	R2-0 = 0	Regulator internal resistor ratio
10.	(internal status)	SEG/COM output VSS level
11.	(internal status)	Read-Modify-Write OFF
12.	SM/S1/S0 = 0/0/0	Static indicator OFF
13.	ST = 0	Display start line address = 0
14.	Y7-0 = 0	Column address = 0
15.	P3~0 = 0	Page address = 0
16.	SHL = 0	Common scan direction = COM0 → COM63
17.	(internal status)	Set reference voltage mode clear
18.	SV5-0 = 10000	Electronic volume register
19.	(internal status)	Test mode cleared

★ For S/W reset , only the 11 ~ 19 items above will be reinitialized.

When doing the H/W reset (RESB = “L”), the V0 will also discharge to VSS level internally, so when using external LCD power sources, please input these power sources only when the H/W reset process has been finished (RESB is backing to “H”) .

Command Table

× : Don't care

INSTRUCTION	A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Display ON / OFF	0	0	1	0	1	0	1	1	1	DON	LCD display On/Off control DON = 0 : display OFF DON = 1 : display On
Display starting line	0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0	Specify the line address for the first COM output
page address	0	0	1	0	1	1	P3	P2	P1	P0	Set page address
Set column address MSB	0	0	0	0	0	1	Y7	Y6	Y5	Y4	Set column address MSB
Set column address LSB	0	0	0	0	0	0	Y3	Y2	Y1	Y0	Set column address LSB
Read status	0	1	BUSY	ADC	ON/OFF	RESB	0	0	0	0	Read the internal status
Write display data	1	0	Write data								Write data into Display RAM
Read display data	1	1	Read data								Read data from Display RAM
ADC select	0	0	1	0	1	0	0	0	0	ADC	SEG output direction select ADC = 0 : SEG0 → SEG131 ADC = 1 : SEG131 → SEG0
Reverse display ON / OFF	0	0	1	0	1	0	0	1	1	REV	Normal / Reverse display select REV = 0 : Reverse display off REV = 1 : Reverse display on
Entire display ON / OFF	0	0	1	0	1	0	0	1	0	EON	Entire display On/Off control EON = 0 : Entire display off EON = 1 : Entire display on
LCD bias select	0	0	1	0	1	0	0	0	1	BS	Select LCD bias
Set Read-modify-write (RMW)	0	0	1	1	1	0	0	0	0	0	Set Read-modify-write mode
Clear RMW	0	0	1	1	1	0	1	1	1	0	Clear Read-modify-write mode
S/W Reset	0	0	1	1	1	0	0	0	1	0	S/W Reset
SHL select	0	0	1	1	0	0	SHL	×	×	×	COM output direction select SHL = 0 : COM0 → COM63 SHL = 1 : COM63 → COM0
Power control	0	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation
Regulator resistor select	0	0	0	0	1	0	0	R2	R1	R0	Select internal resistance ratio of the regulator resistor
Set reference voltage mode	0	0	1	0	0	0	0	0	0	1	Set reference voltage mode (double byte command)
Set reference voltage register	0	0	×	×	SV5	SV4	SV3	SV2	SV1	SV0	Set reference voltage register
Set static indicator mode	0	0	1	0	1	0	1	1	0	SM	Set static indicator mode (double byte command)
Set static indicator register	0	0	×	×	×	×	×	×	S1	S0	Set static indicator register
Power save	-	-	-	-	-	-	-	-	-	-	Compound Instruction of display OFF and entire display ON
NOP	0	0	1	1	1	0	0	0	1	1	No operation (dummy command)
Set Booster Ratio select mode	0	0	1	1	1	1	1	0	0	0	Set Booster ration select mode (double byte command)
Set Booster Ratio register	0	0	x	x	x	x	x	x	BT1	BT0	Set Booster ration BT[1:0] = 00 : x2, x3, x4 BT[1:0] = 01 : x5 BT[1:0] = 11 : x6 BT[1:0] = 10 : (don't use)
Test Instruction	0	0	1	0	0	0	1	0	0	0	Test command (don't use)

COMMAND DESCRIPTION

Display ON / OFF

LCD display On / Off select

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	1	DON

DON = 1 : display ON
DON = 0 : display OFF

Display Starting Line

Sets the starting line address for the first common output (COM0 when SHL = L, COM63 when SHL = H)

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0

ST5	ST4	ST3	ST2	ST1	ST0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

Set Page Address

Sets the Page address of display data RAM for MPU Write/Read access. After setting the Page and/or Column address, user can write/read the internal display RAM consecutively. Only the Column address will auto-incremented by +1 until 83H.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	P3	P2	P1	P0

P3	P2	P1	P0	Page
0	0	0	0	0
0	0	0	1	1
:	:	:	:	:
0	1	1	1	7
1	0	0	0	8

Set Column Address

Sets the Column Address of display data RAM for MPU Write/Read access. After setting the Page and/or Column address, user can write/read the internal display RAM consecutively. Only the Column address will auto-incremented by +1 until 83H

Set Column Address MSB

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	Y7	Y6	Y5	Y4

Set Column Address LSB

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	Y3	Y2	Y1	Y0

Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	1	0	130
1	0	0	0	0	0	1	1	131

Read Status

Indicates the internal status of the IST3004

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BUSY	ADC	ON/OFF	RESB	0	0	0	0

Flag	Description
BUSY	BUSY = 1 : The chip is still under processing, including reset initialization BUSY = 0 : The chip is free to accept MPU commands
ADC	ADC = 1 : SEG direction is SEG131 → SEG0 ADC = 0 : SEG direction is SEG0 → SEG131
DISPLAY ON/OFF	ON/OFF = 1 : Display is turned off ON/OFF = 0 : Display is turned on * The polarity is reversed with DON command !
RESET	RESET = 1 : The chip is doing the H/W or S/W reset RESET = 0 : The chip isn't doing the reset operation * The polarity is reversed with RESB (H/W)

Write Display Data

8-bit display data can be written to the display RAM location specified by the column address and page address by this instruction. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page.

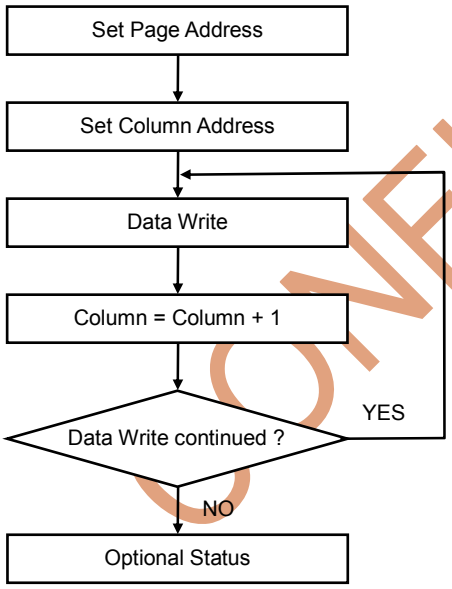
A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	Write data							

Data Read Display Data

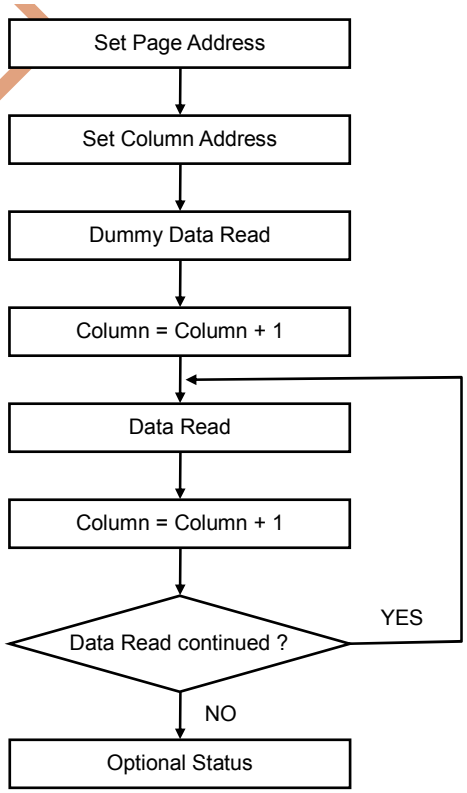
8-bit display data RAM specified by the column address and page address can be read by this instruction. As the column address is increased by 1 automatically after each this instruction, the microprocessor can continuously can continuously read data from the addressed page. A dummy read is required after specified the target column and/or page address. Display data cannot be read through the serial interface.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Read data							

Display RAM Write Sequence



Display RAM Read Sequence



ADC Select (Segment Driver Direction Select)

Defines the relationship between RAM column address and segment driver. The detailed mapping please referred to the “Display RAM Address Mapping” chapter.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	ADC

ADC = 0 : SEG0 → SEG131
ADC = 1 : SEG131 → SEG0

Reverse Display ON / OFF

Reverse the lit and unlit display relation between RAM bit data and LCD cell. This setting will not change the original display RAM data.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	1	REV

REV	RAM bit data = “1”	RAM bit data = “0”
0	LCD pixel will accumulated ON voltage	LCD pixel will accumulated OFF voltage
1	LCD pixel will accumulated OFF voltage	LCD pixel will accumulated ON voltage

Entire Display ON / OFF

Forces the whole LCD points to be turned on regardless of the contents of the display data RAM. This instruction will not change the original display RAM data and has higher priority than the reverse display ON / OFF instruction.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	0	EON

EON = 0 : Normal display
EON = 1 : Entire display ON

Select LCD Bias

Selects LCD bias ratio of the voltage required for driving the LCD.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	1	BS

Duty ratio	LCD bias	
	BS = 0	BS = 1
1/1	1/5	1/4
1/9	1/5	1/4
1/17	1/5	1/4
1/33	1/6	1/5
1/49	1/8	1/6
1/53	1/8	1/6
1/55	1/8	1/6
1/65	1/9	1/7

Set Read-Modify-Write (RMW)

This instruction stops the automatic increment of the column address by the read display data instruction, but the column address is still increased by the write display data instruction. It can reduce the load of microprocessor when the data of a specific area is repeatedly changed during cursor blinking or others. This mode is canceled by the Reset Read-Modify-Write instruction.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	0

Reset Read-Modify-Write

This instruction clears the Read-Modify-Write mode and makes the column address returns to the value when the set Read-Modify-Write instruction has been set.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	1	1	0

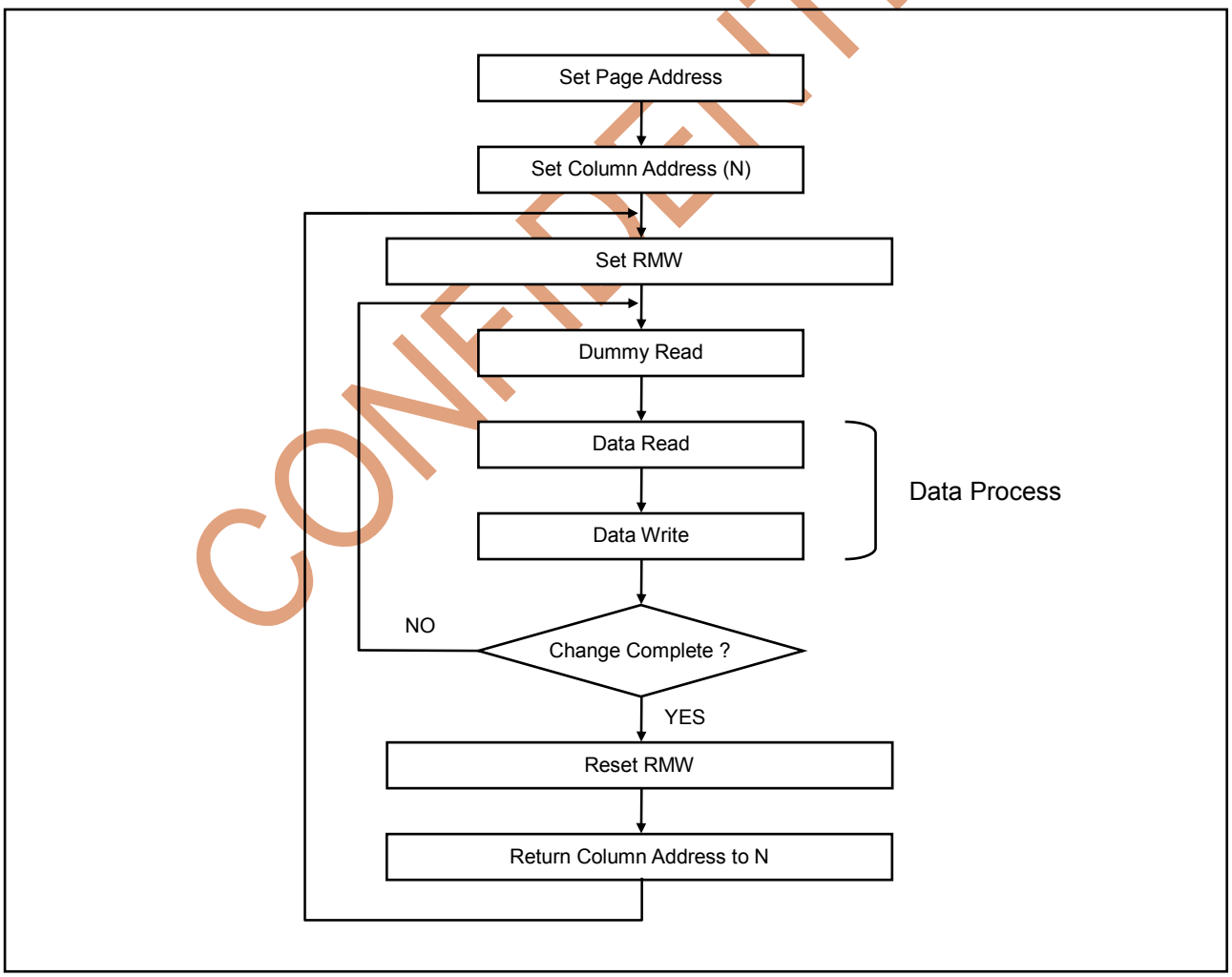


Figure 22. Sequence for Cursor Display

S/W Reset

This instruction will activate the internal S/W reset operation. The covered ranged is different with H/W reset, for details please refer to the “Reset Initialization” section.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	0

SHL Select (Common Output Mode Select)

Selects the COM output direction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	SHL	×	×	×

× : Don’t care

SHL = 0 : COM0 → COM63
SHL = 1 : COM63 → COM0

Power Control

Internal Power supply circuits On/Off control. For details please refer to the “Power Supply Circuits” section.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	1	VC	VR	VF

VC	VR	VF	Status of internal power supply circuits
0 1			Internal Voltage Converter circuit is OFF Internal Voltage Converter circuit is ON
	0 1		Internal Voltage Regulator circuit is OFF Internal Voltage Regulator circuit is ON
		0 1	Internal Voltage Follower circuit is OFF Internal Voltage Follower circuit is ON

Regulator Resistor Select

Select the resistor ratio (1+Rb/Ra) when using internal regulator resistors. For details please refer to the "Power Supply Circuits" section.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	0	R2	R1	R0

R2	R1	R0	(1 + Rb / Ra) ratio
0	0	0	3.0
0	0	1	3.5
0	1	0	4.0
0	1	1	4.5
1	0	0	5.0
1	0	1	5.5
1	1	0	6.0
1	1	1	6.5

Reference Voltage Select (double byte command)

The Reference voltage select instruction consists of 2-byte command. The 1st instruction sets reference voltage mode and the 2nd one is the contents of reference voltage register. These two instructions must be executed adjacently or the following commands sequence will be misinterpreted and lead to unexpected results.

The 1st instruction : Set Reference Voltage Select Mode

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	1

The 2nd instruction : Set Reference Voltage Register

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	×	SV5	SV4	SV3	SV2	SV1	SV0

SV5	SV4	SV3	SV2	SV1	SV0	Reference voltage Parameter (α)	V0	Contrast
0	0	0	0	0	0	63	Minimum	Low
0	0	0	0	0	1	62		
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	31 (default)	:	:
:	:	:	:	:	:	:	:	:
1	1	1	1	1	0	1		
1	1	1	1	1	1	0	Maximum	High

Set Static Indicator State

This command is used to control the Static indicator to be turned on or off and select the blinking mode.

When want to turn off the Static indicator, it is one-byte command and just setting SM = 0 is enough.

When want to turn on the Static indicator, it is two-byte command; the 1st byte command setting SM = 1, the 2nd byte command selects the blinking mode. It must be highlighted that whenever the SM is setting to 1, the 2nd byte instruction must be launched to satisfy the two-byte command cycle even though the blinking mode needs not to be changed.

The 1st instruction : Set Static Indicator Mode (NO / OFF)

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	0	SM

SM = 0 : static indicator OFF (One-byte command)
SM = 1 : static indicator ON (Two-byte command)

The 2nd instruction : Set Static Indicator Register

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	×	×	×	×	×	S1	S0

S1	S0	Status of static indicator output
0	0	OFF
0	1	ON (about 1 second blinking)
1	0	ON (about 0.5 second blinking)
1	1	ON (always ON)

NOP

No-Operation command (dummy command).

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	1

Booster Ratio Select (double byte command)

The Booster ratio will be decided by the Booster ratio registers' setting & the external Booster capacitors' configuration. About the Booster external capacitors' configuration please refer to the illustration described in the "Voltage Converter Circuits" section.

The 1st instruction : Set Booster Ration Select Mode

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	1	0	0	0

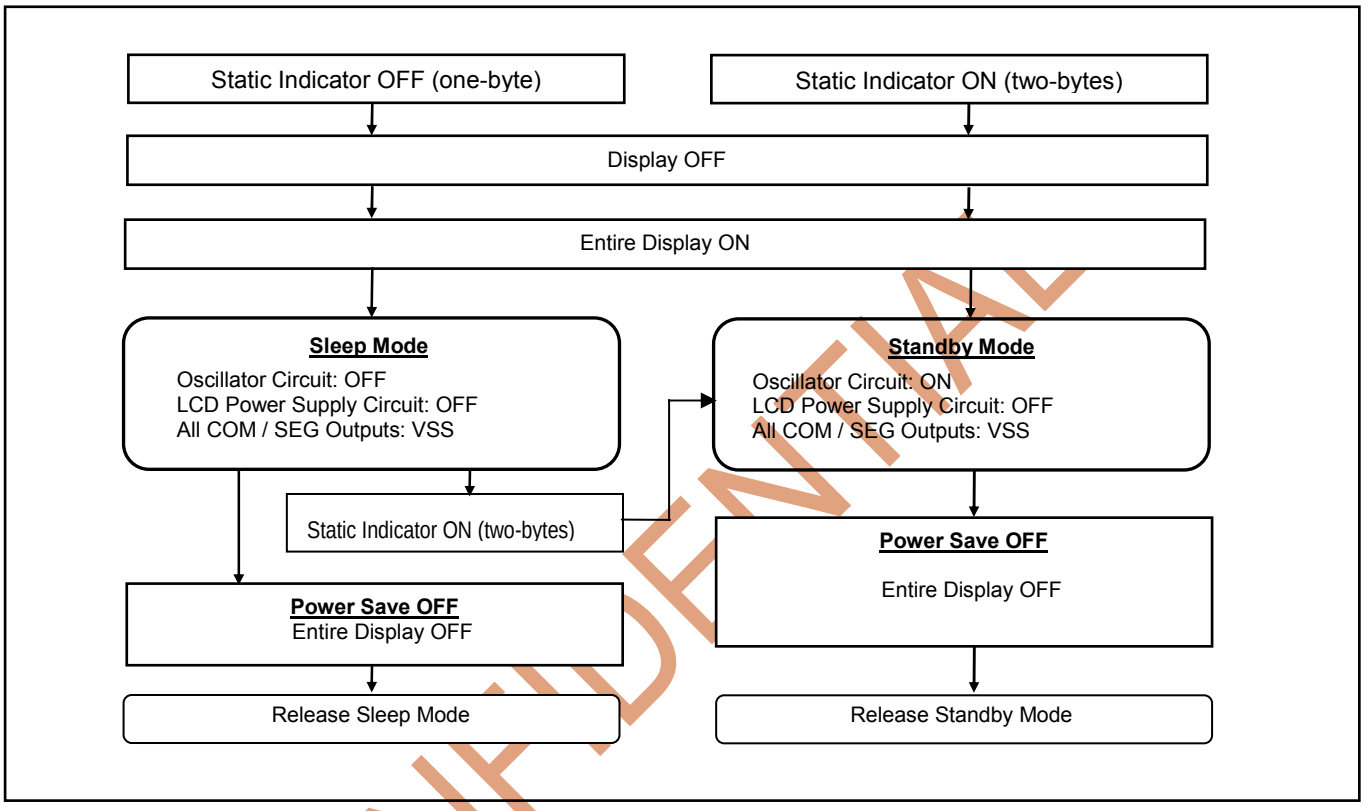
The 2nd instruction : Set Booster Ratio Register

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	×	×	×	×	×	BT1	BT0

BT1	BT0	Booster Ratio	Decsription
0	0	x2, x3, x4	* The external Booster capacitors' configuration will decide the exact Booster ratio is x2 , x3 or x4
0	1	x5	* Must also follow the x5 Booster capacitors' configuration
1	0	(don't use)	
1	1	x6	* Must also follow the x6 Booster capacitors' configuration

Power Save (Compound Instruction)

If the “Entire display ON / OFF” instruction is issued during the “Display OFF” state, IST3004 enters the Power Save mode to reduce the power consumption. There’re two types of Power Save mode, Sleep and Standby mode, depending on the Static Indicator status. It’ll enter Sleep mode if the Static Indicator is in OFF state or it’ll enter Standby mode if the Static Indicator is in ON state. Power Save mode is released by the Entire display OFF instruction.



- Sleep Mode

  It’ll stop all the operations in this chip, as long as there are no accesses from the MPU, the power consumption is close to the static leakage current.
  The internal statuses during sleep mode are as below:

  a. The oscillator circuit and the LCD power supply circuit are turned off.
  b. All liquid crystal drive circuits are stop, all the LCD driving outputs (SEGx/COMx/COMSx) output VSS level..

- Standby Mode

  The internal status and LCD outputs are the same as Sleep mode, except the Static Indicator driving system and also Oscillator circuits are still enabled. When S/W Reset command is performed in Standby mode, the system will enter Sleep mode immediately.

OTP PROGRAMMING CONTROL

OTP Command Table

INSTRUCTION	A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
OTP Command Entry	0	0	1	0	0	0	0	0	0	0	OTP Command decode entry
OTP Adjust Control	0	0	0	0	0	0	0	0	OTP ADJ	0	OTPADJ=1/0: Enable/Disable OTP adjust control
OTP Read Address Set	0	0	0	0	0	0	0	1	OTPRA		OTP Read address select
OTP V1 Offset Adjust	0	0	0	0	0	0	1	VF1<2:0>			VF1 = V1 offset adjust
OTP V4 Offset Adjust	0	0	0	0	0	1	0	VF4<2:0>			VF4 = V4 offset adjust
OTP CTA Offset Adjust	0	0	0	1	0	1	CTA<3:0>				CTA = 1st SV (Contrast) offset
OTP CTB Offset Adjust	0	0	0	1	1	0	CTB<3:0>				CTB = 2nd SV (Contrast) offset
OTP Program Enable	0	0	1	0	1	0	0	0	0	0	Enable OTP Program
OTP Program Start	0	0	1	1	1	1	0	0	0	1	Start to program OTP
NOP	0	0	1	1	1	0	0	0	1	1	OTP command section release

OTP Command Entry (80h)

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	0

IST3004 embedded OTP (One-Time-Programming) memories for users to store individual settings by modules to keep a consistent display quality. User can use 80h command to enter the OTP command mode and then the following commands will be interpreted as OTP commands (listed as above). After the OTP commands' setting have been finished, use NOP (E3h) command can leave the OTP command section and then back to the normal command section.

After entered the OTP command section, user can first use the provided OTP adjustable parameters to preview the adjusted display results, after the display quality has been satisfied, then use OTP Program Start(F1h) command to start programming all the ready registered settings into OTP memory cells at the same time. After the OTP programming has been be finished, the programmed OTP values will be automatically reloaded. When H/W or S/W reset has been executed, the OTP programmed settings will also be reloaded.

OTP Adjust Control

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	OTPADJ	0

* default OTPADJ=1

OTPADJ can enable/disable the OTP adjust function. When OTADJ = 0, all the programmed OTP settings will be ignored.

Once the OTP parameters (CTA, CTB, VF1, VF2) have been programmed to a non-zero values and reload automatically, If OTPADJ=1, the programmed settings stored in OTP memory cells will substitute for the really active parameters and ignore the registered OTP command settings. If OTPADJ=0, the OTP command register settings will take the place of really active parameters and ignore the settings stored in OTP memory cells.

OTP Program Enable

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	0

Once execute OTP Program Enable (A0h) command, the OTP programming section is enabled and waiting for the OTP Program Start command to automatically start the whole OTP programming section.

OTP Program Start

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	0	0	1

Once execute OTP Program Start (F1h) command, the OTP programming section will automatically get started, it takes about 10ms to complete the whole OTP programming section.

OTP 1st/2nd Contrast Offset adjust (CTA/CTB)

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	1	CTA<3:0>			
0	0	0	1	1	0	CTB<3:0>			

CTA/CTB SV Offset adjust Table

CTA<3:0>/CTB<3:0>				SV adjusted
0	0	0	0	0(default)
0	0	0	1	+1
0	0	1	0	+2
0	0	1	1	+3
0	1	0	0	+4
0	1	0	1	+5
0	1	1	0	+6
0	1	1	1	+7
1	1	1	1	-1
1	1	1	0	-2
1	1	0	1	-3
1	1	0	0	-4
1	0	1	1	-5
1	0	1	0	-6
1	0	0	1	-7

IST3004 provides 2-time SV(Contrast) offset OTP adjust function (CTA & CTB). The default setting of CTA & CTB are all 0's. If CTB is keeping at 0's, then the SV offset value will be decided by CTA, but if CTB has been setting to a non-zero value, then the SV offset will only be decided by CTB and the CTA settings will just be ignored.

Users can first use CTA command to try out the optimized contrast setting, if this setting is not yet satisfied, then user has the second chance to program CTB to reach the optimized contrast setting again.

The Contrast offset setting (CTA or CTB) will be added up to the original Contrast setting (SV), such that the final effective Contrast setting is SV + CTA or SV + CTB. If the total sum over 63 ,it will keep 63, and if the total sum under 0,then it will keep at 0

For example

SV	*CTA*	*CTB*	*Total sum*
32	*5*	*0*	*37*
32	*5 (Ignore)*	*3*	*35*
32	*-3 (1101)*	*0*	*29*
32	*-3(Ignore)*	*-5(1011)*	*27*
60	*5*	*0*	*63*
2	*-3 (1101)*	*0*	*0*

.

VF1 / VF4 level adjustment

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	VF1<2:0>		
0	0	0	0	0	1	0	VF4<2:0>		

VF1 Adjustment Table

VF1<2:0>			V1
1	1	0	+50mv
1	0	1	+25mv
0	0	0	+0mv(default)
0	0	1	-25mv
0	1	0	-50mv

VF4 Adjustment Table

VF4<2:0>			V4
1	1	0	+50mv
1	0	1	+25mv
0	0	0	+0mv(default)
0	0	1	-25mv
0	1	0	-50mv

The IST3004 provides additional V1 and V4 level adjustment parameters (VF1 and VF4) for user to fine tune the V1 and V4 output levels. It can be used to improve the display quality and reduce the cross-talk phenomenon.

OTP Write Flow

The suggested OTP write flow is listed as below : (Where the VPP Pin keeps Floating.)

OTP Write Flow

Step	A0	RW	Command	Description
0	--	--	(Initial)	■ Set Display ON, Power Configuration, Contrast (SV), … etc.
1	0	0	80h	■ Enter OTP command mode
2	0	0	00h	■ Set OTPADJ=0
3[A1]	0	0	CTA (or CTB)	■ OTP CTA adjust (50h~5Fh) if doing the 1st -time adjust ■ OTP CTB adjust (60h~6Fh) if doing the 2nd -time adjust
4[A1]	0	0	VF1	■ OTP VF1 adjust (08h~0Fh) if necessary
5[A1]	0	0	VF4	■ OTP VF4 adjust (10h~17h) if necessary
6	0	0	A0h	■ OTP Program enable
7	0	0	E3h	■ Use NOP command to release OTP command mode
8	0	0	AEh	■ Set Display OFF
9[A2]	0	0	21h	■ Set R-Gain = 3.5
10	0	0	81h	■ Enable setting SV (Contrast)
11[A2]	0	0	3Fh	■ Set SV = 3Fh
12	0	0	(waiting)	■ Wait 200ms for internal VPP to be stabilized
13	0	0	80h	■ Enter OTP command mode
14	0	0	F1h	■ OTP programming start
15	0	0	(Waiting)	■ OTP programming section, idle about 10ms to wait the OTP programming section finished
16	0	0	02h	■ Set OTPADJ=1
17	--	--	--	■ H/W reset
18	--	--	(Initial)	■ Set Display ON, Power Configuration, Contrast (SV), … etc.

Annotation -

A1: Step 3~5 maybe need some iterations to get the best display result.

A2: The R-Gain and Contrast here are the suggested values aims to get the proper OTP programming voltage. This programming voltage should be at least 6.6V which is sourced from the internal power, V0. Users shall follow the suggested R-Gain and Contrast to get the correct programming result.

OTP Read Flow

The OTP memory cells data can be read back through parallel interfaces. The suggested OTP read flow is listed as below : (Where the VPP Pin keeps Floating.)

OTP Read Flow

Step	A0	RW	Command	Description
1	0	0	80h	■ Enter OTP command mode
2	0	0	04h or 05h	■ Set OTP read address (OTPRA) ■ 04h(OTPRA=00h) → Select CTA & CTB ■ 05h(OTPRA=01h) → Select VF1 & VF4
3	0	1	OTP data read	■ When OTPRA=00h → DB<7:4> = CTA<3:0>, DB<3:0> = CTB<3:0> ■ When OTPRA=01h → DB<5:3> =VF1<2:0>, DB<2:0> =VF4<2:0> (DB<7:6> just ignored)
4	0	0	E3h	■ Use NOP command to release OTP command mode

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply voltage range	VDD/VDD2	-0.3 ~ 7	V
	V0,VOUT	-0.3 ~ 17	V
Supply voltage range	V1/V2/V3/V4	-0.3 ~ V0	V
Input voltage range	VIN	-0.3 to VDD + 0.3	V
Operating temperature range	TOPR	-40 to +85	
Storage temperature range (Bare chip)	TSTR	-55 to +125	

NOTES:

1. VDD and VLCD are based on VSS = 0V
2. The Voltage levels relation V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS must always be satisfied.
3. If supply voltage exceeds the absolute maximum range, this LSI may be damaged permanently.

DC CHARACTERISTICS

(VSS = 0V, Ta = -30 to 80)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Operating Voltage(1)		VDD		2.4	-	3.6	V	VDD *1
Operating Voltage(2)		VDD2		2.4	-	3.6	V	VDD2 *9
Operating Voltage(3)		V0		4.0	-	13.5	V	V0 *2
Input voltage	High	V_{IH}		0.8*VDD	-	VDD	V	*3
	Low	V_{IL}		VSS	-	0.2*VDD		
Output voltage	High	V_{OH}	I_{OH} = -0.5mA	0.8*VDD	-	VDD	V	*4
	Low	V_{OL}	I_{OL} = 0.5mA	VSS	-	0.2*VDD		
Input leakage current		I_{IL}	V_{IN} = VDD or VSS	-1.0	-	+1.0	μA	*5
Output leakage current		I_{OL}	V_{IN} = VDD or VSS	-3.0	-	+3.0	μA	*6
LCD driver ON Resistance		R_{ON}	Ta = 25 , V0 = 13V	-	2.0	3.0	kΩ	SEGn COMn *7
Oscillator frequency (internal)		F_{OSC}	Ta = 25 Duty = 1/65,33,17,9,1	17	20	24	kHz	
			Ta = 25 Duty = 1/55,53,49	25	30	35	kHz	
Oscillator frequency (External)		F_{CL}	Ta = 25 Duty = 1/65,33,17,9,1	17	20	24	kHz	CL
			Ta = 25 Duty = 1/55,53,49	25	30	35	kHz	
Voltage converter circuit		VOUT				13.5	V	VOUT
Reference voltage		VREF	Ta = 25 T.C = -0.05%/	2.06	2.1	2.14	V	
OTP programming voltage		VPP	No loading	6.5	6.62	6.75	V	VPP
		IPP				200uA /1bit	uA	

Dynamic Current Consumption

(Ta = -30~80)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Dynamic current consumption	I_{DYN}	VDD2=VDD= 3.0V X4 Boost V0 – VSS = 11.0V Display ON (HPMB=1, Checker pattern)	-	100	250	µA	*8 $I_{VDD+VDD2}$

Static Current Consumption

(Ta = -30~80)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Sleep mode current	I_{SLP}	Sleep mode, VDD=VDD2=3.0V	-	2	8	µA	$I_{VDD+VDD2}$
Standby mode current	I_{STB}	Standby mode, VDD=VDD2=3.0V	-	5	15	µA	$I_{VDD+VDD2}$

NOTE

*1. Although the wide range of DC operating voltages is guaranteed, but if the voltage fluctuation is too large during MPU accessing, the performance can't be guaranteed.

*2. In case of external power supply is applied.

*3. CS1B, CS2, A0, DB0~ DB7, E_RDB, RW_WRB, RESB, MS, C68, PS, IRS, CLS, CL, FR, DOF pins.

*4. DB0 ~ DB7, FR, FRS, DOF, CL pins.

*5. CS1B, CS2, A0, DB [7:0], E_RDB, RW_WRB, RESB, MS, C68, PS, IRS, CLS, CL, FR, DOF pins.

*6. Applies when the DB0 ~ DB7, FR, FRS, DOF, and CL pins are in high impedance.

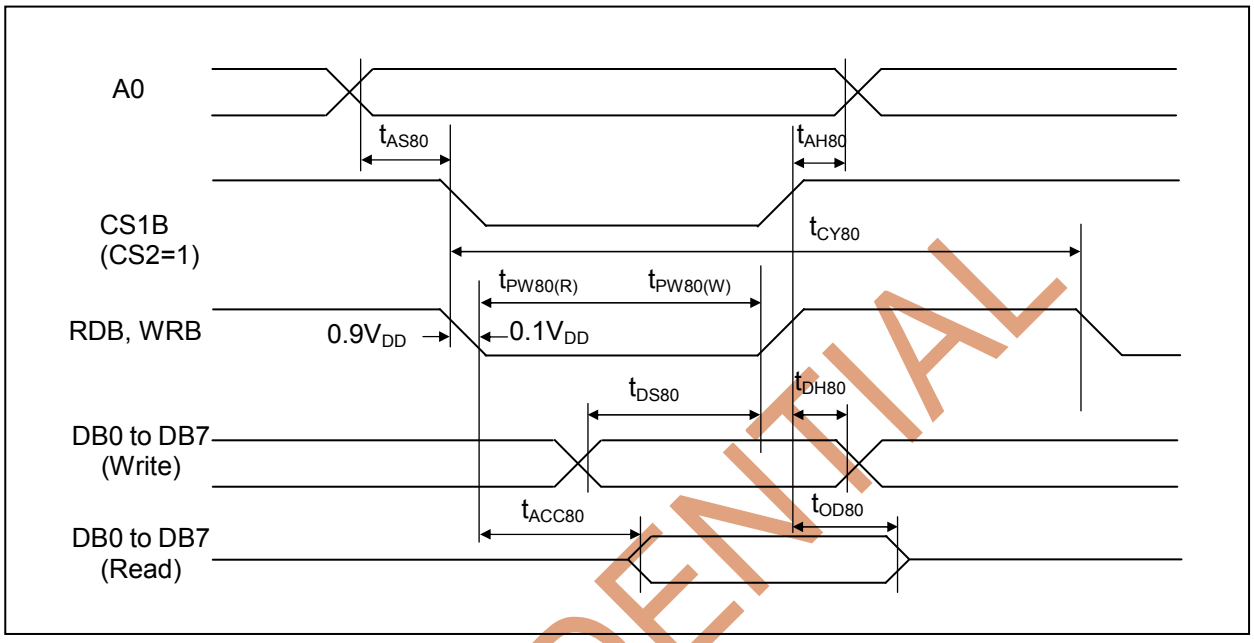
*7. Resistance value when 0.1mA is applied during the ON status of the output pin SEGn or COMn.
RON= ΔV / 0.1 [KΩ] (ΔV: voltage change when 0.1mA is applied in the ON status.)

*8. Applies to the case where the on-chip oscillation circuit is used and no access is made from the MPU & the LCD outputs (COMx, SEGx) are just floating, without any loading

*9. Because VDD2 is also the embedded Booster input voltage source, the boosted output (decided by the Booster ratio selection) can not over the VOUT's maximum limitation .

AC CHARACTERISTICS

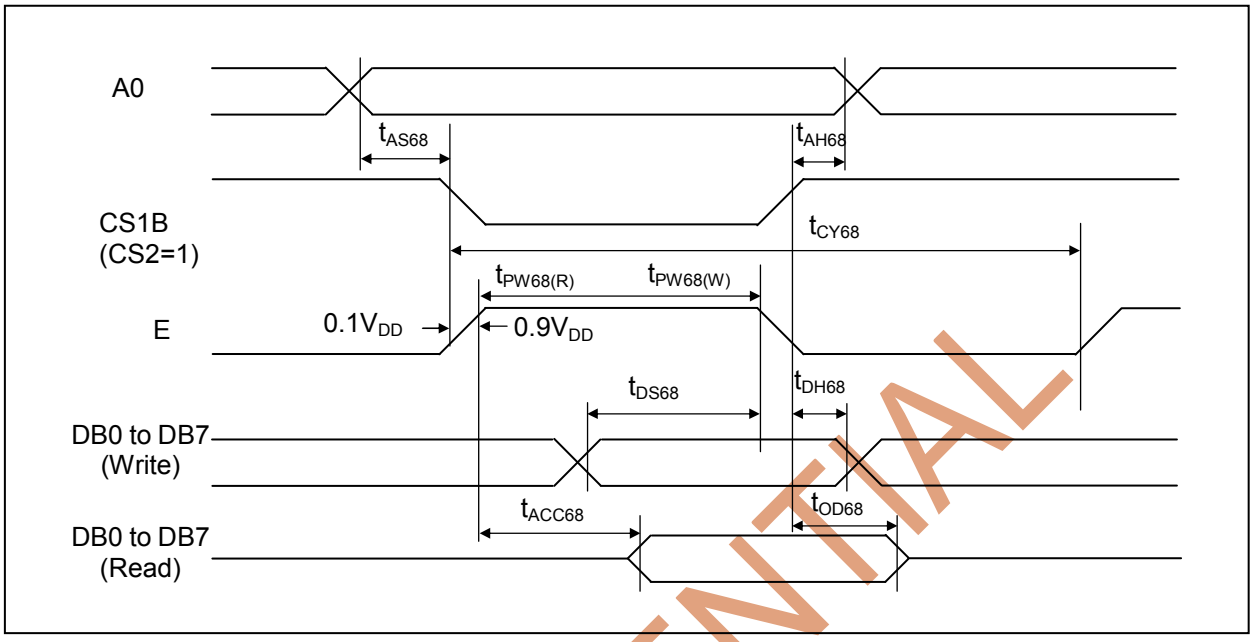
Read / Write Characteristics (8080-series MPU)



(VDD = 2.4 ~ 3.6V, Ta = -30~80)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	A0	tAS80 tAH80	0 0	-	-	ns	
System cycle time		tCY80	300	-	-	ns	
Pulse width (WRB)	RW_WRB	tPW80(W)	150	-	-	ns	
Pulse width (RDB)	E_RDB	tPW80(R)	150	-	-	ns	
Data setup time Data hold time	DB7 to DB0	tDS80 tDH80	60 0	-	-	ns	
Read access time Output disable time		tACC80 tOD80	140 -	-	- 10	ns	(No load)

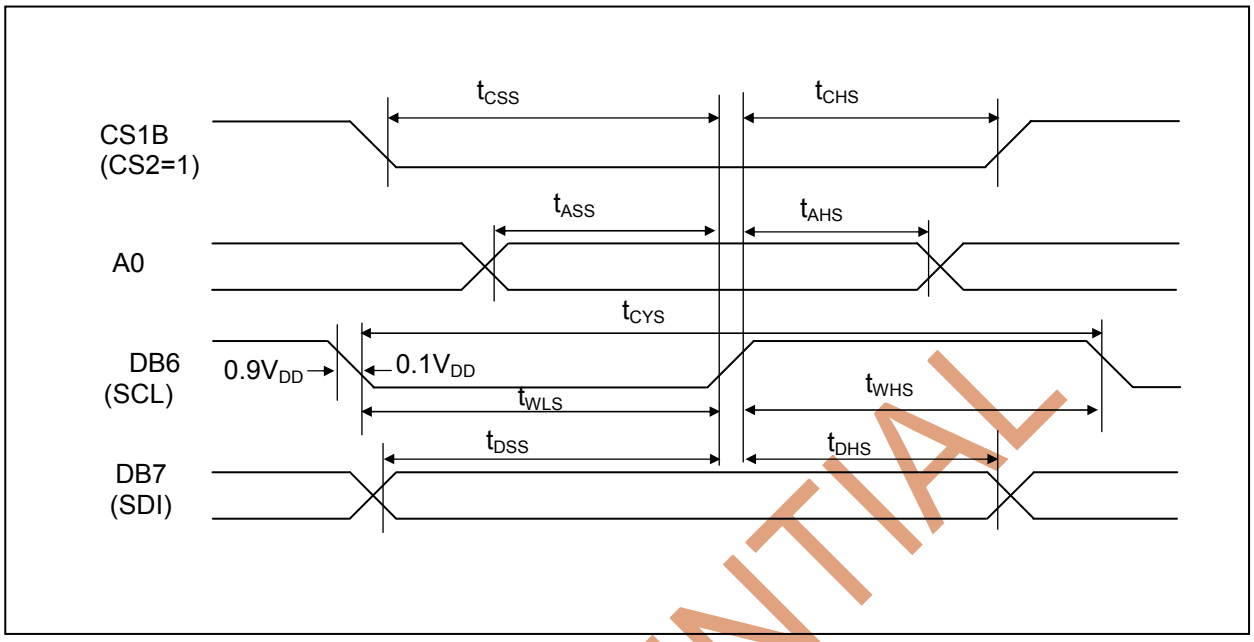
Read / Write Characteristics (6800-series Microprocessor)



(VDD = 2.4 ~ 3.6V, Ta = -30~80)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	A0	tAS68 tAH68	0 0	-	-	ns	
System cycle time		tCY68	300	-	-	ns	
Pulse width (E)	RW_WRB	tPW68(W)	150	-	-	ns	
Pulse width (E)	E_RDB	tPW68(R)	150	-	-	ns	
Data setup time Data hold time	DB7 to DB0	tDS68 tDH68	60 0	-	-	ns	
Read access time Output disable time		tACC68 tOD68	140 -	-	- 10	ns	(No load)

Serial Interface Characteristics



(VDD = 2.4 ~ 3.6V, Ta = -30~80)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle SCL high pulse width SCL low pulse width	DB6 (SCL)	tCYS tWHS tWLS	200 90 90	- - -	- - -	ns	
Address setup time Address hold time	A0	tASS tAHS	45 45	- -	- -	ns	
Data setup time Data hold time	DB7 (SDI)	tDSS tDHS	45 45	- -	- -	ns	
CS1B setup time CS1B hold time	CS1B	tCSS tCHS	90 90	- -	- -	ns	

Reset Input Timing

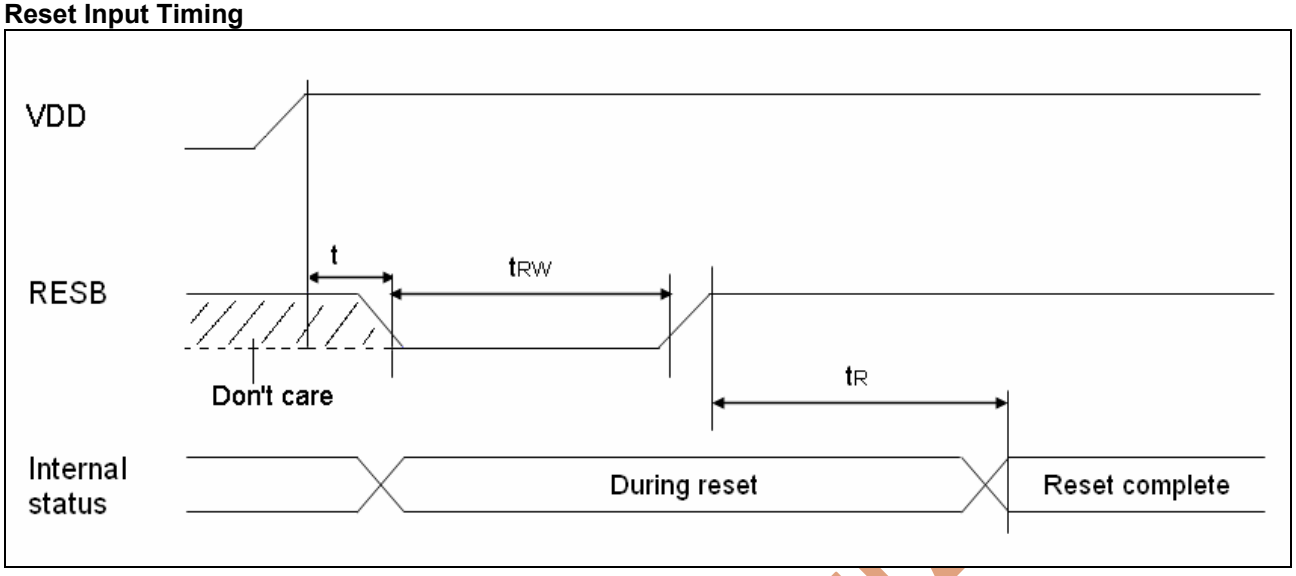


Figure 32. Reset Input Timing

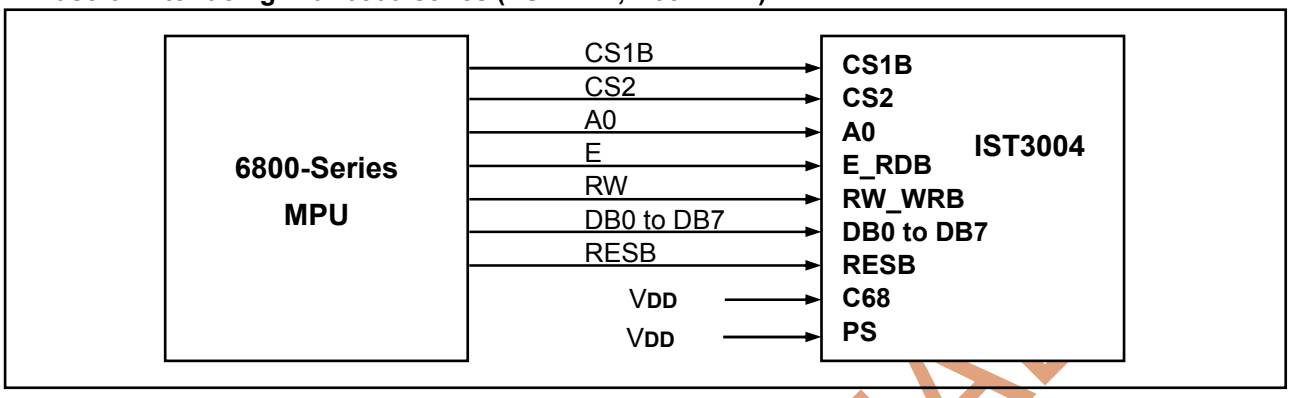
(V_{DD} = 2.4V ~ 3.6V, Ta = -30~80)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Reset low pulse width	RESB	t_{RW}	2	-	-	us	
Reset time	-	t_R	-	-	2	us	
Reset time	RESB	t	0	-	-	us	

REFERENCE APPLICATIONS

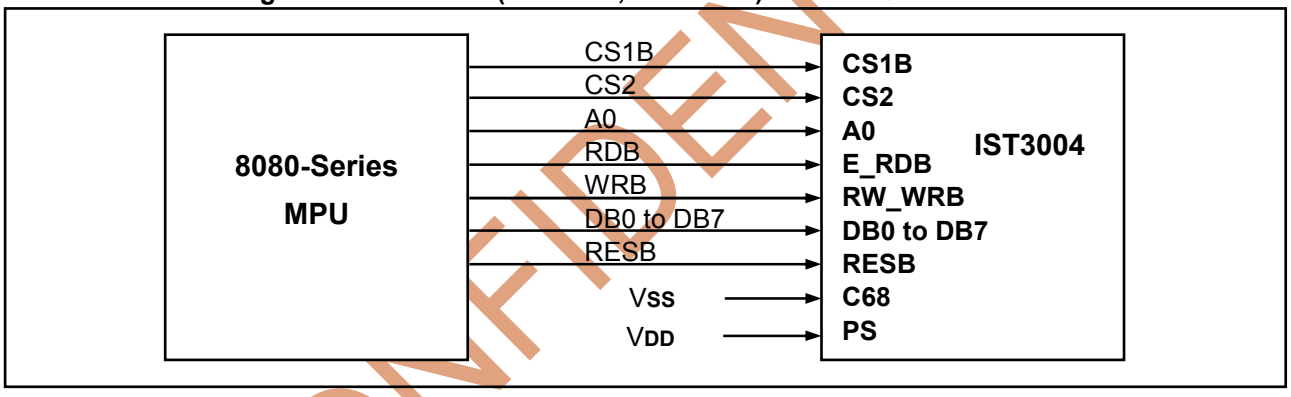
MPU Interface

In Case of Interfacing with 6800-series (PS = "H", C68 = "H")



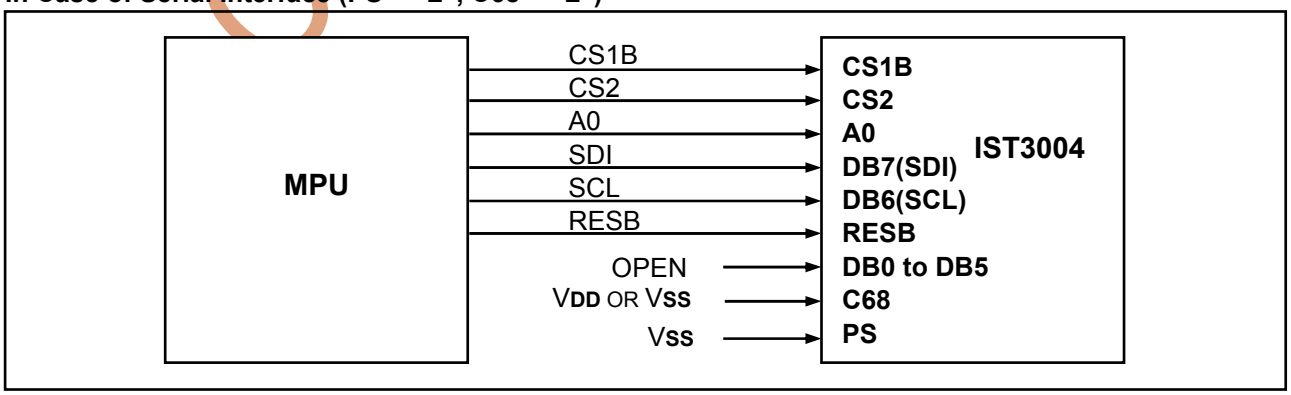
Interfacing with 6800-series (PS = "H", C68 = "H")

In Case of Interfacing with 8080-series (PS = "H", C68 = "L")



Interfacing with 8080-series (PS = "H", C68 = "L")

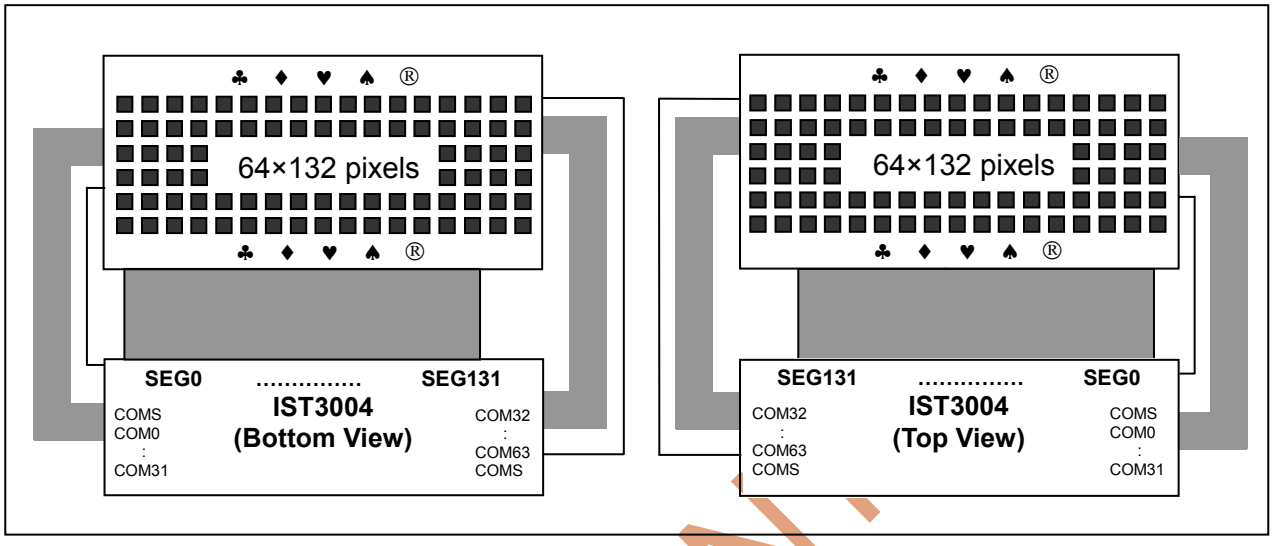
In Case of Serial Interface (PS = "L", C68 = "L")



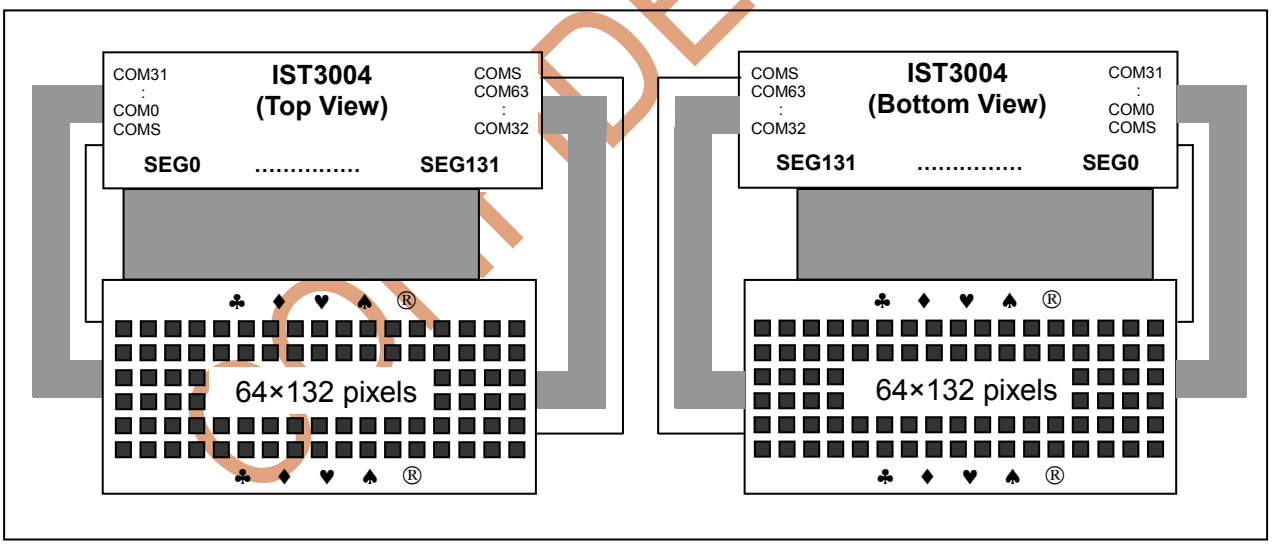
Serial Interface (PS = "L", C68 = "L")

Connections between IST3004 and LCD Panel

Single Chip Structure (1/65 Duty Configurations)

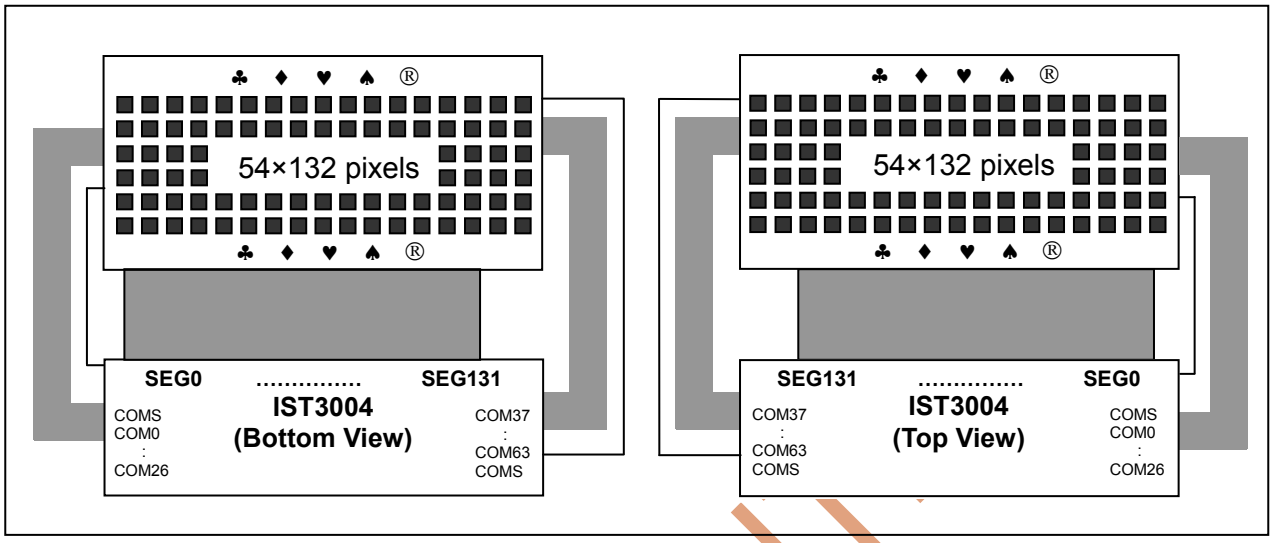


SHL = 1, ADC = 0 **SHL = 1, ADC = 1**

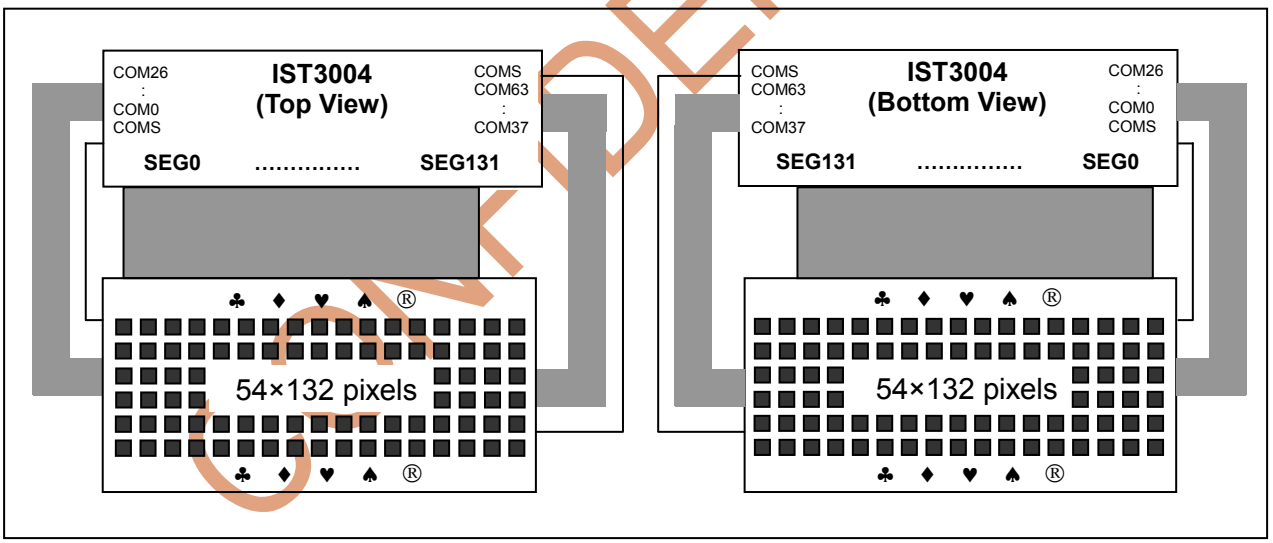


SHL = 0, ADC = 0 **SHL = 0, ADC = 1**

Single Chip Structure (1/55 Duty Configurations)

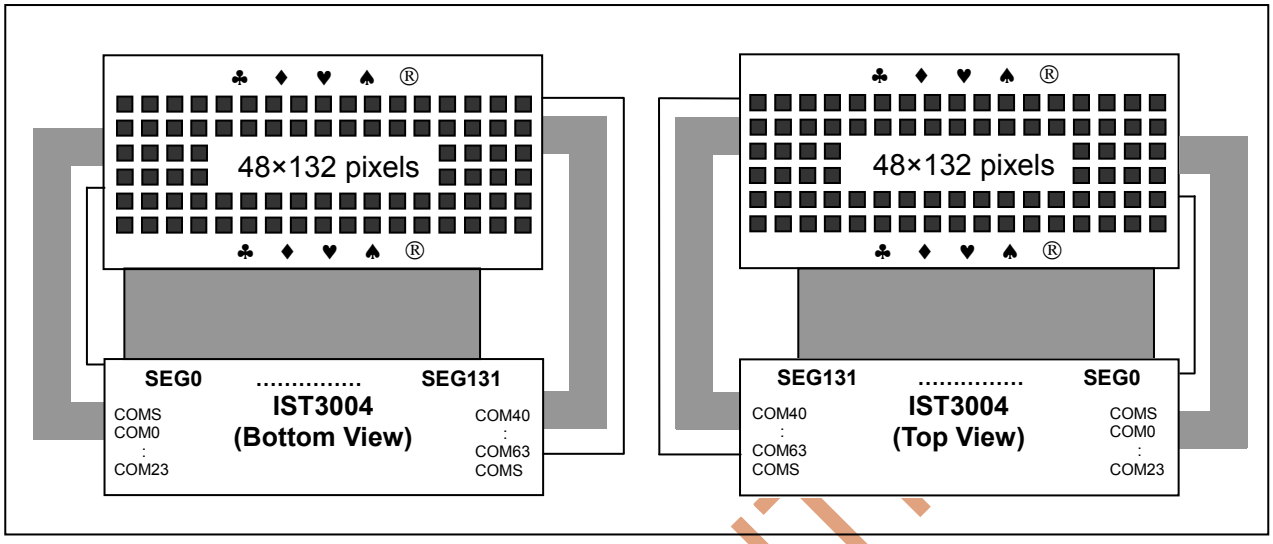


SHL = 1, ADC = 0 **SHL = 1, ADC = 1**

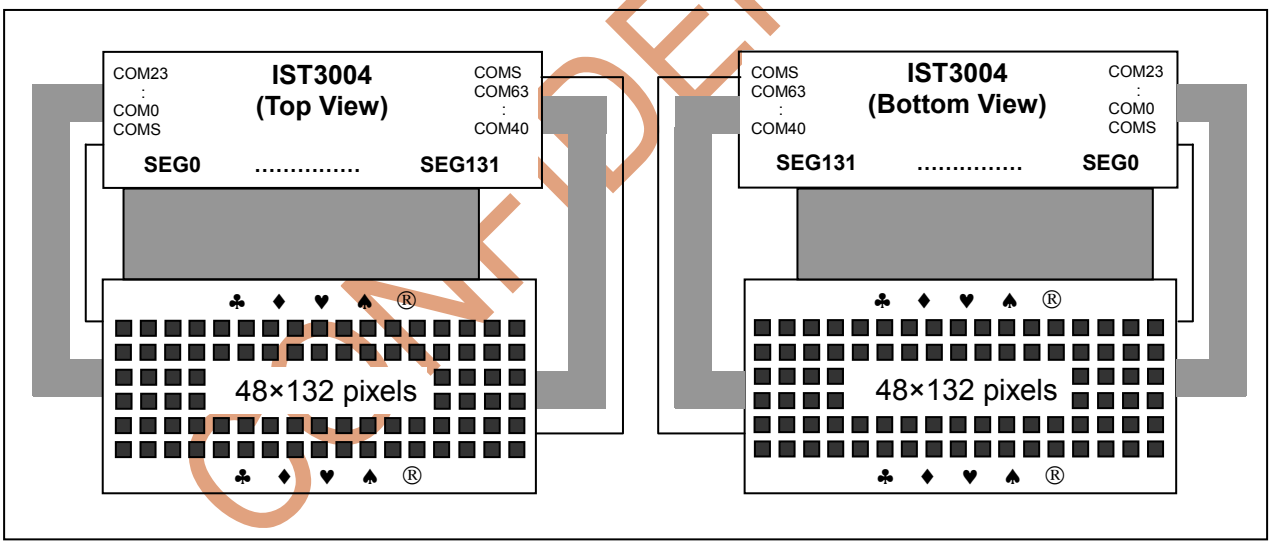


SHL = 0, ADC = 0 **SHL = 0, ADC = 1**

Single Chip Structure (1/49 Duty Configurations)

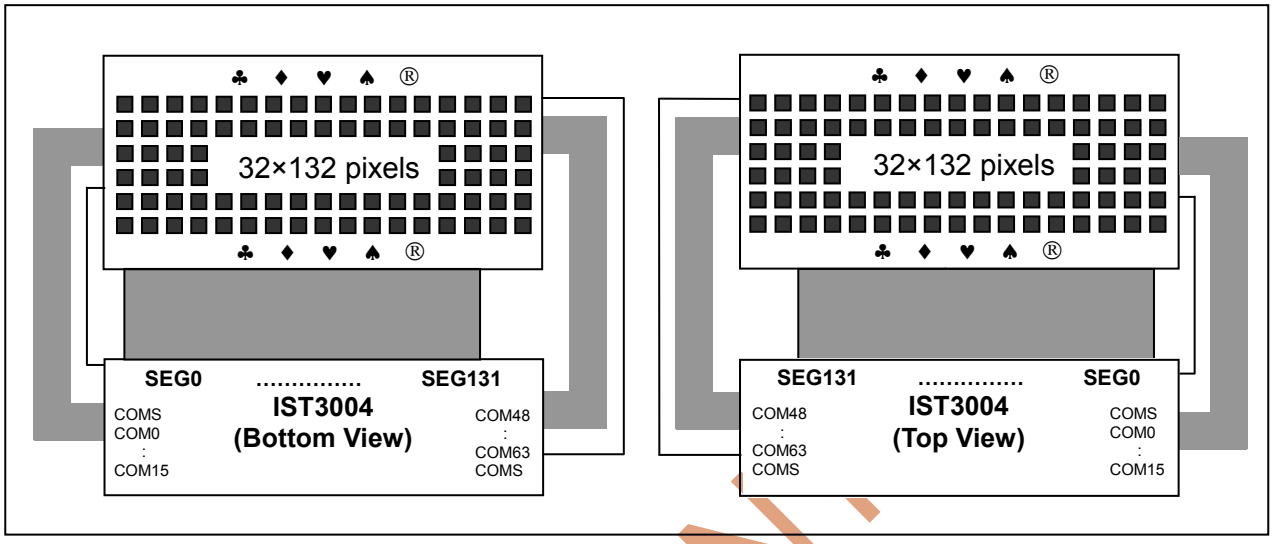


SHL = 1, ADC = 0 **SHL = 1, ADC = 1**

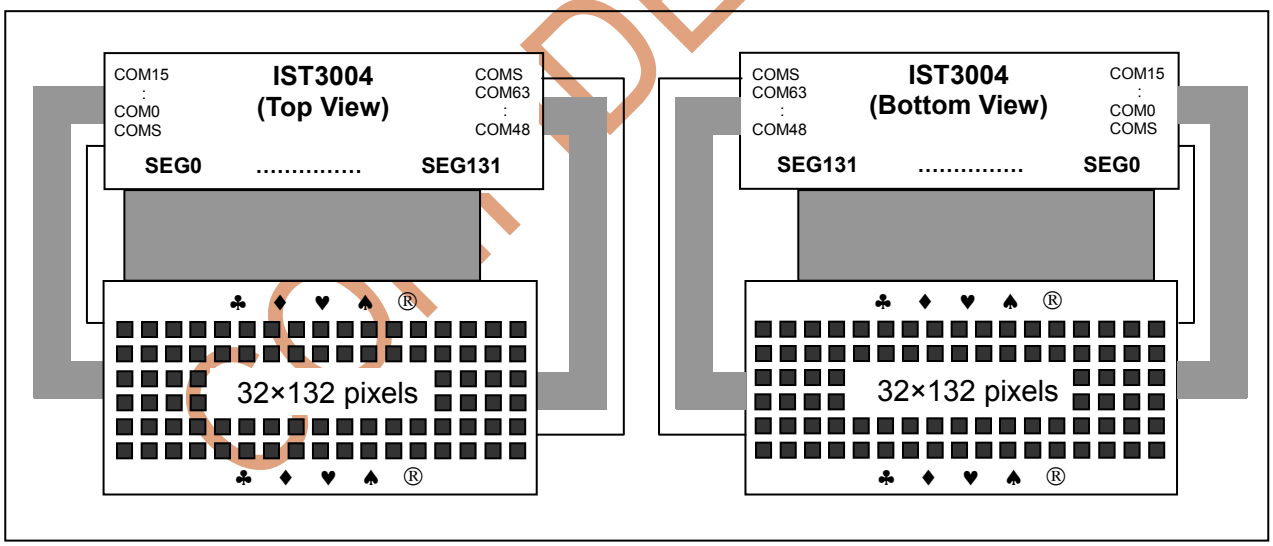


SHL = 0, ADC = 0 **SHL = 0, ADC = 1**

Single Chip Structure (1/33 Duty Configurations)

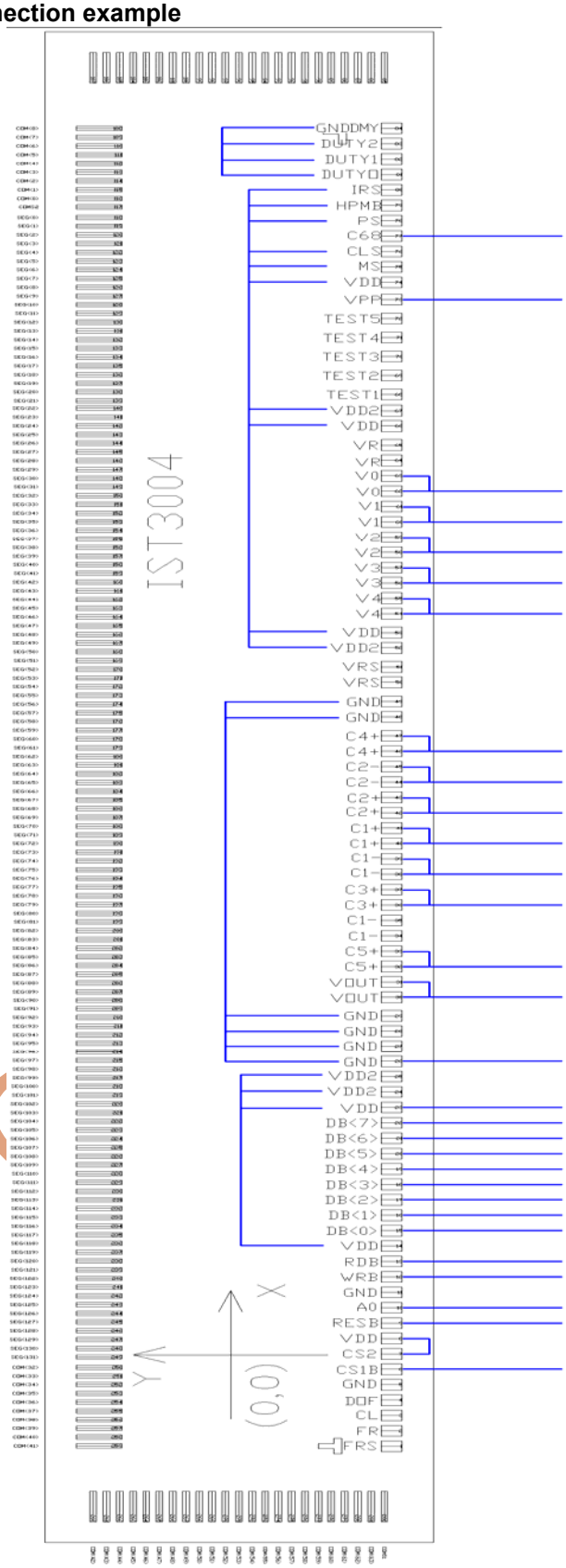


SHL = 1, ADC = 0 **SHL = 1, ADC = 1**

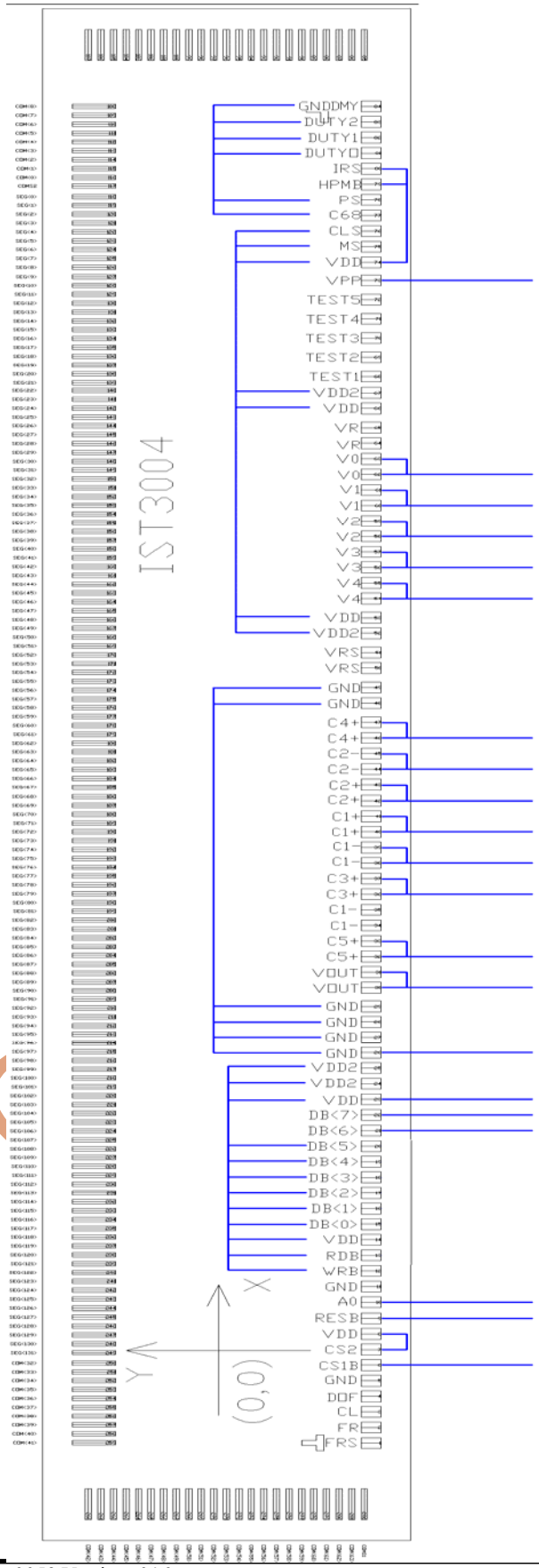


SHL = 0, ADC = 0 **SHL = 0, ADC = 1**

IST3004 ITO connection example



IST3004 parallel interface



IST3004 serial interface