EPL09060

9 COM / 60 SEG
LCD Driver

Product Specification

DOC. VERSION 1.0

ELAN MICROELECTRONICS CORP.

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Contents

Specification Revision History

Doc. Version	Revision Description	Date
0.1	Initial version	2004/02/20
0.2	Deleted the background confidential mark.	2004/03/04
0.3	Modified the VREF20 Range at the DC characteristics table.	2005/03/28
1.0	Removed the background Preliminary mark.	2005/12/28

1 General Description

The EPL09060 is a driver and controller LSI for graphic dot-matrix liquid crystal display systems. It can be interfaced to the MPU via serial or 8-bit interface. It contains 9 common and 60 segment driver circuits. A single chip can drive a graphic display system with a maximum of 60 × 9 dots.

2 Features

- Direct Correspondence between Display Data RAM and LCD Pixel
- Display Data RAM : 43 × 102 = 4386 bits
- 69 LCD Drivers : 60-seg segment drivers, 8-common drivers and 1-icon
- Serial Interface (SPI) or 8-Bit Parallel Interface Mode (80-/68-series MPU)
- On-chip oscillator circuit
- Programmable Duty Ratio:

Duty Ratio	Common	Segment
1: 8 (+ ICON)	8 (+ ICON)	60
1:16 (+ICON)	16 (+ICON)	60

Note: ICON = "0" : Pin disable
ICON = "1" : Pin enable

- Selectable LCD driving bias level :
  1/3,1/3.5,1/4,1/4.5,1/5,1/5.5,1/6,1/6.5,1/7,1/7.5,1/8 bias
- Selectable LCD display clock frequency
- Electronic contrast control function (64 steps)
- Built-in useful Instruction Set : Display data read/write, Display on/off, Inverse display, Page address set, Common address set, LCD display contrast control, Set Sleep mode, Standby mode, etc.
- Operating Voltage range :
  – Supply voltage : 2.2V to 3.4 V
  – LCD driving voltage : 3.0V to 6 V
- Package (Ordering information):

Part Number	Package	Description	Package Information
EPL09060H	Bare die	NA	Page 6

Note: The EPL09060 series has the following sub-codes, depending on their shapes.
H: Bare die (Aluminum pad without bump); **GH**: Gold bumped die
F: COF package; **T**: TAB (TCP) package

Example:
EPL09060H → EPL09060 Elan; H: Bare die

3 Applications

Organizer	Electronic Dictionary
Scientific calculator	Cellular phone
Graphic pager	Handy Terminals (PDA)

4 Pin Configuration (Package)

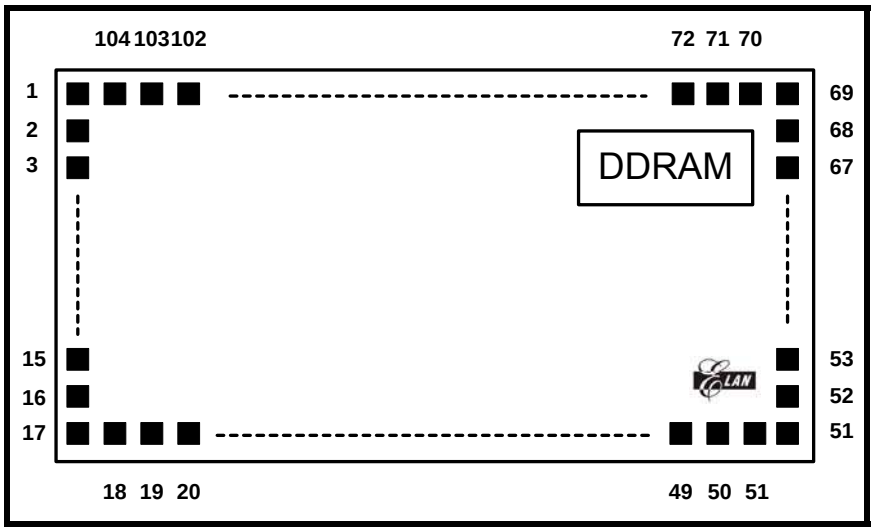


Figure 1 Pin Configuration

NOTE

With the Elan logo at the right bottom corner (as shown in the figure) and DDRAM (black color) at the right side, Pin 1 is at the upper left corner.

Pad Configuration

Item	Pad No.	Size		Unit
		X	Y	
Chip size	–	4040	2070	μm
Pad size (Type A)	1, 17~21, 30~52, 69~104	85	90	
Pad size (Type B)	2, 14~15, 22~29	90	90	
Pad size (Type C)	4~13, 16, 53~68	90	85	
Pad pitch	Type A	105		
	Type B	110		

Pad Coordinates Table

Pad No.	Symbol	X	Y
1	COMI1	-3852.5	-75.3
2	VDD	-3860.0	-229.15
3	VDD	-3860.0	-353.9
4	C1+	-3868.1	-473.1
5	C1-	-3868.1	-578.1
6	C2+	-3868.1	-683.1
7	VOUT	-3868.1	-788.1
8	V0	-3868.1	-893.1
9	V1	-3868.1	-998.1
10	V2	-3868.1	-1103.1
11	V3	-3868.1	-1208.1
12	V4	-3868.1	-1313.1
13	VR	-3868.1	-1418.1
14	GND	-3860.0	-1541.3
15	GND	-3860.0	-1651.3
16	PS	-3868.1	-1774.2
17	C86	-3870.7	-1898.1
18	CLS	-3765.7	-1898.1
19	OSC	-3660.7	-1898.1
20	IRS	-3555.7	-1898.1
21	/RES	-3450.7	-1898.1
22	D7	-3318.2	-1890.0
23	D6	-3208.2	-1890.0
24	D5	-3098.2	-1890.0
25	D4	-2988.2	-1890.0
26	D3	-2878.2	-1890.0
27	D2	-2768.2	-1890.0
28	D1	-2658.2	-1890.0
29	D0	-2548.2	-1890.0
30	CS2	-2403.5	-1898.1
31	/CS1	-2298.5	-1898.1
32	A0	-2193.5	-1898.1
33	/WR	-2088.5	-1898.1
34	/RD	-1983.5	-1898.1
35	TEST	-1878.5	-1898.1
36	COM7	-1752.5	-1898.1
37	COM6	-1647.5	-1898.1
38	COM5	-1542.5	-1898.1
39	COM4	-1437.5	-1898.1
40	COM3	-1332.5	-1898.1
41	COM2	-1227.5	-1898.1
42	COM1	-1122.5	-1898.1
43	COM0	-1017.5	-1898.1
44	COMI2	-912.5	-1898.1
45	SEG59	-807.5	-1898.1
46	SEG58	-702.5	-1898.1
47	SEG57	-597.5	-1898.1
48	SEG56	-492.5	-1898.1
49	SEG55	-387.5	-1898.1
50	SEG54	-282.5	-1898.1
51	SEG53	-177.5	-1898.1
52	SEG52	-72.5	-1898.1

Pad No.	Symbol	X	Y
53	SEG51	-75.1	-1774.2
54	SEG50	-75.1	-1669.2
55	SEG49	-75.1	-1564.2
56	SEG48	-75.1	-1459.2
57	SEG47	-75.1	-1354.2
58	SEG46	-75.1	-1249.2
59	SEG45	-75.1	-1144.2
60	SEG44	-75.1	-1039.2
61	SEG43	-75.1	-934.2
62	SEG42	-75.1	-829.2
63	SEG41	-75.1	-724.2
64	SEG40	-75.1	-619.2
65	SEG39	-75.1	-514.2
66	SEG38	-75.1	-409.2
67	SEG37	-75.1	-304.2
68	SEG36	-75.1	-199.2
69	SEG35	-72.5	-75.3
70	SEG34	-177.5	-75.3
71	SEG33	-282.5	-75.3
72	SEG32	-387.5	-75.3
73	SEG31	-492.5	-75.3
74	SEG30	-597.5	-75.3
75	SEG29	-702.5	-75.3
76	SEG28	-807.5	-75.3
77	SEG27	-912.5	-75.3
78	SEG26	-1017.5	-75.3
79	SEG25	-1122.5	-75.3
80	SEG24	-1227.5	-75.3
81	SEG23	-1332.5	-75.3
82	SEG22	-1437.5	-75.3
83	SEG21	-1542.5	-75.3
84	SEG20	-1647.5	-75.3
85	SEG19	-1752.5	-75.3
86	SEG18	-1857.5	-75.3
87	SEG17	-1962.5	-75.3
88	SEG16	-2067.5	-75.3
89	SEG15	-2172.5	-75.3
90	SEG14	-2277.5	-75.3
91	SEG13	-2382.5	-75.3
92	SEG12	-2487.5	-75.3
93	SEG11	-2592.5	-75.3
94	SEG10	-2697.5	-75.3
95	SEG9	-2802.5	-75.3
96	SEG8	-2907.5	-75.3
97	SEG7	-3012.5	-75.3
98	SEG6	-3117.5	-75.3
99	SEG5	-3222.5	-75.3
100	SEG4	-3327.5	-75.3
101	SEG3	-3432.5	-75.3
102	SEG2	-3537.5	-75.3
103	SEG1	-3642.5	-75.3
104	SEG0	-3747.5	-75.3

Note: For PCB layout, the IC substrate must be connected to VSS or floating.

5 Functional Block Diagram

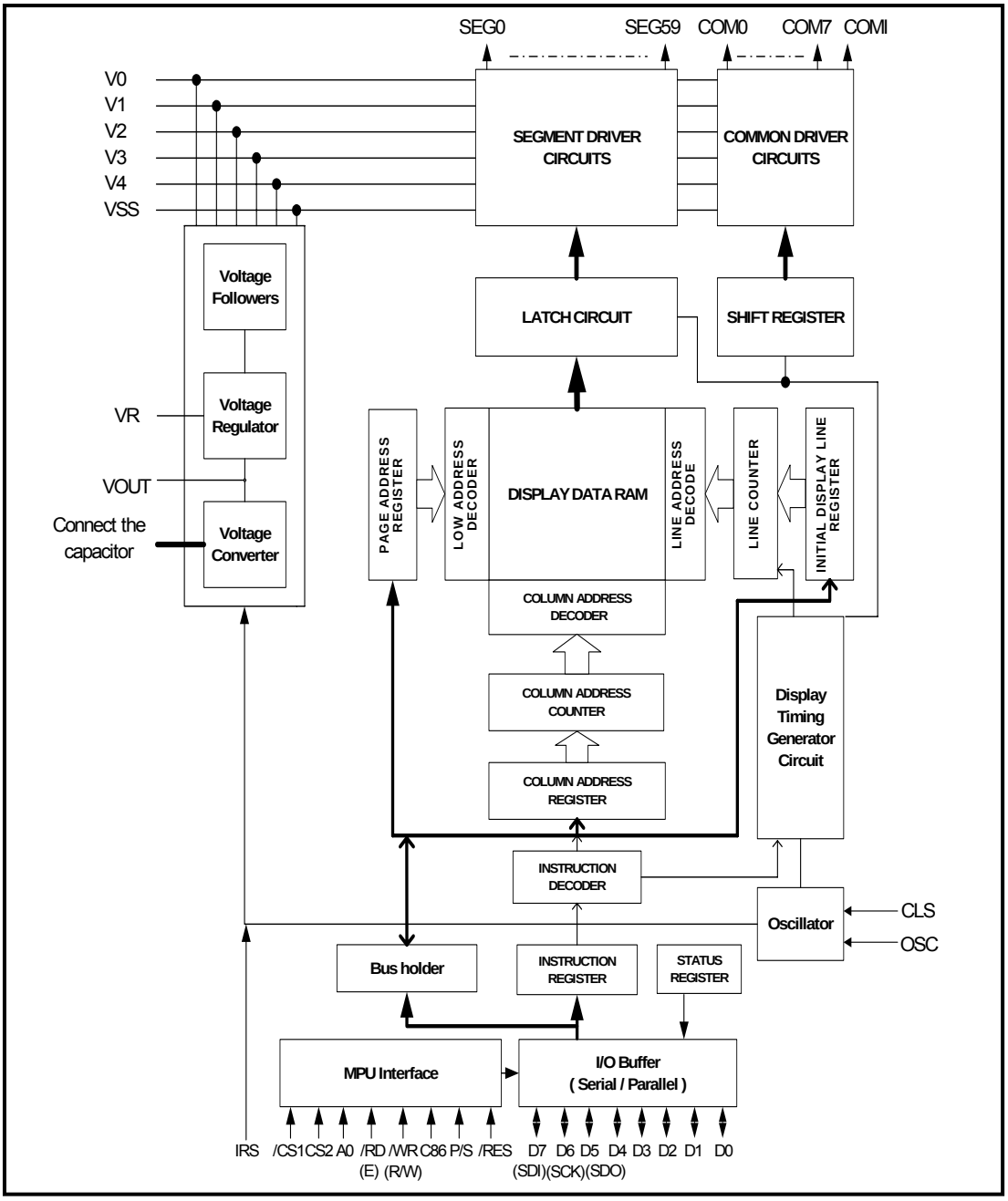


Figure 2 System Block Diagram

6 Pin Description

Power Supply

Name	I/O	Description
VDD	Power	VDD Power Supply
VSS	Power	0V (GND)
V_0 V_1 V_2 V_3 V_4	Power	LCD driver supply voltages. The voltage applied is determined by the LCD pixel and is changed through changing the impedance using an operational amplifier (OPA) for various applications. Voltage levels are determined based on V_0, and must maintain the relative magnitudes shown below: $V_0 \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_{SS}$ When the internal power circuit is active, these voltages are generated according to the state of LCD bias, The selection of voltages is determined by the "LCD bias select" instruction, as shown in the table below.

LCD Bias	V_1	V_2	V_3	V_4
1/8 Bias	$7/8 \times V_0$	$6/8 \times V_0$	$2/8 \times V_0$	$1/8 \times V_0$
1/7.5 Bias	$6.5/7.5 \times V_0$	$5.5/7.5 \times V_0$	$2/7.5 \times V_0$	$1/7.5 \times V_0$
1/7 Bias	$6/7 \times V_0$	$5/7 \times V_0$	$2/7 \times V_0$	$1/7 \times V_0$
1/6.5 Bias	$5.5/6.5 \times V_0$	$4.5/6.5 \times V_0$	$2/6.5 \times V_0$	$1/6.5 \times V_0$
1/6 Bias	$5/6 \times V_0$	$4/6 \times V_0$	$2/6 \times V_0$	$1/6 \times V_0$
1/5.5 Bias	$4.5/5.5 \times V_0$	$3.5/5.5 \times V_0$	$2/5.5 \times V_0$	$1/5.5 \times V_0$
1/5 Bias	$4/5 \times V_0$	$3/5 \times V_0$	$2/5 \times V_0$	$1/5 \times V_0$
1/4.5 Bias	$3.5/4.5 \times V_0$	$2.5/4.5 \times V_0$	$2/4.5 \times V_0$	$1/4.5 \times V_0$
1/4 Bias	$3/4 \times V_0$	$2/4 \times V_0$	$2/4 \times V_0$	$1/4 \times V_0$
1/3.5 Bias	$2.5/3.5 \times V_0$	$1.5/3.5 \times V_0$	$2/3.5 \times V_0$	$1/3.5 \times V_0$
1/3 Bias	$2/3 \times V_0$	$1/3 \times V_0$	$2/3 \times V_0$	$1/3 \times V_0$

LCD Driver Supply

Name	I/O	Description
C1+ C1-	O	Boosted capacitor connecting terminals used for voltage booster.
C2+	O	Boosted capacitor connecting terminals used for voltage booster.
VOUT	I/O	Voltage converter output
VR	I	V_0 voltage adjustment pin

System Control

Name	I/O	Description
P/S	I	Select theInterface mode with the MPU. When PS = "High": Parallel interface mode When PS = "Low": Serial interface mode
C86	I	Select the kinds of the MPU to interface. When C86 = "High": 68-series MPU interface mode When C86 = "Low": 80-series MPU interface
CLS	I	Internal oscillator circuit enable / disable select pin. CLS = “H”: Enable the Internal oscillator circuit CLS = “L”: Disable the Internal oscillator circuit (External display clock input to the OSC pin)
OSC	I	When using an external oscillator, input the clock to the OSC pin. When using an internal oscillator, leave this pin open.
IRS	I	Internal resistor select pin. This pin selects the resistors for adjusting the V_0 voltage level and is available only in master mode. - IRS = "H": Internal resistors are used. - IRS = "L": External resistors are used. V_0 voltage is controlled using the external divider resistor connecting the VR pin.
TEST	I	Test pin. Must be fixed at VSS.

MPU Interface

Name	I/O	Description
/RES	I	Hardware reset input The LSI is reset when this signal is pulled low (Active low)
/CS1, CS2	I	Chip select signals. The Chip Select of the LSI becomes active when CS1 is "L" and CS2 is "H", which allows input/output of data or commands.

/CS1	CS2	Status
“L”	“L”	The device is not active (D7~D0 is Hi-Z)
“L”	“H”	Data and instruction are available.
“H”	“L”	The device is not active (D7~D0 is Hi-Z)
“H”	“H”	The device is not active (D7~D0 is Hi-Z)

A0	I	Used as register selection input When A0 = "High", Data register When A0 = "Low", Instruction register
/WR (R/W)	I	When C86 = "High"(68-series MPU interface), used as read (/WR = "High"), write (/WR = "Low") When C86 = "Low " (80-series MPU interface), used as write enable input (/WR)
/RD (E)	I	When C86 = "High"(68-series MPU interface), used as read/write enable input (E). When C86 = "Low "(80-series MPU interface), used as read enable input (/RD)
D0 to D7	I/O	When in serial mode, D6 (SCK) is used as serial clock input pin, D7 (SDI) is used as serial data input pin, D5 (SDO) is used as serial data output pin and the others are not used. When in parallel mode, D0 to D7 are used as bidirectional data bus pin.

LCD Driver Output

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>COM0 to COM7</td><td>O</td><td>LCD common output pins
<table>
<tr><th>Scan Data</th><th>FR</th><th>COMs Output Voltage</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>Vss</td></tr>
<tr><td>L</td><td>V0</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V1</td></tr>
<tr><td>L</td><td>V4</td></tr>
<tr><td colspan="2">Power Save Mode</td><td>Vss</td></tr>
</table></td></tr>
<tr><td>COMI</td><td>O</td><td>There are two icon display pins. Both pins output the same signal. Leave these pins open when they are not used.</td></tr>
<tr><td>SEG0 to SEG59</td><td>O</td><td>LCD segment output pins
<table>
<tr><th rowspan="2">Display Data</th><th rowspan="2">FR</th><th colspan="2">SEGs Output Voltage</th></tr>
<tr><th>Normal Display</th><th>Reverse Display</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>V0</td><td>V2</td></tr>
<tr><td>L</td><td>Vss</td><td>V3</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V2</td><td>V0</td></tr>
<tr><td>L</td><td>V3</td><td>Vss</td></tr>
<tr><td colspan="2">Power Save Mode</td><td colspan="2">Vss</td></tr>
</table></td></tr>
</table>

7 Functional Description

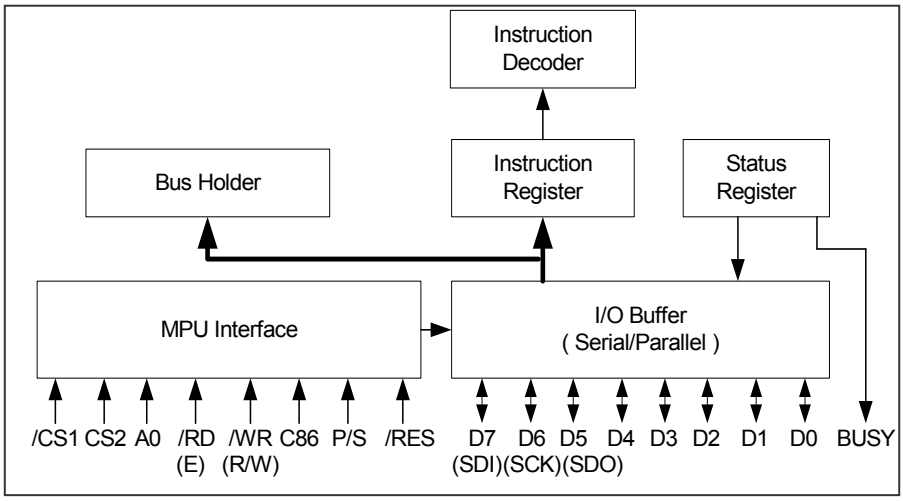


Figure 3 System Interface

7.1 MPU Interface

7.1.1 Chip Select

The EPL09060 has two chip select pins /CS1 and CS2. When /CS1="L" and CS2="H", MPU interface is available. When the chip select pin is inactive (other /CS1 and CS2 condition), D7 to D0 are high impedance (invalid) and input of A0, /RD, or /WR inputs are not effective. If serial interface is selected, the shift register and the counter are both reset. However, reset is always operated in any conditions of /CS1 and CS2.

P/S	C86	A0	WR	/RD	D0~D4	D5	D6	D7
Serial Mode (L)	SPI interface (–)	A0	R/W	–	*	SDO	SCK	SDI
Parallel Mode (H)	80-series (L)	A0	/WR	/RD	D0~D7			
	68-series (H)	A0	R/W	E	D0~D7			

Note: " * " Don't care ("High", "Low" or "Open")

"–" Indicates that it is fixed to either "High" (VDD) or "Low" (VSS)

7.1.2 Selecting the Interface Type

The EPL09060 can be operated with serial interface (SPI) and parallel interface (80-series or 68-series) as selected by P/S pin.

Serial Interface (SPI)

When serial mode (PS = "L"), D6 (SCK) is used as serial clock input pin, D7 (SDI) is used as serial data input pin, D5 (SDO) is used as serial data output pin. When the LSI is active (/CS1="L", CS2="H"), serial data input (D7), serial clock input (D6) inputs and serial data output (D5) are enabled. The 8-bit shift register and 3-bit counter are reset to the initial condition when the chip is not selected. The data input/output from SDI/SDO terminal is MSB first as in the order of D7, D6…D0, and is latched at the rising edge of the serial clock SCK. Serial input data is display data when A0="H" and instruction when A0="L". The A0 input is read in and identified at the rising edge of the (8 x n) serial clock pulse. Since the clock signal (D6) is easy to be affected by the external noise caused by the line length, the operation check on the actual machine is recommended.

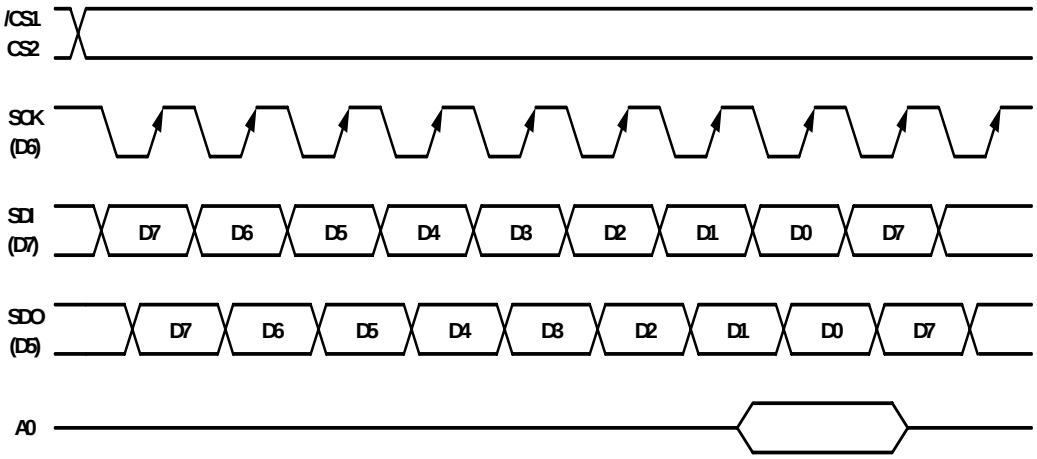
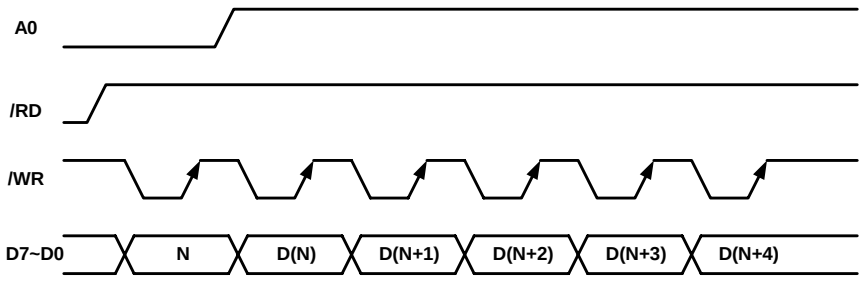


Figure 4 Serial Interface Signal Chart

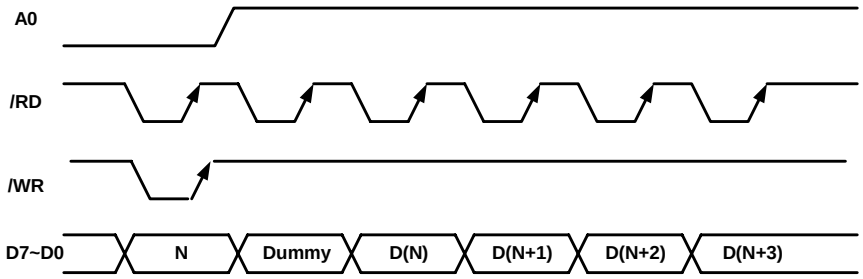
A0	/WR (R/W)	D7 (SDI)	D5 (SDO)
0	0	Instruction Write	Status Read
0	1	Invalid	Status Read
1	0	Display Data Write	Status Read
1	1	Invalid	Display Data Read

Parallel Interface (8-bit Length)

Parallel mode (8-bit length): When parallel input is selected (PS = ”H”), D0~D7 can be connected directly to the 80-series or 68-series MPU by setting the C86 pin to high or low.



Write Timing Diagram



Read Timing Diagram

Figure 5 Write and Read Timing Diagrams

Common	80-Series		68-Series	Description
A0	/RD	/WR	R/W	
H	L	H	H	Display data read
H	H	L	L	Display data write
L	L	H	H	Register status read
L	H	L	L	Writes to Instruction register

7.2 Data Transfer

The EPL09060 uses a bus holder and an internal data bus for data transfer with the MPU. When writing data from the MPU to the DDRAM, data is automatically transferred from the bus holder to the DDRAM. When reading data from the DDRAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from the bus holder for the next data read cycle.

7.2.1 Display Data RAM (DDRAM)

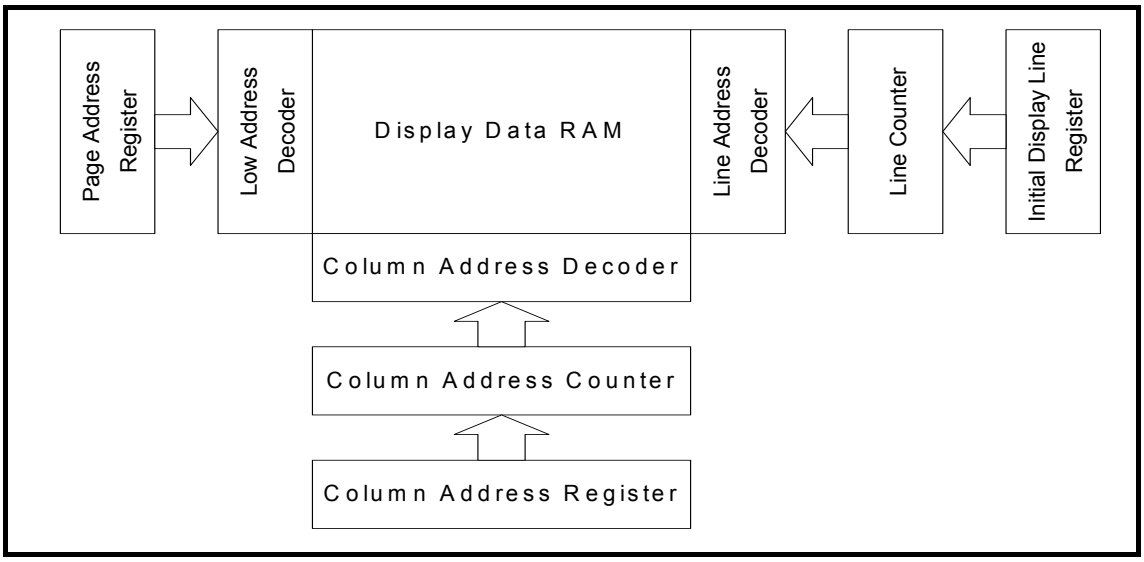


Figure 6 Display Data RAM Diagram

The display data RAM (DDRAM) stores pixel data for the LCD. It is a 43-row × 102-column addressable array. It is possible to access any required bit by specifying the page address and the column address. The 43 rows are divided into five pages of eight lines, one page with two lines (D0, D1) and the seventh page with a single line (D0 only).

Each bit in the Display Data RAM corresponds to each pixel of the LCD panel. Each bit in the Display Data RAM corresponds to each pixel of the LCD panel and controls the display by applying the following bit data.

When in Normal Display : On="1" , Off="0"

When in Inverse Display : On="0" , Off="1"

(Refer to “Inverse Display On/Off” instruction for more details.)

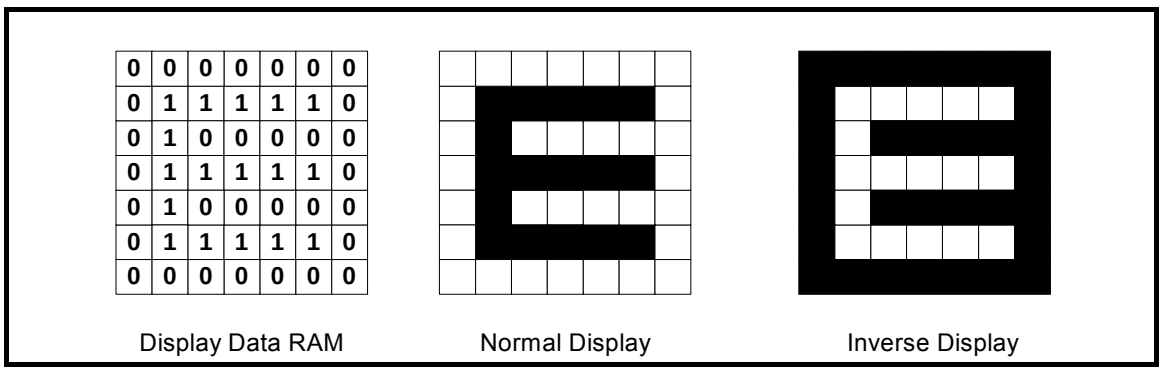


Figure 7 Display Data RAM, Normal and Inverse Liquid Crystal Display Diagrams

7.2.2 Programmable Duty Ratio

The duty ratio is selected by using the “Set Duty Ratio” instruction.

The common output circuits are shown in the following figure. They are separated into three shift registers and controlled by the "duty ratio register".

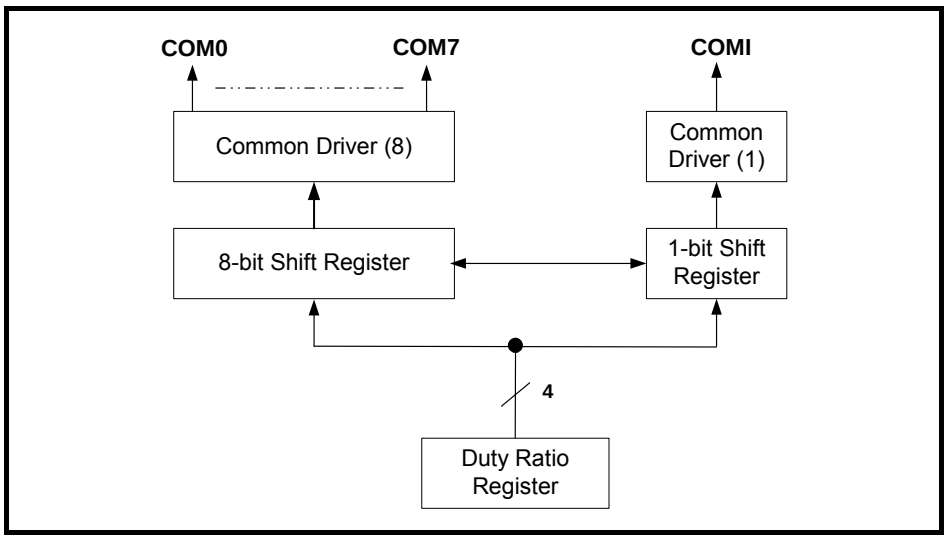


Figure 8 Common Output Circuits

Duty	SHL	Common Output Pins								
		COM0	COM1	COM2	COM3	COM4	COM5	COM6	COM7	COMI
		Line Address								
1/9	0	0	1	2	3	-	-	-	-	COMI
1/8	1	7	6	5	4	-	-	-	-	-
1/17	0	0	1	2	3	4	5	6	7	COMI
1/16	1	F	E	D	C	B	A	9	8	-

Relationship between Duty Ratio and Common Output

It should be noted that when using 1/16 duty (SHL=0), the MCU writes data to the LCD DRAM (Page 0: line addresses 0~7; Page 1: line addresses 8~15) and it will correspond to common output pins (Page 0: COM0~7; Page 1: COM34~41). But the EPL09060 have real output common pins COM0~7 and COMI, the others are invalid.

Initial Display Line Register

The initial display line register assigns a DDRAM line address which corresponds to COM0 by using the “Initial display line set” instruction. It is used not only for normal display but also for vertical display scrolling and page switching without changing the contents of the DDRAM. However, the 9th address for the icon display cannot be assigned for the initial display line address.

Line Counter

The line counter provides a DDRAM line address. It initializes its contents at the switching of frame reversal signal (FR (internal)), and also counts-up in synchronization with the common timing signal.

Column Address Counter

The column address counter is an 8-bit preset counter which provides a DDRAM column address, and is independent of page address register.

It will increment (+1) the column address whenever “display data read” or “display data write” instructions are issued. However, the incrementing of column address is stopped at column address 65H. The count-lock will be released by the “column address set” instruction again. The counter can inverts the correspondence between the column address and segment driver direction by means of “ADC select” instruction.

Page Address Register

The page address register provides a DDRAM page address. The Page Address 6 is used for icon display, and only D0 is valid.

7.3 LCD Driver Circuits

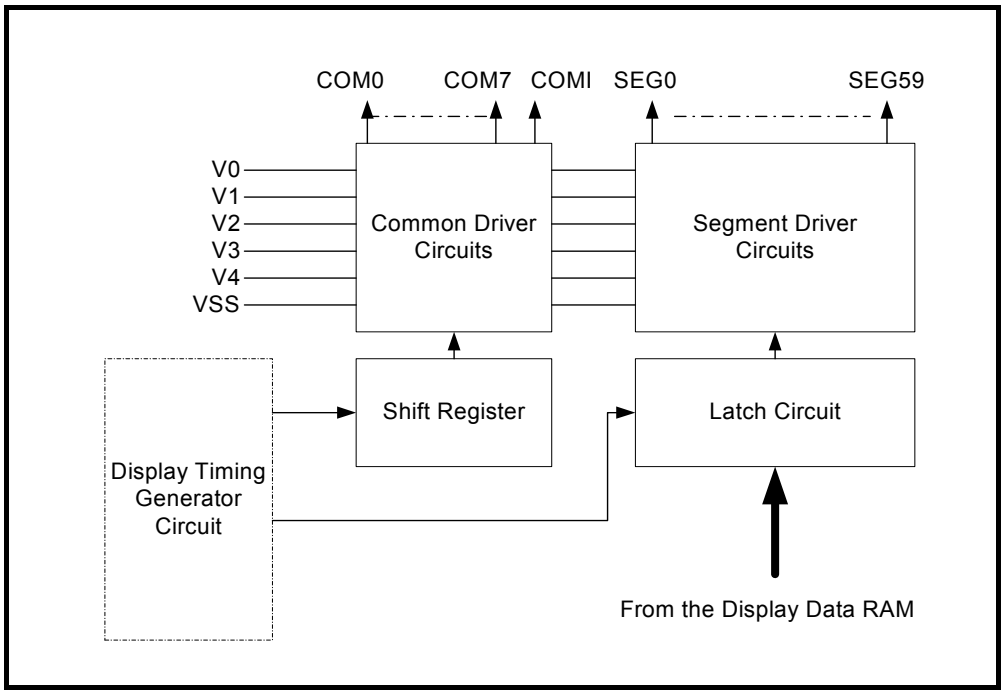


Figure 9 LCD Driver Circuits

This driver circuit is configured by 8-common drivers, 60-segment drivers and 1-icon-common driver. This LCD panel driver voltage depends on the combination of display data and FR (internal) signal.

7.3.1 Display Data Latch Circuit

The display data latch circuit is a latch that temporarily stores the display data that is output to the liquid crystal driver circuit from the display data RAM. “Display on/off”, “Inverse display on/off” and “Entire display on/off” instructions control only the contents of this latch circuit, they cannot change the contents of the DDRAM.

7.3.2 Shift Register Circuit

The circuit contains a 42-bit shift register to shift the turn-on data required for the LCD drive common signals and 1-bit shift register used for icon. The clock of this shift register is generated by display clock CL (internal).

Examples of 1/17 duty (ICON enable) driving waveform

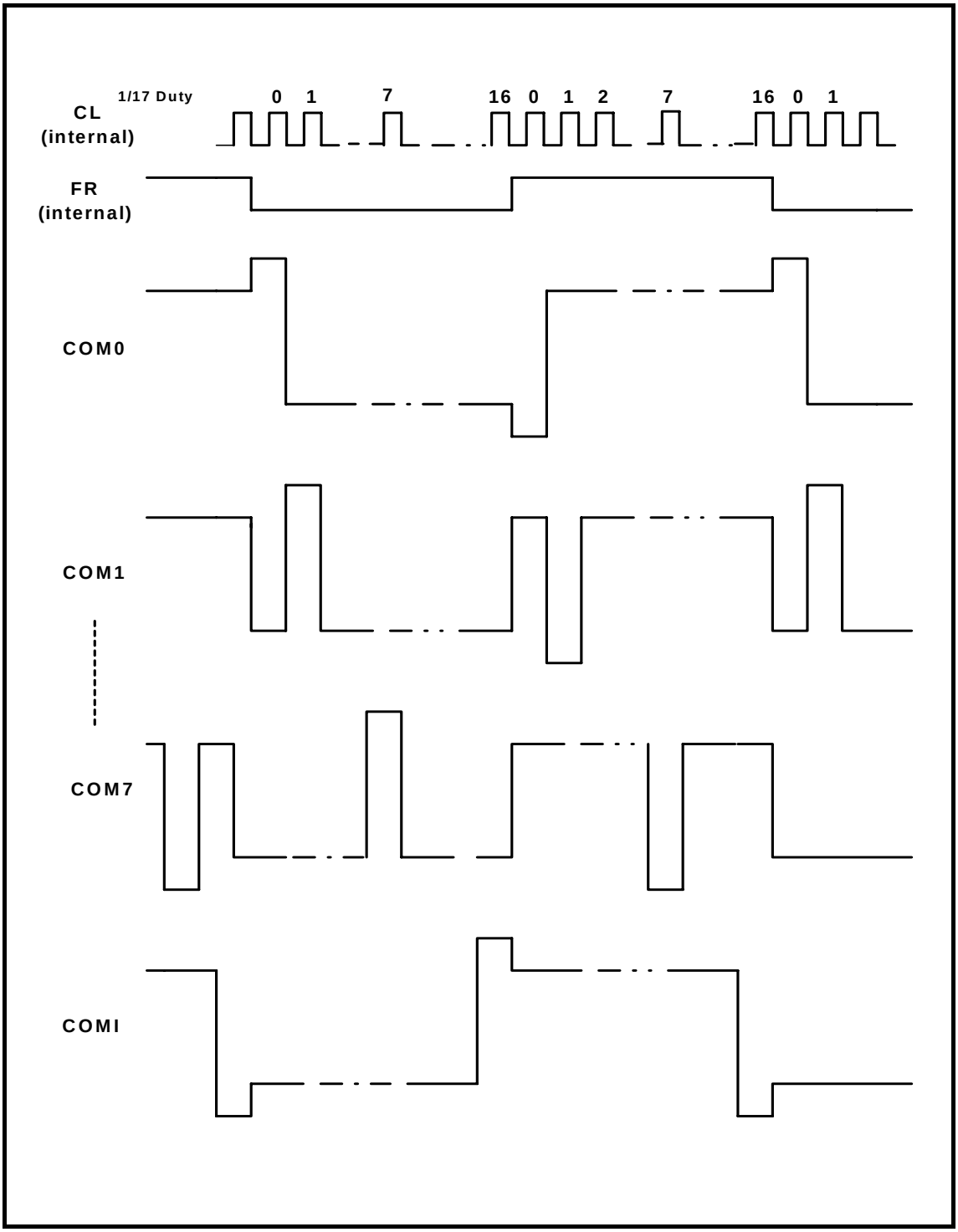


Figure 10 1/17 Duty Driving Waveform

Examples of 1/16 duty (ICON disable) driving waveform

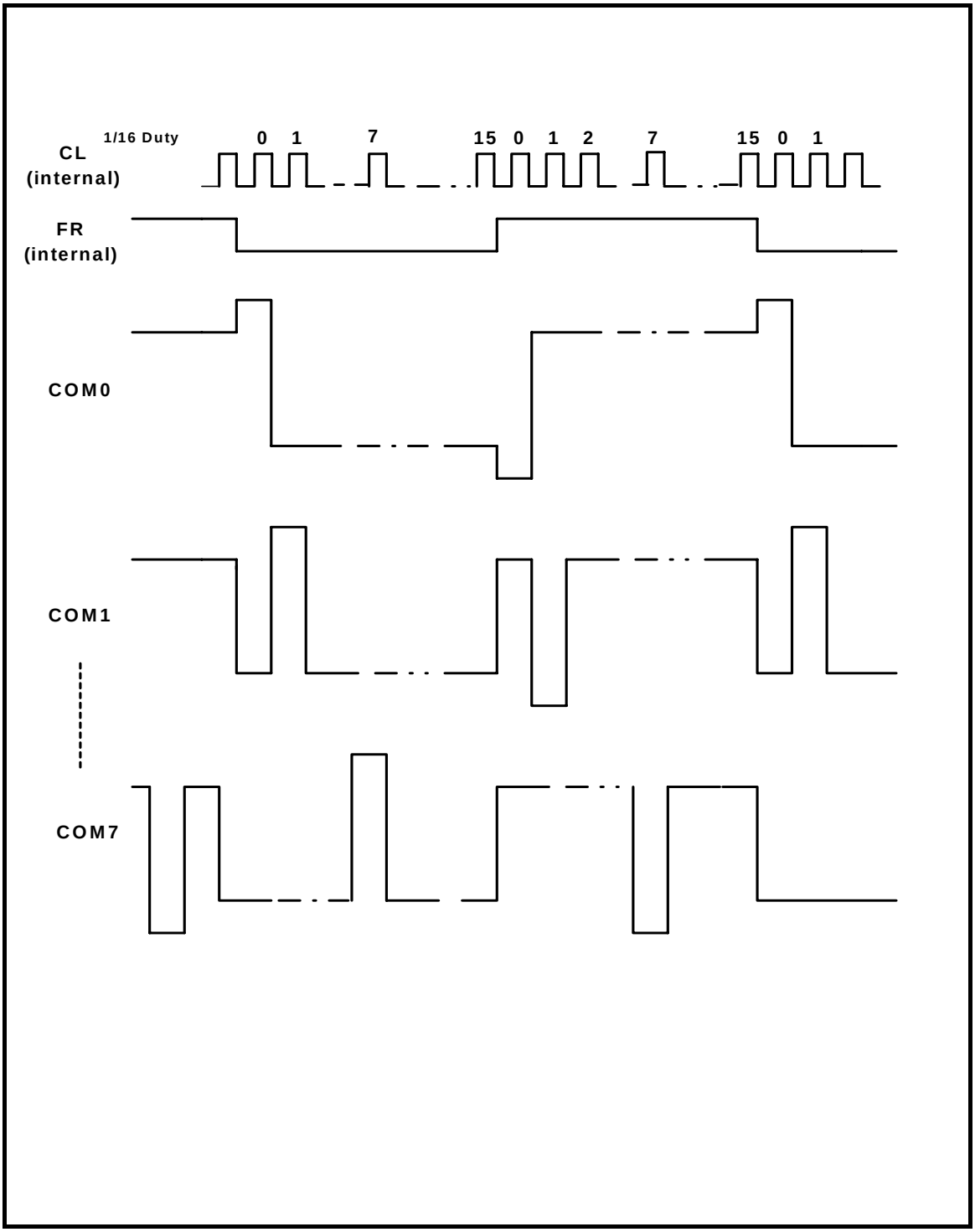
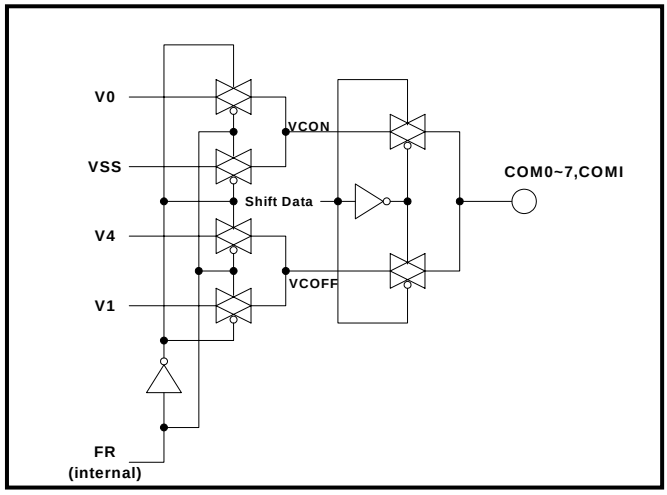


Figure 11 1/17 Duty Driving Waveform

7.3.3 Common Driver Circuit

The Common driver circuit consists of nine drive circuits. One of the four LCD driving level is selected by the combination of FR (internal) and the data from the sift register.

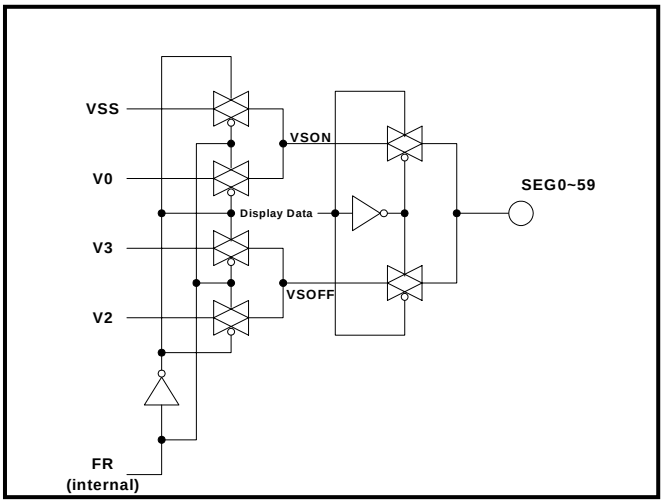


Scan Data	FR	COMs Output Voltage
H	H	VSS
	L	V0
L	H	V1
	L	V4
Power save mode		VSS

Figure 12 Common Driver Circuit

7.3.4 Segment Driver Circuit

The Segment driver circuit consists of 60 driver circuits. One the four LCD driving level is selected by the combination of FR (internal) and the display data transferred from the latch circuit.



Display Data	FR	SEGs Output Voltage	
		Normal Display	Inverse Display
H	H	V0	V2
	L	VSS	V3
L	H	V2	V0
	L	V3	VSS
Power save mode		VSS	

Figure 13 Common Driver Circuit

7.3.5 LCD Driving Waveform

The following illustration is an example of how the common and segment drivers are attached to an LCD panel.

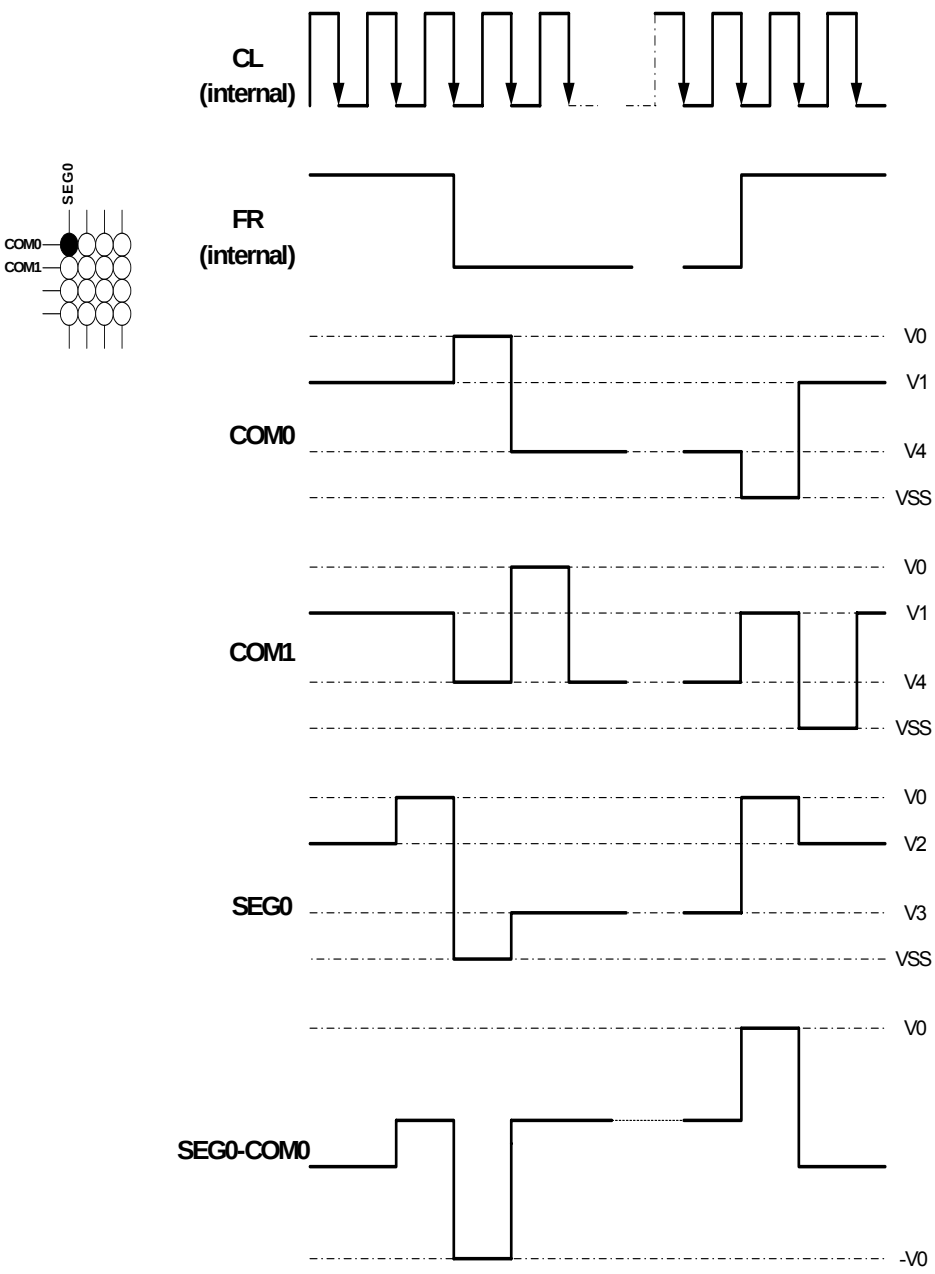


Figure 14 LCD Driver Circuits

7.4 Internal Power Circuits

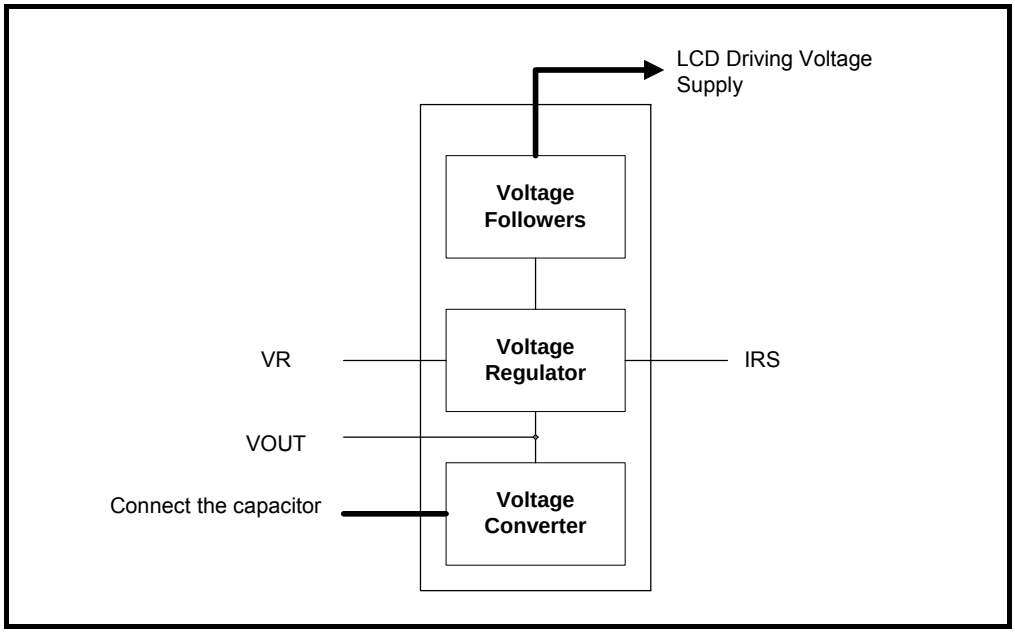


Figure 15 Internal Power Circuits

The internal power supply circuits can generate the voltage levels necessary to drive the liquid crystal driver circuits, with low power consumption and the least components. They comprise of voltage converter (V/C) circuits, voltage regulator (V/R) circuits, and voltage follower (V/F) circuits.

User Setup	Power Control (VC VR VF)	V/C Circuits	V/R Circuits	V/F Circuits	VOUT	V0	V1 ~ V4
Only the internal power supply circuits are used	1 1 1	On	On	On	Open	Open	Open
Only the voltage Regulator circuits and voltage follower circuits are used	0 1 1	Off	On	On	External Input	Open	Open
Only the voltage follower circuits are used	0 0 1	Off	Off	On	Open	External Input	Open
Only the external power supply circuits are used	0 0 0	Off	Off	Off	Open	External Input	External Input

7.4.1 Voltage Converter Circuits

These circuits boost up the electric potential between VDD and VSS to 2 times toward the positive side and the boosted voltage is outputted from VOUT pin. The boosting magnitude of the internal booster circuit is selected by means of the capacitor connection (Refer to Figure 16 below). The internal oscillator is required to be operating when using this converter, since the divided signal provided from the oscillator is used for the internal timing of this circuit.

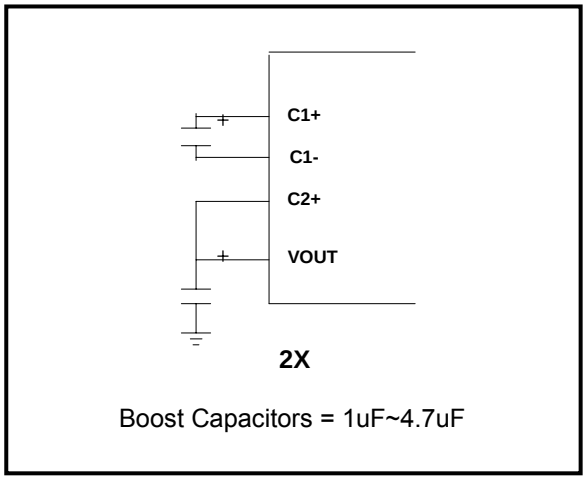


Figure 16 Capacitor Connections

7.4.2 Voltage Regulator Circuits

The voltage regulator determines the LCD driving voltage V0, by adjusting resistors Ra and Rb, within the range of |V0| < |VOUT|. Since VOUT is the operating voltage of the operational-amplifier circuits, it is necessary to be applied either internally or externally. For Equation 1, V0 is determined by Ra, Rb and VEV. Ra and Rb are connected internally or externally through the IRS pin. VEV which is the electronic volume voltage, is determined by Equation 2, where the parameter α is the value selected by the instruction "Set Contrast Control Mode," within the range 0 to 63.

VREF, a constant voltage source is 2 V at TA=25°C.

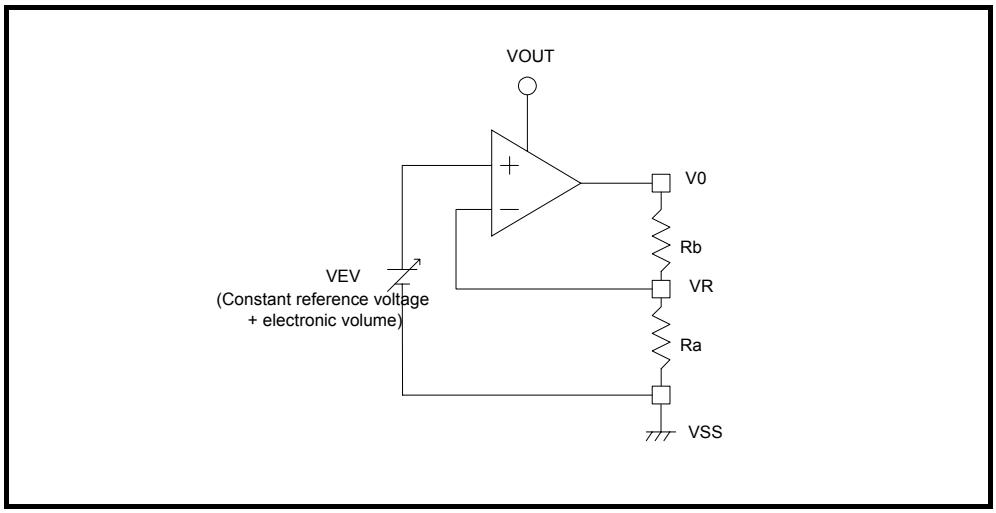


Figure 17 Resistor Connections

$$V0 = (1 + \frac{Rb}{Ra}) \times VEV \quad \text{.....Equation 1}$$

$$VEV = (1 - \frac{(63 - \alpha)}{252}) \times VREF \quad \text{.....Equation 2}$$

Register Value (R2, R1, R0)	1 + (Rb/Ra)
(0, 0, 0)	3.5

Refer to “Regulator Resistor Select” instruction for details.

	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0
1	0	0	0	0	0	1
..	.	.	.	.	.	.
..	.	.	.	.	.	.
62	1	1	1	1	1	0
63	1	1	1	1	1	1

Refer to “Set Contrast Control Mode” instruction for details.

Using Internal Resistors, Ra and Rb (IRS = "H")

When the IRS pin is “H”, resistor Ra is connected internally between VR pin and VSS, and Rb is connected between V0 and VR. V0 is determined by using the two instructions, "Regulator Resistor Select" and "Set Reference Voltage".

Using External Resistors, Ra and Rb (IRS = "L")

When IRS pin is “L”, it is necessary to connect the external regulator resistor Ra between VR and VSS, and Rb between V0 and VR.

For a particular liquid, the optimum VLCD can be calculated for a given multiplex rate.

For a 1/9 duty ratio, the optimum operating voltage of the liquid can be calculated as:

$$V_{LCD} = \frac{1+\sqrt{9}}{\sqrt{2\times\left(1-\frac{1}{\sqrt{9}}\right)}} \times V_{th} = 3.464 \times V_{th}$$

where Vth is the threshold voltage of the liquid crystal material used.

7.4.3 Voltage Follower Circuits

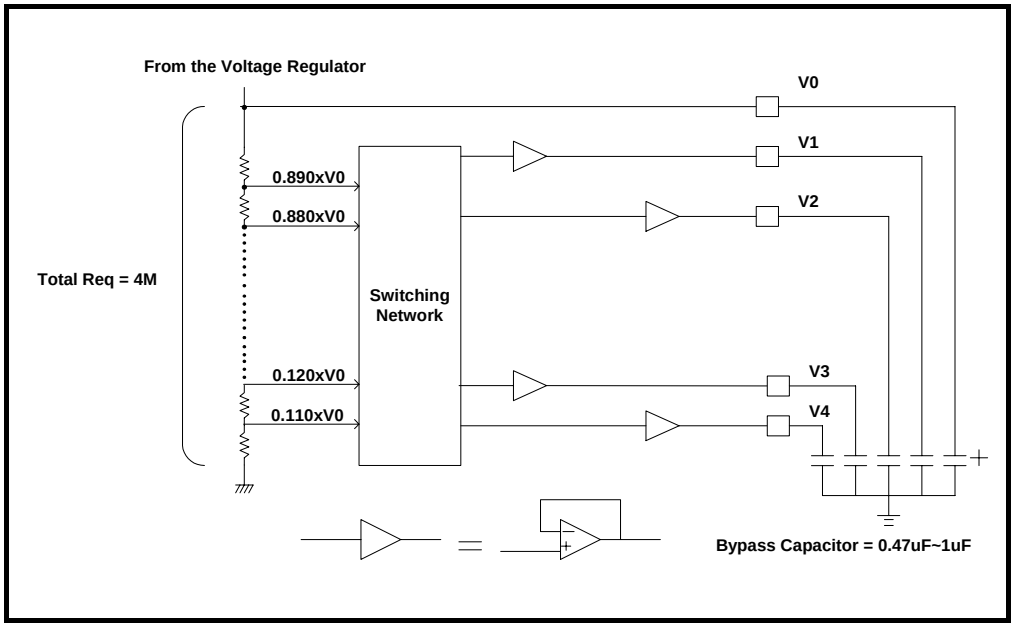


Figure 18 OTP Voltage Follower

The VLCD voltage (V0) is resistively divided into four voltage levels (V1, V2, V3, V4), and those output impedance are converted by the voltage follower (OPA) to increase the drive capability. Total 6 levels LCD reference voltage (V0, V1, V2, V3, V4, VSS) is generated by the voltage follower circuits.

LCD Bias	V1	V2	V3	V4
1/8	0.875×V0	0.750×V0	0.250×V0	0.125×V0
1/7.5	0.865×V0	0.735×V0	0.265×V0	0.135×V0
1/7	0.855×V0	0.715×V0	0.285×V0	0.145×V0
1/6.5	0.845×V0	0.690×V0	0.310×V0	0.155×V0
1/6	0.835×V0	0.665×V0	0.335×V0	0.165×V0
1/5.5	0.820×V0	0.635×V0	0.365×V0	0.180×V0
1/5	0.800×V0	0.600×V0	0.400×V0	0.200×V0

LCD Bias	V1	V2	V3	V4
1/4.5	0.780×V0	0.555×V0	0.445×V0	0.220×V0
1/4	0.750×V0	0.500×V0	0.500×V0	0.250×V0
1/3.5	0.715×V0	0.430×V0	0.570×V0	0.285×V0
1/3	0.665×V0	0.335×V0	0.665×V0	0.335×V0

Different duty radio requires different bias level. For optimum bias level, BL can be calculated using the following equation:

$$B_L = \frac{1}{\sqrt{Duty\ ratio} + 1}$$

Changing the bias system from the optimum will have an effect on the contrast and viewing angle.

The LCD Bias affects the display quality. But to reduce the current consumption, an unsuitable bias may be selected. Hence, the LCD Bias could be selected by “Select LCD bias” instruction.

7.4.4 Oscillator

The on-chip RC type oscillator provides the display clock and voltage converter timing clock. It has low power consumption and its frequency is nearly independent of VDD.

When “CLS”=”H”, the oscillator circuit is enabled. When CLS=”L”, the oscillator is stopped, and the oscillator clock has to be input to the OSC pin.

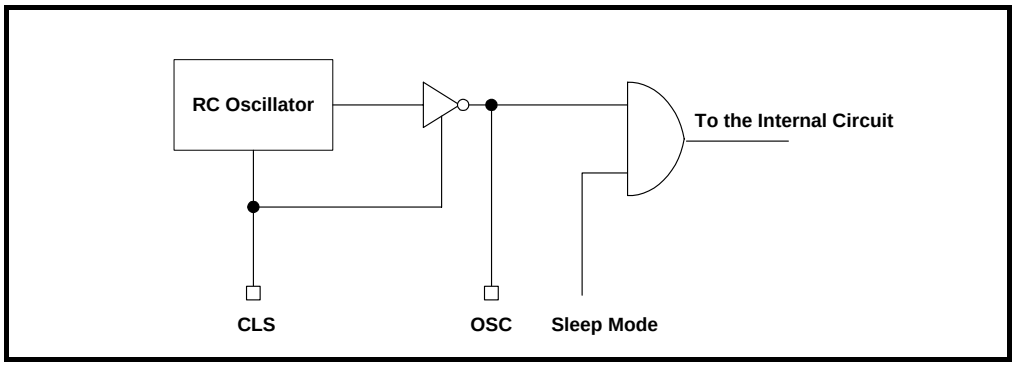


Figure 19 RC Oscillator

7.4.5 Oscillator Frequency

The EPL09060 contains an RC oscillator. The frame frequency (f_{FM}) is derived from the RC circuit’s oscillation frequency (f_{OSC}) by giving it an appropriate value. The relationship between the oscillation frequency (f_{OSC}), display clock frequency (f_{CL}) and the frame frequency (f_{FM}) is shown below.

The f_{OSC} could be selected from an internal or external oscillator via the CLS pin, f_{CL} could be selected via “Set display clock CL frequency” instruction, and frame frequency could be calculated using the following equation.

$$f_{CL} = (\text{Duty ratio}) \times (\text{Frame frequency})$$

7.5 Reset Circuit

When the /RES input comes to the “L” level, this LSI returns to its default state. The default settings are as follows:

- Display OFF
- Normal display
- ADC select: Normal (ADC select instruction D0 = “L”)
- SHL select: Normal (SHL select instruction D3 = “L”)
- Power Control Register: (D2, D1, D0) = (0, 0, 0)
- Serial interface internal register data clear
- Duty ratio = 1/43, (D3~D0) = (1, 1, 0, 1)
- CL frequency Register (D4, D3, D2, D1, D0) = (0, 0, 0, 0, 1, 1)
- LCD power supply bias level = (1/8), (D3~D0) = (1, 0, 1, 0)
- Entire display OFF (Entire display instruction D0 = “L”)
- Power saving clear
- Modify-Read OFF
- Display initial line set to first line : 0
- Column address set to Address : 0
- Page address set to Page : 0
- V0 voltage regulator internal resistor ratio set mode clear: (R2, R1, R0) = (0, 0, 0)
- Contrast control set mode clear
- Contrast control register : (D5, D4, D3, D2, D1,D0) = (1, 0, 0, 0, 0, 0)

NOTE

After issuing the command “reset”, the registers “Duty ratio” and “bias” must be set with a suitable value.

8 Control Register

Instruction	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Description
Read Display Data	1	0	1	Read Data								Read data from DDRAM
Write Display Data	1	1	0	Write Data								Write data into DDRAM
Read Status	0	0	1	Status				0	0	0	0	Read the internal status
Set Duty Ratio Mode	0	1	0	1	0	0	0	0	1	0	0	Set duty ratio Mode
Duty Ratio Register	0	1	0	*	*	*	*	ICON	D2	D1	D0	Select the duty ratio
Set CL frequency Mode	0	1	0	1	0	0	0	0	0	1	0	Set CL frequency Mode
CL frequency Register	0	1	0	*	*	*	D4	D3	D2	D1	D0	Set CL frequency Register
Set LCD Bias select Mode	0	1	0	1	0	0	0	0	1	0	1	Set LCD Bias select Mode
LCD Bias select Register	0	1	0	*	*	*	*	D3	D2	D1	D0	Select the LCD Bias
Display On/Off	0	1	0	1	0	1	0	1	1	1	Don	Turn on/off LCD panel When DON=0: display off When DON=1: display on
Initial Display Line	0	1	0	0	1	0	0	0	D2	D1	D0	Specify DDRAM line for COM0
Set Contrast Control Mode	0	1	0	1	0	0	0	0	0	0	1	Set Contrast Control Mode
Set Contrast Control Register	0	1	0	*	*	D5	D4	D3	D2	D1	D0	Set Contrast Control Register
Set Page Address	0	1	0	1	0	1	1	Page Address				Set page address
Set Column Address MSB	0	1	0	0	0	0	1	Higher order Column Add				DDRAM column address of Higher 4-bits
Set Column Address LSB	0	1	0	0	0	0	0	Lower order Column Add				DDRAM column address of lower 4-bits
ADC Select	0	1	0	1	0	1	0	0	0	0	ADC	Select segment direction When ADC=0: normal direction (SEG0 →SEG59) When ADC=1: reverse direction (SEG59→SEG0)
Inverse Display ON/OFF	0	1	0	1	0	1	0	0	1	1	REV	Select normal/inverse display 0 : Normal display 1 : Inverse display on
Entire Display ON/OFF	0	1	0	1	0	1	0	0	1	0	EON	Select normal/entire display ON When EON=0: normal display. When EON=1: entire display ON
Set Modify-read	0	1	0	1	1	1	0	0	0	0	0	Set modify-read mode
Reset Modify-read	0	1	0	1	1	1	0	1	1	1	0	Release modify-read mode
Reset	0	1	0	1	1	1	0	0	0	1	0	Initialize the internal functions
SHL Select	0	1	0	1	1	0	0	SHL	*	*	*	Select COM output direction When SHL=0: normal direction (COM0 -> COM7) When SHL=1: reverse direction (COM7 -> COM0)
Power Control	0	1	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation
Regulator Resistor Select	0	0	0	0	0	1	0	0	0	0	0	Select internal resistance ratio ofthe regulator resistor
Power Save	-	-	-	-	-	-	-	-	-	-	-	Compound instruction of display OFF and entire display ON

Note: * : Don't care

Read Display Data

The 8-bit data from the display data RAM specified by the column address and page address can be read by this instruction. As the column address is automatically incremented by 1 after each instruction execution, the microprocessor can continuously read data from the addressed page.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read Data							

Write Display Data

The 8-bit display data from the microprocessor can be written to the RAM location specified by the column address and page address. After writing the display data, the column address is automatically incremented so that the microprocessor can continuously write data to the addressed page.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write Data							

Read Status

This instruction reads out the internal status regarding “ADC select”, “Display On/Off” and “Reset”.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	-	ADC	On/Off	RESET	0	0	0	0

Flag	Description
ADC	It shows the correspondence between the column address and segment drivers. ADC = 0 : Normal direction (SEG0 → SEG59) ADC = 1 : Reverse direction (SEG59 → SEG0)
On/Off	This bit indicates the ON/OFF state of the display. 0 : Display ON 1 : Display OFF
RESET	Indicates that the initialization is in progress, by the RESETB signal. RESET = 0 : Normal display operation state RESET = 1 : Internal reset operation state with reset command.

Set Duty Ratio (Two-Byte instruction)

The first instruction sets the duty ratio mode, the second one updates the contents of the duty ratio register. After the second instruction, the set duty mode is released. The LSI cannot accept any instructions except the “Set duty ratio register” during the set duty ratio mode.

Set Duty Ratio Mode (First Instruction)

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	1	0	0

Set Duty Ratio Register (Second Instruction)

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Duty Ratio
0	1	0	*	*	*	*	ICON	0	0	0	8 (+ICON)
								0	0	1	16 (+ICON)
								0	1	0	24 (+ICON)
								0	1	1	32 (+ICON)
								1	0	0	36 (+ICON)
								1	0	1	42 (+ICON)

Note: "*" means "Don't care"

ICON: "0" Disable COMI (icon display) pin
"1" Enable COMI (icon display) pin

Set Display Clock CL Frequency (Two-Byte Instruction)

The display clock CL affects the current consumption and the frame frequency affects the flicker, so fine adjustment is required for the display clock CL (internal) and the frame frequency.

Set CL Frequency Select Mode (First Instruction)

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	1	0

Set CL Frequency Select Register (Second Instruction)

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	CL Frquency
0	1	0	*	*	*	0	0	0	0	0	fOSC
						0	0	0	0	1	fOSC / 2
						0	0	0	1	0	fOSC / 3
						0	0	0	1	1	fOSC / 4
						0	0	1	0	0	fOSC / 5
						0	0	1	0	1	fOSC / 6
						0	0	1	1	0	fOSC / 7
						0	0	1	1	1	fOSC / 8
						0	1	0	0	0	fOSC / 9
						0	1	0	0	1	fOSC / 10
						0	1	0	1	0	fOSC / 11
						0	1	0	1	1	fOSC / 12
						0	1	1	0	0	fOSC / 13
						0	1	1	0	1	fOSC / 14
						0	1	1	1	0	fOSC / 15
						0	1	1	1	1	fOSC / 16
						1	*	*	*	*	fOSC / 32

Note: "*" means "Don't care"

Select LCD Bias (Two-Byte Instruction)

This instruction selects the LCD bias ratio of the voltage required for driving the LCD.

Set LCD Bias Select Mode (First Instruction)

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	1	0	1

Set LCD Bias select Register (Second instruction)

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	LCD Bias
0	1	0	*	*	*	*	0	0	0	0	1/3
							0	0	0	1	1/3.5
							0	0	1	0	1/4
							0	0	1	1	1/4.5
							0	1	0	0	1/5
							0	1	0	1	1/5.5
							0	1	1	0	1/6
							0	1	1	1	1/6.5
							1	0	0	0	1/7
							1	0	0	1	1/7.5
							1	0	1	0	1/8

Note: "*" means "Don't care"

Display ON/OFF

This instruction is used to control the turning on or off of the LCD panel, regardless of the contents of the DDRAM.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Display On or Off
0	1	0	1	0	1	0	1	1	1	0	0 :Off
										1	1 :On

Initial Display Line

This instruction sets the line address of the display RAM to determine the initial display line. The initial display line corresponds to COM0. The display area read from the display data RAM corresponds to the number of the lines set by the Duty select command.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Line Address for COM0
0	1	0	0	1	0	0	0	0	0	0	0
								0	0	1	1
								.	.	.	.
								.	.	.	.
								1	1	0	6
								1	1	1	7

Electronic Contrast Control Set (Two-Byte instruction)

The first instruction sets the contrast control mode, the second one updates the contents of the contrast control register. After the second instruction, the contrast control mode is released. The LSI cannot accept any instructions except for the "Set Contrast Control Register" during the Contrast Control Mode.

Set Contrast Control Mode (First instruction)

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

Set Contrast Control Register (Second instruction)

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Electronic Volume Value (α)
0	1	0	*	*	0	0	0	0	0	0	0 Minimum
					0	0	0	0	0	1	1
					.	.	.	.	.	.	.
					.	.	.	.	.	.	.
					1	1	1	1	1	0	62
					1	1	1	1	1	1	63

Set Page Address

This instruction sets the page address of the display data RAM from the microprocessor into the page address register. It is possible to access any required bit in the display data RAM by specifying the page address and the column address.

Along with the column address, the page address defines the address of the display RAM used to write or read the display data. Changing the page address does not affect the display status. Page 6 is assigned for the icon display. Only D0 is valid.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Page Address
							0	0	0	0	0
							0	0	0	1	1
							.	.	.	.	.
0	1	0	1	0	1	1	.	.	.	.	.
							.	.	.	.	.
							.	.	.	.	.
							0	1	1	0	6

Set Column Address

This instruction sets the column address of the display data RAM from the microprocessor into the column address register. When accessing the display data RAM from the MPU, the column address is incremented. The incrementing of the column address is stopped at address 65H.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Column Address Setting
0	1	0	0	0	0	1	0	0	A5	A4	Upper 4-bit
						0	A3	A2	A1	A0	Lower 4-bit

A5	A4	A3	A2	A1	A0	Column Address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	1	1	0	1	0	58
1	1	1	0	1	1	59

ADC Select

This instruction selects the segment driver direction. Normal or reverse can be selected in the correlation between the display data RAM column address and the segment output terminal.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Segment Driver Direction
0	1	0	1	0	1	0	0	0	0	0 1	Normal Reverse

D0 = 0 Normal Column addresses 00H to 3BH corresponds to segment outputs 0 to 59.

D0 = 1 Reverse Column addresses 2AH to 65H corresponds to segment outputs 59 to 0.

Inverse Display ON/OFF

This instruction is used to invert the display status on the LCD panel without rewriting the contents of the display data RAM.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Display Status
0	1	0	1	0	1	0	0	1	1	0 1	Normal Inverse

D0 = 0 Normal Display data “1” makes the LCD on.
D0 = 1 Inverse Display data “0” makes the LCD on.

Entire Display ON/OFF

This instruction forces the whole LCD points to be turned on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM will be retained. This instruction has priority over the Reverse Display On/Off instruction.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Entire display on/off
0	1	0	1	0	1	0	0	1	0	0 1	Normal Entire display on

Set Modify-Read

This instruction stops the automatic increment of the column address by the Read Display Data instruction, but the column address is still incremented by the Write Display Data instruction. This instruction can reduce the load of the MPU, during the display, the data in a specific DDRAM area is repeatedly changed for cursor blinking or others. This mode is canceled by the Reset Modify-read instruction.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

Reset Modify-Read

This instruction cancels the Modify-read mode. The column address of the display data RAM returns to the address before the Read Modify Write is executed.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

Reset

This instruction resets the initial display line, column address, page address, and the common output status is reset to their initial status, but does not affect the contents of display data RAM. This instruction cannot initialize the LCD power supply, which is initialized by the /RES pin.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

Reset status by “Reset” instruction:

Read modify write off

Initial display line address : (00)H

Column address : (00)H

Page address : (0) page

SHL select : Normal mode (D3=0)

Regulator resistor select register: (R2, R1, R0) = (0, 0, 0)

Sets contrast control set mode off and contrast control register : (20)H

SHL Select

COM output scanning direction is selected by this instruction which determines the LCD driver output status.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Common Driver Direction
0	1	0	1	1	0	0	0 1	*	*	*	Normal Reverse

Note: “*” means “Don’t care”

D3 =0 Normal Normal direction (COM0 → COM 7) → (1/16duty ratio, Page 0)

D3 =1 Reverse Reverse direction (COM7 → COM 0) → (1/16duty ratio, Page 1)

Power Control

Selects one of eight power circuit functions by using the 3-bit register. An external power supply and part of internal power supply functions can be used simultaneously.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	1	VC	VR	VF

VC: Voltage converter
VR: Voltage regulator
VF: Voltage follower
0: Off 1: ON

Regulator Resistor Select

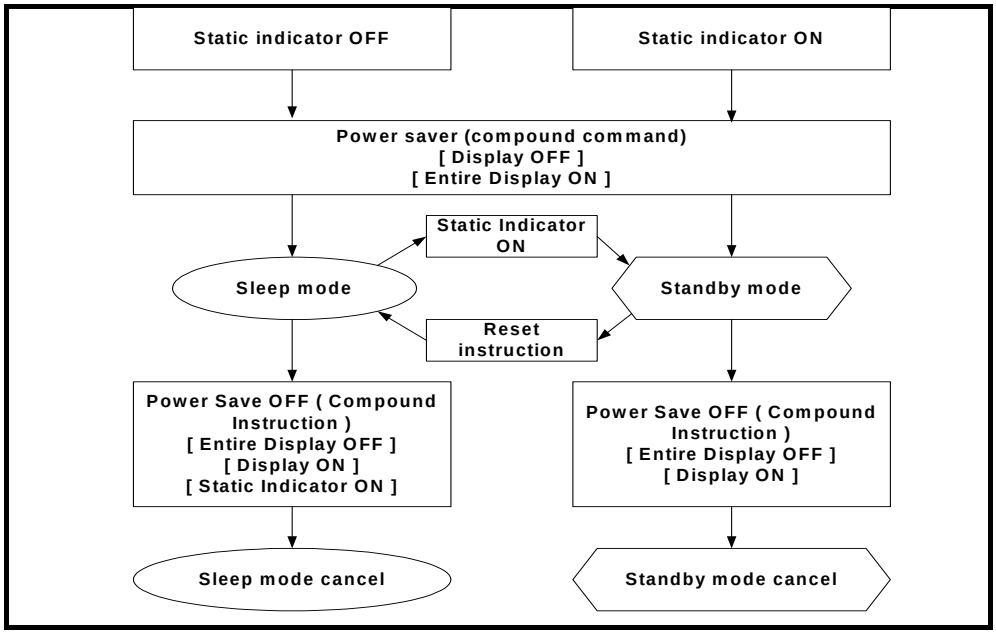
Selects the resistance ratio of the internal resistor used in the internal voltage regulator. See the voltage regulator section in power supply circuit for more details.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	R2	R1	R0

R2	R1	R0	[Rb/Ra] Ratio
0	0	0	3.5

Power Save (Compound Instruction)

The current consumption can be greatly reduced by entering the power save status and inputting the “Entire Display ON” instruction while the display is in OFF mode. According to the status in static indicator mode, power save is entered through one of two modes (sleep and standby mode). Power Save mode is released by the “Display ON” & “Entire Display OFF” instructions.



Sleep Mode

This stops all operations in the LCD display system, and as long as there are no accesses from the MPU, the current consumption is reduced to a value near the static current. The internal modes during sleep mode are as follows:

The oscillator circuit and the LCD power supply circuit are stopped.

All liquid crystal drive circuits are stopped, as well as the segment and common driver output VSS level.

When a “static indicator on” instruction is issued in the sleep mode, the LSI goes into the standby mode.

Standby Mode

All operations of the dynamic LCD display section are stopped, only the static display circuits for the indicators operate and hence the current consumption will be the minimum necessary for static drive. The internal conditions in the standby state are as follows:

The power supply circuit for LCD drive is stopped. The oscillator circuit will still be operating.

The LCD drive circuits for dynamic display are stopped and the segment and common driver outputs will be at the VSS level. The static display section will still be operating.

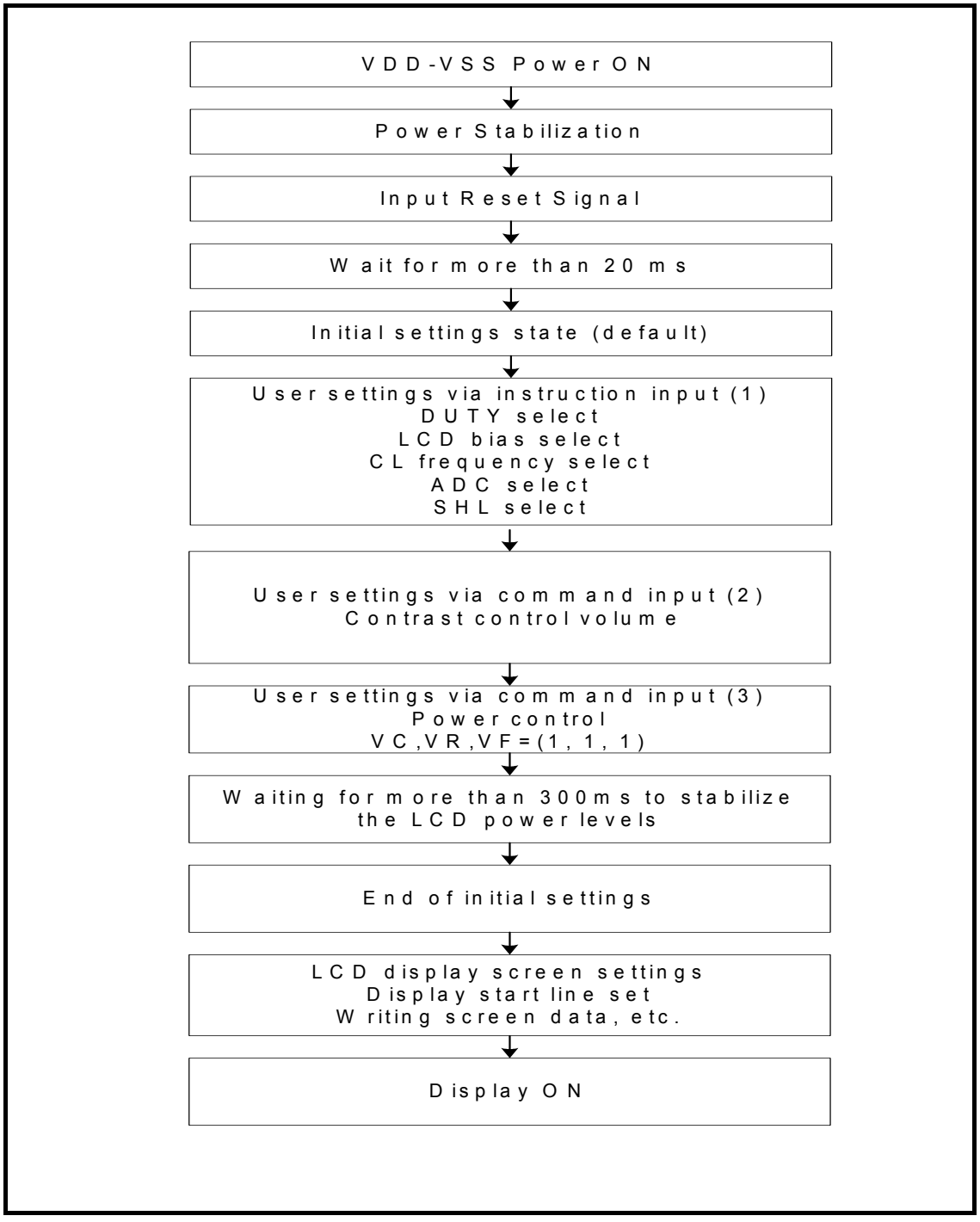
When a reset instruction is issued in the standby mode, the LSI goes into a sleep mode.

9 Application Information

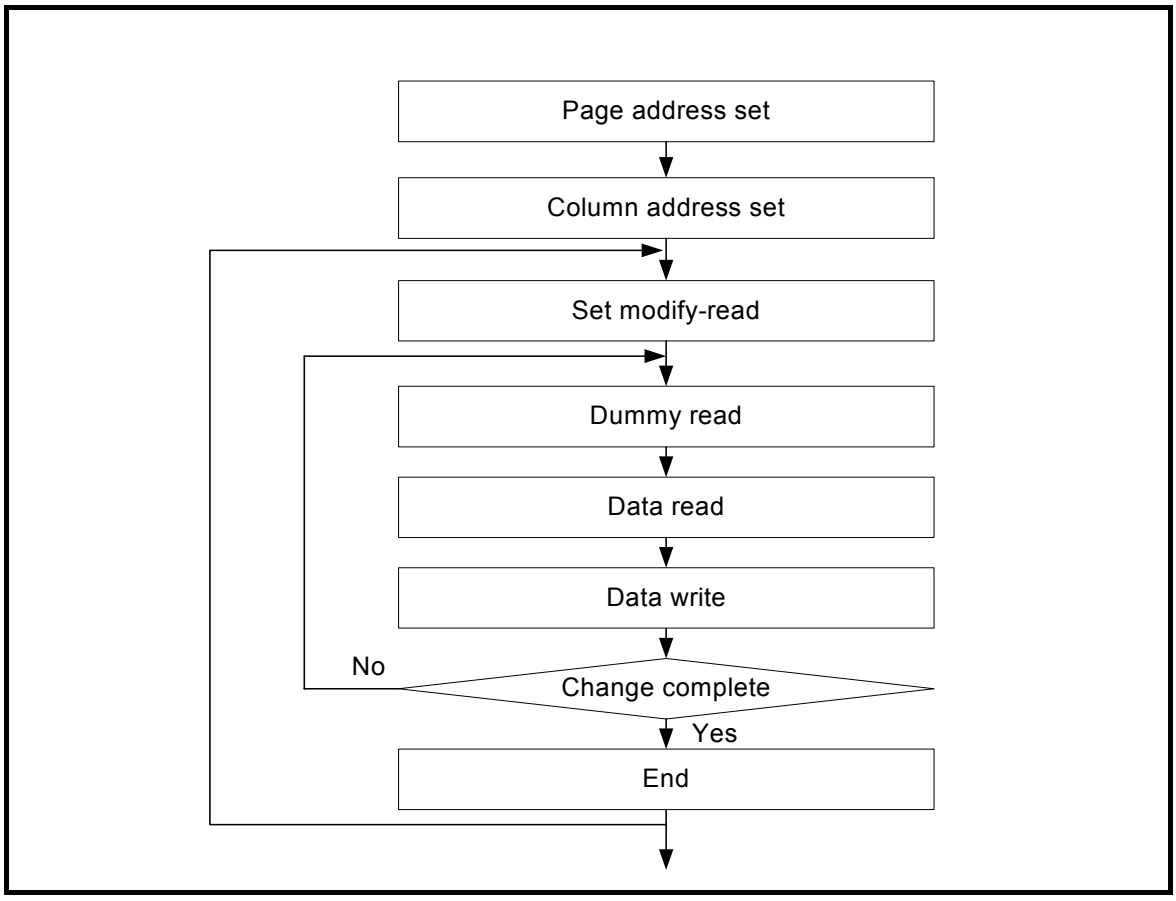
9.1 Instruction Procedure Examples

9.1.1 Initial Setup

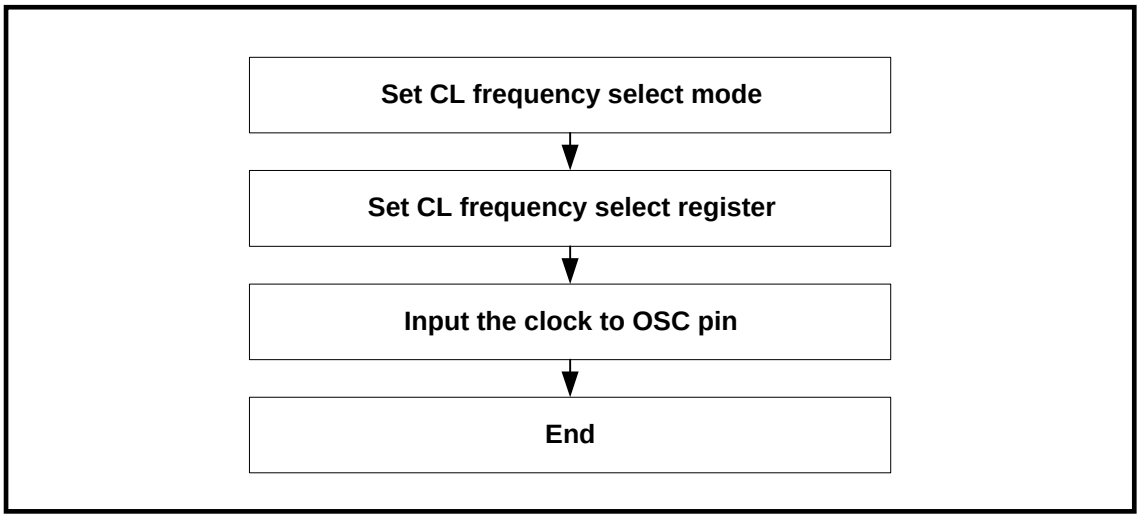
(From power application to display ON using internal power supply circuits)



The “Modify-read” sequence



The “External oscillator input” sequence



PROGRAM EXAMPLES

Use Elan Risc II MCU assembly

```
;*************************************************************************
;          Initialization Setting Example of EPL09060
;*************************************************************************
INI_DRIVER_IC:
MOV     A,#LCD_COM_RESET          ;INITIAL SETTINGS STATE (DEFAULT)
CALL    WRITE_LCD_1BYTE
MOV     A,#LCD_COM_DUTY           ;SET DUTY 1ST INSTRUCTION
CALL    WRITE_LCD_1BYTE
MOV     A,#DUTY_SET               ;SET DUTY 2ND INSTRUCTION
CALL    WRITE_LCD_1BYTE
MOV     A,#LCD_COM_BIAS           ;SET LCD BIAS 1ST INSTRUCTION
CALL    WRITE_LCD_1BYTE
MOV     A,BIAS_SET                ;SET BIAS 2ND INSTRUCTION
CALL    WRITE_LCD_1BYTE
MOV     A,#LCD_COM_FREQ           ;SET LCD CL FREQUENCY 1ST INSTRUCTION
CALL    WRITE_LCD_1BYTE
MOV     A,#CL_FREQ                ;SET CL FREQUENCY 2ND INSTRUCTION
CALL    WRITE_LCD_1BYTE
MOV     A,#LCD_ADC_SET            ;SET ADC FUNCTION SELECT
CALL    WRITE_LCD_1BYTE
MOV     A,#LCD_SHL_SET            ;SET SHL FUNCTION SELECT
CALL    WRITE_LCD_1BYTE
MOV     A,#LCD_REGULATOR_RES_SET  ;SET REGULATOR RESISTOR 1+(Rb/Ra)
CALL    WRITE_LCD_1BYTE
MOV     A,#LCD_COM_CONTRAST       ;SET CONTRAST 1ST INSTRUCTION
CALL    WRITE_LCD_1BYTE
MOV     A,#CONTRAST_SET           ;SET CONTRAST 2ND INSTRUCTION
CALL    WRITE_LCD_1BYTE
MOV     A,#LCD_POWER_CONTROL_SET  ;SET POWER CONTROL (INTERNAL OR EXTERNAL)
CALL    WRITE_LCD_1BYTE
BS      REG_CPUCON,F_CKS          ;ADD CLOCK BY OSC PIN (CLOCK FROM CPU)
MOV     A,#150                    ;WAITING FOR LCD POWER TO STABILIZE
CALL    WAIT_A_MS
CALL    LCD_DISPLAY_ON            ;TURN ON LCD
MOV     A,#LCD_DISPLAY_INI_LINE   ;SET INITIAL DISPLAY LINE
CALL    WRITE_LCD_1BYTE
CALL    LCD_DATA_WRITE            ;WRITING SCREEN DATA
RET
```

```
;*******************************************************************************
```

; Write Display_Picture Data into Display Data Ram of EPL09060

```
;*******************************************************************************
DATA_WRITE:
  TBPTL   #DISPLAY_PICTURE*2      ;DEFINE DISPLAY PICTURE DATA INDEX
  TBPTM   #DISPLAY_PICTURE/0x80
  TBPTH   #DISPLAY_PICTURE/0x8000
DATA_WRITE_09060:
  MOV     A,#LINE_Y_MAX           ;MAX PAGES OF DDRAM
  MOV     REG_LCDARH,A
DATA_W1:
  MOV     A,#LINE_X_MAX           ;SET MAX SEGMENTS OF DDRAM
  MOV     REG_LCDARL,A
  BC      REG_PORTB,F_LCD_A0      ;SET LCD /A0 = 0 INSTRUCTION OUTPUT
  MOV     A,#LCD_COM_PAGE
  ADD     A,REG_LCDARH
  CALL    WRITE_LCD_1BYTE
  MOV     A,#0b00000000           ;SET LOWER ORDER COLUMN ADDRESS=0000
  CALL    WRITE_LCD_1BYTE
  MOV     A,#0b00010000           ;SET HIGHER ORDER COLUMN ADDRESS=0000
  CALL    WRITE_LCD_1BYTE
  BS      REG_PORTB,F_LCD_A0      ;SET LCD /A0 = 1 DATA OUTPUT
DATA_W2:
  TBRD    01,REG_ACC              ;ACCESS THE DATA OF DISPLAY_PICTURE
  CALL    WRITE_LCD_1BYTE
  DEC     REG_LCDARL
  JBS     REG_STATUS,F_C,DATA_W2  ;IDENTIFY RES_STATUS CARRY BIT SET OR NOT
  DEC     REG_LCDARH
  JBS     REG_STATUS,F_C,DATA_W1
  BC      REG_PORTB,F_LCD_A0      ;LCD /A0 = 0 FOR INSTRUCTION OUTPUT
RET
```

```
;*****************************************************************************
```

; Write One Byte Data Into DDRAM (Parallel Mode 80 Series)

```
;*****************************************************************************
;AT FIRST DEFINE A0 TO IDENTIFY DATA OR INSTRUCTION WRITE
WRITE_LCD_1BYTE:
  JBS     REG_DCRG,F_LAHEN,WRITE_LCD_1BYTE_1    ;CHECK REG_DCRG LAHEN BIT=1 OR NOT
  BC      REG_PORTC,F_LCD_WR            ;SET /WR=0 ENABLE WRITE
  MOV     REG_DATA,A                    ;MOVE A==> PORT_G
  NOP                                   ;Write low pulse( Wait for
                                        ;2 instruction cycles)
  NOP
  BS      REG_PORTC,F_LCD_WR            ;SET /WR=1 DISABLE WRITE
  NOP
  NOP
  NOP
  NOP
  RET
WRITE_LCD_1BYTE_1:
  MOV     REG_DATA,A                    ;MOVE A==> PORT_G
  RET


;*****************************************************************************
```

;; Read One Byte Data Into DDRAM (Parallel Mode 80 Series)

```
;;*****************************************************************************
;AT FIRST DEFINE A0 TO IDENTIFY DATA OR INSTRUCTION READ
READ_LCD_1BYTE:
  BC      REG_PORTB,F_LCD_RD            ;SET /RD=0 ENABLE READ
  NOP
  NOP
  MOV     A,REG_DATA                    ;MOVE PORT_G ==> A
  NOP
  BS      REG_PORTB,F_LCD_RD            ;SET /RD=1 DISABLE READ
  NOP
  RET
```

9 Relationship between Setting and Common/Display RAM

The microprocessor (MPU) can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM simultaneously as data is being displayed without causing the LCD to flicker.

Page Address P3,P2,P1,P0	Data	Column Address																Line Address (HEX)	Common Output pins SHL=0 (1/8)	Common Output pins SHL=1 (1/8)	Common Output pins SHL=0 (1/16)	Common Output pins SHL=1 (1/16)
0 0 0 0	D0					PAGE0												00	COM0	COM7	COM0	
	D1																	01	COM1	COM6	COM1	
	D2																	02	COM2	COM5	COM2	
	D3																	03	COM3	COM4	COM3	
	D4																	04			COM4	
	D5																	05			COM5	
	D6																	06			COM6	
	D7																	07			COM7	
0 0 0 1	D0					PAGE1												08				COM7
	D1																	09				COM6
	D2																	0A				COM5
	D3																	0B				COM4
	D4																	0C				COM3
	D5																	0D				COM2
	D6																	0E				COM1
	D7																	0F				COM0
0 0 1 0	D0					PAGE2												10				
	D1																	11				
	D2																	12				
	D3																	13				
	D4																	14				
	D5																	15				
	D6																	16				
	D7																	17				
0 0 1 1	D0					PAGE3												18				
	D1																	19				
	D2																	1A				
	D3																	1B				
	D4																	1C				
	D5																	1D				
	D6																	1E				
	D7																	1F				
0 1 0 0	D0					PAGE4												20				
	D1																	21				
	D2																	22				
	D3																	23				
	D4																	24				
	D5																	25				
	D6																	26				
	D7																	27				
0 1 0 1	D0					PAGE5												28				
	D1																	29				
0 1 1 0	D0					PAGE6													COMI	COMI		
Column Address (HEX)	ADC = 0	00	01	02	03	----------				38	39	3A	3B									
	ADC = 1					----------				2D	2C	2B	2A	----------	02	01	00					
LCD Output		SEGMENT0	SEGMENT1	SEGMENT2	SEGMENT3	----------				SEGMENT56	SEGMENT57	SEGMENT58	SEGMENT59	None segment								

Note: 1. The data on Page Address 2~5 would not be output to the common pins, but can be regarded as general data RAM.
2. The EPL09060 will output RAM data (Page 0) to COM0 ~ COM7 (COMI) when using 1/16 (1/17) duty and SHL=0.

10 Absolute Maximum Ratings

Parameter	Applicable Pins	Symbol	Condition	Rate Value	Unit
Power supply voltage	VDD	VDD	-	-0.3 to +7	V
Driver supply voltage	VOUT	VLCD	-	-0.3 to +17	
Input voltage	All Input	VIN	-	-0.3 to VDD+0.3	
Operating temperature range	-	TA	-	-30 to +80	°C
Storage temperature range	-		-	-55 to +125	

Recommended Operating Conditions

Parameter	Applicable Pins	Symbol	Condition	Rated Value			Unit
				Min.	Typ.	Max.	
Power supply Voltage	VDD	VDD	-	2.2	-	3.4	V
Voltage converter output voltage	VOUT	VOUT	-	4.0	-	6.8	
V0 output voltage	V0	V0	-	3.0	-	6.0	
Output voltage		VOH	-	0.7VDD	-	VDD	
		VOL	-	VSS	-	0.3VDD	
Input voltage		VIH	-	0.7VDD	-	VDD	
		VIL	-	VSS	-	0.3VDD	
Operating temperature range	-	TA	-	0		40	OC

11 DC Characteristics

VSS = 0V, VDD = 2.6 to 3.3V, TA = -30~80°C

Parameter	Applicable Pins	Symbol	Condition	Rated Value			Unit
				Min.	Typ.	Max.	
Power Supply Voltage	V_{DD}	V_{DD}		2.2	-	3.4	V
Voltage Converter Input Voltage	V_{DD}	V_{DD2}	2 × boost	2.2	-	3.4	
Reference Voltage	-	VREF0	TA=0°C	2.07	2.16	2.25	
		VREF20	TA=20°C	1.96	1.98	2.05	
		VREF40	TA=40°C	1.86	1.94	2.02	
Regulated Voltage	V_0 [1]	V0	TA=0~40°C	V0-4%	V0	V0+4%	
OP Amp Voltage Output of LCD Power supply	V_0	VOUT0	No load [2 and 3]		V0		mV
	V_1	VOUT1			V1		
	V_2	VOUT2			V2		
	V_3	VOUT3			V3		
	V_4	VOUT4			V4		
Voltage Converter Output Voltage	VOUT	VOUT	× 2 (no-load)	95	99	100	%
LCD Driver ON Resistance	COMn SEGn	RON	Current load load= 50 µA	-	2	5	kΩ
Reset Resistor	/RES	RRESET	VDD=3V, Vin=0V	400	800	1200	
			VDD=3V, Vin=1.7V	25	50	75	
Output Current (Source and Drain)	[5]	IOH	VDD=3V, VOH=2.4V	-3	-4	-5	mA
		IOL	VDD=3V, VOL=0.2V	1.2	2.2	3.2	
Input Leakage Current	All Input [4]	IIL	VIN=VDD or 0V	-	-	±1	µA
Output Tri-state	[5]					± 3	
Dynamic Current Consumption (1/17 duty)		I_{DDD1}	VDD=3V, 2 boosting, TA=25°C, internal OSC. f_{OSC}=22kHz, 1/17 duty ratio,1/4.5 bias ratio, DV value=10H, regulator=(0, 0,0), CL=(0, 0, 0), all display pattern off, no load	-	40	55	
V1 Sink Capability	V1	Isv1	V0=3.6V, V1=2.4V (No load) VOH=2.8V	0.75	1	-	
V4 Source Capability	V4	Isv4	V0=3.6V, V4=1.2V (No load) VOL=0.8V	-0.75	-1	-	
Current Consumption		I_{DD1}	Standby mode	-	5	10	
Current Consumption		I_{DD2}	Sleep mode	-	1	2	
Frame Frequency		f_{FM}		-	85	-	Hz
Internal Oscillator Frequency	-	f_{OSC}	TA=25°C	17	22	27	kHz
External Input Oscillator	OSC	f_{OSC}	TA=25°C	-	22	-	

Note [1]: $V0 = (1 + \frac{Rb}{Ra}) \times VEV \;\; ; \;\; VEV = (1 - \frac{(63 - \alpha)}{252}) \times VREF$

[2]:

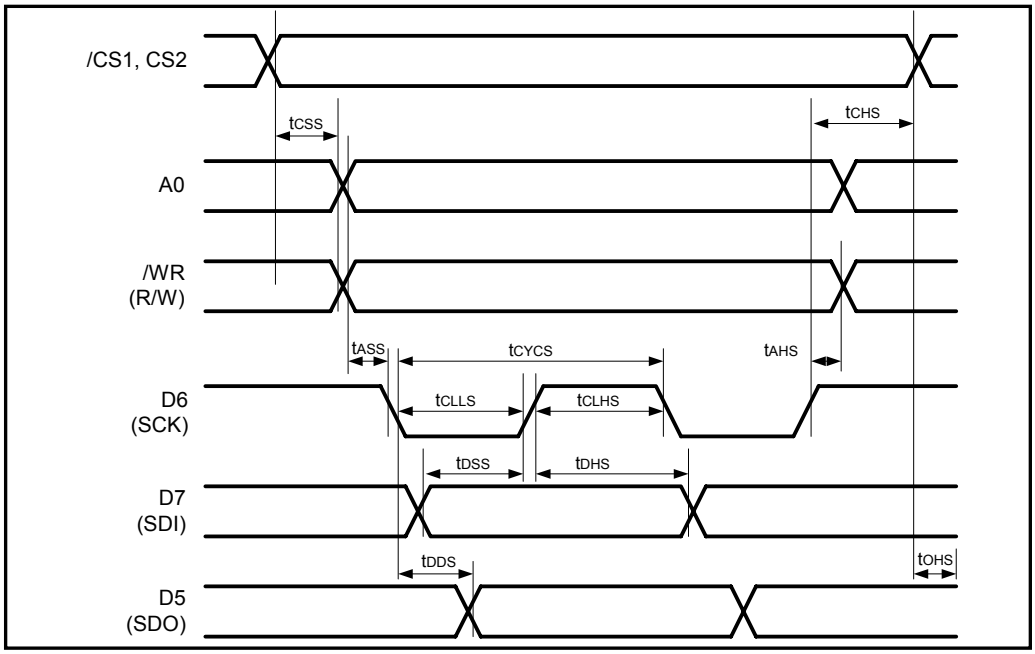
LCD Bias	V0	V1	V2	V3	V4
1/8 Bias		(7/8) × V_0	(6/8) × V_0	(2/8) × V_0	(1/8) × V_0
1/7.5 Bias		(6.5/7.5) × V_0	(5.5/7.5) × V_0	(2/7.5) × V_0	(1/7.5) × V_0
1/7 Bias		(6/7) × V_0	(5/7) × V_0	(2/7) × V_0	(1/7) × V_0
1/6.5 Bias		(5.5/6.5) × V_0	(4.5/6.5) × V_0	(2/6.5) × V_0	(1/6.5) × V_0
1/6 Bias		(5/6) × V_0	(4/6) × V_0	(2/6) × V_0	(1/6) × V_0
1/5.5 Bias		(4.5/5.5) × V_0	(3.5/5.5) × V_0	(2/5.5) × V_0	(1/5.5) × V_0
1/5 Bias		(4/5) × V_0	(3/5) × V_0	(2/5) × V_0	(1/5) × V_0
1/4.5 Bias		(3.5/4.5) × V_0	(2.5/4.5) × V_0	(2/4.5) × V_0	(1/4.5) × V_0
1/4 Bias		(3/4) × V_0	(2/4) × V_0	(2/4) × V_0	(1/4) × V_0
1/3.5 Bias		(2.5/3.5) × V_0	(1.5/3.5) × V_0	(2/3.5) × V_0	(1/3.5) × V_0
1/3 Bias		(2/3) × V_0	(1/3) × V_0	(2/3) × V_0	(1/3) × V_0

[3]: The target value of V0~V4 is Theoretical Value ± 50 mV

[4]: Input pin D0~D7, A0, /RD, /WR, /CS1, CS2, CLS, C86, IRS

[5]: Output pin D0~D7

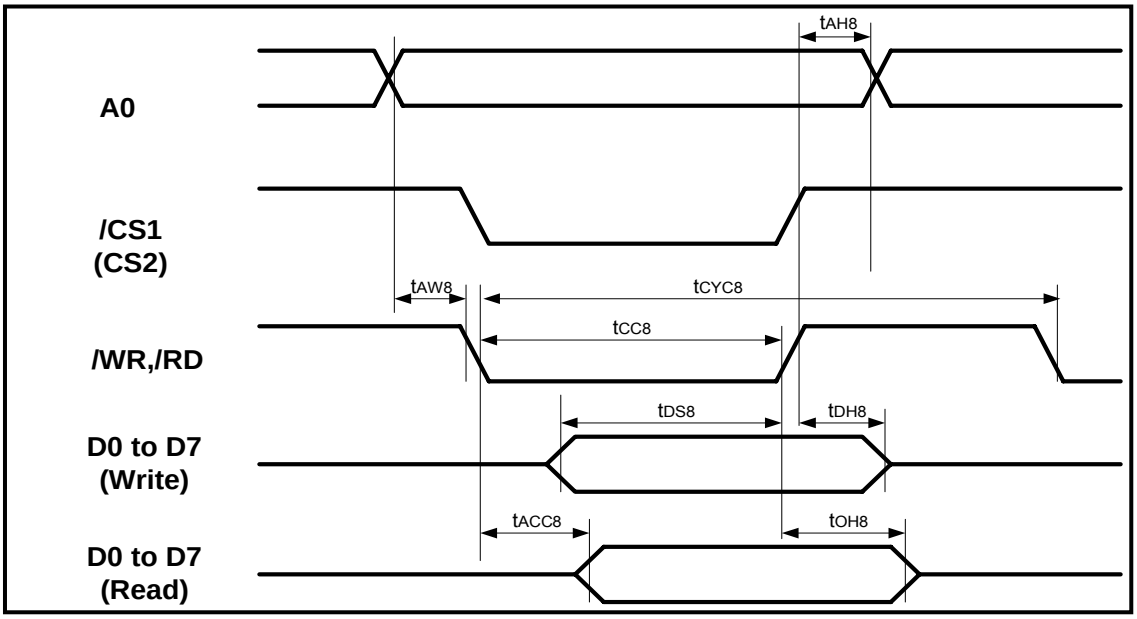
12 AC Characteristics



Serial Interface Timing Characteristics

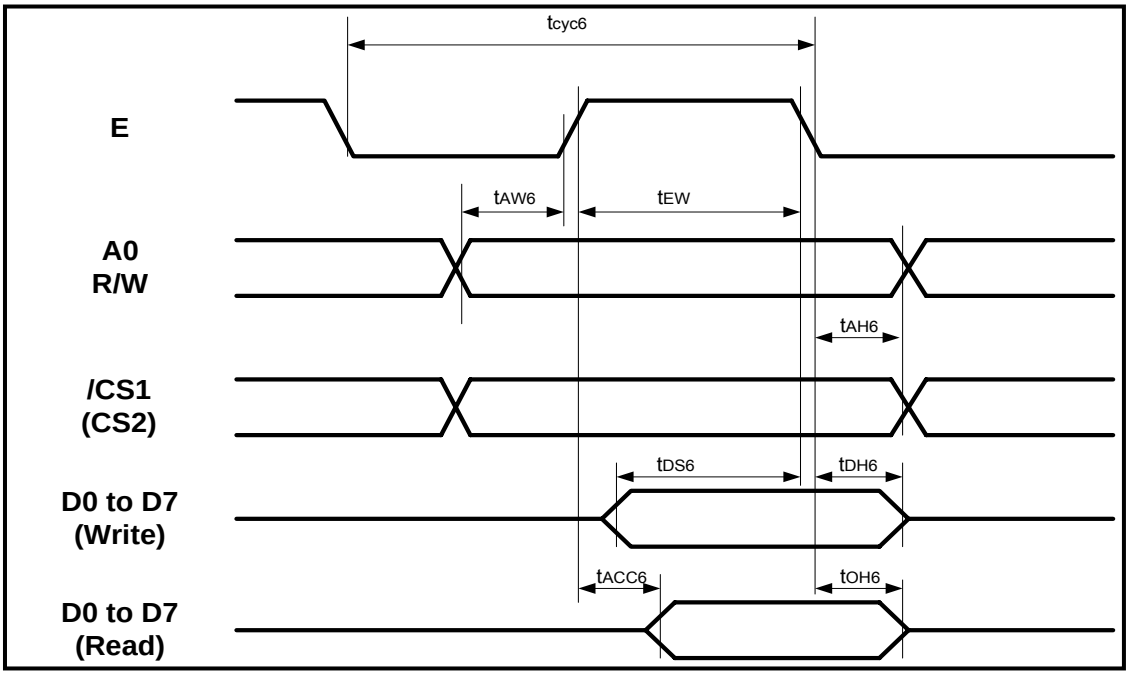
Parameter	Applicable Pins	Symbol	Condition	Rated Value		Unit
				Min.	Max.	
Chip Select Setup Time Chip Select Hold Time	/CS1 CS2	tCSS tCHS		100 100	-	ns
Address Setup time Address Hold time	A0 R/W	tASS tAHS		100 100	-	
Data Setup Time Data Hold Time	D7 (SDI)	tDSS tDHS	DATA→SCK↑ SCK↑→DATA	80 80	-	
Clock Cycle Time Clock L Time Clock H Time	D6 (SCK)	tCYCS tCLLS tCLHS		300 100 100	-	
Data Delay Time Data Disable Time	D5 (SDO)	tDDS tOHS	CL= 100 pF	 10	80 50	

80-Family MPU Read/Write Timing Characteristics (VSS= 0V, VDD= 2.6~3.3V, TA=0~40°C)



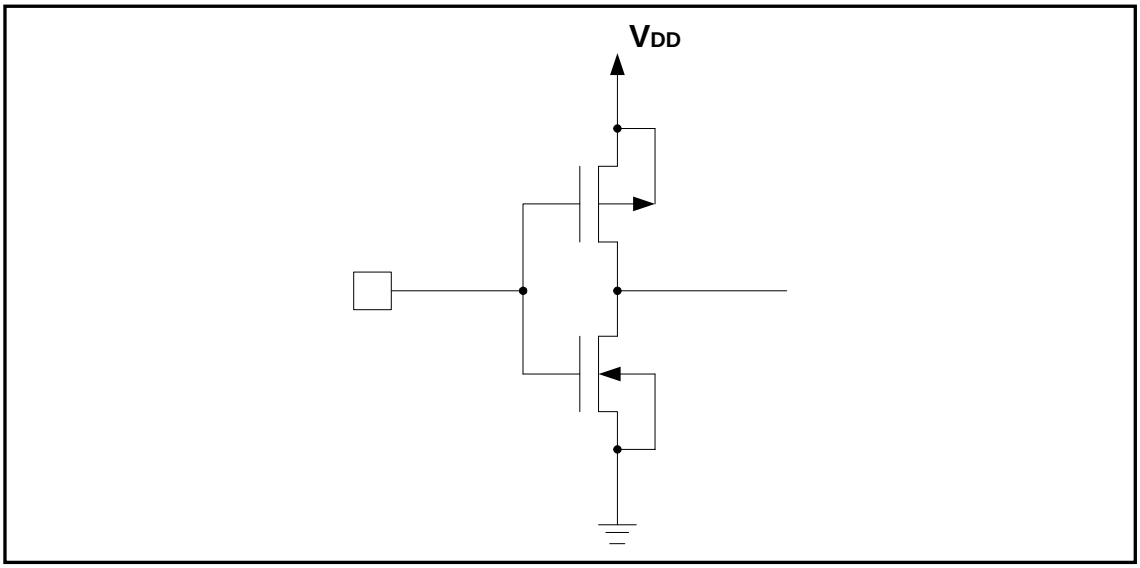
Parameter	Applicable pins	Symbol	Condition	Rated value		Unit
				Min.	Max.	
Address Setup Time Address Hold Time	A0	tAW8 tAH8		0 0	-	ns
System Cycle Time	A0	tCYC8		500	-	
Pulse Width(/WR) Pulse Width(/RD)	/WR /RD	tCC8		160 200	-	
Data Setup Time Data Hold Time	D0~D7	tDS8 tDH8		20 10	-	
Read Access Time Output Disable Time		tACC8 tOH8	CL=100pF	- 10	60 40	

68-Family MPU Read/Write Timing Characteristics (VSS = 0V, VDD = 2.6~3.3V, TA=0~40°C)

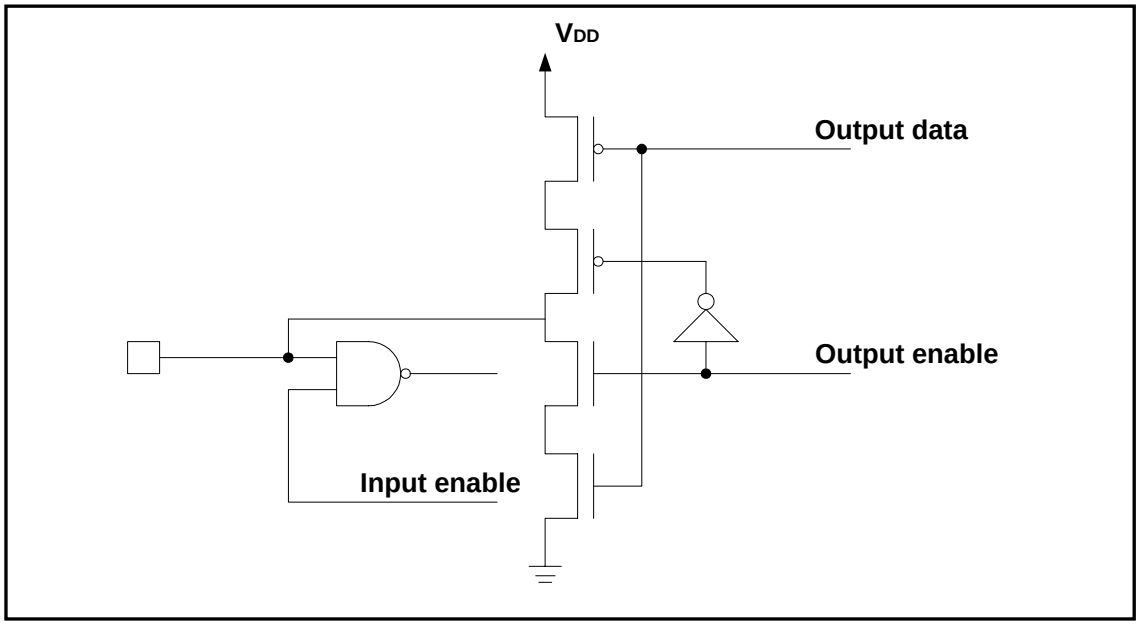


Parameter	Applicable Pins	Symbol	Condition	Rated Value		Unit
				Min.	Max.	
Address Setup Time Address Hold Time	A0 R/W	tAW6 tAH6		0 0	-	ns
System Cycle Time	A0	tCYC6		500	-	
Pulse Width (/WR) Pulse Width (/RD)	E	tEW		160 200	-	
Data Setup Time Data Hold Time	D0~D7	tDS6 tDH6		20 10	-	
Read Access Time Output Disable Time		tACC6 tOH6	CL=100pF	- 10	60 40	

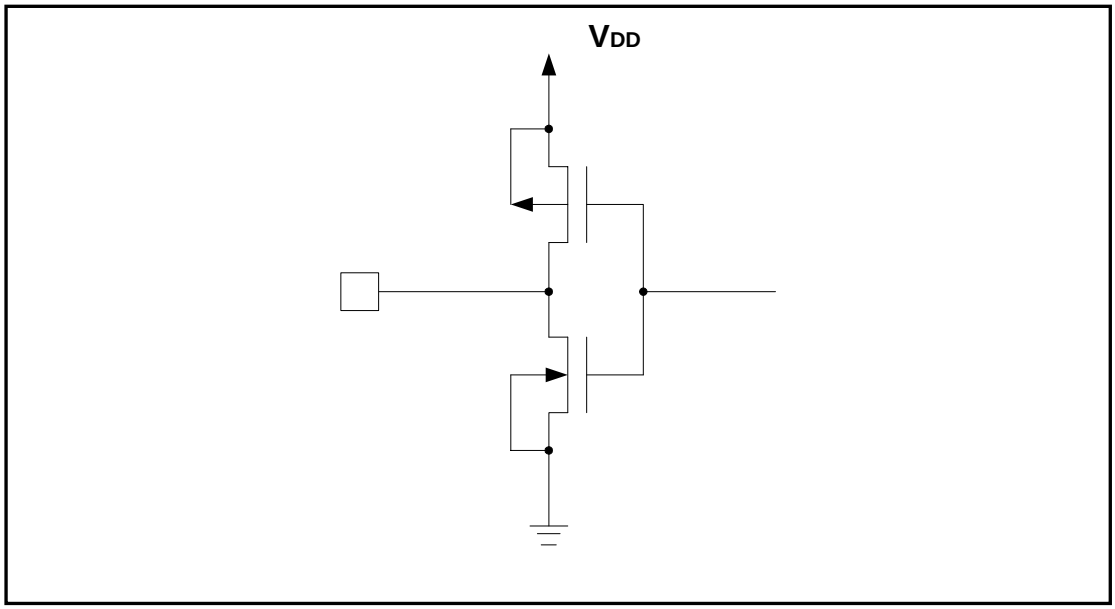
Input Pin Configuration (VSS = 0V, VDD = 2.6V~3.3V, TA = 0~40°C)



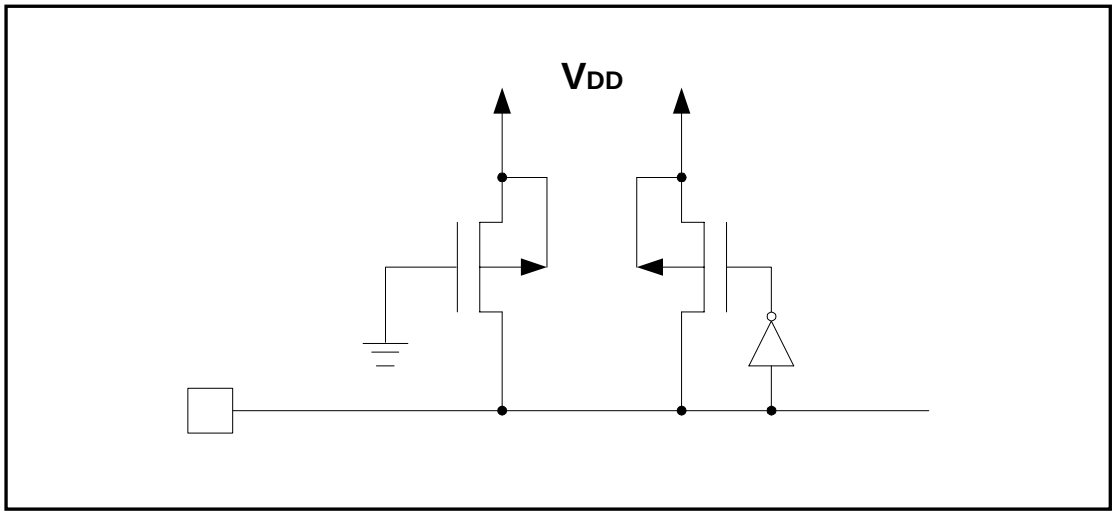
Input/Output Pin Configuration



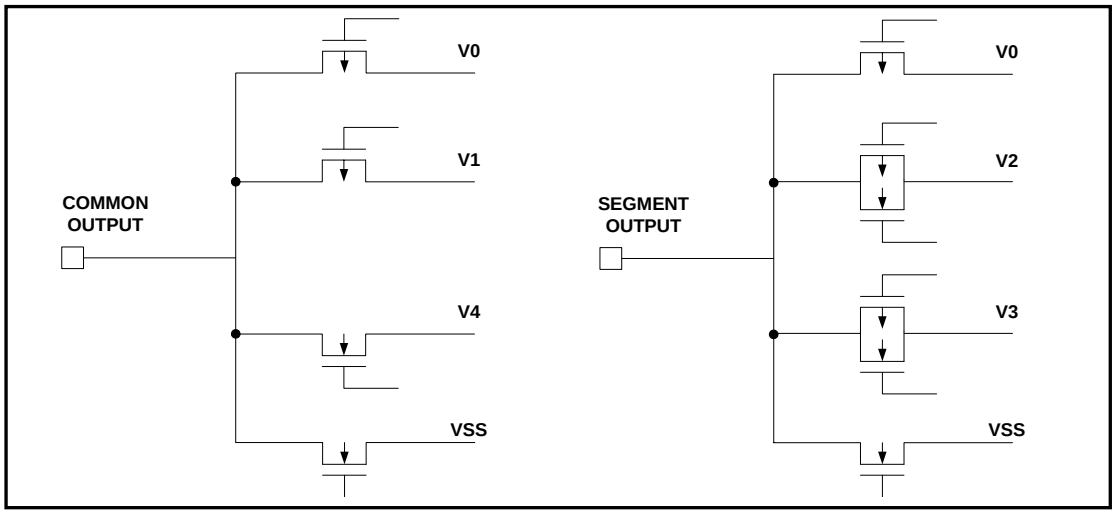
Output Pin Configuration



Reset Input Pin Configuration

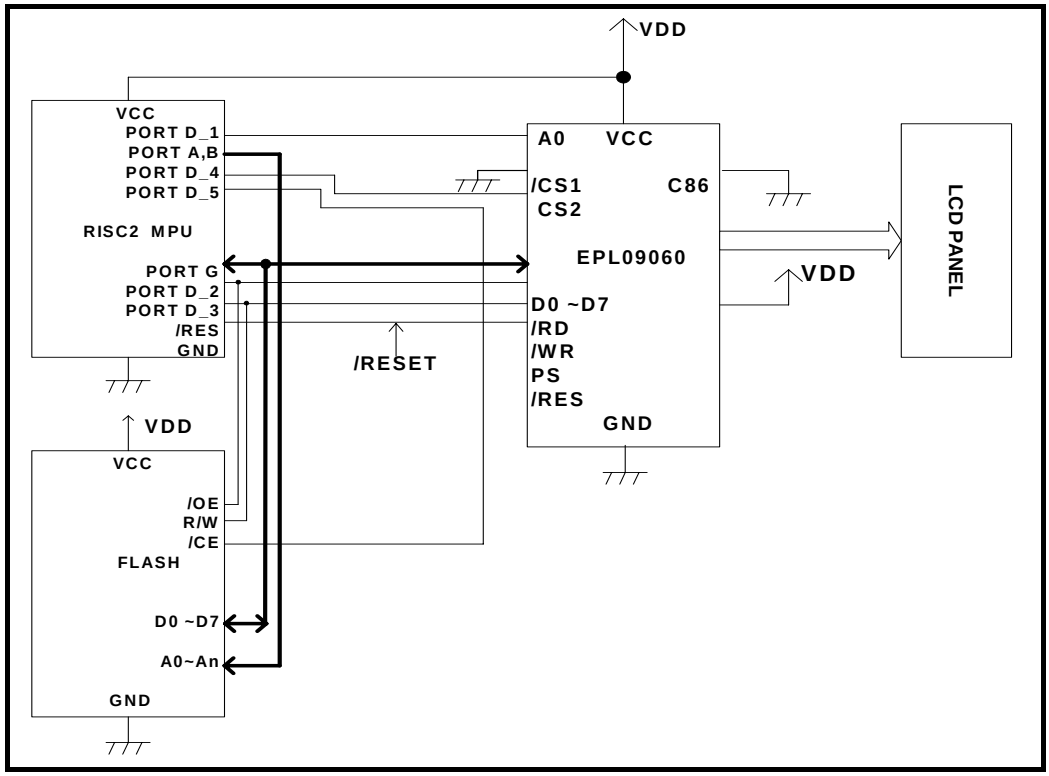


LCD Output Pin Configuration

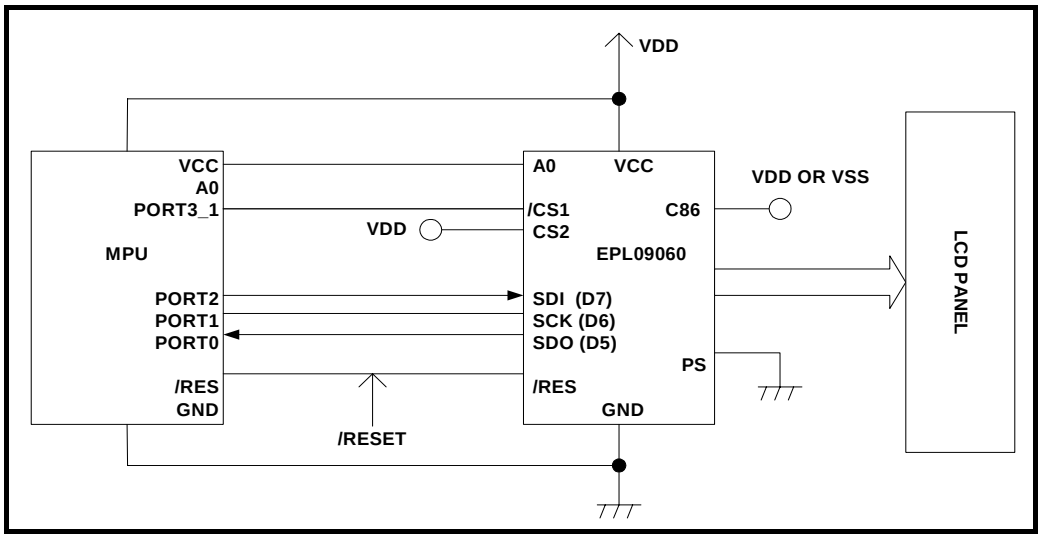


MPU Interface

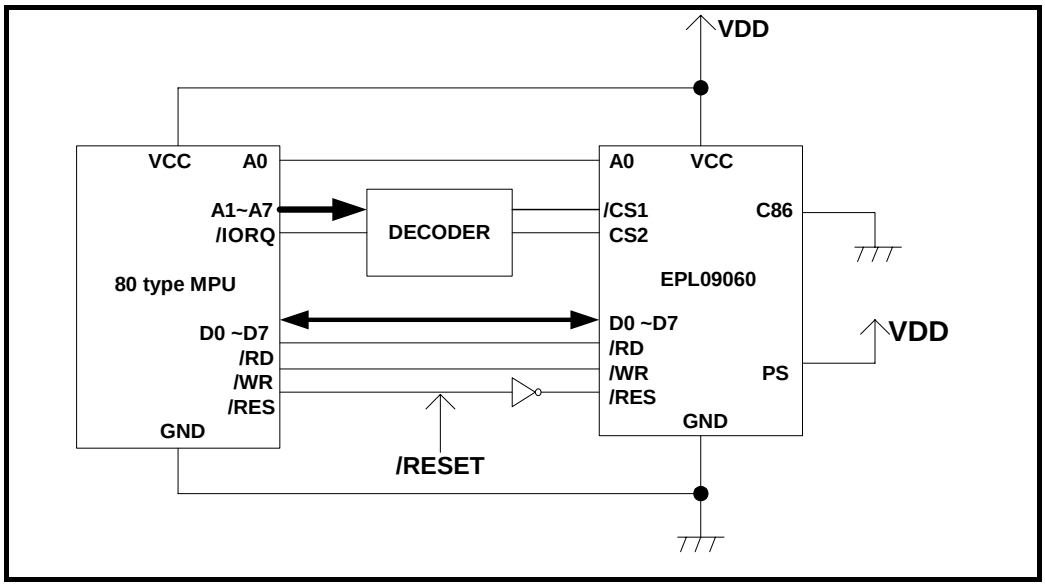
Elan 8-bit MPU (with external memory)



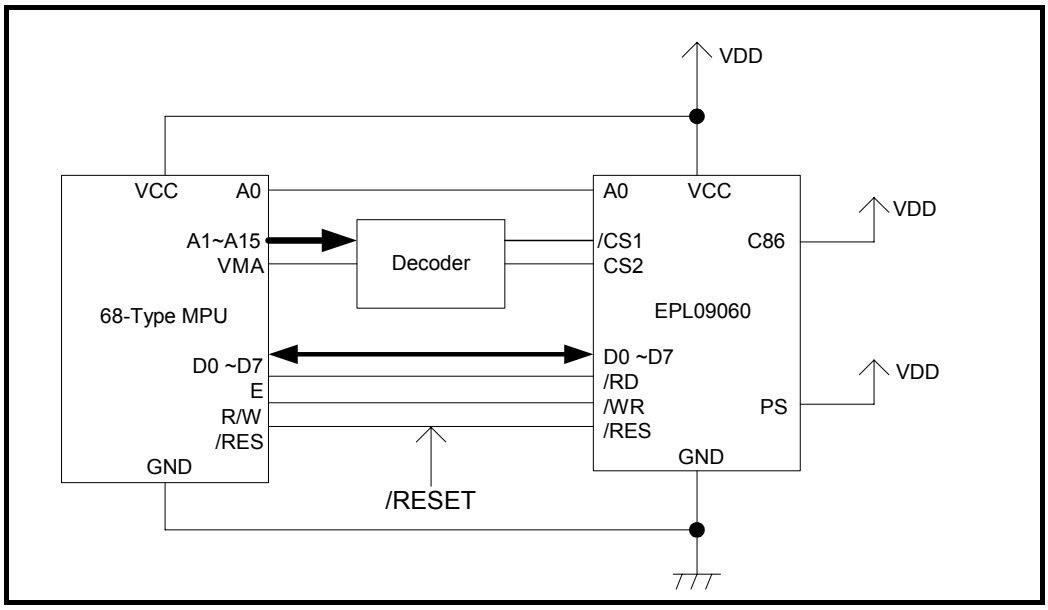
Serial Interface (SPI)



80-Family MPU



68-Family MPU



13 Application Circuit

For customer application circuit