EM65168

80 COM/SEG LCD Driver

Product Specification

DOC. VERSION 1.0

ELAN MICROELECTRONICS CORP.

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ELAN MICROELECTRONICS CORPORATION

Headquarters:

No. 12, Innovation Road 1
Hsinchu Science Park
Hsinchu, TAIWAN 30077
Tel: +886 3 563-9977
Fax:+886 3 563-9966
http://www.emc.com.tw

Hong Kong:

Elan (HK) Microelectronics Corporation, Ltd.

Rm. 1005B, 10/F Empire Centre
68 Mody Road, Tsimshatsui
Kowloon , HONG KONG
Tel: +852 2723-3376
Fax: +852 2723-7780
elanhk@emc.com.hk

USA:

Elan Information Technology Group (U.S.A.)

1821 Saratoga Ave., Suite 250
Saratoga, CA 95070
USA
Tel: +1 408 366-8225
Fax: +1 408 366-8220

Europe:

Elan Microelectronics Corp. (Europe)

Siewerdtstrasse 105
8050 Zurich, SWITZERLAND
Tel: +41 43 299-4060
Fax: +41 43 299-4079
http://www.elan-europe.com

Shenzhen:

Elan Microelectronics Shenzhen, Ltd.

SSMEC Bldg., 3F, Gaoxin S. Ave.
Shenzhen Hi-Tech Industrial Park
Shenzhen, Guandong, CHINA
Tel: +86 755 2601-0565
Fax: +86 755 2601-0500

Shanghai:

Elan Microelectronics Shanghai, Ltd.

23/Bldg. #115 Lane 572, Bibo Road
Zhangjiang Hi-Tech Park
Shanghai, CHINA
Tel: +86 21 5080-3866
Fax: +86 21 5080-4600

Contents

Specification Revision History

Doc. Version	Revision Description	Date
0.1	Initial version	2002/12/23
0.2	1. Added Pin Configuration 2. Added COB bonding diagram	2003/03/28
0.3	Added BF, DON, HPM, and RES control registers	2003/03/31
0.4	1. Modified the DC characteristics 2. Modified the RF registers	2003/04/29
0.5	1. Modified EM65168 to EM65168/EM65168A. 2. Added compatibility feature of EM65168A and EM83040A on Section 2. 3. Added a Note about EM65168A control registers on the BF Register section. 4. Added the resistor value level limitation of Ra and Rb when using external resistor. 5. Added a Note on adding a capacitor across V1 and Vreg, and its recommended value.	2003/05/28
0.6	1. Modified the LCD waveform (Fig. 7-7). 2. Added a description for all COM/SEG voltage state when EN=1 on Section 6 Pin Description. 3. Added a Note about RAMW and RAMR after the DC Characteristics table on Section 9.	2003/09/17
0.7	Modified the IOH1 and IOL1 DC Characteristics values	2003/11/05
0.8	1. Modified the VEV values of REG [5:0] vs VEV table. 2. Modified the VEV and REG [5:0] setting values on Section 9, DC Characteristics.	2003/12/18
0.9	Added a Note about High Power Mode for large LCD panel, on the HPM Section	2004/04/29
1.0	1. Added C64 S256 Application Circuit 2. Added package	2006/04/26

1 General Description

The EM65168/EM65168A is a dot matrix, RAM mapping and multi-function LCD driver, implemented with low power, high speed CMOS technology. This device integrates an 80-bit shift register, 80-bit data latch and 80-bit level driver. An on-chip LCD RAM can be mapped to an LCD signal, converts RAM data to parallel data and output a waveform to an LCD.

2 Features

- Operating voltage: 2.5V~5.5V
- LCD driver voltage: 3.6V to 15V
- Internal RAM: 6,400 bits
- RAM can be controlled by eight signals including 4/8 bits bus
- Duty: 1/32, 1/48, 1/64, 1/80
- Built-in DC/DC converter: double, triple, quad and five times
- Modularized function: connect to another EM65168/EM65168A to extent LCD matrix
- One DC converter enabled and other EM65168/EM65168A can share with this
- Internal regulator output for DC/DC converter
- Bias Selectable: 1/5, 1/6, 1/7, 1/8, 1/9
- Internal RC clock: 24kHz
- CMOS process (P-type silicon substrate)
- EM65168A is compatible with EM83040A
- Package (Ordering information):

Part Number	Versions	Description	Package information
EM65168H	Bare chip	NA	Page 31
EM65168AH	Bare chip	NA	Page 31

Note: The EM65168 series has the following sub-codes, depending on their shapes.
H: Bare chip (Aluminum pad without bump) **GH**: Gold bumped chip
F: COF package **T**: TAB (TCP) package

3 Application

- Data Bank
- LCD leisure products
- Educational computer

4 Pin Configuration

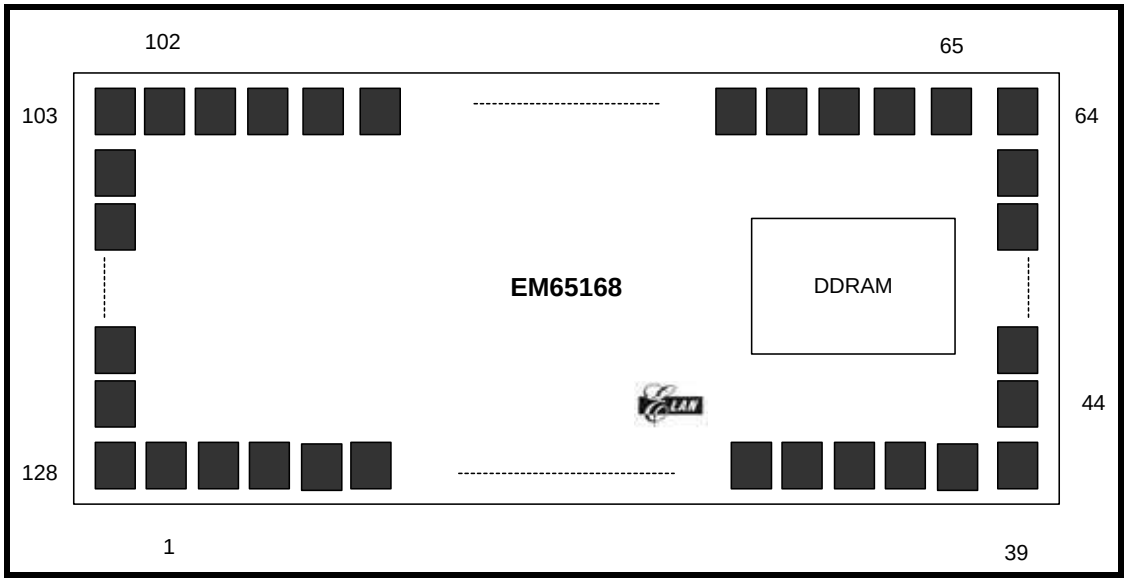


Figure 4-1 Pin Configuration

NOTE
With the Elan logo in the center (as shown figure) and DDRAM (black color) on the right side the pin 1 is in the down left corner.

Pin Dimensions

Item	Pad No.	Size		Unit
		X	Y	
Chip size	-	4260	2150	µm
Pad size (min.)	-	85	90	
Pad pitch (min.)	100			
Coordinate Origin	Chip center			

Pad Coordinates (Total of 114 pins)

Pin No	Pad Name	Coordinate (X, Y)	Pin No	Pad Name	Coordinate (X, Y)
1	GND	-1880.0 , -948.8	36	O18	1660.0 , -948.8
2	CA	-1770.0 , -948.8	37	O19	1770.0 , -948.8
3	VSS2+	-1660.0 , -948.8	38	O20	1880.0 , -948.8
4	VSS2-	-1555.0 , -948.8	39	O21	2003.8 , -948.8
5	V2	-1450.0 , -948.8	40	-	-
6	V3	-1350.0 , -948.8	41	-	-
7	VREG	-1250.0 , -948.8	42	-	-
8	V1	-1150.0 , -948.8	43	-	-
9	V4	-1050.0 , -948.8	44	O26	2003.8 , -825.0
10	V5	-950.0 , -948.8	45	O27	2003.8 , -715.0
11	O1	-850.0 , -948.8	46	O28	2003.8 , -605.0
12	VOUT	-750.0 , -948.8	47	O29	2003.8 , -500.0
13	O2	-650.0 , -948.8	48	O30	2003.8 , -400.0
14	VSS4	-550.0 , -948.8	49	O31	2003.8 , -300.0
15	O3	-450.0 , -948.8	50	O32	2003.8 , -200.0
16	VSS3	-350.0 , -948.8	51	O33	2003.8 , -100.0
17	O4	-250.0 , -948.8	52	O34	2003.8 , 00.0
18	CB	-150.0 , -948.8	53	O35	2003.8 , 100.0
19	O5	-50.0 , -948.8	54	O36	2003.8 , 200.0
20	O6	50.0 , -948.8	55	O37	2003.8 , 300.0
21	O25	150.0 , -948.8	56	O38	2003.8 , 400.0
22	O7	250.0 , -948.8	57	O39	2003.8 , 500.0
23	O24	350.0 , -948.8	58	O40	2003.8 , 605.0
24	O8	450.0 , -948.8	59	O41	2003.8 , 715.0
25	O23	550.0 , -948.8	60	O42	2003.8 , 825.0
26	O9	650.0 , -948.8	61	-	-
27	O22	750.0 , -948.8	62	-	-
28	O10	850.0 , -948.8	63	-	-
29	O11	950.0 , -948.8	64	O47	2003.8 , 948.8
30	O12	1050.0 , -948.8	65	O48	1880.0 , 948.8
31	O13	1150.0 , -948.8	66	O49	1770.0 , 948.8
32	O14	1250.0 , -948.8	67	O50	1660.0 , 948.8
33	O15	1350.0 , -948.8	68	O51	1555.0 , 948.8
34	O16	1450.0 , -948.8	69	O52	1450.0 , 948.8
35	O17	1555.0 , -948.8	70	O53	1350.0 , 948.8

Pin No	Pad Name	Coordinate (X, Y)	Pin No	Pad Name	Coordinate (X, Y)
71	O54	1250.0 , 948.8	101	O76	-1770.0 , 948.8
72	O55	1150.0 , 948.8	102	MAIN	-1880.0 , 948.8
73	O56	1050.0 , 948.8	103	MD	-2003.8 , 948.8
74	O57	950.0 , 948.8	104	-	-
75	O58	850.0 , 948.8	105	-	-
76	O46	750.0 , 948.8	106	-	-
77	O59	650.0 , 948.8	107	M1	-2003.8 , 825.0
78	O45	550.0 , 948.8	108	M0	-2003.8 , 715.0
79	O60	450.0 , 948.8	109	EN	-2003.8 , 605.0
80	O44	350.0 , 948.8	110	RAMENB	-2003.8 , 500.0
81	O61	250.0 , 948.8	111	RAMADS	-2003.8 , 400.0
82	O43	150.0 , 948.8	112	RAMW	-2003.8 , 300.0
83	O62	50.0 , 948.8	113	RAMR	-2003.8 , 200.0
84	O63	-50.0 , 948.8	114	RAMD7	-2003.8 , 100.0
85	O80	-150.0 , 948.8	115	RAMD6	-2003.8 , 00.0
86	O64	-250.0 , 948.8	116	RAMD5	-2003.8 , -100.0
87	O79	-350.0 , 948.8	117	RAMD4	-2003.8 , -200.0
88	O65	-450.0 , 948.8	118	RAMD3	-2003.8 , -300.0
89	O78	-550.0 , 948.8	119	RAMD2	-2003.8 , -400.0
90	O66	-650.0 , 948.8	120	RAMD1	-2003.8 , -500.0
91	O77	-750.0 , 948.8	121	RAMD0	-2003.8 , -607.5
92	O67	-850.0 , 948.8	122	VDD	-2003.8 , -715.0
93	O68	-950.0 , 948.8	123	LOAD	-2003.8 , -825.0
94	O69	-1050.0 , 948.8	124	-	-
95	O70	-1150.0 , 948.8	125	-	-
96	O71	-1250.0 , 948.8	126	-	-
97	O72	-1350.0 , 948.8	127	-	-
98	O73	-1450.0 , 948.8	128	FR	-2003.8 , -948.8
99	O74	-1555.0 , 948.8			
100	O75	-1660.0 , 948.8			

Note: For PCB Layout, the IC substrate must be connected to GND.

5 Block Diagram

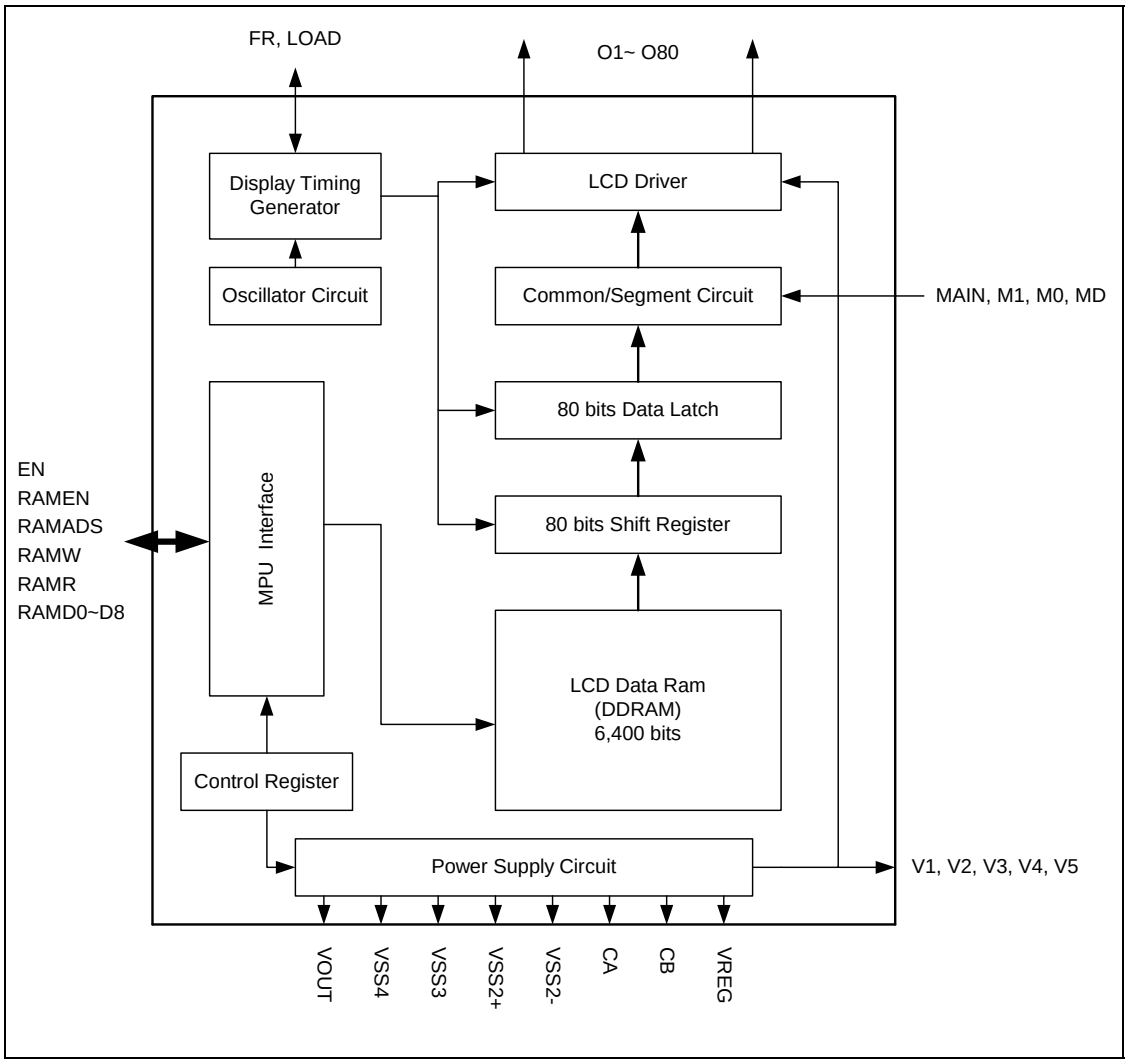


Fig 5-1 Block Diagram

6 Pin Description

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No of Pins</th></tr>
<tr><td>VDD</td><td>-</td><td>System power supply</td><td>1</td></tr>
<tr><td>GND</td><td>-</td><td>Ground</td><td>1</td></tr>
<tr><td>VOUT</td><td>-</td><td>Voltage converter input/output pin
Connect this pin to GND through capacitor
EN=1, VOUT=VDD-Vt</td><td>1</td></tr>
<tr><td>VSS4</td><td>-</td><td>Step-up capacitor</td><td>1</td></tr>
<tr><td>VSS3</td><td>-</td><td>Step-up capacitor</td><td>1</td></tr>
<tr><td>VSS2+</td><td>-</td><td>Step-up capacitor</td><td>1</td></tr>
<tr><td>VSS2-</td><td>-</td><td>Step-up capacitor</td><td>1</td></tr>
<tr><td>VREG</td><td>-</td><td>Output voltage regulator terminal. Provides the voltage between V1 and GND through a resistive voltage divider.</td><td>1</td></tr>
<tr><td>MAIN</td><td>I</td><td>Master or slave control signal.
MAIN=1, master unit
MAIN=0, slave unit</td><td>1</td></tr>
<tr><td>EN</td><td>I</td><td>This pin controls the whole chip's power. This IC works when this pin is connected to ground, otherwise the device is ddisable when connect to VDD.
EN=0 and MAIN=1 the chip will generate VSS2+, VSS2-VSS3, VSS4, VOUT, LOAD, FR signal and internal RC clock.
EN=1, standby mode (all COM/SEG output to GND level)</td><td>1</td></tr>
<tr><td>MD</td><td>I</td><td>MD=0: 4-bit bus mode, the RAMD3~RAMD0 is valid, RAMD7~DAMD4 must be connected to VDD or GND level
MD=1: 8-bit bus mode, the RAMD7~RAMD0 is valid</td><td>1</td></tr>
<tr><td>M1</td><td>I</td><td>Mode select</td><td>1</td></tr>
<tr><td>M0</td><td>I</td><td>Mode select</td><td>1</td></tr>
<tr><td>RAMEN</td><td>I</td><td>RAM read and write control signal.
0 : can read and write
1 : cannot read and write</td><td>1</td></tr>
<tr><td>RAMADS</td><td>I</td><td>RAM bus (RAMD [7:0]) select signal
0 : RAM Address bus
1 : RAM Data bus</td><td>1</td></tr>
<tr><td>RAMW</td><td>I</td><td>RAM write signal, low active</td><td>1</td></tr>
<tr><td>RAMR</td><td>I</td><td>RAM read signal, low active
<table>
<tr><th>RAMW</th><th>1</th><th>1</th><th>0</th><th>0</th></tr>
<tr><td>RAMR</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>RAMD[7:0]</td><td>Tri-state</td><td>Output</td><td>Input</td><td>Tri-state</td></tr>
</table></td><td>1</td></tr>
</table>

Pin Name	I/O	Function	No of Pins
RAMD [7:0]	I/O	RAM data or address bus For 4-bit bus mode, RAMD [3:0] is valid and RAMD [7:4] is not used, it must be connected to VDD or VSS level. For 8-bit bus mode, RAMD [7:0] is valid.	8
LOAD	I/O	LCD load signal between one common signal to another. MAIN=1: master outputs a LOAD signal MAIN=0: slave accepst the signal from the master	1
FR	I/O	Liquid crystal alternating current signal I/O terminal. MAIN=1: master unit outputs an FR signal MAIN=0: slave accepts the signal from the master	1
CA	I	Step-up capacitor	1
CB	I	Step-up capacitor	1
V1~V5	I	Reference voltage input, V1≧V2≧V3≧V4≧V5	5
O1~O80	O	LCD waveform output	80

7 Function Description

■ Using MAIN pin to choose either master or slave

MAIN	Unit	Function
1	Master	Generate these signals: FR, LOAD, V1, V2, V3, V4, V5 Internal RC clock
0	Slave	Accept these Master signals: FR, LOAD, V1, V2, V3, V4, V5 No internal RC clock

■ Using M1, M2 to choose four modes

Master	MAIN	M1	M0	Segment	Common	Bias
Mode 1	1	0	0	O (16:1) = S (16:1)	O (80:17) = C (64:1)	1/9
Mode 2	1	0	1	-	O (80:1) = C (80:1)	1/9
Mode 3	1	1	0	O (32:1) = S (32:1)	O (80:33) = C (48:1)	1/7
Mode 4	1	1	1	O (48:1) = S (48:1)	O (80:49) = C (32:1)	1/5
Slave	**MAIN**	**M1**	**M0**	**Segment**	**Common**	**Bias**
Mode 1	0	0	0	O (80:1) = S (80:1)	-	1/9
Mode 2	0	0	1	O (80:1) = S (80:1)	-	1/9
Mode 3	0	1	0	O (80:1) = S (80:1)	-	1/7
Mode 4	0	1	1	O (80:1) = S (80:1)	-	1/5

* S = Segment, C = Common, * (M1, M0) Master must be the same as the Slave

- Relationship between FOSC, LOAD and FR Frequency

MAIN	M1	M0	Description	f_{OSC}	LOAD	FR
1	0	0	64 common (1/64 duty)	24kHz	f_{OSC}/5=4.8K	LOAD/64=75.0 Hz
1	0	1	80 common (1/80 duty)	24kHz	f_{OSC}/4=6.0K	LOAD/80=75.0 Hz
1	1	0	48 common (1/48 duty)	24kHz	f_{OSC}/7=3.4K	LOAD/48=71.4 Hz
1	1	1	32 common (1/32 duty)	24kHz	f_{OSC}/10=2.4K	LOAD/32=75.0 Hz

- RAM Control

The LCD RAM can be read or written via control signal. When #RAMEN pin is at low state, the RAM can be read or written in data. The RAMADS can be set as RAMD [7:4] to be used as address bus or data bus. When it is used as Address and in 4-bit mode, the #RAMEN pin should remain low and user needs to set three times Address as RAMD [3:0] by following the Address setting sequence: Address [11:8] (a11, a10, a9, a8), Address [7:4] (a7, a6, a5, a4), and Address [3:0] (a3, a2, a1. a0). If the Address bus is in 8-bit mode, user needs to set two times Address as RAMD [7:0] by following the Address setting sequence: Address [10:8] (x, x, x, x, x, a10, a9, a8), Address [7:0] (a7, a6, a5, a4, a3, a2, a1. a0).

When it is used as Data bus, the #RAMEN pin is at high state, user can read or write a single data or continuously read or write multiple data. When reading or writing data to the RAM, the Address is incremented by 1, and once #RAMEN pin is at a high state, user cannot read or write to RAM.

7.1 LCD RAM Write Mode

4-bit Bus Mode

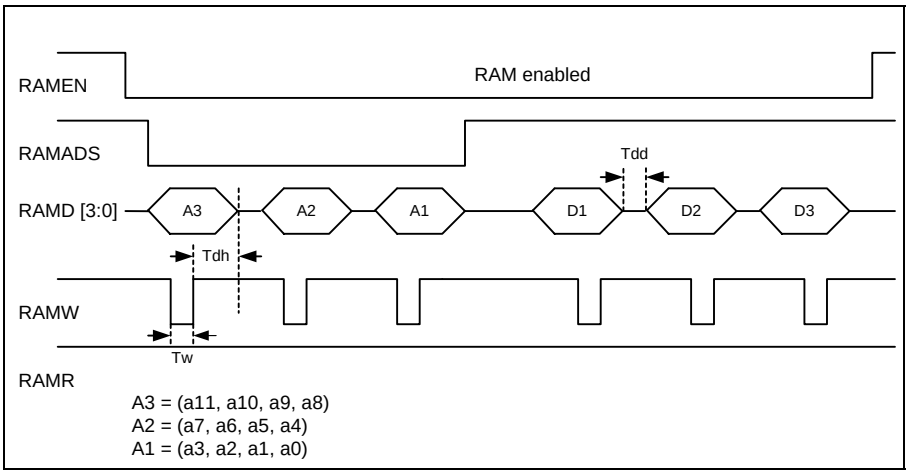


Fig 7-1 LCD RAM Write Mode for a 4-bit Bus

8-bit Bus Mode

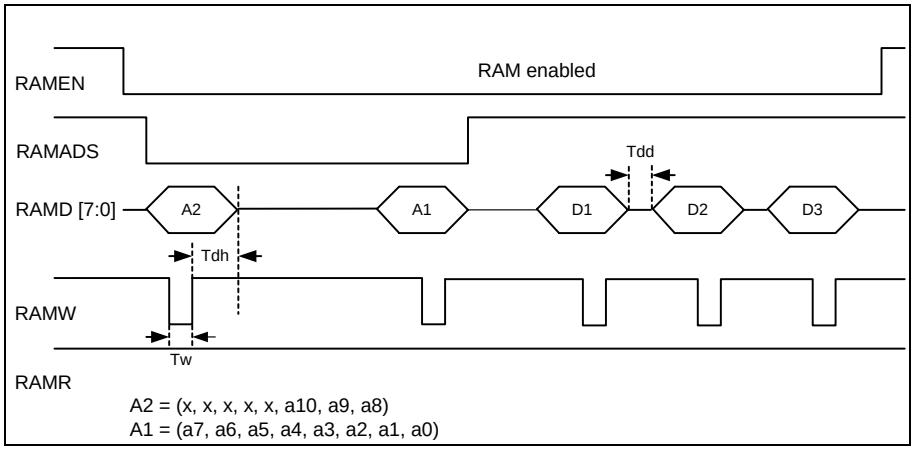


Fig 7-1 LCD RAM Write Mode for an 8-bit Bus

7.2 LCD RAM Read Mode

4-bit bus mode

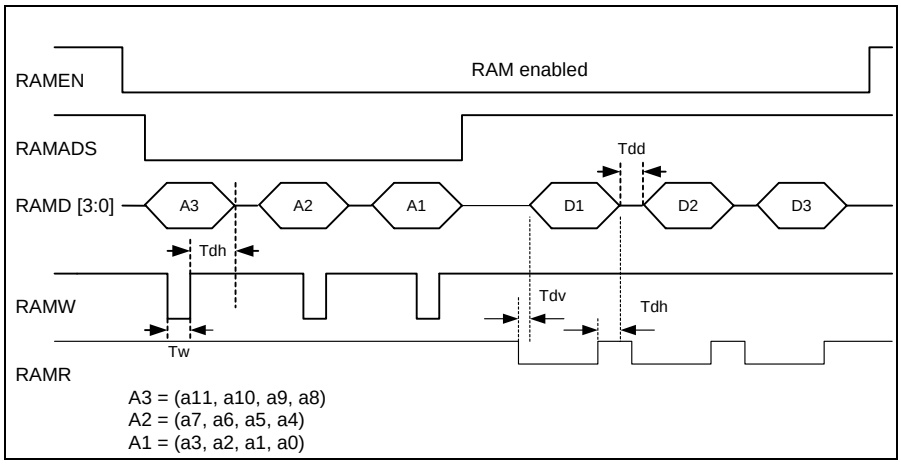


Fig 7-3 LCD RAM Read Mode for 4-bit Bus

8-bit bus mode

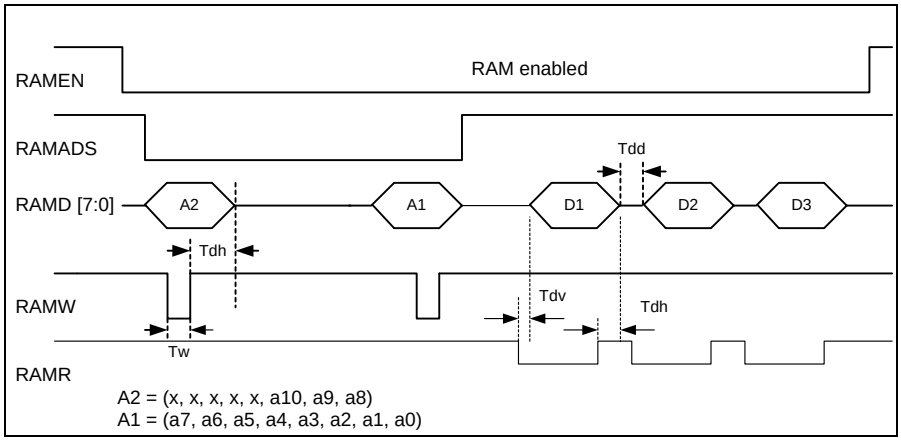


Fig 7-4 LCD RAM Read Mode for 8-bit Bus

- RAM Mapping

4-bit bus mode: RAM address is from 000H to address A05H, control register is from A00H to A05H

8-bit bus mode: RAM address is from 000H to address 503H, control register is from 500H to 502H

When user sets the LCD RAM to “1”, the LCD driver will generate a “light” waveform. Otherwise, it will generate a “dark” waveform. The LCD RAM area is mapped to Segment 1 ~ Segment 80. Refer to Fig 7-5, 7-6 and Table 1 to have idea on the LCD ram mapping. The other RAM (Area 11) is prohibited.

Table 1: LCD RAM Mapping Area

Master/Slave	Master Common No.	Segment No.	LCD Display Area
Master	32	48	1,2,3
Master	48	32	1,2,5,6
Master	64	16	1,5,8
Master	80	0	No RAM mapping
Slave	32	80	1, 2, 3, 4
Slave	48	80	1, 2, 3, 4, 5, 6, 7
Slave	64	80	1, 2, 3, 4, 5, 6, 7, 8, 9
Slave	80	80	1, 2, 3, 4, 5, 6, 7, 8, 9, 10
Any	Any	Any	Area 11 is prohibited

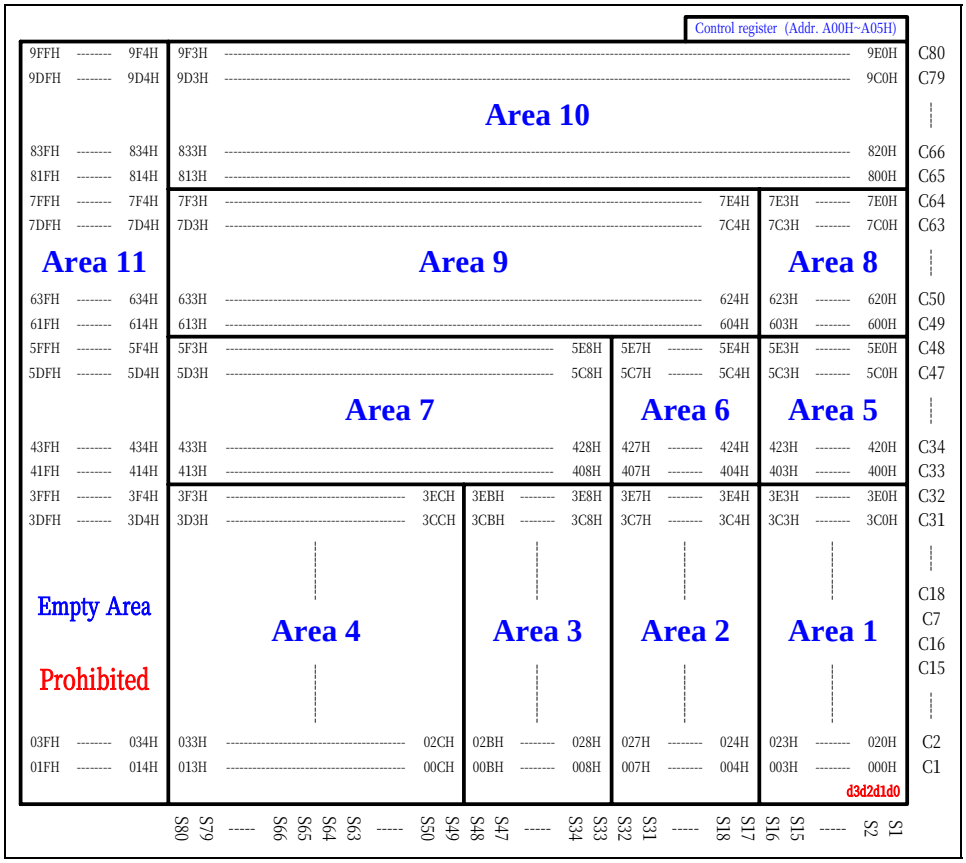


Fig 7-5 LCD Display RAM Mapping for 4 Bits Bus Mode

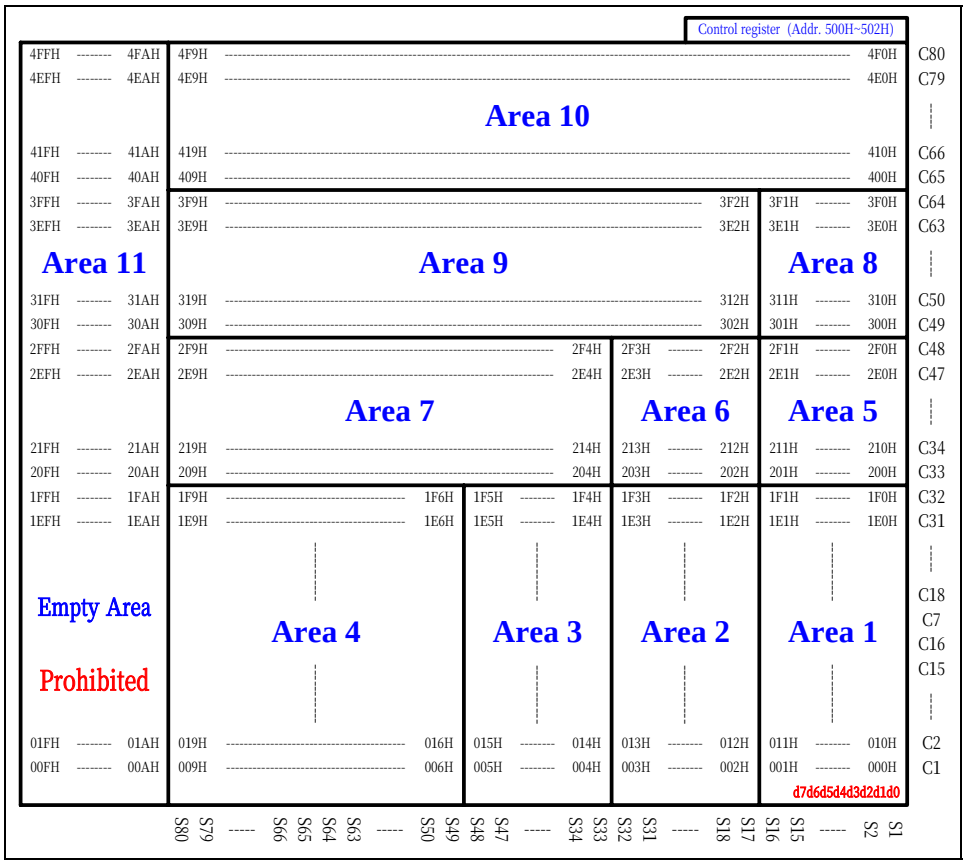


Fig 7-6 LCD Display RAM Mapping for 8 Bits Bus Mode

■ LCD Waveform

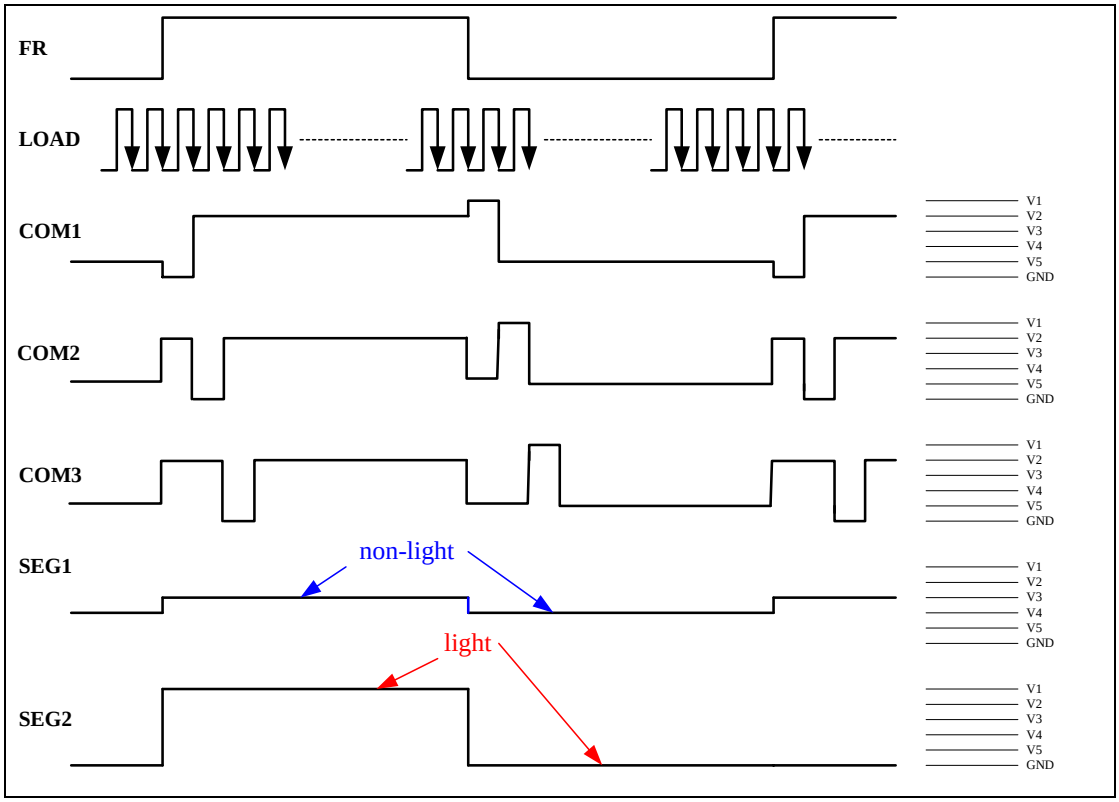


Fig 7-7 LCD Waveform

■ Control Register

4-bit mode data bus

Address	Bit 3	Bit 2	Bit 1	Bit 0	Initial State
A00H	REG3	REG2	REG1	REG0	0000 (0H)
A01H	PMS1	PMS0	REG5	REG4	0000 (0H)
A02H	IRS	IR2	IR1	IR0	0010 (2H)
A03H	BSE	BS2	BS1	BS0	0000 (0H)
A04H	X	DON	HPM	RES	0000 (0H)
A05H	BF	RF2	RF1	RF0	0000 (0H)

8-bit mode data bus

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial State
500H	PMS1	PMS0	REG5	REG4	REG3	REG2	REG1	REG0	00000000 (00H)
501H	BSE	BS2	BS1	BS0	IRS	IR2	IR1	IR0	00000010 (02H)
502H	BF	RF2	RF1	RF0	X	DON	HPM	RES	00000000 (00H)

Power supply circuit mode select (PMS1, PMS0)

User Settings	PMS1	PMS0	Step-up Circuit	V Regulator Circuit	V/F Circuit	External Voltage Input
Only the internal power supply is used	1	1	✓	✓	✓	×
Only the V regulator circuit and the V/F circuit are used	1	0	×	✓	✓	VOUT
Only the V/F circuit is used	0	1	×	×	✓	V1
Only the external power supply is used	0	0	×	×	×	V1 to V5

Note: "✓" = function is available if enabled "×" = function is Not available

Voltage Regulator Circuit, (REG5~REG0) is selected as the voltage of VEV

REG5	REG4	REG3	REG2	REG1	REG0	VEV	VEV Step
0	0	0	0	0	0	1.2 V	0.0127V
0	0	0	0	0	1	1.212 V	
↓						↓	
0	1	1	1	1	1	1.593 V	
1	0	0	0	0	0	1.606 V	
↓						↓	
1	1	1	1	1	0	1.987 V	
1	1	1	1	1	1	2.0 V	

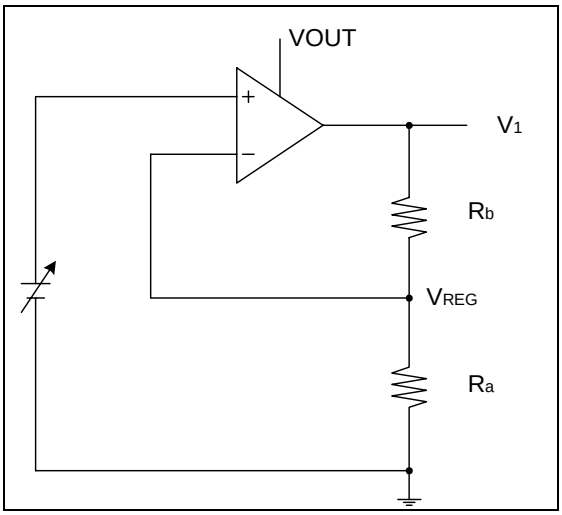


Fig. 7-8 a

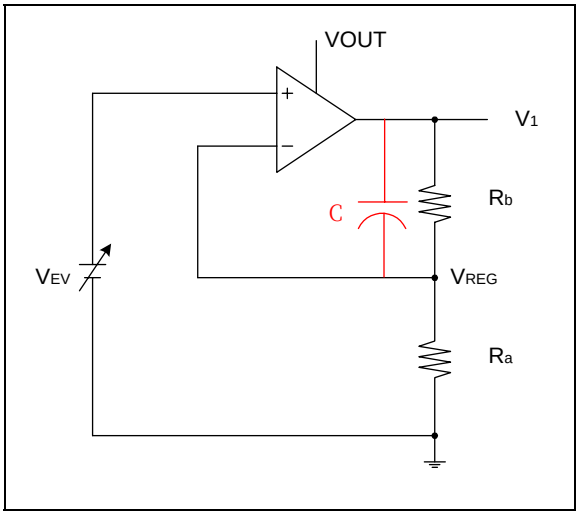


Fig. 7-8 b

The internal resistor select (IRS) and (IR2, IR1, IR0) are selected for the V1 voltage regulator internal resistance ratio.

IRS=0: internal regulator resistor is used.

IRS=1: internal regulator resistor is not used (external resistor is used)

IR2	IR1	IR0	Resistor Ratio (1+Rb/Ra)
0	0	0	3.0
0	0	1	3.5
0	1	0	4.0
0	1	1	4.5
1	0	0	5.0
1	0	1	5.5
1	1	0	6.0
1	1	1	6.5

The V1 voltage can be calculated using equation A within the range where **VDD<V1≦VOUT**

$$V1=\left(\frac{1+Rb}{Ra}\right)\times V_{EV}*(97\sim 103\%)$$ Equation A

Example: Default: IRS=0 (internal regulator resistor is used), (IR2, IR1, IR0) = (0, 1, 0), and (REG5~0) = (000000)

$$V1=\left(\frac{1+Rb}{Ra}\right)\times V_{EV}*(0.97\sim 1.03)=4.0\times 1.2*(0.97\sim 1.03)=4.656V\sim 4.944V$$

When IRS=0 (internal regulator resistor is used), (IR2, IR1, IR0) = (0, 1, 1), and (REG5~0) = (100000)

$$V1=\left(\frac{1+Rb}{Ra}\right)\times V_{EV}*(0.97\sim 1.03)=4.5\times 1.606*(0.97\sim 1.03)=7.01V\sim 7.44V$$

The output voltage of V1 is determined by function of the V1 voltage regulator ratio register (1+Rb/Ra), and the electric volume resistor (REG5~REG0).

Note: When external resistor is used (Fig 7-8 b),

1. **Ra and Rb values must to be in MΩ level. For example, if the desired value of (1+Rb/Ra) is 3.0, we give Ra=1 MΩ and Rb=2 MΩ.**
2. **Add a capacitor across V1 and Vreg, and the recommended value of C is 10nF~100nF.**

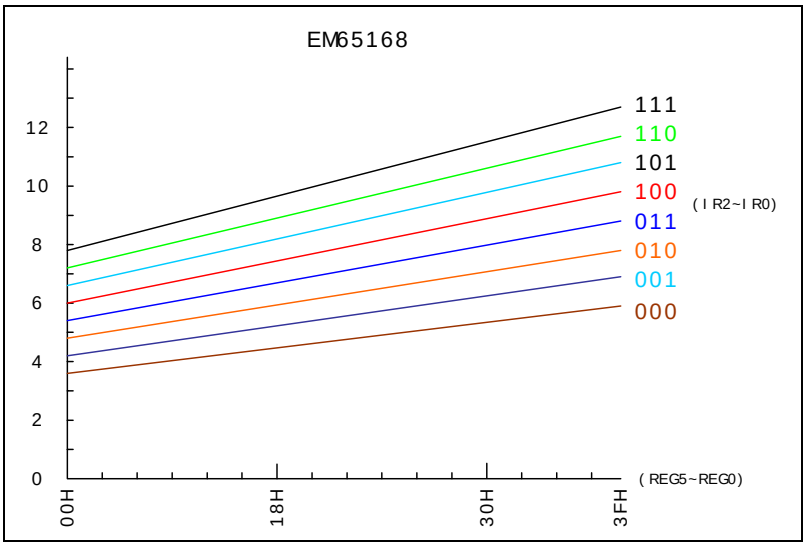


Fig 7-9 Output Voltage Curve of V1

LCD Bias set

BSE=0: LCD bias is not selectable

M1	M0	Bias
0	0	1/9
0	1	1/9
1	0	1/7
1	1	1/5

BSE=1: LCD bias is selectable by setting BS2, BS1, BS0

BS2	BS1	BS0	Bias
0	0	0	1/5
0	0	1	1/6
0	1	0	1/7
0	1	1	1/8
1	0	0	1/9
1	0	1	Prohibit (1/9)
1	1	0	Prohibit (1/9)
1	1	1	Prohibit (1/9)

RES

The internal circuit can be initialized. This register, which is a read-only bit, is effective only in Master operation mode.

RES = "**0**" : Normal operation

RES = "**1**" : Initialization is ON

When the reset operation begins internally after RES register is set to "1", the RES register is automatically cleared to "0".

[Caution: It is necessary to wait for more than 20 ms after setting the RES bit]

HPM

The HPM register is the power control for the power supply circuit for liquid crystal drive.

HPM = "**0**" : Normal mode

HPM = "**1**" : High power mode

NOTE

For large LCD panel (heavy loading), use high power mode and add one resistor (100~200 KΩ) between Pin V4 and Pin VSS.

DON

The DON register controls the turning on/off of the LCD display.

DON= "**0**" : Display OFF (All COM/SEG output GND level)

DON= "**1**" : Display ON

The RF registers (RF2, RF1, RF0) can control the resistance ratio of the RC oscillator. Hence, the frame frequency can change the RF registers setting.

RF2	RF1	RF0	Operation
0	0	0	Initial resistance ratio
0	0	1	1.2 times initial resistance ratio
0	1	0	0.9 times initial resistance ratio
0	1	1	Initial resistance ratio
1	0	0	0.8 times initial resistance ratio
1	0	1	Initial resistance ratio
1	1	0	1.1 times initial resistance ratio
1	1	1	Initial resistance ratio

BF

The BF register controls the operating frequency of the booster.

BF	Operating Clock Frequency in the Booster
0	1.5kHz × 4
1	1.5kHz

NOTE

IF the Step-up capacitor (C2 as shown in Fig. 12) is less than 1 µF, the BF control register must be set to "0".

Note that the EM65168A has fixed some control bits of the Control Register, so those original user using EM83040A can use external resistor and set V_{EV}=1.56V, to get

$$V_1 = (1 + \frac{Rb'}{Ra'}) \cdot V_{EV} = 1.56 \cdot (1 + \frac{Rb'}{Ra'})$$

by adding external resistors, Ra', Rb', but Ra' and Rb' values must to be MΩ level; the fixed control bits are shown below:

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Fixed Bits
500H	PMS1	PMS0	REG5	REG4	REG3	REG2	REG1	REG0	11011110
501H	BSE	BS2	BS1	BS0	IRS	IR2	IR1	IR0	0xxx1xxx
502H	BF	RF2	RF1	RF0	X	DON	HPM	RES	0000x100

NOTE

- *The control register (500H) is fixed at 11011110*
- *The BSE bit is fixed at 0, and the IRS bit is fixed at 1*
- *The control register (502H) is fixed at 0000x100*

■ Step-up Voltage Circuit

Placing capacitor C2 in different configurations and across VOUT and VSS boosts the voltage coming from VDD and VSS n-times and outputs the boosted voltage to VOUT pin.

(a) Double step-up, (b) Triple step-up, (c) Quad step-up (d) five times step-up

C1=0.47 to 3.3μf, C2=0.1 to 2.2μf

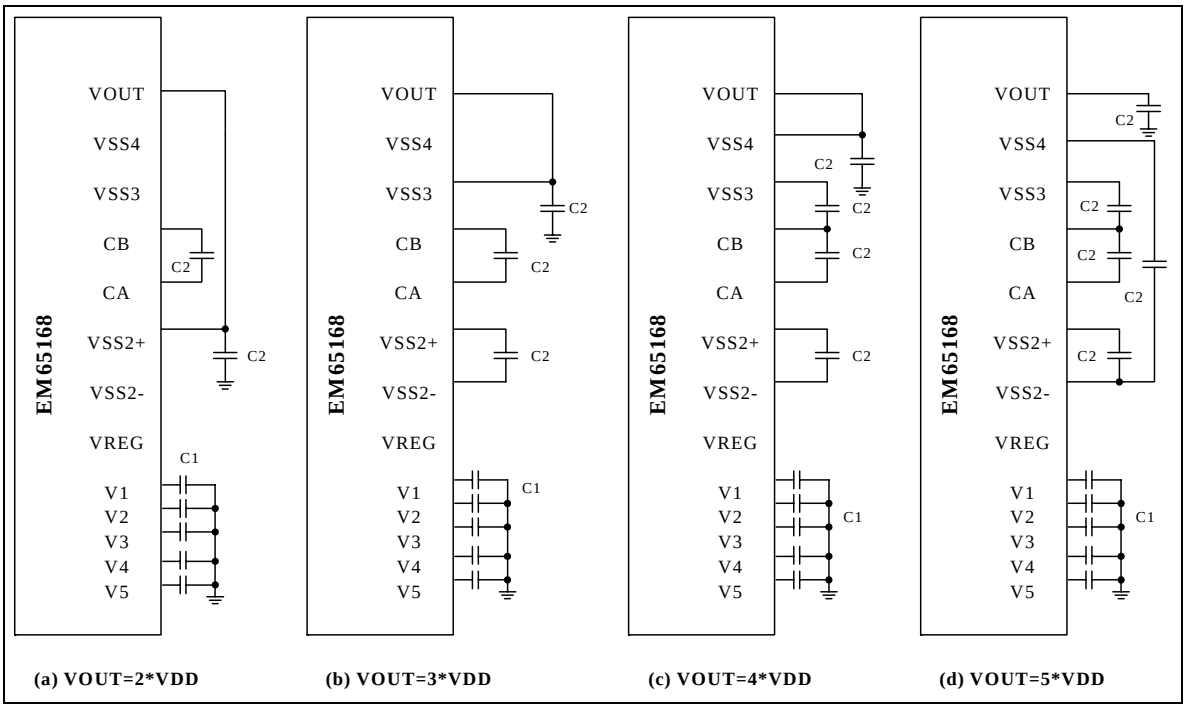


Fig 7-10 Step-up Voltage Circuit

■ Reference circuit examples, as shown in Fig 7-11

a. Only the internal power supply is used, control register (PS1, PS0, IRS) = (1, 1, 0)

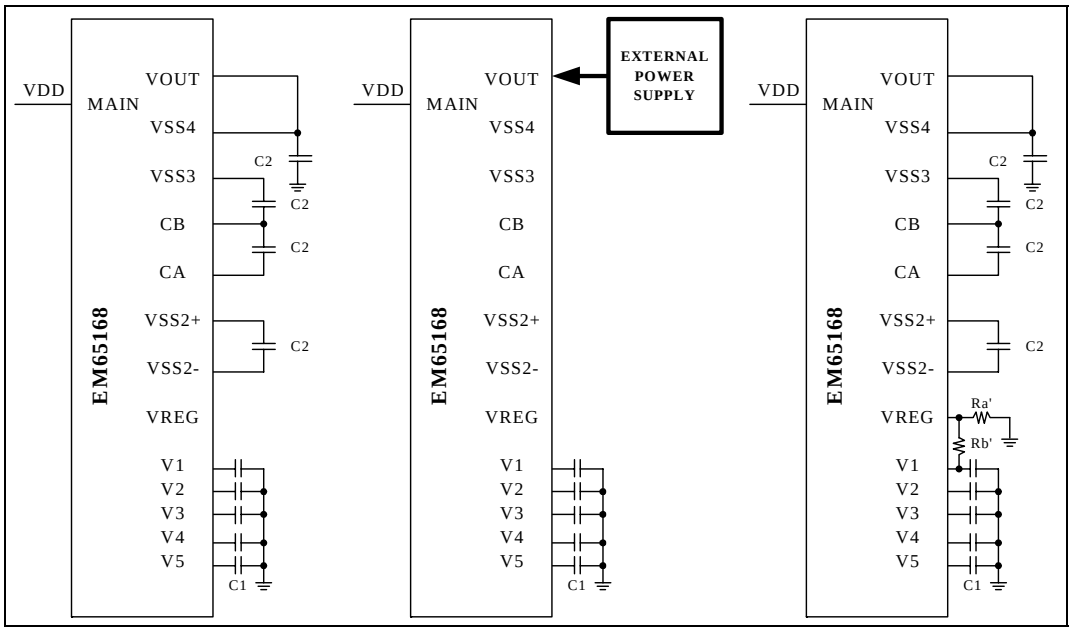
b. Only the V regulator circuit and the V/F circuit are used, the control register (PS1, PS0, IRS) = (1,0,0)

c. Only the internal power supply is used, the control register (PS1, PS0, IRS) = (1, 1, 1). When internal regulator resistor is not used (external resistor is used), V1=VREG*(1+Rb'/Ra')

d. Only the V regulator circuit and the V/F circuit are used, the control register (PS1, PS0, IRS) = (1, 0, 1). When the internal regulator resistor is not used (external resistor is used), V1=VREG*(1+Rb'/Ra')

e. Only the V/F circuit is used, the control register (PS1, PS0) = (0, 1)

f. Only the external power supply is used, the control register (PS1, PS0) = (0, 0)



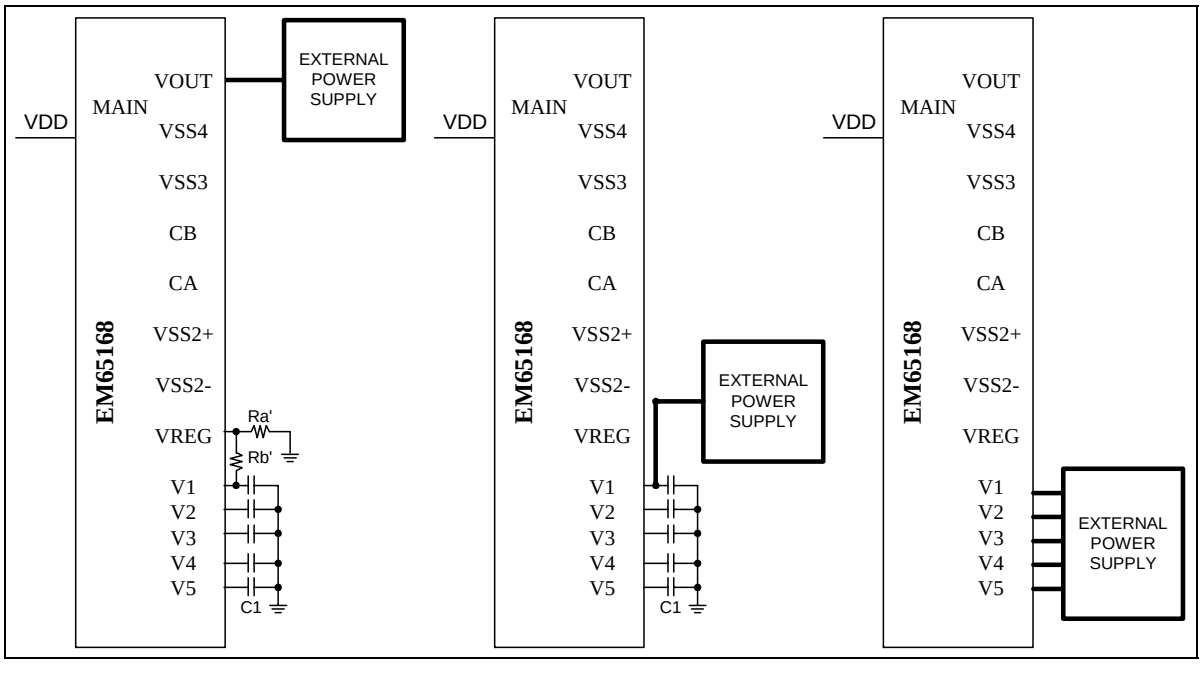


Fig 7-11 Reference Circuit Examples

8 Absolute Maximum Rating

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	< 6	V
Input Voltage	Vin	-0.5 TO Vdd +0.5	V
Operating Temperature Range	Ta	-30 TO 80	°C

9 DC Characteristics

Test condition: If not specified, Ta=25°C, VDD=3V, VSS=0V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VDD	Input voltage	With double step-up	2.5	-	5.5	V
		With triple step-up	2.5	-	5.5	
		With quad step-up	2.5	-	4.0	
		With five times step-up	2.5	-	3.3	
VIH	High level input voltage	[1]	0.8VDD	0.9VDD	VDD	V
VIL	Low level input voltage	[1]	0	0.1VDD	0.2VDD	V
IOH1	High level output current	VOH = VDD-0.4V [2]	-2.4	-3.2	-4.5	mA
IOL1	Low level output current	VOL= 0.4V [2]	2.4	3.2	4.5	mA
IOH2	High level output current	VOH = VDD-0.4V [3]	-0.8	-1.0	-1.2	mA
IOL2	Low level output current	VOL= 0.4V [3]	0.8	1.0	1.2	mA
ILI	Input leakage current	VI = VSS or VDD [4]	-2	0	2	µA
ILO	Output leakage current	VI = VSS or VDD [5]	-2	0	2	µA
Iop	Operating current	EN=0. MAIN =1 (MASTER), DC converter enable, Five times step-up, Display All On pattern (M1, M0)=(1, 1), V1=11V 24kHz clock, No load	-	110	160	µA
		EN=0. MAIN =1 (MASTER), DC converter enable, Three times step-up, Display All On pattern (M1, M0)=(1, 1), V1=11V 24kHz clock, No load	-	85	135	µA
Isb	Standby mode	EN=1	-	1	2	µA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VEV	Voltage variation of regulator	Ta=0°C; REG [5:0]=111111	0.97×VEV	TBD	1.03×VEV	V
		Ta=25°C; REG [5:0]=111111	1.94	2.0	2.06	V
		Ta=40°C; REG [5:0]=111111	0.97×VEV	TBD	1.03×VEV	V
VOUT	Step-up circuit output voltage	x2/x3/x4/x5 RL=500k (Step-up Capacitor =1 µF)	95	99	100	%
Cv	LCD voltage capacitor	V1, V2, V3, V4, V5	0.47	1	3.3	µF
Cs	Step-up capacitor	CA, CB, VSS2+, VSS2-, VSS3, VSS4	0.1	1	2.2	µF
fosc	Internal oscillator frequency	Ta=25°C	20	24	28	kHz
RON	LCD ON resistance	V1=9V, 1/9bias |ΔV|=0.5V	-	1.2	2	KΩ

Note: [1]: RAMD [7:0], MAIN, EN, M1, M0, RAMEN, RAMADS, RAMW, RAMR pins

[2]: RAMD [7:0] pins

[3]: FR, LOAD pins

[4]: MAIN, EN, M1, M0, RAMEN, RAMADS, RAMW, RAMR pins.

[5]: Applied when RAMD [7, 0], FR and LOAD pins are in a state of high impedance

10 AC Characteristics

Ta= -30°C ~ 80°C, VDD=3V, VSS=0V

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vrc	RC clock variable	-20	-	+20	%
Tframe	Frame period	1/60	1/75	1/90	S
Tw	Write low pulse	700	-	-	nS
Tdh	Data hold time	100	-	-	nS
Tdd	Data to data time	100	-	-	nS
Tdv	Data valid time	700	-	-	nS

11 AC Timing

4-bits data bus mode

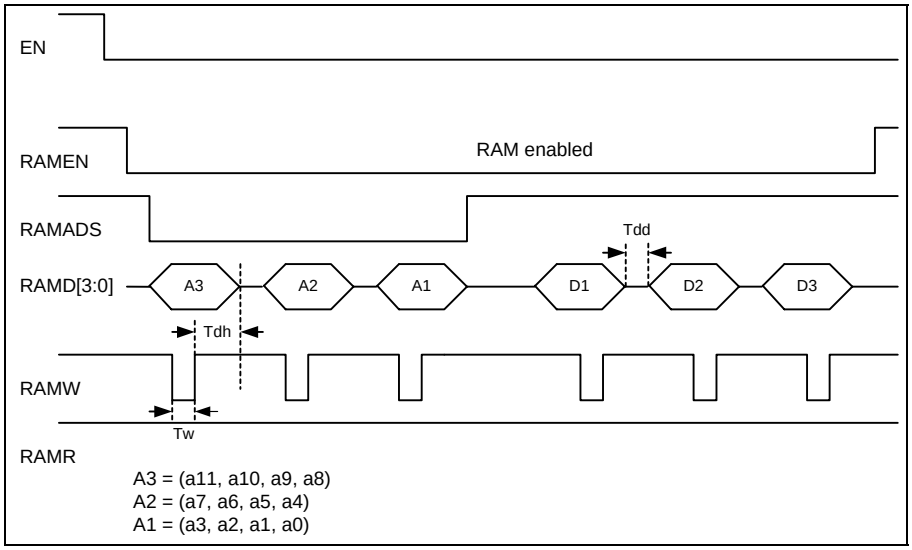


Fig 11-1 LCD RAM Write Mode

8-bits data bus mode

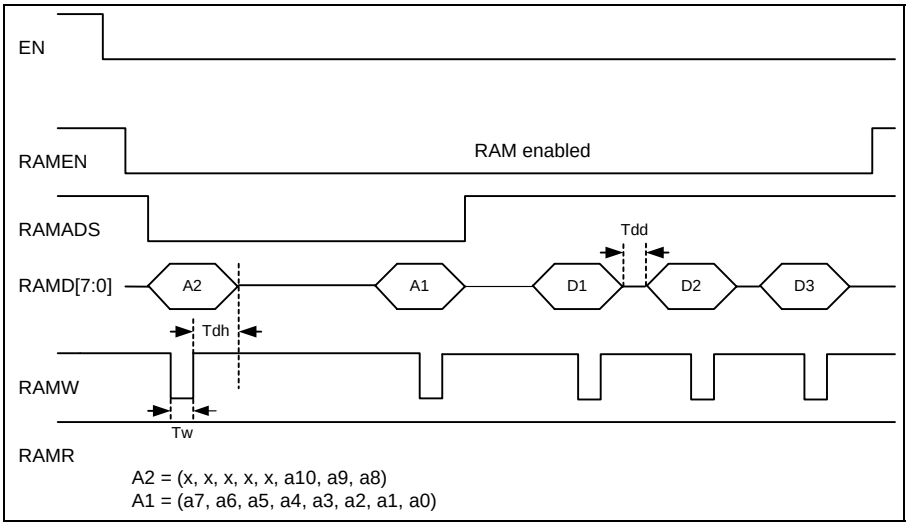


Fig 11-2 LCD RAM Write Mode

4-bits data bus mode

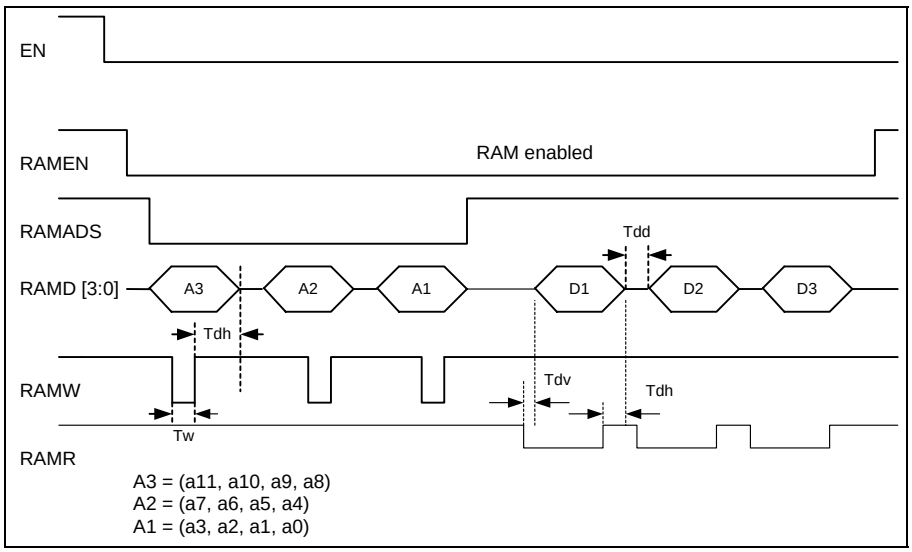


Fig 11-3 LCD RAM Read Mode

8-bits data bus mode

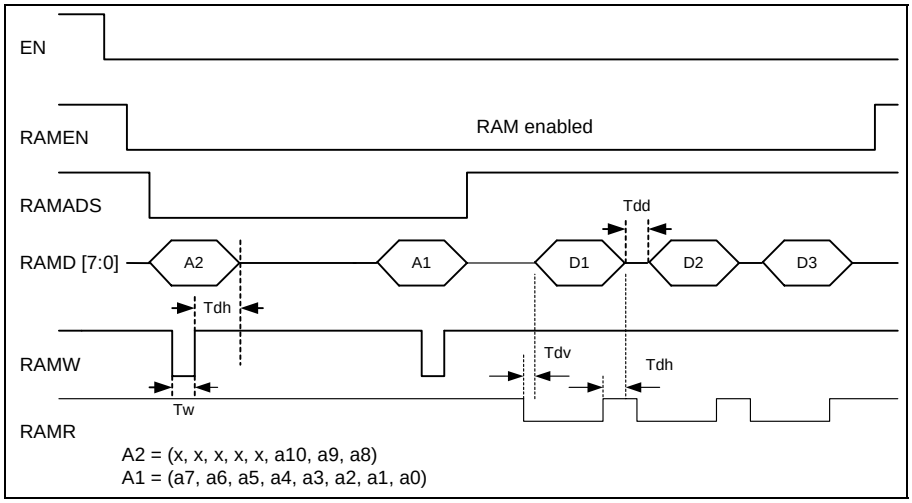


Fig 11-4 LCD RAM Read Mode

12 Application Circuit

- C32 x S48

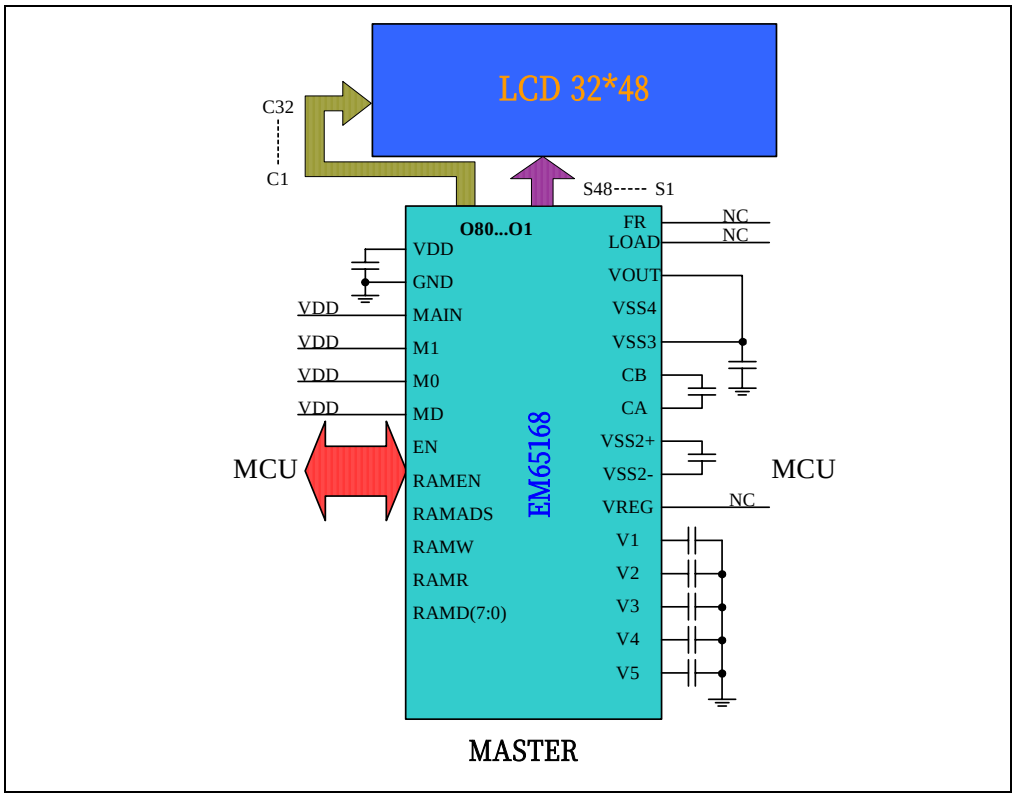


Fig 12-1 32 Common x 48 Segment Application Circuit

- C32 x S128

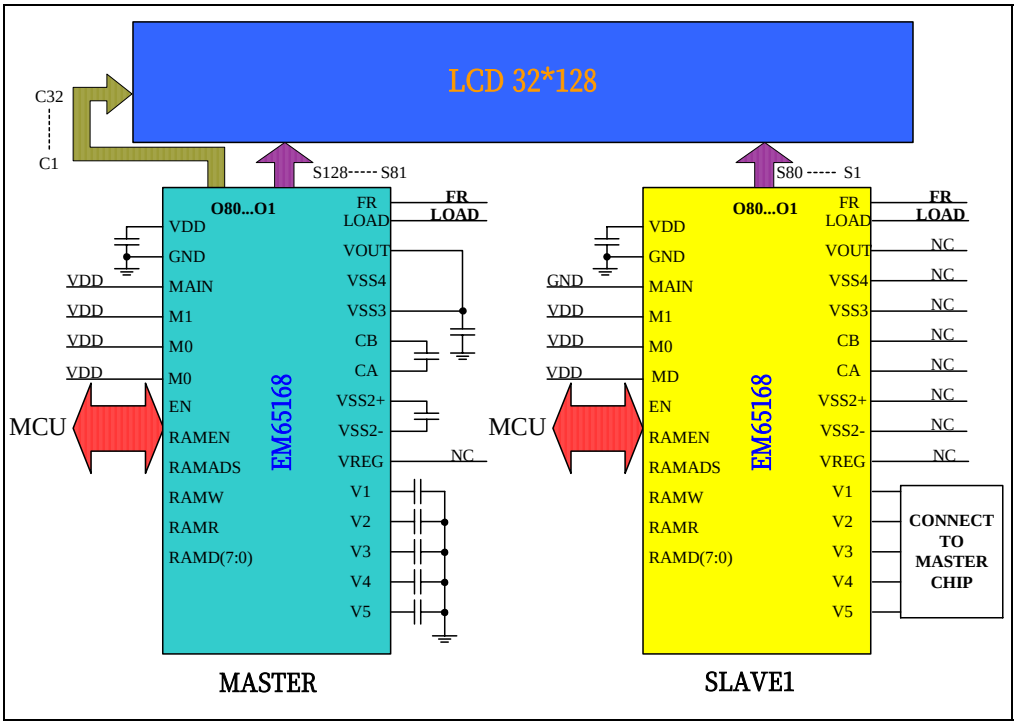


Fig 12-2 32 Common x 128 Segment Application Circuit

■ C48 x S112

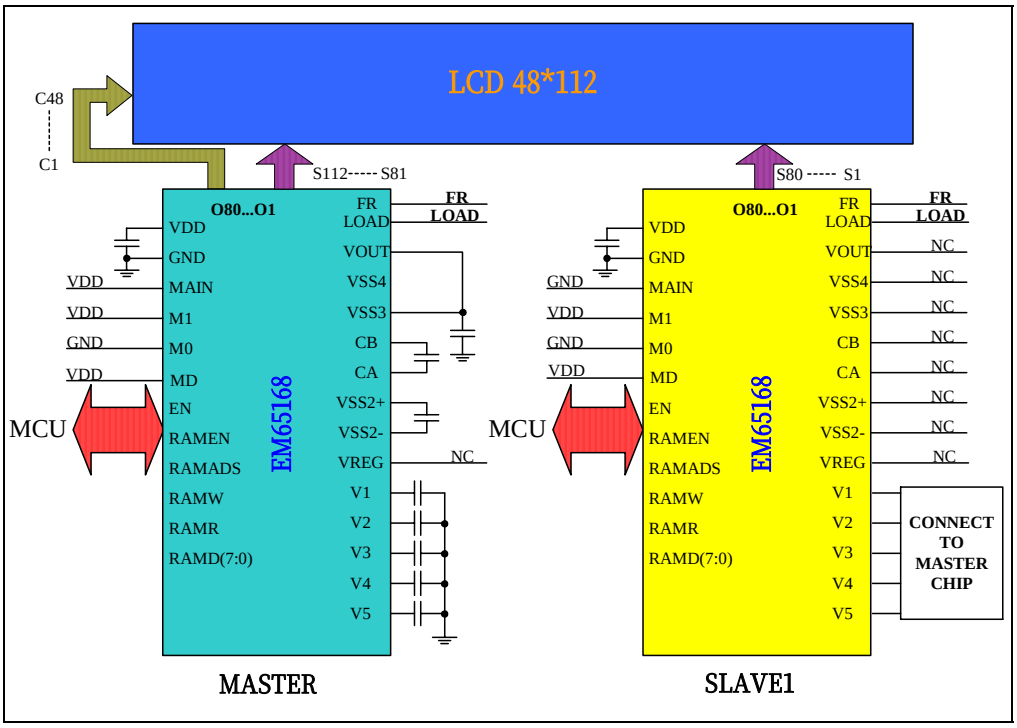


Fig 12-3 48 Common x 112 Segment Application Circuit

■ C64 x S96

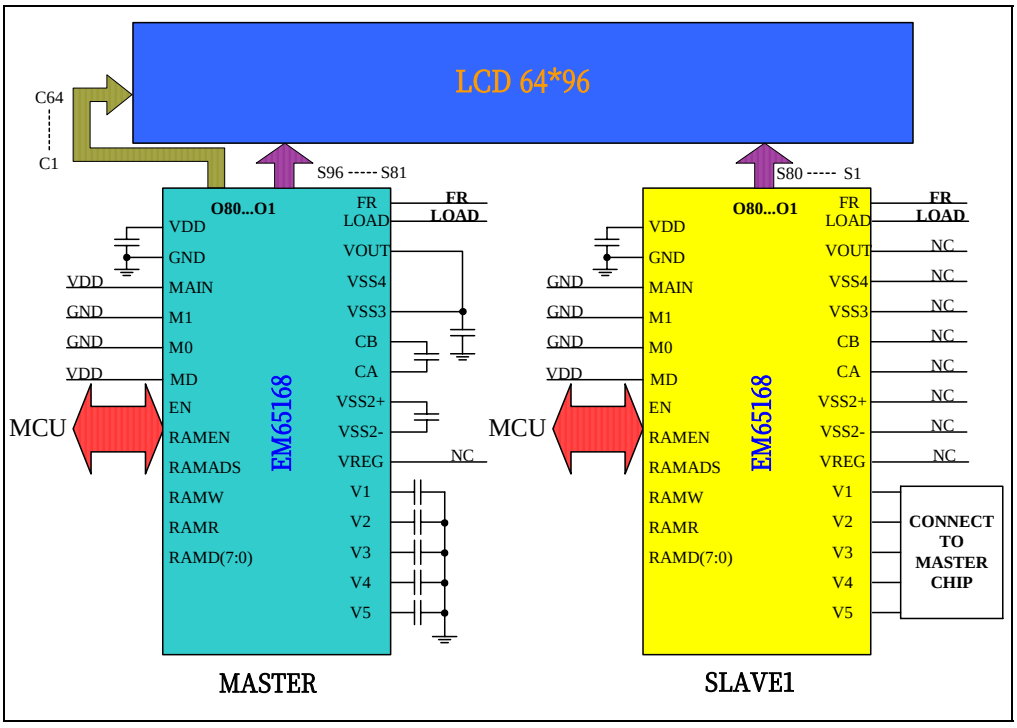


Fig 12-4 64 Common x 96 Segment Application Circuit

■ C80 x S160

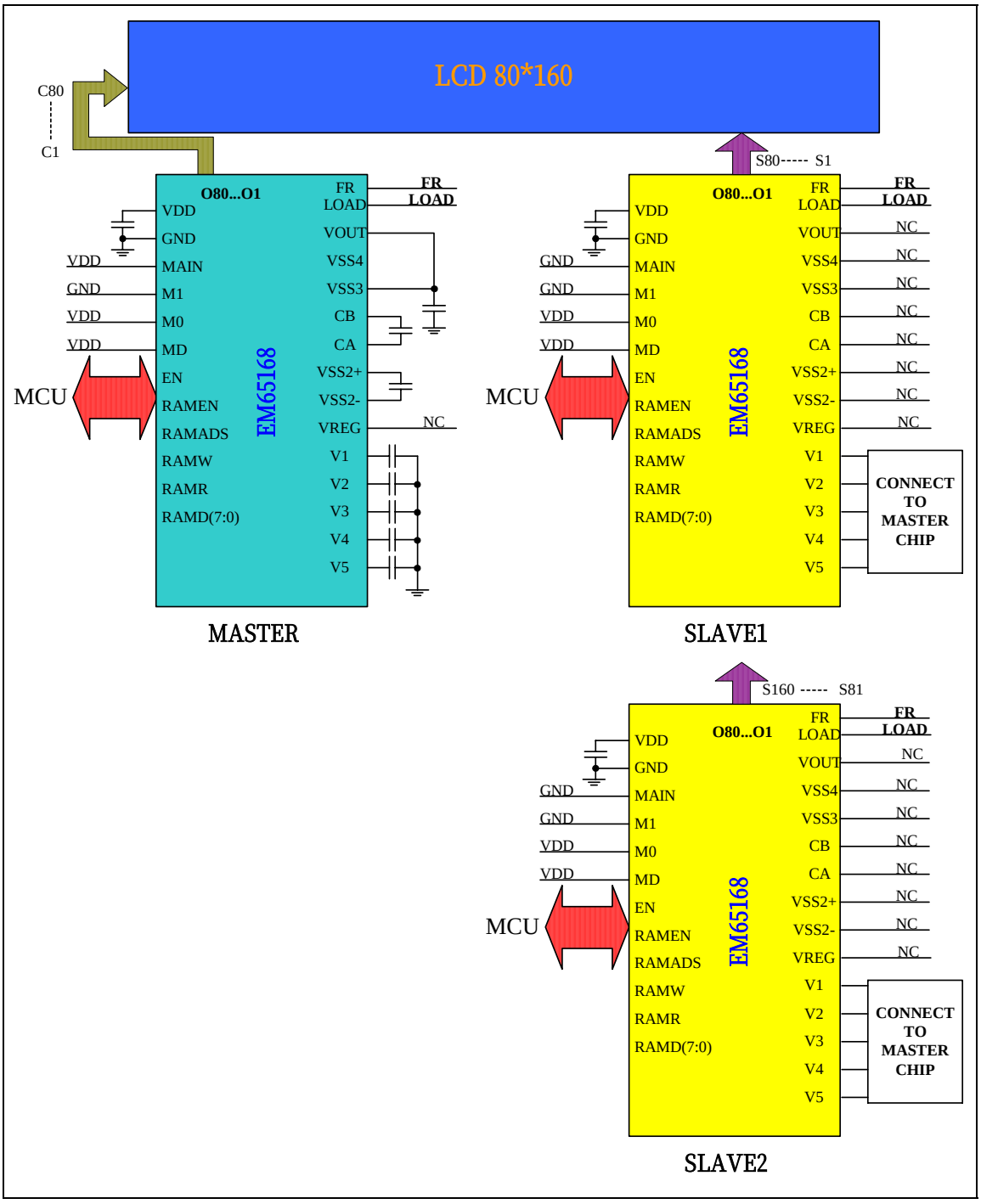


Fig 12-5 80 Common x 160 Segment Application Circuit

■ C64 x S256

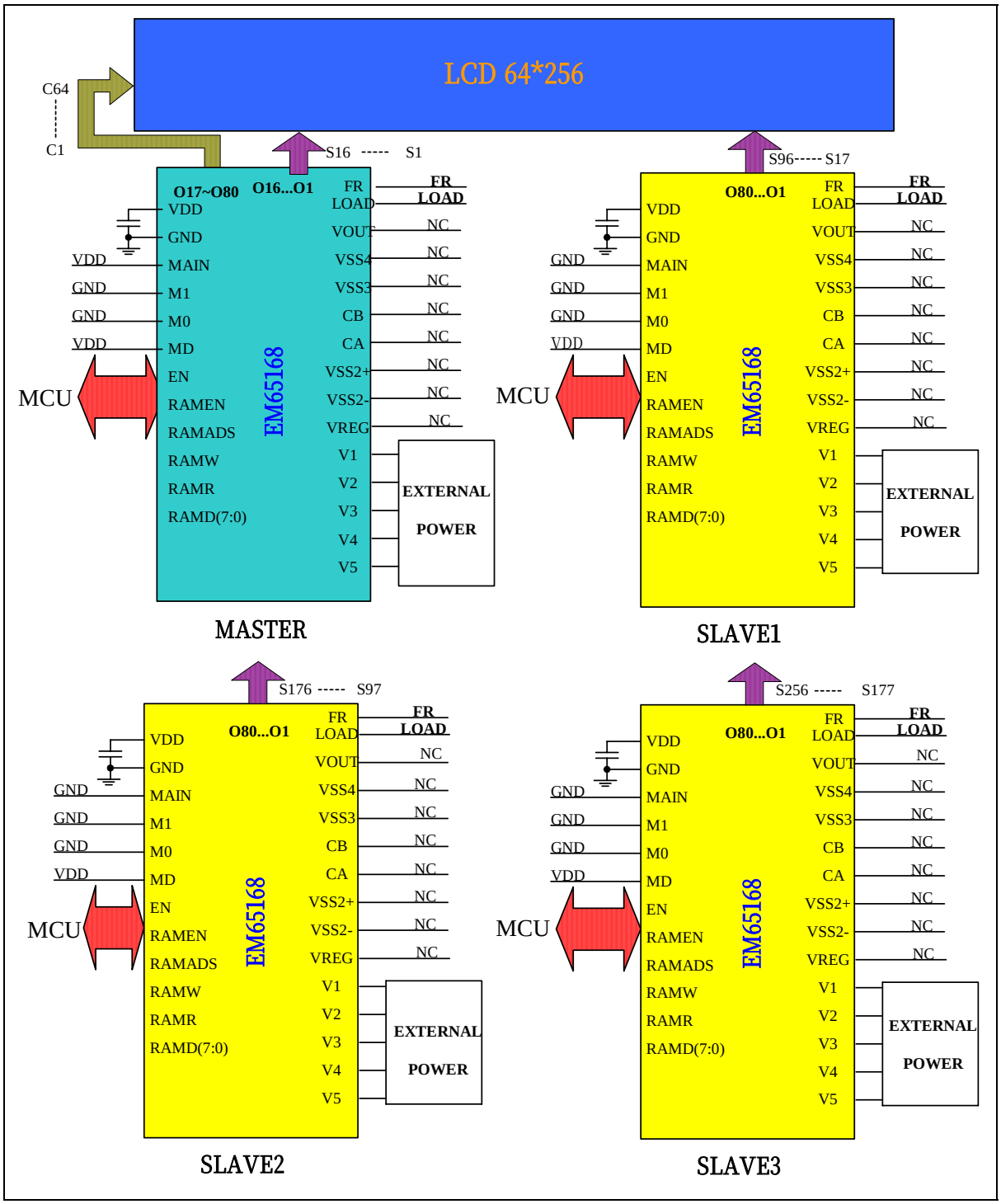


Fig 12-6 64 Common x 256 Segment Application Circuit

13 Package Information

EM65168/EM65168A COB Bonding Diagram

(It is recommended to use the following method to improve the bonding yield)