Elan Microelectronics Crop.

CONFIDENTIAL

EM65100

69COM/ 101SEG 4 Gray Level STN LCD Driver

March 08, 2005

Version 0.6

EM65100 Specification Revision History		
Version	**Content**	**Date**
0.1	Initial version	April 13, 2003
0.2	Page 12:Power circuit block diagram Page 16:Parallel input order Page 16,51:delete slave mode Page 18,60:First step to read the specific register Page 21:RAM address of Monochrome mode Page 38: bank number Page 40,41: write/read one byte data into DDRAM Page 57:The table of SC register set up Page 63,64: driver sink current, Ron value of SSEG and SCOM DC characteristics values	June 3,2003
0.3	Remove the word “Preliminary” Page 6: Modify RESB ITO Resistor value Page 7: CSB and WRB exchange pad sequence Page 15: “CK” pin voltage for using internal clock.	August 1,2003
0.4	Modify dynamic current of Display off on page 63	August 28,2003
0.5	Modify ITO value	October 12,2004
0.6	Modify RESET time	March 08,2005

Contents

1. General description

EM65100 is one STN-LCD drivers for 4-gray scale display. The sub-screen display function makes it possible to display different images and data in a sub-screen inside the main LCD screen. It also has a built-in display RAM, a power supply circuit for LCD drive, and an LCD controller circuit, therefore contributing to compact system design. Its partial display function realizes low power consumption.

*Partial display function: A function that utilizes only part of the screen, thus reducing power consumption.

2. Feature

- Display RAM capacity
  - Graphic: 104*67*2=13,936 bits
  - Icons: 104*2*2=416 bits
- Ratio of display duty cycle: 1/10, 1/18, 1/26, 1/34, 1/42, 1/50, 1/58, 1/69
- Outputs
  - Segment:101 outputs, Common: 67 outputs
  - Static driver: 2 outputs
- Built-in display104x69x2=14352bit RAM and power supply circuit
- Partial display functions
- Bus connection with 80-family/ 68-family and Elan MPU
- Serial interface is available
- Logic power supply voltage: 1.8 to 3.3 V
- LCD driving voltage: 5.0 to 12.0 V
- Booster: 2 to 4 times
- Write system cycle: 140 ns
- Package(Ordering information):

Part Number	Package	Description	Package information
EM65100AGH	Gold bumped chip	NA	Page 5

Note: The EM65100 series has the following sub-codes depending on their shapes.

H: Bare chip (Aluminum pad without bumped); **GH**: Gold bumped chip;

F: COF package; **T**: TAB (TCP) package

Example EM65100AGH → EM65100: Elan number ; A: Package Version ;GH: COF Gold bumped chip

3. Applications

- Mobile phone
- Small PDA

4. Pin configurations (package)

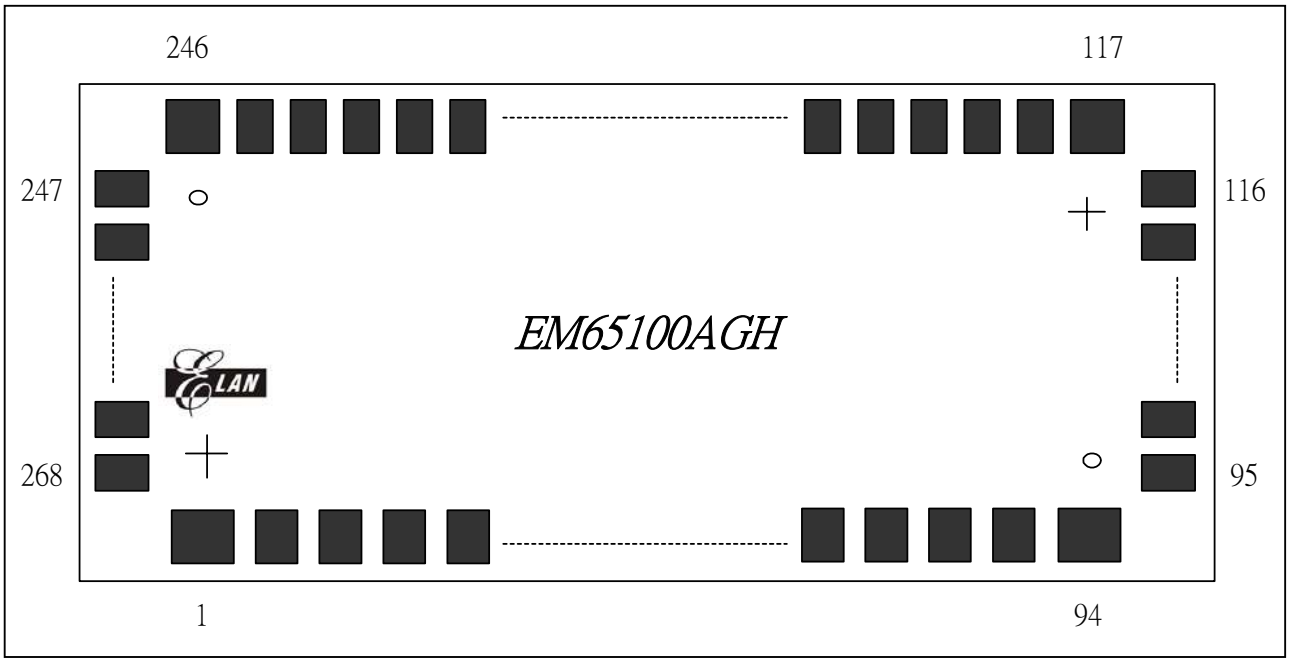
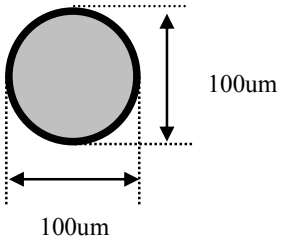


Figure 1. Pin configuration

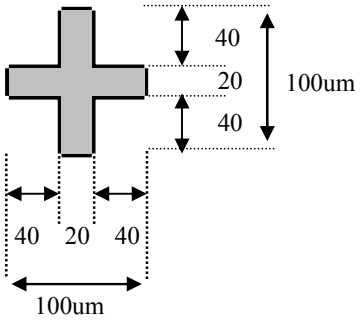
Note: With the Elan logo in down left the pin 1 is in the down left corner

Mark	Coordinate (X,Y)	Mark	Coordinate (X,Y)
U-Left	-3195.0,350.0	U-Right	3195.0,350.0
D-Left	-3195.0,-350.0	D-Right	3195.0,-350.0

U-Left and D-Right:



D-Left and U-Right:



Pad configuration

Item	Pad No.	Size		Unit
		X	Y	
Chip size	-	7260	1570	μm
Bump Size	1~94	56	63	
	95,96,267,268	63	56	
	97~115,248~266	63	36	
	116,247	63	48	
	117,246	48	63	
	118~245	36	63	
Pad Pitch	50 (min.)			
Die thickness (excluding bumps)	508 +/- 25.4			
Bump Height	All Pad 17 +/- 3 (within die)			
Minimum Bump Gap	14			
Coordinate Origin	Chip center			

Recommended COG ITO Traces Resistor

Interface	ITO Traces resistances
V0~V4 CAP1+,CAP1-,CAP2+,CAP2-,CAP3+,Vcc VDD,Vci VSSL,VSSH	Max=50Ω
WRB,RDB,CSB,…,D0~D7	Max=3KΩ
RESB	Max=5~10 KΩ

PAD Coordinates Table

Pin NO	*Pad Name*	*Coordinate* (X,Y)	*Pin NO*	*Pad Name*	*Coordinate* (X,Y)
1	WRB	-3348.6 ,-654.5	51	CAP1-	338.6 ,-654.5
2	RESB	-3278.6 ,-654.5	52	CAP1+	408.6 ,-654.5
3	RS	-3208.6 ,-654.5	53	CAP1+	478.6 ,-654.5
4	CSB	-3138.6 ,-654.5	54	CAP1+	548.6 ,-654.5
5	RDB	-3068.6 ,-654.5	55	CAP1+	618.6 ,-654.5
6	D0	-2998.6 ,-654.5	56	CAP1+	688.6 ,-654.5
7	D1	-2928.6 ,-654.5	57	CAP2+	758.6 ,-654.5
8	D2	-2858.6 ,-654.5	58	CAP2+	828.6 ,-654.5
9	D3	-2788.6 ,-654.5	59	CAP2+	898.6 ,-654.5
10	D4	-2718.6 ,-654.5	60	CAP2+	968.6 ,-654.5
11	D5	-2648.6 ,-654.5	61	CAP2+	1038.6 ,-654.5
12	D6	-2578.6 ,-654.5	62	CAP2-	1108.6 ,-654.5
13	D7	-2508.6 ,-654.5	63	CAP2-	1178.6 ,-654.5
14	VSS	-2438.6 ,-654.5	64	CAP2-	1248.6 ,-654.5
15	CK	-2368.6 ,-654.5	65	CAP2-	1318.6 ,-654.5
16	CKS	-2298.6 ,-654.5	66	CAP2-	1388.6 ,-654.5
17	VREF	-2228.6 ,-654.5	67	V4	1458.6 ,-654.5
18	VREF	-2158.6 ,-654.5	68	V4	1528.6 ,-654.5
19	VREF	-2088.6 ,-654.5	69	V4	1598.6 ,-654.5
20	VREF	-2018.6 ,-654.5	70	V4	1668.6 ,-654.5
21	VREF	-1948.6 ,-654.5	71	V3	1738.6 ,-654.5
22	VDD	-1878.6 ,-654.5	72	V3	1808.6 ,-654.5
23	VDD	-1808.6 ,-654.5	73	V3	1878.6 ,-654.5
24	VDD	-1738.6 ,-654.5	74	V3	1948.6 ,-654.5
25	VDD	-1668.6 ,-654.5	75	V2	2018.6 ,-654.5
26	VDD	-1598.6 ,-654.5	76	V2	2088.6 ,-654.5
27	Vci	-1528.6 ,-654.5	77	V2	2158.6 ,-654.5
28	Vci	-1458.6 ,-654.5	78	V2	2228.6 ,-654.5
29	Vci	-1388.6 ,-654.5	79	V1	2298.6 ,-654.5
30	Vci	-1318.6 ,-654.5	80	V1	2368.6 ,-654.5
31	Vci	-1248.6 ,-654.5	81	V1	2438.6 ,-654.5
32	VSSL	-1178.6 ,-654.5	82	V1	2508.6 ,-654.5
33	VSSL	-1108.6 ,-654.5	83	V0	2578.6 ,-654.5
34	VSSL	-1038.6 ,-654.5	84	V0	2648.6 ,-654.5
35	VSSL	-968.6 ,-654.5	85	V0	2718.6 ,-654.5
36	VSSL	-898.6 ,-654.5	86	V0	2788.6 ,-654.5
37	Vcc	-828.6 ,-654.5	87	VSSH	2858.6 ,-654.5
38	Vcc	-758.6 ,-654.5	88	VSSH	2928.6 ,-654.5
39	Vcc	-688.6 ,-654.5	89	VSSH	2998.6 ,-654.5
40	Vcc	-618.6 ,-654.5	90	VSSH	3068.6 ,-654.5
41	Vcc	-548.6 ,-654.5	91	VSSH	3138.6 ,-654.5
42	CAP3+	-478.6 ,-654.5	92	TEST	3208.6 ,-654.5
43	CAP3+	-408.6 ,-654.5	93	P/S	3278.6 ,-654.5
44	CAP3+	-338.6 ,-654.5	94	VDD	3348.6 ,-654.5
45	CAP3+	-268.6 ,-654.5	95	NC1	3499.5 ,-469.5
46	CAP3+	-198.6 ,-654.5	96	SCOM	3499.5 ,-399.5
47	CAP1-	58.6 ,-654.5	97	COM33	3499.5 ,-339.5
48	CAP1-	128.6 ,-654.5	98	COM32	3499.5 ,-289.5
49	CAP1-	198.6 ,-654.5	99	COM31	3499.5 ,-239.5
50	CAP1-	268.6 ,-654.5	100	COM30	3499.5 ,-189.5

Pin NO	*Pad Name*	*Coordinate* (X,Y)	*Pin NO*	*Pad Name*	*Coordinate* (X,Y)
101	COM29	3499.5 ,-139.5	151	SEG19	1525.0 ,654.5
102	COM28	3499.5 ,-89.5	152	SEG20	1475.0 ,654.5
103	COM27	3499.5 ,-39.5	153	SEG21	1425.0 ,654.5
104	COM26	3499.5 ,10.5	154	SEG22	1375.0 ,654.5
105	COM25	3499.5 ,60.5	155	SEG23	1325.0 ,654.5
106	COM24	3499.5 ,110.5	156	SEG24	1275.0 ,654.5
107	COM23	3499.5 ,160.5	157	SEG25	1225.0 ,654.5
108	COM22	3499.5 ,210.5	158	SEG26	1175.0 ,654.5
109	COM21	3499.5 ,260.5	159	SEG27	1125.0 ,654.5
110	COM20	3499.5 ,310.5	160	SEG28	1075.0 ,654.5
111	COM19	3499.5 ,360.5	161	SEG29	1025.0 ,654.5
112	COM18	3499.5 ,410.5	162	SEG30	975.0 ,654.5
113	COM17	3499.5 ,460.5	163	SEG31	925.0 ,654.5
114	COM16	3499.5 ,510.5	164	SEG32	875.0 ,654.5
115	COM15	3499.5 ,560.5	165	SEG33	825.0 ,654.5
116	COM14	3499.5 ,616.5	166	SEG34	775.0 ,654.5
117	COM13	3231.0 ,654.5	167	SEG35	725.0 ,654.5
118	COM12	3175.0 ,654.5	168	SEG36	675.0 ,654.5
119	COM11	3125.0 ,654.5	169	SEG37	625.0 ,654.5
120	COM10	3075.0 ,654.5	170	SEG38	575.0 ,654.5
121	COM9	3025.0 ,654.5	171	SEG39	525.0 ,654.5
122	COM8	2975.0 ,654.5	172	SEG40	475.0 ,654.5
123	COM7	2925.0 ,654.5	173	SEG41	425.0 ,654.5
124	COM6	2875.0 ,654.5	174	SEG42	375.0 ,654.5
125	COM5	2825.0 ,654.5	175	SEG43	325.0 ,654.5
126	COM4	2775.0 ,654.5	176	SEG44	275.0 ,654.5
127	COM3	2725.0 ,654.5	177	SEG45	225.0 ,654.5
128	COM2	2675.0 ,654.5	178	SEG46	175.0 ,654.5
129	COM1	2625.0 ,654.5	179	SEG47	125.0 ,654.5
130	COM0	2575.0 ,654.5	180	SEG48	75.0 ,654.5
131	COMA	2525.0 ,654.5	181	SEG49	25.0 ,654.5
132	SEG0	2475.0 ,654.5	182	SEG50	-25.0 ,654.5
133	SEG1	2425.0 ,654.5	183	SEG51	-75.0 ,654.5
134	SEG2	2375.0 ,654.5	184	SEG52	-125.0 ,654.5
135	SEG3	2325.0 ,654.5	185	SEG53	-175.0 ,654.5
136	SEG4	2275.0 ,654.5	186	SEG54	-225.0 ,654.5
137	SEG5	2225.0 ,654.5	187	SEG55	-275.0 ,654.5
138	SEG6	2175.0 ,654.5	188	SEG56	-325.0 ,654.5
139	SEG7	2125.0 ,654.5	189	SEG57	-375.0 ,654.5
140	SEG8	2075.0 ,654.5	190	SEG58	-425.0 ,654.5
141	SEG9	2025.0 ,654.5	191	SEG59	-475.0 ,654.5
142	SEG10	1975.0 ,654.5	192	SEG60	-525.0 ,654.5
143	SEG11	1925.0 ,654.5	193	SEG61	-575.0 ,654.5
144	SEG12	1875.0 ,654.5	194	SEG62	-625.0 ,654.5
145	SEG13	1825.0 ,654.5	195	SEG63	-675.0 ,654.5
146	SEG14	1775.0 ,654.5	196	SEG64	-725.0 ,654.5
147	SEG15	1725.0 ,654.5	197	SEG65	-775.0 ,654.5
148	SEG16	1675.0 ,654.5	198	SEG66	-825.0 ,654.5
149	SEG17	1625.0 ,654.5	199	SEG67	-875.0 ,654.5
150	SEG18	1575.0 ,654.5	200	SEG68	-925.0 ,654.5

Pin NO	*Pad Name*	*Coordinate* (X,Y)	*Pin NO*	*Pad Name*	*Coordinate* (X,Y)
201	SEG69	-975.0 ,654.5	251	COM52	-3499.5 ,410.5
202	SEG70	-1025.0 ,654.5	252	COM53	-3499.5 ,360.5
203	SEG71	-1075.0 ,654.5	253	COM54	-3499.5 ,310.5
204	SEG72	-1125.0 ,654.5	254	COM55	-3499.5 ,260.5
205	SEG73	-1175.0 ,654.5	255	COM56	-3499.5 ,210.5
206	SEG74	-1225.0 ,654.5	256	COM57	-3499.5 ,160.5
207	SEG75	-1275.0 ,654.5	257	COM58	-3499.5 ,110.5
208	SEG76	-1325.0 ,654.5	258	COM59	-3499.5 ,60.5
209	SEG77	-1375.0 ,654.5	259	COM60	-3499.5 ,10.5
210	SEG78	-1425.0 ,654.5	260	COM61	-3499.5 ,-39.5
211	SEG79	-1475.0 ,654.5	261	COM62	-3499.5 ,-89.5
212	SEG80	-1525.0 ,654.5	262	COM63	-3499.5 ,-139.5
213	SEG81	-1575.0 ,654.5	263	COM64	-3499.5 ,-189.5
214	SEG82	-1625.0 ,654.5	264	COM65	-3499.5 ,-239.5
215	SEG83	-1675.0 ,654.5	265	COM66	-3499.5 ,-289.5
216	SEG84	-1725.0 ,654.5	266	COMB	-3499.5 ,-339.5
217	SEG85	-1775.0 ,654.5	267	SSEG	-3499.5 ,-399.5
218	SEG86	-1825.0 ,654.5	268	M86	-3499.5 ,-469.5
219	SEG87	-1875.0 ,654.5			
220	SEG88	-1925.0 ,654.5			
221	SEG89	-1975.0 ,654.5			
222	SEG90	-2025.0 ,654.5			
223	SEG91	-2075.0 ,654.5			
224	SEG92	-2125.0 ,654.5			
225	SEG93	-2175.0 ,654.5			
226	SEG94	-2225.0 ,654.5			
227	SEG95	-2275.0 ,654.5			
228	SEG96	-2325.0 ,654.5			
229	SEG97	-2375.0 ,654.5			
230	SEG98	-2425.0 ,654.5			
231	SEG99	-2475.0 ,654.5			
232	SEG100	-2525.0 ,654.5			
233	COM34	-2575.0 ,654.5			
234	COM35	-2625.0 ,654.5			
235	COM36	-2675.0 ,654.5			
236	COM37	-2725.0 ,654.5			
237	COM38	-2775.0 ,654.5			
238	COM39	-2825.0 ,654.5			
239	COM40	-2875.0 ,654.5			
240	COM41	-2925.0 ,654.5			
241	COM42	-2975.0 ,654.5			
242	COM43	-3025.0 ,654.5			
243	COM44	-3075.0 ,654.5			
244	COM45	-3125.0 ,654.5			
245	COM46	-3175.0 ,654.5			
246	COM47	-3231.0 ,654.5			
247	COM48	-3499.5 ,616.5			
248	COM49	-3499.5 ,560.5			
249	COM50	-3499.5 ,510.5			
250	COM51	-3499.5 ,460.5			

Note: For PCB layout, IC substrate must be floated or connected to VSS

5. Functional block diagram

5.1 System Block Diagram

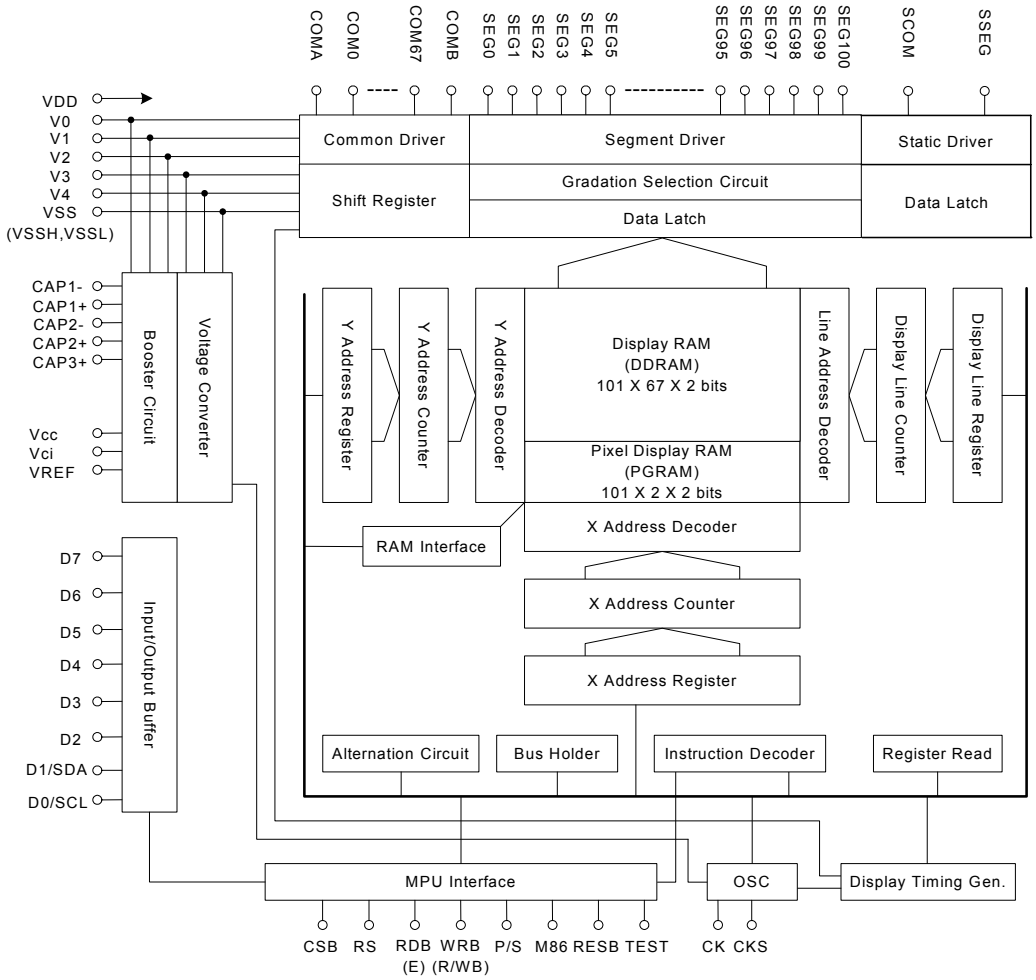


Figure 2. System Block Diagram

5.2 Power Circuit Block Diagram

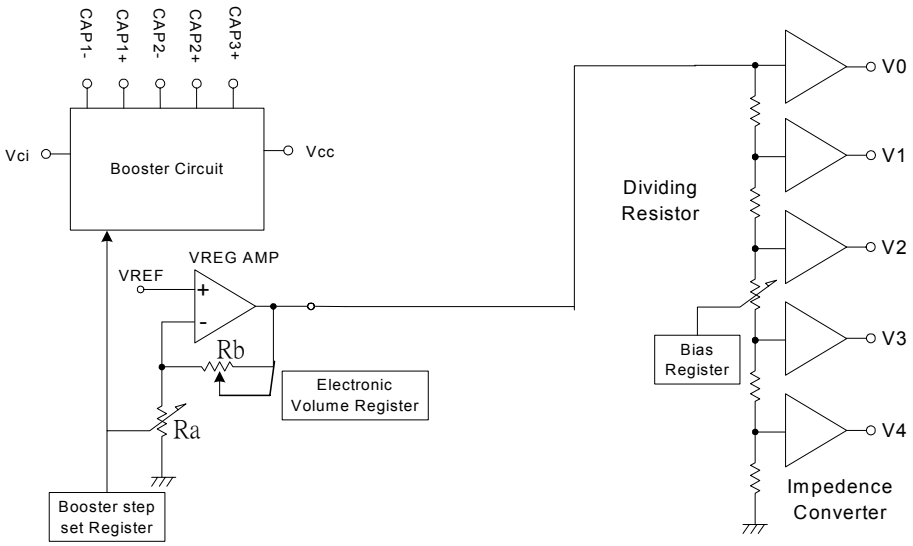


Figure 3. Power Circuit Block Diagram

6. Pin Description

6.1 Power Supply Pins

Symbol	*I/O*	*Description*
VDD	Power Supply	Power supply pin for logic circuit to +1.8 to 3.3V
VSSL	Power Supply	Ground pin for logic circuit, connect to 0V
VSSH	Power Supply	Ground pin for high voltage circuit, connected to 0V
V0 V1 V2 V3 V4	Power Supply	Bias power supply pin for LCD drive voltage When using an external power supply, convert impedance by using resistance-division of LCD drive power supply or operation amplifier before adding voltage to the pins. These voltages should have following relationship: VSS<V4<V3<V2<V1<V0 When the internal power supply circuit is active, these voltages are generated by the built-in booster and voltage converter. Then, must connect capacitor each to VSS.

6.2 LCD Power Supply Circuit Pins

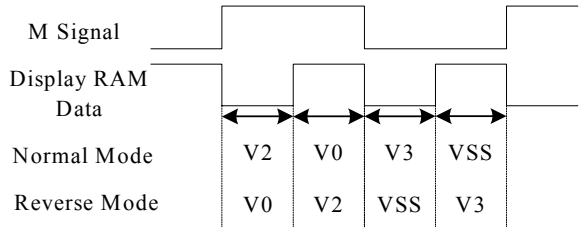
Symbol	*I/O*	*Description*
CAP1+	O	When internal Booster circuit is used, external capacitor(s) is/are connected to these pin
CAP1-	O	
CAP2+	O	
CAP2-	O	
CAP3+	O	
VREF	I	Voltage input pin for generating reference power source
Vci	Power Supply	Voltage supply pin for booster circuit. Usually the same voltage level as VDD.
Vcc	O	Output pin of boosted voltage in the built-in booster. The capacitor must be connected between this pin and VSS.

6.3 System Bus Pins

<table>
<tr><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>RESB</td><td>I</td><td>Reset input pin.
When RESB is “L”, initialization is executed.</td></tr>
<tr><td>D0/SCL
D1/SDA
D2-D7</td><td>I/O</td><td>Data bus / Signal interface related pins.
When parallel interface is selected (P/S = “H”), The D7-D0 are 8-bits bi-directional data bus, connect to MPU data bus.
When serial interface is selected (P/S = “L”), D0 and D1 (SCL, SDA) are used as serial interface pins.
SCL: Input pin for data transfer clock
SDA: Serial data input pin
SDA data is latched at the rising edge of SCL.
Internal serial/parallel conversion into 8-bit data occurs at the rising edge of 8th clock of SCL
After completing data transferring, or when making no access, be sure to set SCL to “L”.</td></tr>
<tr><td>CSB</td><td>I</td><td>Chip Select input pin.
CSB = “L”: accepts access from MPU
CSB = “H”: denies access from MPU</td></tr>
<tr><td>RS</td><td>I</td><td>RAM/Register select input pin.
RS = “0”: D7-D0 are display RAM data
RS = “1”: D7-D0 are control register data</td></tr>
<tr><td>RDB
(E)</td><td>I</td><td>Read/Write control pin
Select 80-family MPU type (M86 = “L”)
The RDB is a data read signal. When RDB is “L”, D7-D0 are in an output status.
Select 68-family MPU type (M86 = “H”)
R/WB = “H”: When E is “H”, D7-D0 are in an output status.
R/WB = “L”: The data on D7-D0 are latched at falling edge of the E signal.</td></tr>
<tr><td>WRB
(R/WB)</td><td>I</td><td>Read/Write control pin
Select 80-family MPU type (M86 = “L”)
The WRB is a data write signal. The data on D7-D0 are latched at rising edge of the WRB signal.
Select 68-family MPU type (M86 = “H”)
Read/Write control input pin.
R/W = “H”: Read
R/W = “L”: Write</td></tr>
<tr><td>M86</td><td>I</td><td>MPU interface type selecting input pin.
M86 = “H”: 68-family interface
M86 = “L”: 80-family interface
Fixed at either “H” or “L”</td></tr>
<tr><td>P/S</td><td>I</td><td>Parallel/Serial interface select pin.
<table>
<tr><th>P/S</th><th>Chip select</th><th>Data identification</th><th>Data</th><th>Read/Write</th><th>Serial clock</th></tr>
<tr><td>H</td><td>CSB</td><td>RS</td><td>D0-D7</td><td>RDB, WRB</td><td>-</td></tr>
<tr><td>L</td><td>CSB</td><td>RS</td><td>SDA</td><td>Write only</td><td>SCL</td></tr>
</table>
P/S = “H”: For parallel interface.
P/S = “L”: For serial interface. Fix D15-D5 pins are Hi-Z, RDB and WRB pins to either “H” or “L”.</td></tr>
<tr><td>TEST</td><td>I</td><td>For testing. Fix to “L”.</td></tr>
</table>

6.4 LCD Drive Circuit Signals

<table>
<tr><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>SEG0-
SEG101</td><td>O</td><td>Segment output pins for LCD drives.
According to the data of the Display RAM data, non-lighted at “0”, lighted at “1” (Normal Mode). non-lighted at “1”, lighted at “0” (Reverse Mode) and, by a combination of M signal and display data, one signal level among V0,V2,V3 and VSS signal levels are selected.

(When Monochrome Display)
 
</td></tr>
<tr><td>COM0-
COM66</td><td>O</td><td>Common output pins for LCD drivers. By a combination of the scanning data and M signal, one signal level among V0, V1, V4 and VSS signal level is selected.
<table>
<tr><th>Data</th><th>M</th><th>Output level</th></tr>
<tr><td>H</td><td>H</td><td>VSS</td></tr>
<tr><td>L</td><td>H</td><td>V1</td></tr>
<tr><td>H</td><td>L</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V4</td></tr>
</table></td></tr>
<tr><td>COMA</td><td>O</td><td>Common output pin for LCD drive exclusively for icons.</td></tr>
<tr><td>COMB</td><td>O</td><td>Common output pin for LCD drive exclusively for icons.</td></tr>
<tr><td>SCOM
SSEG</td><td>O</td><td>LCD driver output pin for static driver</td></tr>
</table>

6.5 Oscillating Circuit Pin

Symbol	*I/O*	*Description*
CKS	I	Display timing clock source select input pin. CKS = "H": Use external clock from CK pin. CKS = "L": Use internal oscillated clock.
CK	I	External clock input pin for display timing. When use internal clock, fix the CK pin at "L".

7. Functional Description

7.1 MPU Interface

7.1.1 Selection of Interface Type

The EM65100 transfers data through 8-bit parallel I/O (D7-D0) or serial data input (SDA, SCL). The parallel interface or serial interface can select by state of P/S pin. When select serial interface, data reading cannot be performed, only data writing can operate.

P/S	*I/F Type*	*CSB*	*RS*	*RDB*	*WRB*	*M86*	*SDA*	*SCL*	*Data*
H	Parallel	CSB	RS	RDB	WRB	M86	-	-	D7~D0
L	Serial	CSB	RS	-	-	-	SDA	SCL	-

7.1.2 Parallel Input

When parallel interface is selected with the P/S pin, the EM65100 allows data to be transferred in parallel to an 8-bit MPU through the data bus. For the 8-bit MPU, either the 80-family MPU interface or the 68-family MPU interface can be selected with the m86 pin.

M86	*MPU Type*	*CSB*	*RS*	*RDB*	*WRB*	*Data*
H	68-family MPU	CSB	RS	E	R/WB	D7~D0
L	80-family MPU	CSB	RS	RDB	WRB	D7~D0

7.1.3 Read/Write functions of Register and display RAM

The EM65100 have four read/write functions at parallel interface mode. Each read/write function select by combinations of RS, RDB and WRB signals.

RS	*68-family R/WB*	*80-family*		*Function*
		RDB	*WRB*	
1	1	0	1	Read internal Register
1	0	1	0	Write internal Register
0	1	0	1	Read display data
0	0	1	0	Write display data

7.1.4 Serial Interface

The serial interface of EM65100 can accept inputs of SDA and SCL in the state of chip select (CSB="L"). When not in the state of chip select. The internal shift register and counter are reset in the initial condition. Serial data SDA are input sequentially in order of D7 to D0 at the rising of serial clock (SCL) and are converted into 8-bit parallel data (by serial to parallel conversion) at the rising edge of the 8^{th} serial clock, being processed in accordance with the data. The identification whether are serial data inputs (SDA) are display data or control register data is judged by input to RS pin.

RS = "L": display RAM data

RS = "H": control register data

After completing 8-bit data transferring, or when making no access, be sure to set serial clock input (SCL) to "L". Cares of SDA and SCL signals against external noise should be taken in board wiring. To prevent transfer error due to external noise, release chip select (CSB = "H") every completion of 8-bit data transferring.

When serial interface is used, access is only made for 8-bit data transfer.

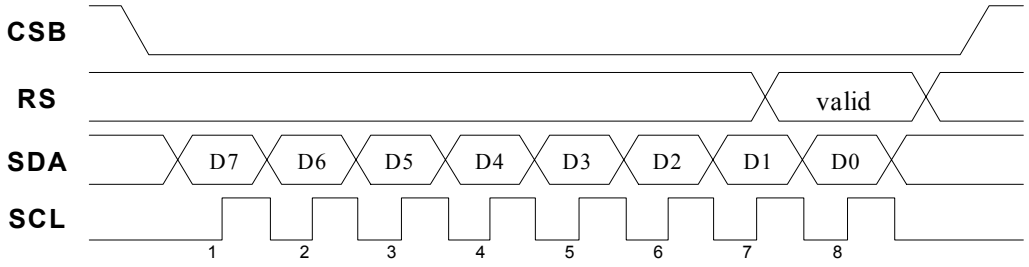


Figure 4. Serial Interface

7.2 Data write to Display RAM and Control Register

The data write to display RAM and Control Register use almost same procedure, only different setting of RS that select access object.

RS = "L": Display RAM data

RS = "H": Control register data

In the case of the 80-family MPU, the data is written at the rising edge of WRB. In the case of the 68-family MPU, the data is written at the falling edge of signal E.

Data write operation

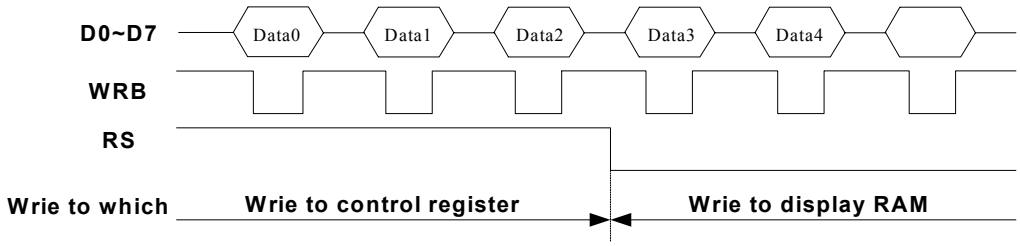


Figure 6. Data write operation

7.3 Internal Register Read

In the case of display RAM read operation, need dummy read one time. The designated address data are not output to read operation immediately after the address set to AX or AY register, but are output when the second data read. Dummy read is always required one time after address set and write cycle.

Read display RAM operation

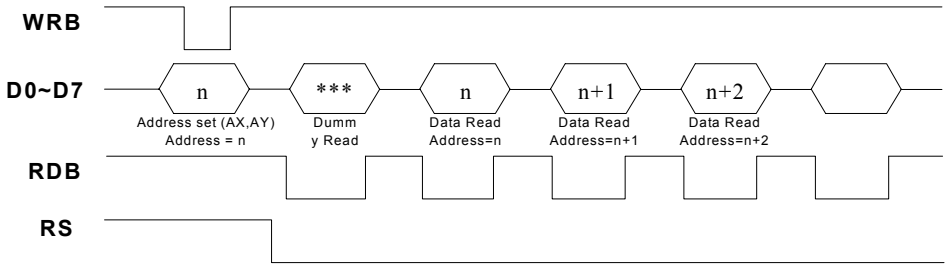


Figure 7. Read display RAM operation

The EM65100 can be read the control registers, in case of control register read operation, data bus upper nibble (D3-D0) use for register address (0 to FH). In maximum, 16 registers can access directly. But number of register is more than 16 registers. Therefore, EM65100 has register bank control. The RE register is set bank number to access. And the RE address is 0FH, in any bank can access RE register. It is need 4-steps to read the specific register in maximum case.

(1) Write 02H to RE register for access to RA register.

(2) Writes specific register address to RA register.

(3) Write specific register bank to RE register.

(4) Read specific register contents.

Register read operation

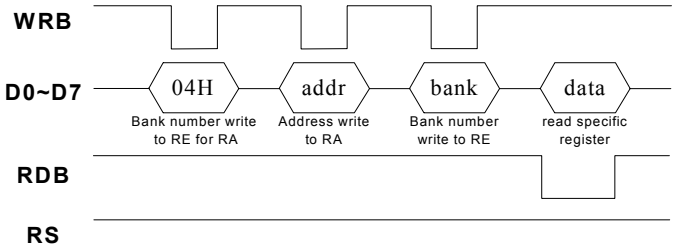


Figure 8. Register read operation

7.4 Display Start Address Register

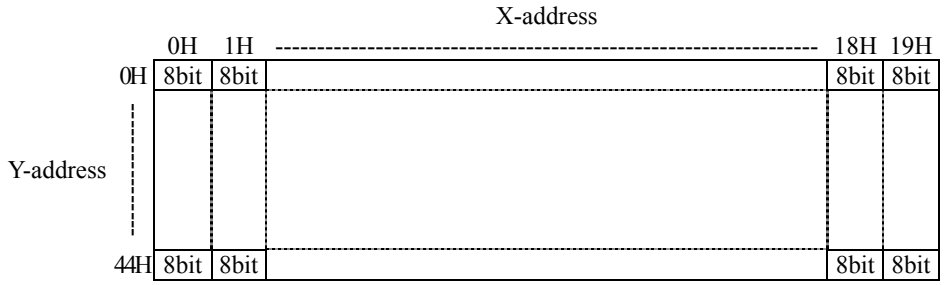
This register determines the Y-address of the display RAM corresponding to the display start line. The display RAM data that addressed Display Start Address register output to common driver start line. The actual common start line of LCD panel depend on Display Start Common register and SHIFT bit of Display Control register. The register are preset every timing of FLM signal variation in the display line counter. The line counter counts up being synchronized with LP input and generates line addresses which read out sequentially 288 bits data from display RAM to LCD drive circuit.

7.5 Addressing of Display RAM

The EM65100 has built-in bit mapped display RAM. The display RAM consists of 208 bits in the X-direction and 69 bits in the Y-direction. In the gradation display mode, the EM65100 provides segment driver output for 4-gradation display using 2 bits. When connected to an STN LCD panel, the EM65100 can display 101*69 pixels with 4-gradation display. The address area in the X-direction depends on the access bus size. When use 8-bits bus size, can access 00H to 19H address. In the X-direction, X Address register use to access; and in the Y-direction, Y Address register use to access. Do not specify any address outside the effective address area in each access mode because it is not permitted.

In Gradation Display Mode (MON="0")

8-bits bus size access



The addresses, X Address and Y Address are possible to be set up so that they can increment automatically with the address control register. The increment is made every time display RAM is read or written from MPU. In the Y-direction, 208 bits of data are read out to the display data latch circuit by internal operation when the LP rises in a one-line cycle. They are output from the display data latch circuit when the LP fails. When FLM signals being output in one frame cycle are at "H", the values in the display starting line register are preset in the line counter and the line counter counts up at the falling of LP signals. The display line address counter is synchronized with each timing signal of the LCD system to operate and is independent of address counters X and Y.

7.6 Display RAM Data and LCD (only monochrome mode)

One bit of display RAM data corresponds to one dot of LCD. Normal display and reverse display by REV register are set up as follows.

Normal display (REV=0): RAM data = "0" not lighted

RAM data = "1" lighted

Reverse display (REV=1): RAM data = "0" lighted

RAM data = "1" not lighted

7.7 Segment Display Output Order/Reverse Set up

The order of display output, SEG0 to SEG100 can be reversed. If REF control bit set to "1", display by reversing access to display RAM from MPU by using REF register, lessen the limitation in placing IC when assembling an LCD panel module.

7.8 Relationship between Display RAM and Address

The Display RAM block diagram shows in the figure below:

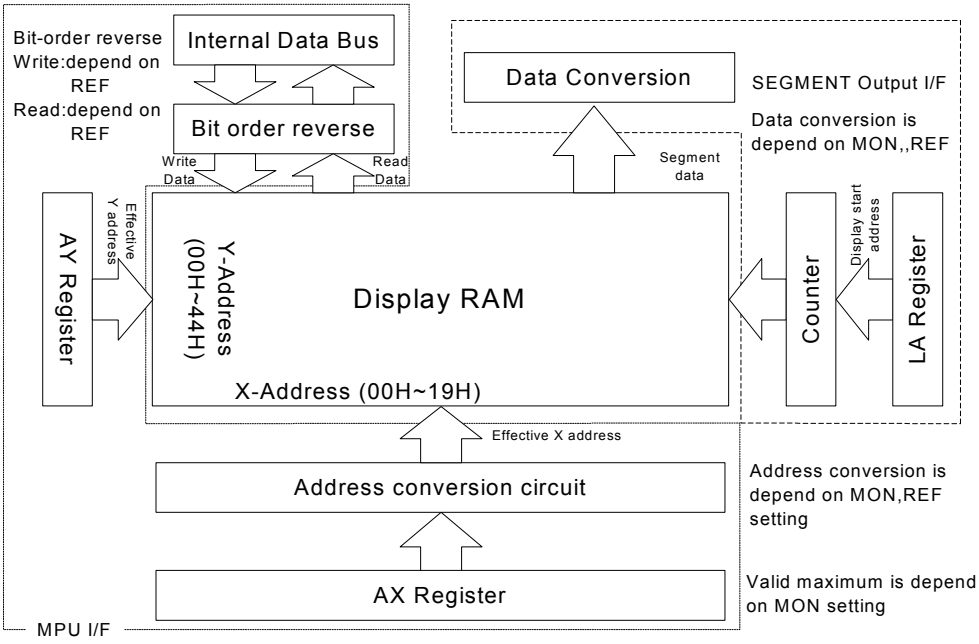
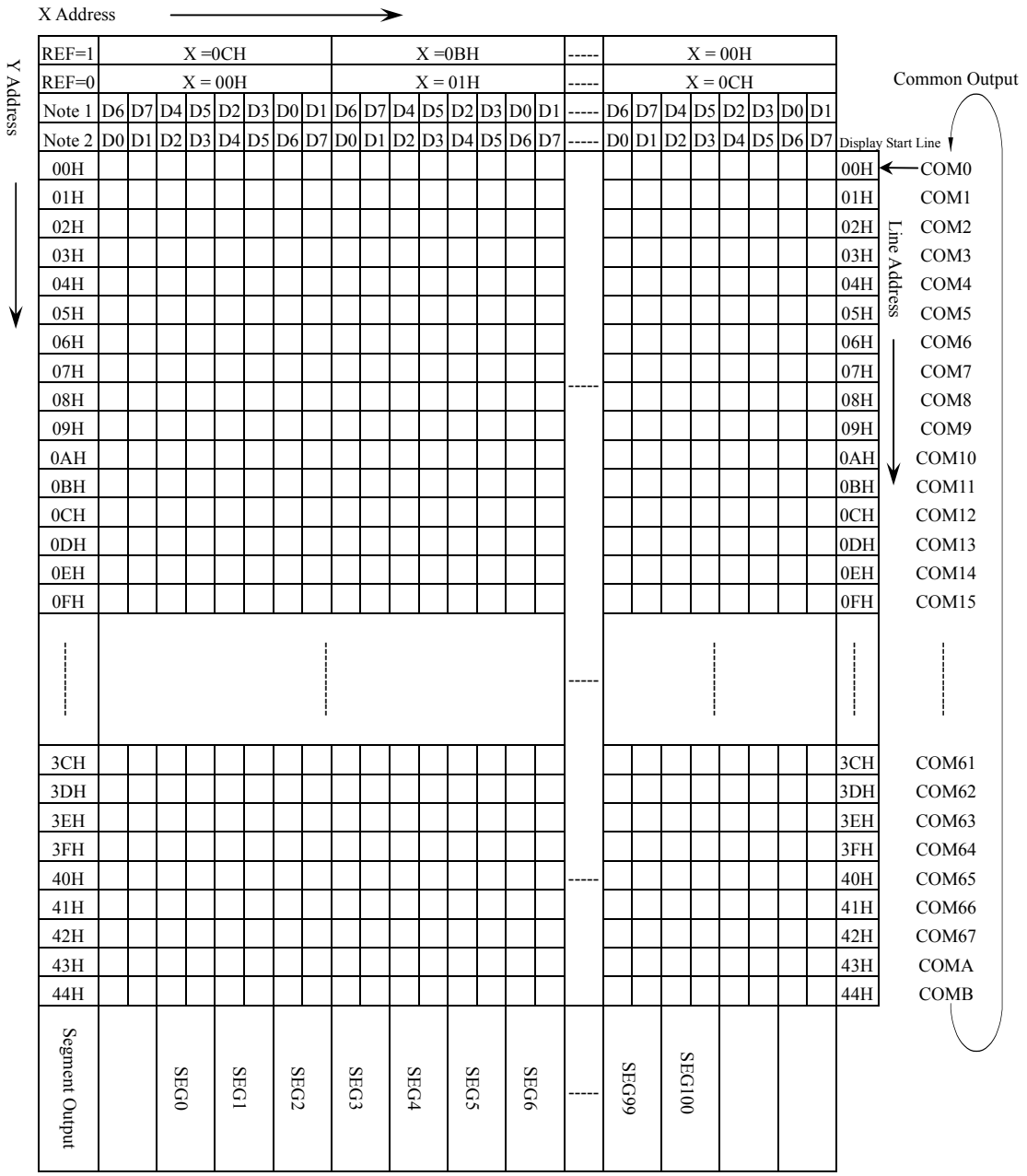


Figure 10. The Display RAM block diagram

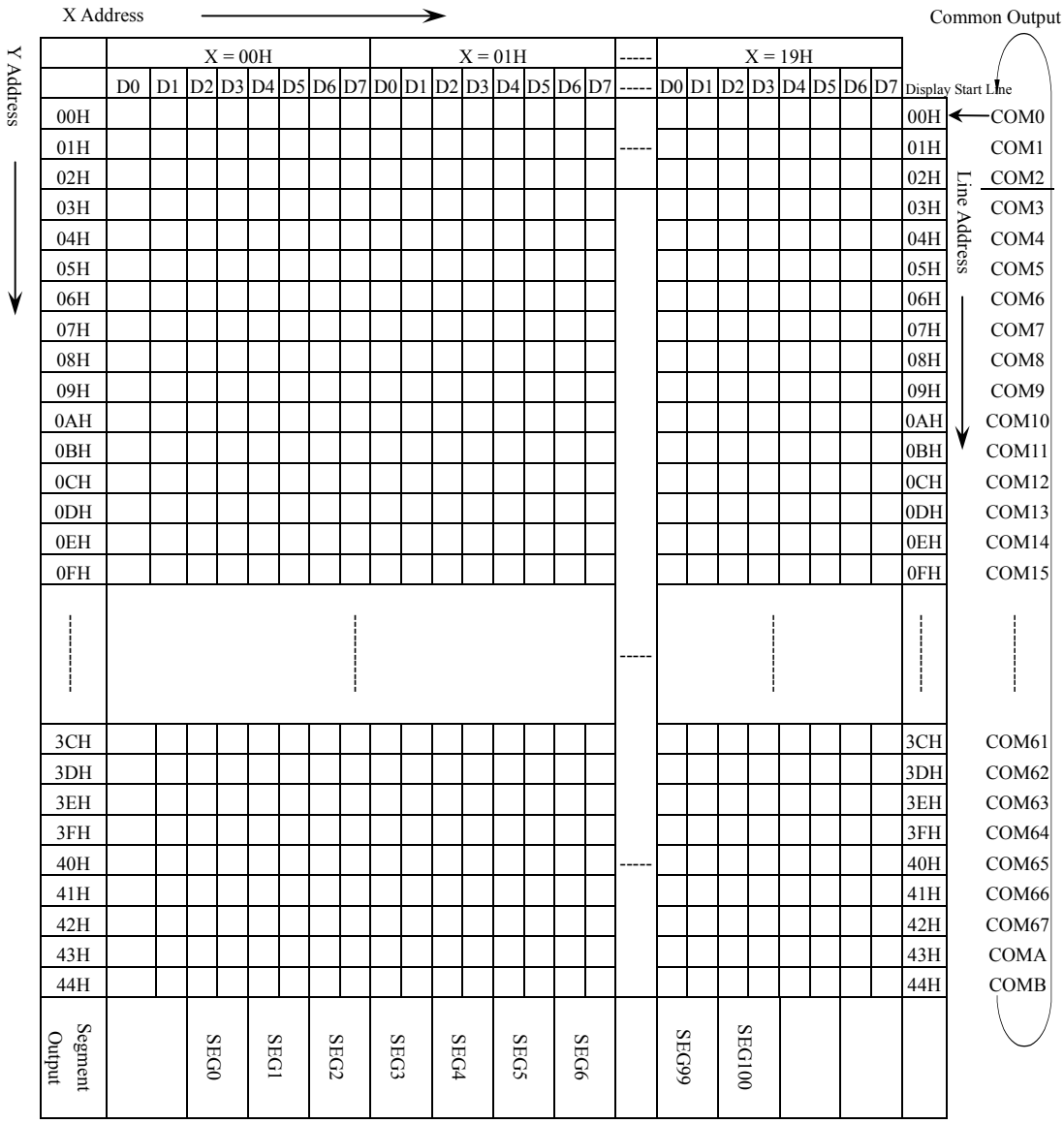
The EM65100 execute address conversion that depends on control register setting. In case of auto increment mode, usually AX register is added one. For instance when REF and AXI are both "1", AX register is added one, but effective X address seems decrement because of address conversion. The effective Y address use AY register values as it is.

(1) Monochrome mode, 8-bits Access mode



Note1: REF=1
Note2: REF=0

(2)Gradation mode, 8 bits access mode, REF =0



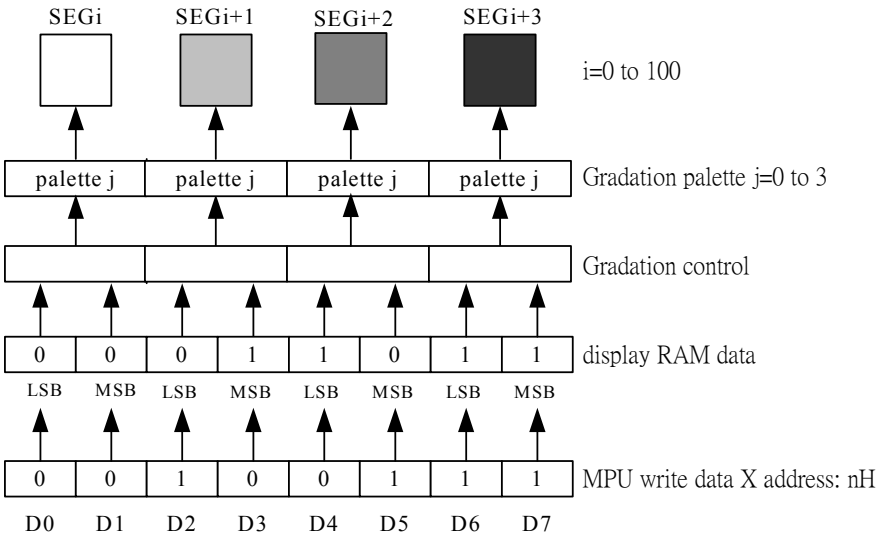
7.9 Display Data Structure and Gradation Control

For the purpose of gradation control, one pixel requires multiple bits of display RAM. The EM65100 has 2-bit data per output to achieve the gradation display.

The EM65100 is connected to an STN LCD panel. It can display 101*69 pixels with 4-gray level. In this case, since the gradation display data is processed by a single access to the memory, the data can be rewritten fast and naturally.

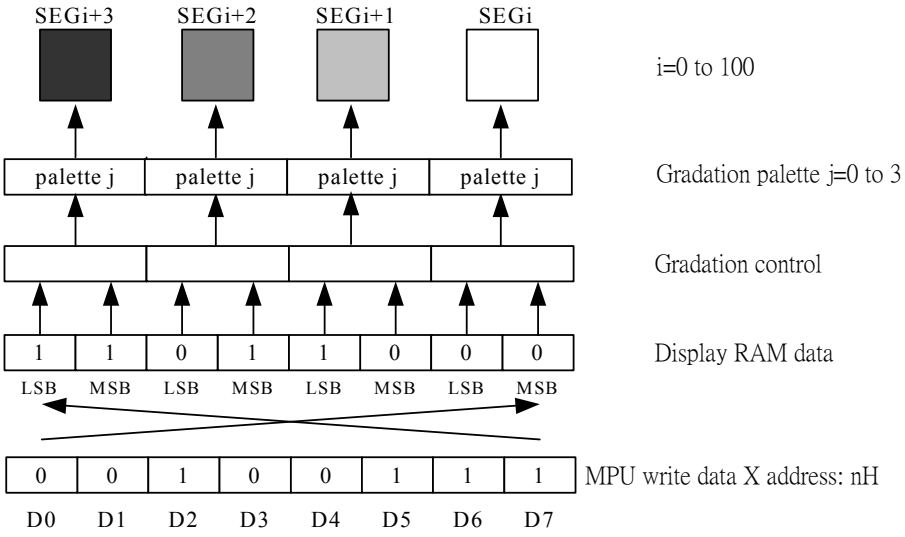
The weighting for each data bit is dependent on the status of the REF bit that is selected when data is written to the display RAM.

- REF=0



Note : Internal X address : nH (REF="0")
: 19H-nH (REF="1")

- REF=1



Note : Internal X address : nH (REF="0")
: 19H-nH (REF="1")

7.10 Gradation Palette

The EM65100 has two gradation display modes, the gradation fixed display mode and the gradation variable display mode. Select either of the two modes using the gradation display mode register.

PWM = "0": Selects the variable display mode using 4 gradation selected from 16 gradation.
PWM = "1": Selects the fixed display mode using specific 4 gradation.

To select the best gradation level suited to the LCD panel, use the gradation palette register among the 16-level gradation palettes in the gradation variable display mode. The segment driver output is set up by the selected 4-levels of gradation palettes.

Each register consists of a 2-bit register, selecting 4-gradations from the pattern for 16-gradations.

Initial values on gradation palette register

[Three groups of palettes WAj~WDj, LAj~LDj, DAj~DDj, and BAj~BDj are available]

(MSB) RAM data (LSB)		Register Name	Initial value
0	0	Gradation Palette 0	0 0 0 0
0	1	Gradation Palette 1	0 1 0 1
1	0	Gradation Palette 2	1 0 1 0
1	1	Gradation Palette 3	1 1 1 1

Gradation level table (PWM = "0", variable mode)

[Three groups of palettes WAj~WDj, LAj~LDj, DAj~DDj, and BAj~BDjand Cj (j=0-3) are available]

Palette	Gradation level	Remark
0 0 0 0	0	Gradation palette 0
0 0 0 1	1/15	
0 0 1 0	2/15	
0 0 1 1	3/15	
0 1 0 0	4/15	
0 1 0 1	5/15	Gradation palette 1
0 1 1 0	6/15	
0 1 1 1	7/15	
1 0 0 0	8/15	
1 0 0 1	9/15	
1 0 1 0	10/15	Gradation palette 2
1 0 1 1	11/15	
1 1 0 0	12/15	
1 1 0 1	13/15	
1 1 1 0	14/15	
1 1 1 1	15/15	Gradation palette 3

Caution: Different gradation levels can't be set in the same palette.

Gradation level table (PWM = "1", fixed mode)

(MSB) RAM data (LSB)		Gradation level
0	0	0
0	1	1/3
1	0	2/3
1	1	3/3

7.11 Display Timing Circuit

The display timing circuit generates internal signals and timing pulses (internal LP, FLM, M) by clock. It can select external input (CK) or internal oscillation.

Symbol	*Description*
LP(internal)	The LP is latch clock signal. At the rising edge, count the display line counter. At the falling edge output the LCD drive signal.
FLM(internal)	The signal for LCD display synchronous signals (first line maker). When FLM is set to "H", the display start-line address is preset. In the display line counter
M(internal)	The signal for alternated signals of LCD drive output.

7.12 Signal Generation to Display Line Counter, and Display Data Latching Circuit

Both the clock to the line counter and clock to display data latching circuit from the display clock (internal LP) are generated. Synchronized with the display clock (internal LP), the line addresses of Display RAM are generated and 208-bits display data are latched to display data latching circuit to output to the LCD drive circuit (Segment outputs). Read-out of the display data to the LCD drive circuit is completely independent of MPU. Therefore, MPU that has no relationship the read-out operation of the display data can access.

7.13 Generation of the Alternated Signal (internal M) and the Synchronous Signal (internal FLM)

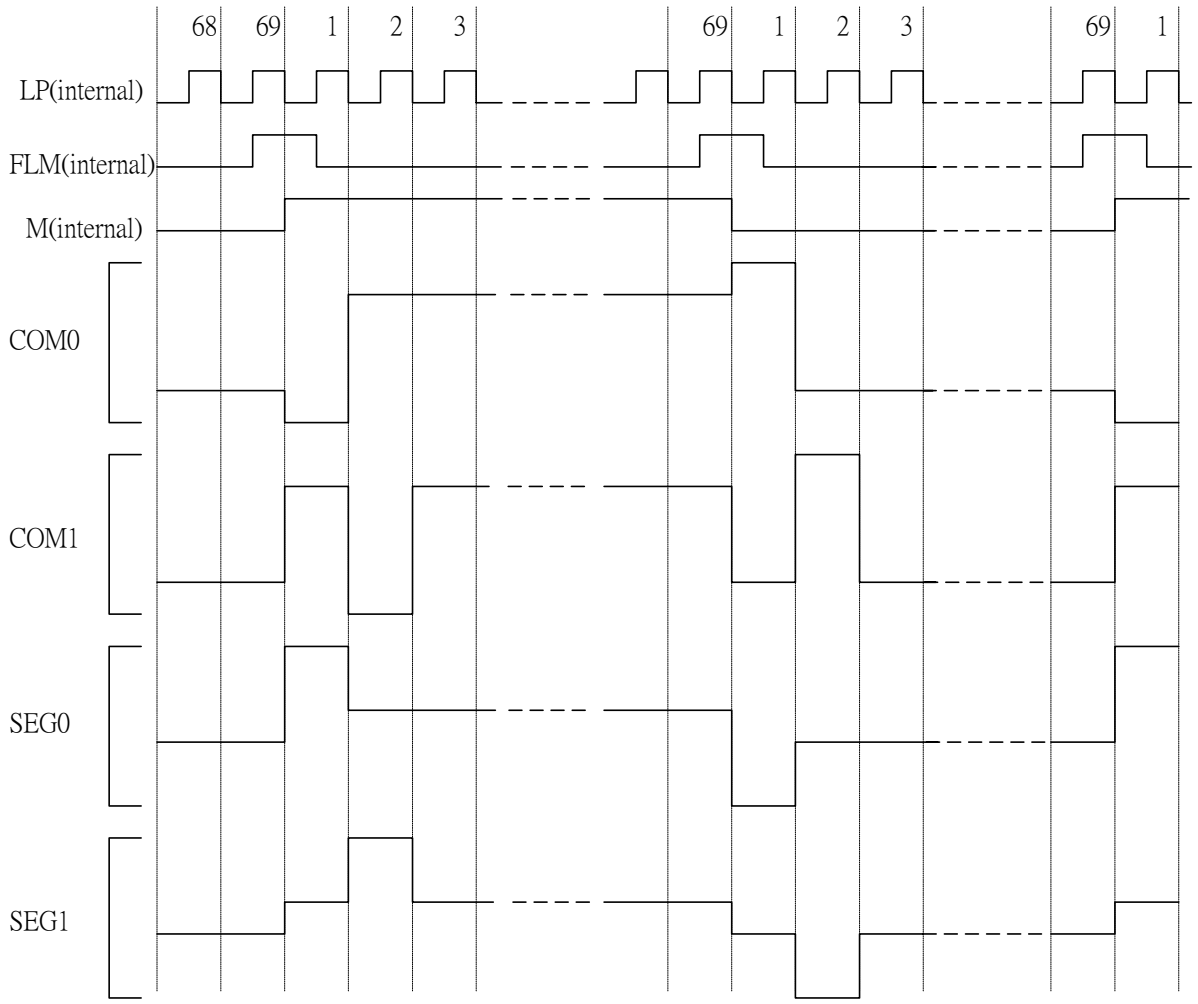
LCD alternated signal (internal M) and synchronous signal (internal FLM) are generated by the display clock (internal LP). The FLM generates alternated drive waveform to the LCD drive circuit. Normally, the FLM generates alternated drive waveform every frame (M-signal level is reversed every one frame). However, by setting up data (n-1) in an n-line reverse register and n-line alternated control bit (NLIN) at "1", n-line reverse waveform is generated.

7.14 Display Data Latching Circuit

Display data latching Circuit temporally latches display data that is output display data to LCD driver circuit from display RAM every one common period. Normal display/reverse display, display ON/OFF, and display all on functions are operated by controlling data in display data latch. Therefore, no data within display RAM changes.

7.15 Output Timing of LCD Driver

Display timing at Normal mode (not reverse mode), 1/69 DUTY, and on monochrome mode.



7.16 LCD Drive Circuit

This drive circuit generates four levels LCD drive voltage. The circuit has 101 segment outputs and 69 common outputs and outputs combined display data and M signal. Two of common outputs, COMA and COMB, are special outputs. The COMA and COMB outputs be not influenced by partial setting. Mainly use for display. The common drive circuit that has shift register sequentially outputs common scan signals.

7.17 Oscillating Circuit

The EM65100 has the CR oscillator. The output from this oscillator is used as the timing signal source of the display and the boosting clock to the booster.

This can use only in the master operation mode.

When in the master operation mode and external clock is used, feed the clock to CK pin.

The duty cycle of the external clock must be 50%.

The resistance ratio of CR oscillator is programmable. If change this ratio, also change frame frequency for display.

7.18 Power Supply Circuit

This circuit supplies voltages necessary to drive a LCD. The circuit consists of booster and voltage converter.

Boosted voltage from the booster is fed to the voltage converter that converts this input voltage into V0, V1, V2, V3 and V4 that are used to drive the LCD. This internal power supply should not be used to drive a large LCD panel containing many pixels. Otherwise, display quality will degrade considerably. Instead, use an external power supply. When using the external power supply, turn off the internal power supply (AMPON, DCON="00"), disconnect pins CAP1+, CAP1-, CAP2+, CAP2-, CAP3+, Vcc, Vci, VREF Then, feed external LCD drive voltages to pins V0, V1, V2, V3 and V4. The power circuit can be control by power circuit related register. So partial function of built-in power circuit can use with external power supply.

DCON	AMPON	Booster circuit	Voltage conversion circuit	Extemal voltage input	Note
0	0	DISABLE	DISABLE	V0,V1,V2,V3 and V4 are supplied	※1
0	1	DISABLE	ENABLE	Vcc is supplied	※2
1	1	ENABLE	ENABLE	-	-

※ 1 Because the booster and voltage converter not operating, disconnect pins
CAP1+, CAP1-, CAP2+, CAP2-, CAP3+,, Vcc, Vci, and VREF.
Apply external LCD drive voltages to corresponding pin.

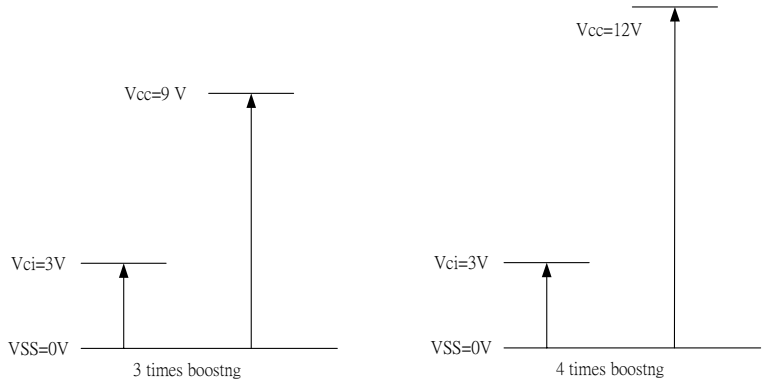
※ 2 Because the booster is not operating, disconnect pins
CAP1+, CAP1-, CAP2+, CPA2-, CAP3+
Derive the voltage source to be supplied to the voltage converter from Vcc pin and then
Input the reference voltage at VREF pin.

7.19 Booster Circuit

Using the booster voltage circuit equipped within the EM65100 chip it is possible to product a four times step-up, and a three times , and two times step-up of the Vci voltage level. The twice, third, or fourth boosted voltage output to the Vcc pin by the boost step register set. The boost step registers set by the command.

(1) In case of using only twice boosted voltage, placing Capacitor across CAP1+ and CAP1-, and connect CAP2+ and CAP3+.
(2) In case of using only third boosted voltage, placing Capacitor across CAP1+ and CAP1-, across CAP2+ and CAP2-.
(3) In case of using only fourth boosted voltage, placing Capacitor across CAP1+ and CAP1-, across CAP2+ and CAP2-, across CAP3+ and CAP1-

When use built-in booster circuit, output voltage (Vcc) must less than recommended operating voltage (12.0 Volt). If output voltage (Vcc) over recommended operating voltage, correct work of chip can not guarantee.



7.20 Electronic volume

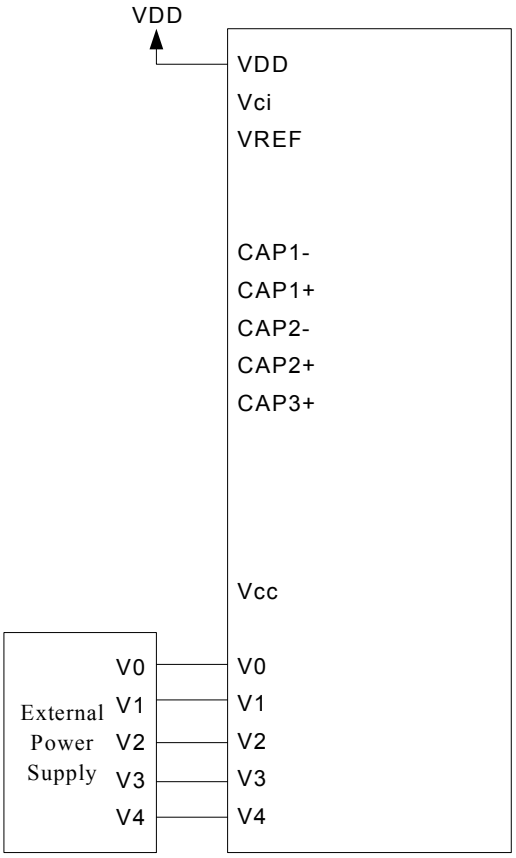
The voltage conversion circuit has built-in an electronic volume, which allows the LCD drive voltage level V0 to be controlled with DV register setting and allows the tone of LCD to be controlled. The DV registers are 7-bits, so can select 128 voltage values for the LCD drive voltage V0.

7.21 Voltage Regulator

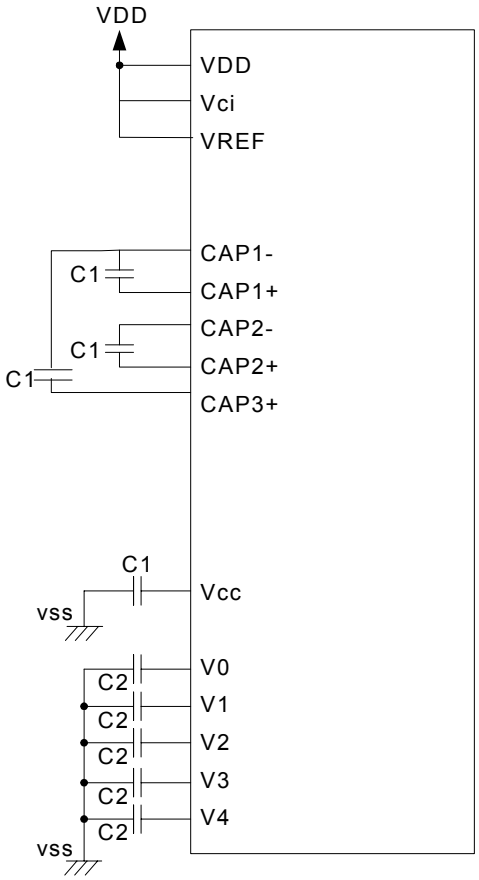
The EM65100 has built-in reference voltage regulator, which generate the voltage amplified by input voltage from VREF pin. The generated voltage is output at the VREG (internal). Even if the boosted voltage level fluctuates, VREG (internal) remains stable so far as Vcc is higher than VREG Stable power supply can be obtained using this constant voltage, even if the load fluctuates. The EM65100 uses the generated VREG level for the reference level of the electronic volume to generate LCD drive voltage.

7.22 LCD Drive Voltage Generation Circuit

The voltage converter contains the voltage generation circuit. The LCD drive voltages other than V0, that is, V1, V2, V3 and V4 are obtained by dividing V0 through a resistor network. The LCD drive voltage from EM65100 is biased at 1/5, 1/6, 1/7, 1/8 or 1/9. When using the internal power supply, connect a stabilizing capacitor C2 to each of pins V0 to V4. The capacitance of C2 should be determined while observing the LCD panel to be used. When using the external power supply, apply external LCD drive voltages to V0, V1, V2, V3, V4, disconnect pins CAP1+, CAP1-, CAP2+, CAP2-, CAP3+, Vcc, Vci, and VREF. When using only the voltage conversion circuit, turn off the internal booster circuit, disconnect pins CAP1+, CAP1-, CAP2+, CAP2-, CAP3+, and Vci. Derive the voltage source to be supplied to the voltage converter from Vcc pin and then input the reference voltage to VREF pin.



When using external power supply.

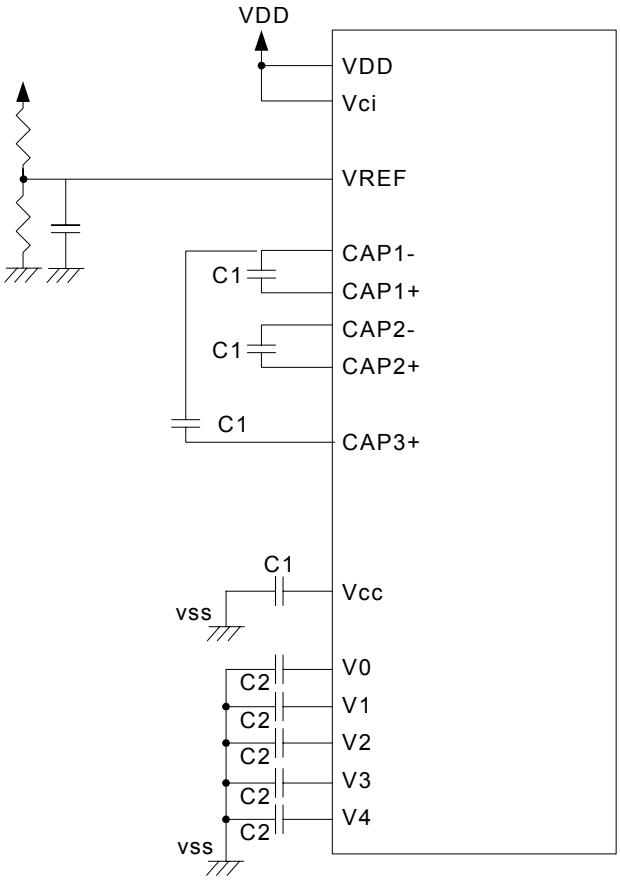


When using internal power circuit.
(4 times boosting)

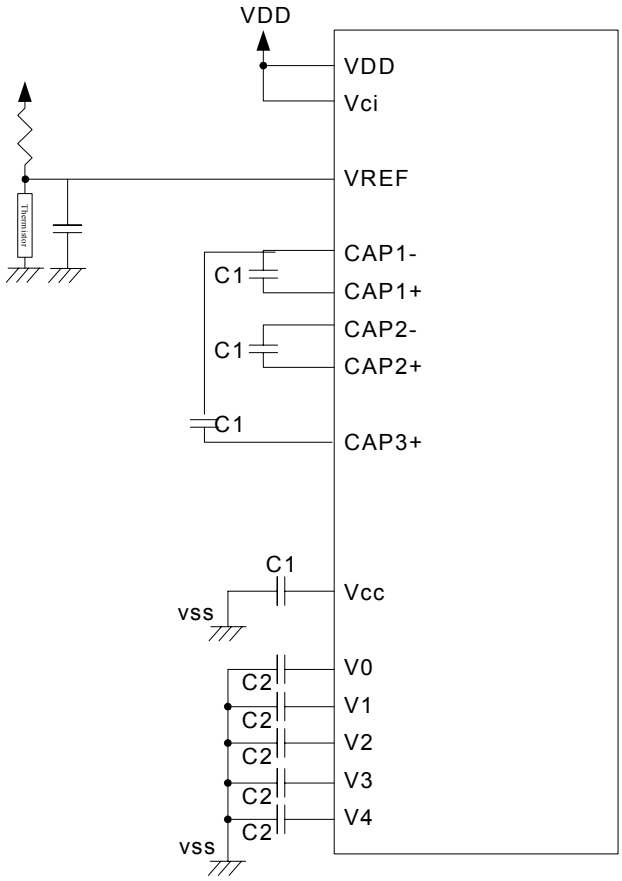
Recommended value.

C1	1.0 to 4.7 μF
C2	1.0 to 2.2 μF

Note: External Capacitance must be use B characteristic.



When using internal power circuit with external reference voltage input.
(4 times boosting)

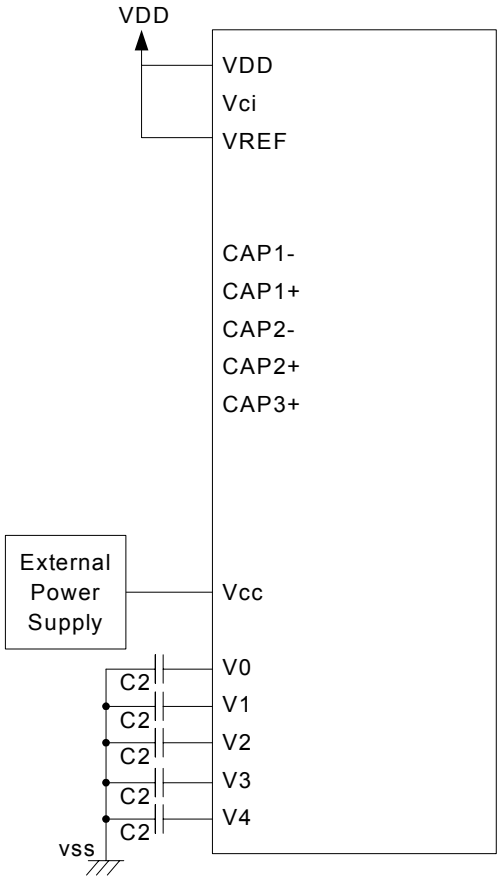


When using internal power circuit with thermistor for temperature independt.
(4 times boosting)

Recommended value.

C1	1.0 to 4.7 μF
C2	1.0 to 2.2 μF

Note: External Capacitance must be use B characteristic.



When using internal power circuit.

(Vcc supplied from external, no use boosting circuit)

Recommended value.

C2	1.0 to 2.2 μF

Note: External Capacitance must be use B characteristic.

7.23 Partial Display Function

The EM65100 has the partial display function, which can display a part of graphic display area. This function is used be set lower bias ratio, lower boost step, and lower LCD drive voltage. Since setting partial display function, EM65100 provides low power consumption. Partial display function is the most suitable for clock indication or calendar indication when a portable equipment stand-by.

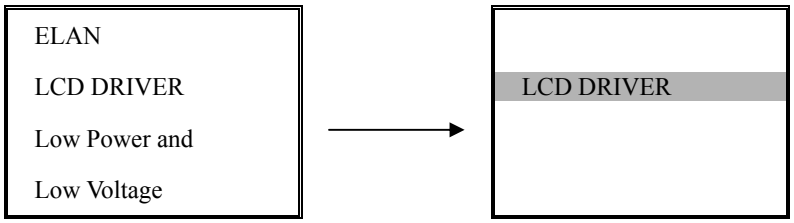
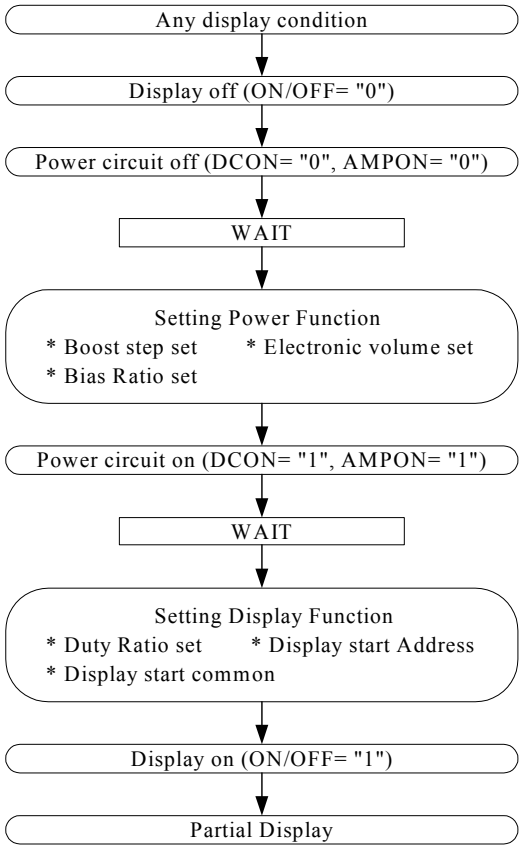


Image of partial Display

When using the partial display function, it is necessary to keep following sequence.



Select a display duty ratio for the partial display from 1/10, 1/18, 1/26, 1/34, 1/42, 1/50 and 1/58 using the DS(LCD duty ratio) register. Set the most suitable values for LCD drive bias ratio, LCD drive voltage, electronic volume, the number of boosting steps, and others according to the actually used LCD panel and the selected duty ratio.

7.24 Discharge circuit

The EM65100 has built-in the discharge circuit, which discharges electricity from capacitors for a stability of power sources(V0~V4).

The discharge circuit is valid, while the DIS register is set to "1" or the RESB pin is set "L". When the built-in power supply is used, should be set DIS="1" after the power source is turned off (DCON, AMPON)=(0, 0). And don't turn on both the built-in power source and the external power source (V0~V4, Vcc) while DIS="1".

7.25 Initialization

The EM65100 is initialized by setting RESB pin to "L". Normally, RESB pin is initialized together with MPU by connecting to the reset pin of MPU. When power ON, be sure to make RESB="L".

ITEM	Initial value
Display RAM	Not fixed
X Address	00H set
Y Address	00H set
Display starting line	Set at the first line(0H)
Display ON/OFF	Display OFF
Display Normal/Reverse	Normal
Display duty	1/69
n-line alternated	every frame unit
Common shift direction	COMO→COM67, COMA, COMB
Increment mode	Increment OFF
REF mode	Normal
Register in electronic volume	(0,0,0,0,0,0,0)
Power Supply	OFF
Display mode	Gradation display mode
Bias ratio	1/9 bias
Gradation palette 0	(0, 0, 0, 0, 0)
Gradation palette 1	(0, 0, 1, 0, 1)
Gradation palette 2	(0, 1, 0, 1, 0)
Gradation palette 3	(0, 1, 1, 1, 0)
Gradation display mode	Variable mode
RAM access data length	8-bits mode
Discharge Register	"0"
Booster frequency	(0,0)
Static Pictograh	OFF

7.26 Precaution when Power ON and Power OFF

This LSI may be permanently damaged by high current that may flow if a voltage is supplied to the LCD driver power supply while the system power supply is floating. The detail is as follows.

(i)When using as external power supply

・ Procedure for Power ON

(1) Logic system (VDD) power ON, make reset operation.

(2) Supply external LCD drive voltage to corresponding pins (V0, V1, V2, V3 and V4)

・ Procedure for Power OFF

(1) Set HALT register to "1" or make reset operation.

(2) Cut off external LCD drive voltage.

(3) Logic system(VDD) power OFF.

Note: connect the serial resistor (50 to 100Ω) or fuse to the LCD drive power V0 or Vcc(when only use internal voltage conversion circuit) of the system as a current limiter. Moreover, set up the suitable value of the resistor in consideration of LCD display grade.

(ii)When using the built-in power supply

・ Procedure for Power ON

(1) Logic system (VDD) power ON

(2) Booster circuit system (Vci) power ON

(3) Make reset operation, booster and voltage conversion circuit enable.

If VDD and Vci voltages aren't same potential, power on logic system (VDD) first.

・ Procedure for Power OFF

(1) Set HALT register to "1" or make reset operation.

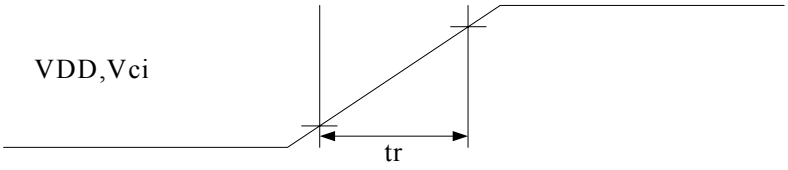
(2) Booster circuit system (Vci) power ON

(3) Logic system (VDD) power OFF.

If VDD and Vci are not same potential, cut off Vci first. After Vci, Vcc, V0, V1, V2, V3 and V4 voltages are below LCD ON voltage (threshold voltage for Liquid crystal turn on), power off logic system (VDD).

(iii)Power supply rising time

Though especially there is no constraint on the rising time of the power supply, the tr (rising time) of the following is recommended in the practical use.

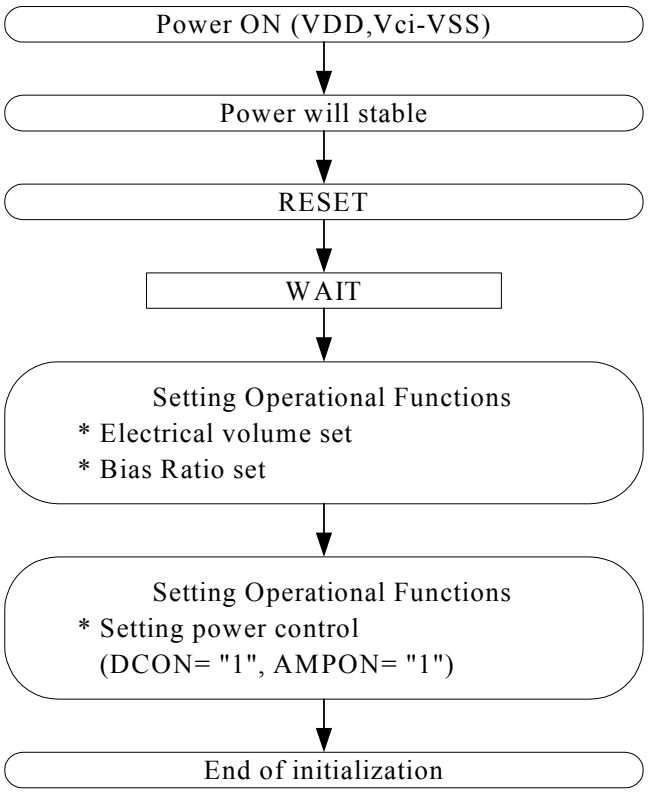


Item	Recommended rising time	Applicable Power
tr	30us ~ 10ms	VDD, Vci

Note: The rising time is the time from 10% of VDD, VEE to 90%.

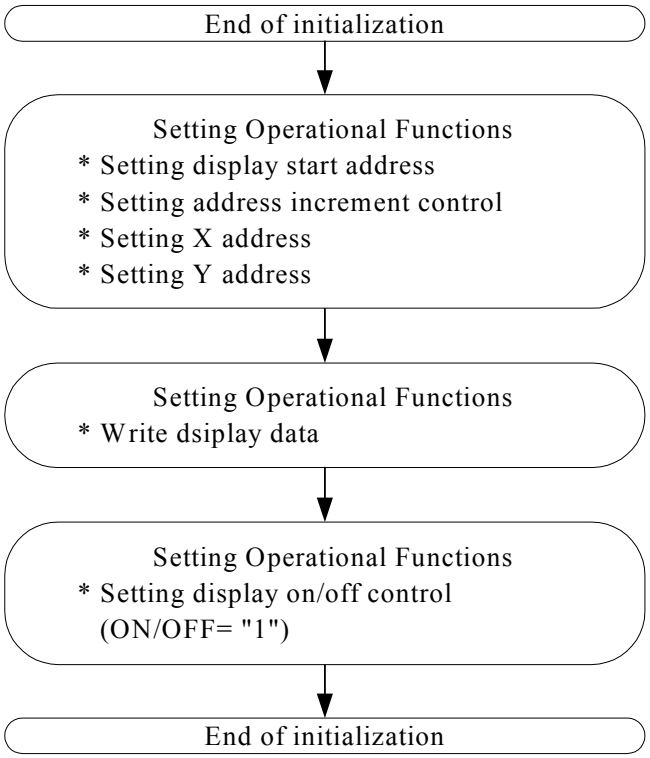
7.27 Example of Setting Registers

(1) Initialization

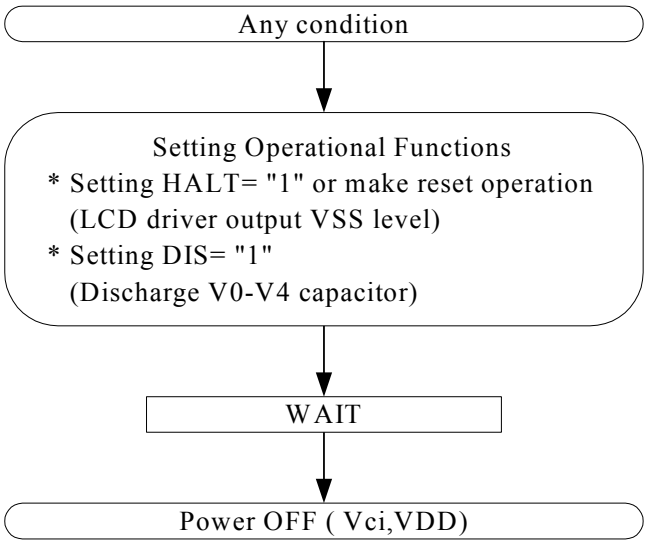


If VDD and Vci voltage are not same, connect the logic system power supply (VDD) first.

(2) Display data



(3) Power OFF



When turning off the power, set HALT command or make reset operation.

If VDD and Vci voltage are not same, disconnect the booster circuit power supply (Vci) first.

PROGRAM EXAMPLES Use Elan Risc II MCU assembly

```
;*************************************************************************
; INITIALIZATION SETTING EXAMPLE OF EM65100
;*************************************************************************
WRITEOR macro REGSEL,INSDAT ; Write macro
MOV       A,INSDAT                          ; Write data
OR        A,REGSEL                          ; Write register address
CALL      WRITE_LCD_1BYTE                   ;Write A to LCD
endm
EM65100_INI:
WRITEOR    #REREGISTERSET,#0b00000000       ;SET RE FLAG 000--> INSTRUCTION bank 0
WRITEOR    #POWERCONTROL,#0b00000001 ;      ;SET ACL(B0)=1 initialization ON
MOV        A,#50                            ;WAIT 50ms FOR EM65100 INITIAL SETTING
CALL       WAIT_A_MS
WRITEOR   #BOOSTERSET,#0b00000011           ;BOOSTER x 4 (B1,B0=1,1)
WRITEOR    # POWERCONTROL,#0b00001010       ;BOOSTER CIRCUIT(B1) ON,OPAMP(B3) ON
WRITEOR    #BIASRATIOCONTROL,#0b00000000    ;BIAS=1/9(B2,B1,B0=000)
WRITEOR    #LCDDUTYSET,#0b00000000          ;LCD DUTY SET 1/69 DUTY(B2,B1,B0=000)
WRITEOR    #INCREMENTCONTROL,#0b00000011    ;X INCREMENT(B0),Y INCREMENT(B1)
WRITEOR   #DISPLAYSTARTLINELOWER,#0b00000000   ;SET DISPLAY START LOWER LINE=0
WRITEOR   #DISPLAYSTARTLINEUPPER,#0b00000000   ;SET DSIPLAY START UPPER LINE=0
WRITEOR   #XADDRESSLOWER,#0b00000000         ;SET X ADDRESS=0
WRITEOR   #XADDRESSUPPER,#0b00000000
WRITEOR    #YADDRESSLOWER,#0b00000000        ;SET Y ADDRESS=0
WRITEOR    #YADDRESSUPPER,#0b00000000
WRITEOR    #DISPLAYCONTROL1,#0b00000000      ;DISPLAY(B0) OFF ; SHIFT(B3) = '0'
WRITEOR   #REREGISTERSET,#0b00000010         ;SET RE FLAG 010--> INSTRUCTION bank 2
WRITEOR   #ELECTRONICVOLUMEUPPER,#0b00000111   ;SET ELECTRONIC UPPER TO MAX 0111
WRITEOR   #ELECTRONICVOLUMELOWER,#0b00001111 ;SET ELECTRONIC LOWER TO MAX 1111
WRITEOR   #COMMONSTARTLINESET,#0b00000000 ;SET COMMON START FROM COM 0 (B2,B1,B0=000)
WRITEOR   #STATICPICTGRAPHCONTROL,#0b00000000   ;Static Pictograph Control =000
WRITEOR   #DISPLAYSELECTCONTROL,#0b00001000 ;PWM (B3)=1 4-gradation fixed display
WRITEOR   #DISCHARGECONTROL,#0b00000000 ;Discharge(B0) off; High power mode(B1) off
WRITEOR   #REREGISTERSET,#0b00000000 ;SET RE FLAG 000--> INSTRUCTION bank 0
RET
```

```
;*************************************************************************
; WRITE DISPLAY_PICTURE DATA INTO DISPLAY DATA RAM OF EM65100
;*************************************************************************
DATA_WRITE_65100:
BS          REG_PORTB,RS                    ; LCD RS = 1 INSTRUCTION OUTPUT
WRITEOR #XADDRESSLOWER,#0b00000000  ;SET X Add=0
WRITEOR #XADDRESSUPPER,#0b00000000
WRITEOR #YADDRESSLOWER,#0b00000000  ;SET Y Add=0
WRITEOR #YADDRESSUPPER,#0b00000000
MOV     A,#LINE_Y_MAX                   ;COMMON = 44H (68)
MOV     DRAMY,A
DATA_W1:
MOV     A,#LINE_X_MAX                    ;SEGMENT = 19h (25)
MOV     DRAMX,A
BC      REG_PORTB,RS                     ;SET LCD RS=0 DATA READ/WRITE
DATA_W2:
TBRD    01,REG_ACC                      ;WRITE LCD SCREEN FROM DATA INDEX
CALL    WRITE_LCD_1BYTE
DEC     DRAMX
JBS     REG_STATUS,F_C,DATA_W2
DEC     DRAMY
JBS     REG_STATUS,F_C,DATA_W1
BS      REG_PORTB,RS                     ;LCD RS = 1 INSTRUCTION OUTPUT
RET
;*************************************************************************
; WRITE ONE BYTE DATA INTO DDRAM (PARALLEL MODE 80 SERIES)
;*************************************************************************
;AT FIRST DEFINE A0 TO IDENTIFY DATA OR INSTRUCTION WRITE
WRITE_LCD_1BYTE:
BC      PORTB,CSB1                      ;SET CSB LOW
BC      PORTB,WRB                       ;SET /WR=0 ENABLE WRITE
MOV     PORTC,A                        ;MOVE A==> PORT_C
BS      PORTB,WRB                       ;SET /WR=1 DISABLE WRITE
BS      PORTB,CSB1                      ;SET CSB1 HIGH
RET
```

```
;*********************************************************************
;
; READ ONE BYTE DATA INTO DDRAM (PARALLEL MODE 80 SERIES)
;
;*********************************************************************
;AT FIRST DEFINE A0 TO IDENTIFY DATA OR INSTRUCTION READ
READ_LCD_1BYTE:
BC          PORTB,CSB1              ;SET CSB LOW
BC          PORTB,RDB               ;SET /RD=0 READ ENABLE
MOV           A,PORTC               ;MOVE PORT_C ==> A
BS          PORTB,RDB               ;SET /RD=1 READ DISABLE
BS          PORTB,CSB1              ;SET CSB HIGH
RET
```

8. Control Register

8.1 control register

Control Register Table (Bank 0)

Control Register	Pins (for 80-family) & Bank							Address & Code								Function
	CSB	RS	WRB	ROB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Display Data write	0	0	0	1	0/1	0/1	0/1	Write Data								Write to Display RAM
Display Data read	0	0	1	0	0/1	0/1	0/1	Read Data								Read from Display RAM
Internal Register read	0	1	1	0	0/1	0/1	0/1	*	*	*	*	Read Data				Read out Internal Register
X Address (Lower nibble) [0H]	0	1	0	1	0	0	0	0	0	0	0	AX3	AX2	AX1	AX0	Set of X direction Address in display RAM
X Address (Upper nibble) [1H]	0	1	0	1	0	0	0	0	0	0	1	*	*	*	AX4	Set of X direction Address in display RAM
Y Address (Lower nibble) [2H]	0	1	0	1	0	0	0	0	0	1	0	AY3	AY2	AY1	AY0	Set of X direction Address in display RAM
Y Address (Upper nibble) [3H]	0	1	0	1	0	0	0	0	0	1	1	*	AY6	AY5	AY4	Set of X direction Address in display RAM
Display start address (Lower nibble) [4H]	0	1	0	1	0	0	0	0	1	0	0	LA3	LA2	LA1	LA0	Set address of display RAM making common starting line display
Display start address (Upper nibble) [5H]	0	1	0	1	0	0	0	0	1	0	1	*	LA6	LA5	LA4	Set address of display RAM making common starting line display
n-line altemation (Lower nibble) [6H]	0	1	0	1	0	0	0	0	1	1	0	N3	N2	N1	N0	Set the number of altemated reverse line
n-line altemation (Upper nibble) [7H]	0	1	0	1	0	0	0	0	1	1	1	*	N6	N5	N4	Set the number of altemated reverse line
Display control (1) [8H]	0	1	0	1	0	0	0	1	0	0	0	SHIFT	MON	ALLON	ON/OFF	SHIFT: Select common shift direction MON: Select Monochrome/gradation ALLON: All display ON ON/OFF: Display ON/OFF control
Display control (2) [9H]	0	1	0	1	0	0	0	1	0	0	1	REV	NLIN	*	REF	REV: Display normal/reverse NLIN: n line reverse control REF: Seqment normal/reverse
Increment control [AH]	0	1	0	1	0	0	0	1	0	1	0	*	AIM	AYI	AXI	AIM: Select increment mode AYI: Y increment, AXI: X increment
Power control [BH]	0	1	0	1	0	0	0	1	0	1	1	AMPON	HALT	DCON	ACL	AMPON: Intemal AMP. ON HALT: Power saving DCON: Boosting circuit ON ACL: Resetting
LCD Duty Ratio [CH]	0	1	0	1	0	0	0	1	1	0	0	*	DS2	DS1	DS0	Set LCD drive duty ratio
Booster [DH]	0	1	0	1	0	0	0	1	1	0	1	*	*	VU1	VU0	Set number of boosting step for booster circuit
Bias ratio control [EH]	0	1	0	1	0	0	0	1	1	1	0	*	B2	B1	B0	Set bias ratio for LCD driving voltage
Register Access Control [FH]	0	1	0	1	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	TST0: for LS1 test,must set to "0" RE: set register bank number

Note: The "※" mark means "don't care"

Parentheses [ ] shows address for control register.

Control Register Table (Bank 1)

Control Register	Pins (for 80-family) & Bank							Address & Code								Function
	CSB	RS	WRB	ROB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Gray Mode--White 1stFR [0H]	0	1	0	1	0	0	1	0	0	0	0	WA3	WA2	WA1	WA0	Set White 1st frame
Gray Mode--White 2ndFR [1H]	0	1	0	1	0	0	1	0	0	0	1	WB3	WB2	WB1	WB0	Set White 2nd frame
Gray Mode--White 3rdFR [2H]	0	1	0	1	0	0	1	0	0	1	0	WC3	WC2	WC1	WC0	Set White 3rd frame
Gray Mode--White 4thFR [3H]	0	1	0	1	0	0	1	0	0	1	1	WD3	WD2	WD1	WD0	Set White 4th frame
Gray Mode--Light Gray 1stFR [4H]	0	1	0	1	0	0	1	0	1	0	0	LA3	LA2	LA1	LA0	Set Light Gray 1st frame
Gray Mode--Light Gray 2ndFR [5H]	0	1	0	1	0	0	1	0	1	0	1	LB3	LB2	LB1	LB0	Set Light Gray 2nd frame
Gray Mode--Light Gray 3rdFR [6H]	0	1	0	1	0	0	1	0	1	1	0	LC3	LC2	LC1	LC0	Set Light Gray 3rd frame
Gray Mode--Light Gray 4thFR [7H]	0	1	0	1	0	0	1	0	1	1	1	LD3	LD2	LD1	LD0	Set Light Gray 4th frame
Gray Mode--Dark Gray 1stFR [8H]	0	1	0	1	0	0	1	1	0	0	0	DA3	DA2	DA1	DA0	Set Dark Gray 1st frame
Gray Mode--Dark Gray 2ndFR [9H]	0	1	0	1	0	0	1	1	0	0	1	DB3	DB2	DB1	DB0	Set Dark Gray 2nd frame
Gray Mode--Dark Gray 3rdFR [AH]	0	1	0	1	0	0	1	1	0	1	0	DC3	DC2	DC1	DC0	Set Dark Gray 3rd frame
Gray Mode--Dark Gray 4thFR [BH]	0	1	0	1	0	0	1	1	0	1	1	DD3	DD2	DD1	DD0	Set Dark Gray 4th frame
Gray Mode--Black 1stFR [CH]	0	1	0	1	0	0	1	1	1	0	0	BA3	BA2	BA1	BA0	Set Back 1st frame
Gray Mode--Black 2ndFR [DH]	0	1	0	1	0	0	1	1	1	0	1	BB3	BB2	BB1	BB0	Set Back 2nd frame
Register Access Control [FH]	0	1	0	1	0/1	0/1	0/1	1	1	1	1	TS T0	RE2	RE1	RE0	TST0: for LS1 test,must set to "0" RE: set register bank number

Note: The "※" mark means "don't care"

Parentheses [ ] shows address for control register.

Caution: Different gradation levels can't be set in the same palette.

Control Register Table (Bank 2)

Control Register	Pins (for 80-family) & Bank							Address & Code								Function
	CSB	RS	WRB	ROB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Gray Mode--Black 3rdFR [0H]	0	1	0	1	0	1	0	0	0	0	0	BC3	BC2	BC1	BC0	Set Back 3d frame
Gray Mode--Black 4ndFR [1H]	0	1	0	1	0	1	0	0	0	0	1	BD3	BD2	BD1	BD0	Set Back 4th frame
Display start common [6H]	0	1	0	1	0	1	0	0	1	1	0	*	SC2	SC1	SC0	Set Common Driver Start Line
Static Pictograph control [7H]	0	1	0	1	0	1	0	0	1	1	1	*	*	SPC1	SPC0	Set Static Pictgraph Drive Mode
Display Select Control [8H]	0	1	0	1	0	1	0	1	0	0	0	PWM	*	*	*	Select PWM Mode
Electronic Volume (Lower nibble) [AH]	0	1	0	1	0	1	0	1	0	1	0	DV3	DV2	DV1	DV0	Set Electronic Volume Register (lower code)
Electronic Volume (Upper nibble) [BH]	0	1	0	1	0	1	0	1	0	1	1	*	DV6	DV5	DV4	Set Electronic Volume Register (upper code)
Register read Control [CH]	0	1	0	1	0	1	0	1	1	0	0	RA3	RA2	RA1	RA0	Set Register Address for read
Select Rf [DH]	0	1	0	1	0	1	0	1	1	0	1	*	RF2	RF1	RF0	Select Rf ratio of OSC circuit
Extended power control [EH]	0	1	0	1	0	1	0	1	1	1	0	BF1	BF0	HPM	DIS	DIS:Discharge capacitance of V0,V1,V2,V3,V4 Pins HPM : high power mode set BF: Set Booster frequency
Register Access Control [FH]	0	1	0	1	0/1	0/1	0/1	1	1	1	1	TS T0	RE2	RE1	RE0	TST0: for LS1 test,must set to "0" RE: set register bank number

Note: The "※" mark means "don't care"

Parentheses [ ] shows address for control register.

8.2 Functions of Control Registers

The EM65100 has many control registers. In case of control register access, upper nibble of data bus (D7~D4) represent register address, lower nibble of data bus (D3~D0) represent data. The access example is shown in the following. The Pins (CSB, RS, RDB, WRB) setting are for 80-family MPU interface. Only the setting of terminal (RDB,WRB) is different, when it is accessed by the 68-fanily MPU.

(Example) X Address

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	AX3	AX2	AX1	AX0

Register address | Data

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

Pins setting | Register Bank

In the writing to the control register, it is used directly as addressing D7~D4 of the data bus. In case of register read, first set RA register for specific register address, next can read specific register. Therefore, it is need 2-step for register read. Then, specific register output to D3~D0 of data bus. Except D3~D0 of data bus are all "H". Prohibit access to undefined register address area. When RS is "L", all read/write operations are accessed to display RAM. Then data bus doesn't include register address. In case of write, D3~D0 data is written to the register designated at D7~D4 in rising edge of the WRB signal. In case of read, register can output to data bus is RDB active period. Control register and display RAM are the equal access timing.

8.2.1 Data Write to Display RAM

D7	D6	D5	D4	D3	D2	D1	D0
Display RAM write data							

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	0	1	0	0/1	0/1	0/1

The Display RAM data of 8-bit are written in the designated X and Y address.

8.2.2 Data Read from Display RAM

D7	D6	D5	D4	D3	D2	D1	D0
Display RAM read data							

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	0	0	1	0/1	0/1	0/1

The 8-bit contents of Display RAM designated in X. and Y address and read out.
Immediately after data are set in X and Y address, dummy read is necessary one time.

8.2.3 Internal Register Data Read

D7	D6	D5	D4	D3	D2	D1	D0
※	※	※	※	Internal Register read data			

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	0	1	0/1	0/1	0/1

※ Mark shows "Don't care"

This command is used to read data from an internal register. Before executing the command. You need to set the address and RE flag for reading data from the internal register.

8.2.4 X Address Register Set

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	AX3	AX2	AX1	AX0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {AX3, AX2, AX1, AX0}= 0H, read address: 0H)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	※	※	※	AX4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {AX4}= 0H, read address: 1H)

※ Mark shows "Don't care"

The AX register set to X-direction address of display RAM. In data setting, lower place and upper place are divided with 4-bit and 1-bit respectively. Be sure to do setting from the lower bit.

8.2.5 Y Address Register Set

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	AY3	AY2	AY1	AY0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the tine of reset: {AY3, AY2, AY1, AY0}=0H, read address: 2H)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	※	AY6	AY5	AY4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {AY6, AY5, AY4}=0H, read address: 3H)

※ Mark shows "Don't care"

The AY register set to Y-direction address of display RAM. In data setting, lower place and upper place are divided with 4-bit and 3-bit respectively. 00H to 44H are applicable to the values for AY6 to AY0, and 45H to FFH are not permitted. The address for (AY6 to AY0) = 43H, 44H are in the display RAM area for icon display.

8.2.6 Display Start Address Register Set

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	LA3	LA2	LA1	LA0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the tine of reset: {LA3, LA2, LA1, LA0}=0H, read address: 4H)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	※	LA6	LA5	LA4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {LA6,LA5, LA4}=0H, read address: 5H)

※ Mark shows "Don't care"

This display line address is require to designate, and the designated address becomes the display line of COM0. The display of LCD panel is indicated in the increment direction of the designated display starting address to the line address.

LA6	LA5	LA4	LA3	LA2	LA1	LA0	Line Address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
			:				
1	0	0	0	0	1	0	66

8.2.7 n Line Alternated Register Set

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	N3	N2	N1	N0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the tine of reset: {N3, N2, N1, N0}=0H, read address: 6H)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	※	N6	N5	N4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {N6, N5, N4}=0H, read address: 7H)

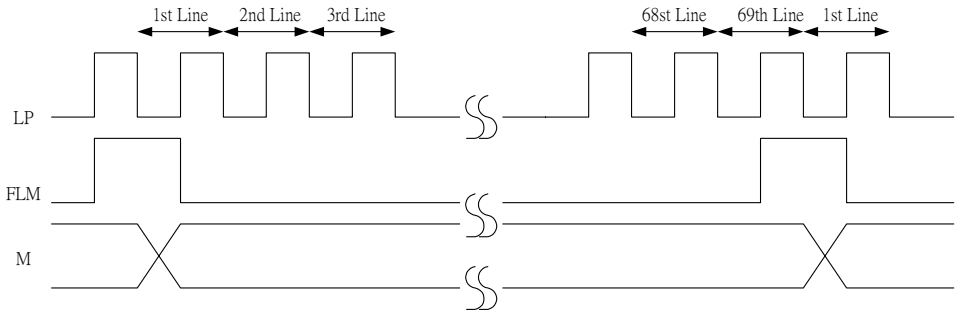
※ Mark shows “Don’t care”

The reverse line number of LCD alternated drive is required to set in the register. The line number has a limit, must keeps between from 2 to 67 lines. The values set up by the alternated register become enable when NLIN control bit is “1”. When NLIN control bit is “0”, alternated drive waveform reverses by each frame is generated.

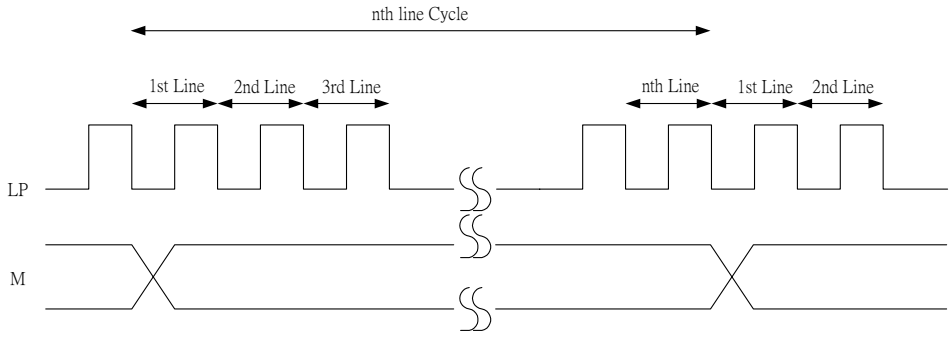
N6	N5	N4	N3	N2	N1	N0	Line Address
0	0	0	0	0	0	0	-
0	0	0	0	0	0	1	2
			:				
1	0	0	0	0	1	0	67

Alternated Timing

(i) NLIN=”0” (in case of 1/69 DUTY Display)



(ii) NLIN="1"



8.2.8 Display Control (1) Register Set

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	SHIFT	MON	ALL ON	ON/ OFF

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the tine of reset: {SHIFT, MON, ALLON, ON/OFF}=0H, read address: 8H)

Various control of display is set up.

ON/OFF

To control ON/OFF of display

ON/OFF = "0": Display OFF

ON/OFF = "1": Display ON

ALLON

Regardless of the data for display, all is on.

This control has priority over display normal/reverse commands.

ALLON = "0": Normal display

ALLON = "1": All display lighted

MON

Select Monochrome or Gradation display

MON = "0": Gradation display mode

MON = "1": Monochrome display mode

SHIFT

The shift direction of display scanning data in the common driver output is selected.

SHIFT = "0": COM0→COM66 shift-scan

SHIFT = "1": COM66 →COM0 shift-scan

8.2.9 Display Control (2) Register

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	REV	NLIN	※	REF

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the tine of reset: {REV, NLIN, REF}=0H, read address: 9H)

※ Mark shows "Don't care"

Various control of display is set up.

REF

When MPU accesses to display RAM, the X address and data can reverse. The REF function shows in the table below: The order of segment driver output can be reversed by register by register setting, lessening the limitation in placing IC when assembling a LCD module.

NLIN

The NLIN control n-line alternated drive.

NLIN = "0": n-line alternated drive OFF. In each frame, the alternated signals (internal M) are reversed.

NLIN ="1": n-line alternated drive ON. According to data set up in n-line alternated register, the alternation is made.

REV

Corresponding to the data of display RAM, the lighting or not-lighting of the display is set up.

REV ="0": When RAM data at "H", LCD at ON voltage (normal)

REV ="1": When RAM data at "L", LCD at ON voltage (reverse)

8.2.10 Increment Control Register Set

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	※	AIM	AYI	AXI

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

※ Mark shows "Don't care"

(At the tine of reset: {AIM, AYI, AXI}=0H, read address: AH)

The increment mode is set up when accessing to display RAM. By AIM, AYI, AXI register, the setting up of increment operation/non-operation for the X address counter and the Y address counter every write access or every read access to display RAM is possible. In setting to this control register, the increment operation of address can be made without setting successive address for writing data or for reading data to display RAM from MPU.

After the increment control register has been set. be sure to assign address to the X and Y address registers starting from the lowest bit. Because it is not assuring the data of X and Y address register after setting increment control register. The increment control of X and Y address by AIM, AYI, AXI registers is as follows.

AIM	*Address Increment Timing*
0	When writing to Display RAM or reading from Display RAM This is effective when access to successive address area
1	Only when writing to Display RAM This is effective the case of "Read Modify Write

AYI	*AXI*	*Select Address Increment Operation*	*Remark*
0	0	Address is not increment	(1)
0	1	X-Address is increment	(2)
1	0	Y-Address is increment	(3)
1	1	X and Y both are increment	(4)

(1) Regardless of AIM, no increment for AX and AY register.

(2) According to the setting-up of AIM, automatically change X address.

In accordance with the REF register, AX register and X address becomes as follows.

REF	Transition of AX Register	Transition of X Address
0	00H→ 01H→.....→ max	Same as AX register
1		max→ maxH →..... →00H

Note: maxH: The internal maximum X-address in each access mode.

(3) According to the setting-up of AIM, automatically change Y address. Regardless of REF, increment by loop of

Transition of AY Register	Transition of Y Address
00H→ 01H→.....→ 44H	Same as AY register

(4) According to the setting-up of AIM, cooperative change X and Y address. When the X address exceed maxH, Y address increment occurs.

REF	Transition of AX and AY Register	Transition of X and Y Address
0	AX: 00H → 00H →– – → max	Same as AX and AY register
1	AY: When each AX exceed maxH, increment AY 00H → 00H →– – → 44H	AX: max→ maxH →– – →00H AY: Same as AY register

Note: maxH: The internal maximum X-address in each access mode.

In each operation mode, the following increment operation is performed:

(i) When gradation display mode and 8-bit access are selected: Address are incremented as described above.

(ii) When monochrome display mode and 8-bit access are selected:

In the monochrome display mode, 0H to 19H are available for X-addresses in the access area.

8.2.11 Power Control Register

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	AMP ON	HAL T	DCO N	ACL

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the tine of reset: {AMPON, HALT, DCON, ACL}=0H, read address: BH)

ACL

The internal circuit can be initialized.

ACL = “0”: Normal operation

ACL = “1”: Initialization ON

When the reset operation begins internally after ACL register sets to “1”, the ACL register is automatically cleared to “0”. The internal reset signal has been generated with a clock (built-in oscillation circuit or CK input) for the display. Therefore, install the WAIT period for the display clock two cycles at least. After WAIT period, next operation can handle. Since built-in oscillation circuit ,the setting of the ACL register becomes the invalidity.

DCON

The internal booster circuit is set ON/OFF

DCON = “0”: Booster circuit OFF

DCON=”1”: Booster circuit ON

HALT

The conditions of power saving are set ON/OFF by this command.

HALT = “0”: Normal operation

HALT=”1”: Power-saving operation

When setting in the power-saving state, the consumed current can be reduced to a value near to the standby current.

The internal condition at power saving are as follows.

(a) The oscillating circuit and power supply circuit are stopped.

(b) The LCD drive is stopped, and output of the segment driver and common driver are VSS level.

(c) The clock input from CK pin is inhibited.

(d) The contents of Display RAM data are maintained.

(e) The operational mode maintains the state of command execution before executing power saving command.

AMPON Command

The internal OP-AMP circuit block (voltage regulator, electronic volume, and voltage conversion circuit) is set ON/OFF by this command.

AMPON = "0": The internal OP-AMP circuit OFF

AMPON = "1": The internal OP-AMP circuit ON

8.2.12 LCD Duty Set

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	※	DS2	DS1	DS0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {DS2, DS1, DS0}=0H, read address: CH)

※ **Mark shows "Don't care"**

The DS register set to LCD display duty.

DS2	DS1	DS0	Display width and Duty
0	0	0	67-dot width display in Y-direction, 1/69 duty
0	0	1	56-dot width display in Y-direction, 1/58 duty
0	1	0	48-dot width display in Y-direction, 1/50 duty
0	1	1	40-dot width display in Y-direction, 1/42 duty
1	0	0	32-dot width display in Y-direction, 1/34 duty
1	0	1	24-dot width display in Y-direction, 1/26 duty
1	1	0	16-dot width display in Y-direction, 1/18 duty
1	1	1	8-dot width display in Y-direction, 1/10 duty

Partial display can be made possible by setting an arbitrary duty ratio.

8.2.13 Booster Set

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	※	※	VU1	VU0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: { VU1, VU0}=0H, read address: DH)

※ Mark shows "Don't care"

The booster steps set to VU register

VU1	*VU0*	*Booster Operation*
0	0	Booster disable (No operation)
0	1	2 times voltage output
1	0	3 times voltage output
1	1	4 times voltage output

8.2.14 Bias Setting Register Set

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
1	1	1	0	※	B2	B1	B0

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	0	0	0

(At the time of reset: {B2, B1, B0}=0H, read address: EH)

※ Mark shows "Don't care"

This register is used to set a bias ratio. A bias ratio can be selected from 1/9, 1/8, 1/7, 1/6, and 1/5 by setting B2, B1, and B0.

B2	*B1*	*B0*	*Bias*
0	0	0	1/9 Bias
0	0	1	1/8 Bias
0	1	0	1/7 Bias
0	1	1	1/6 Bias
1	0	0	1/5 Bias
1	0	1	Prohibit code
1	1	0	Prohibit code
1	1	1	Prohibit code

8.2.15 Register Access Control

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
1	1	1	1	TST0	RE2	RE1	RE0

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	0/1	0/1	0/1

(At the time of reset: {TST0, RE2, RE1, RE0}=0H, read address: FH)

※ Mark shows "Don't care"

The RE register set to number of register bank. Access to each control register, set RE register at first.

The TST0 register use for test of LSI, Therefore this register must be set to "0"

8.2.16 FRC(Frame Rate Control) and PWM(Pulse Width Modulation) control Register data

Caution: Different gradation levels can't be set in the same palette.

Gray Mode--White

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
0	0	0	0	WA3	WA2	WA1	WA0

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	0	0	1

(Read address: 0H)

(At the time of reset: WA3~WA0 = "0000")

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	WB3	WB2	WB1	WB0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(Read address: 1H)

(At the time of reset:WB3~WB0 = “0000”)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	WC3	WC2	WC1	WC0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(Read address: 2H)

(At the time of reset:WC3~WC0 = “0000”)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	WD3	WD2	WD1	WD0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(Read address: 3H)

(At the time of reset:WD3~WD0 = “0000”)

Gray Mode--Light gray

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	LA3	LA2	LA1	LA0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(Read address: 4H)

(At the time of reset:LA3~LA0 = “0101”)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	LB3	LB2	LB1	LB0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(Read address: 5H)

(At the time of reset: LB3~LB0 = “0101”)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	LC3	LC2	LC1	LC0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(Read address: 6H)

(At the time of reset: LC3~LC0 = “0101”)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	LD3	LD2	LD1	LD0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(Read address: 7H)

(At the time of reset: LD3~LD0 = “0101”)

Gray Mode--Dark gray

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	DA3	DA2	DA1	DA0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(Read address: 8H)

(At the time of reset: DA3~DA0 = "1010")

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	DB3	DB2	DB1	DB0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(Read address: 9H)

(At the time of reset: DB3~DB0 = "1010")

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	DC3	DC2	DC1	DC0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(Read address: AH)

(At the time of reset: DC3~DC0 = "1010")

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	DD3	DD2	DD1	DD0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(Read address: BH)

(At the time of reset: DD3~DD0 = "1010")

Gray Mode--Black

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	BA3	BA2	BA1	BA0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(Read address: CH)

(At the time of reset: BA3~BA0 = "1111")

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	BB3	BB2	BB1	BB0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(Read address: DH)

(At the time of reset: BB3~BB0 = "1111")

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	BC3	BC2	BC1	BC0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(Read address: 0H)

(At the time of reset: BC3~BC0 = "1111")

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	BD3	BD2	BD1	BD0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(Read address: 1H)

(At the time of reset: BD3~BD0 = "1111")

Set Gray Scale Mode

RAM Data[2n:2n+1] are used to specify the four gray level's pulse width

RAM DATA		Gray Mode	frame			
2n	2n+1		1st	2nd	3rd	4th
0	0	White	WA	WB	WC	WD
1	0	Light Gray	LA	LB	LC	LD
0	1	Dark Gray	DA	DB	DC	DD
1	1	Black	BA	BB	BC	BD

These gradation palette register set up gradation level. The EM65100 has 16 gradation levels. Gradation level table

[Three groups of palettes WAj~WDj, LAj~LDj, DAj~DDj, and BAj~BDj (j=0-3) are available]

Palette	Gradation level	Remark
0 0 0 0	0	Gradation palette 0
0 0 0 1	1/15	
0 0 1 0	2/15	
0 0 1 1	3/15	
0 1 0 0	4/15	
0 1 0 1	5/15	Gradation palette 1
0 1 1 0	6/15	
0 1 1 1	7/15	
1 0 0 0	8/15	
1 0 0 1	9/15	
1 0 1 0	10/15	Gradation palette 2
1 0 1 1	11/15	
1 1 0 0	12/15	
1 1 0 1	13/15	
1 1 1 0	14/15	
1 1 1 1	15/15	Gradation palette 3

Caution: Different gradation levels can't be set in the same palette.

8.2.17 Display Start Common Set

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	※	SC2	SC1	SC0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(At the time of reset:{ SC2,SC1,SC0}=0H, read address: 6H)

※ Mark shows "Don't care"

The SC register set up the scanning start output of the common driver.

SC2	*SC1*	*SC0*	*Display starting common when SHIFT=0*	*Display starting common when SHIFT=1*
0	0	0	COM0~	COM66~
0	0	1	COM8~	COM58~
0	1	0	COM16~	COM50~
0	1	1	COM24~	COM42~
1	0	0	COM32~	COM34~
1	0	1	COM40~	COM26~
1	1	0	COM48~	COM18~
1	1	1	COM56~	COM10~

SHIFT="0": COM0→ COM66 shift-scan

SHIFT="1": COM66→ COM0 shift-scan

8.2.18 Static Pictograph Control

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	※	※	SPC1	SPC0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

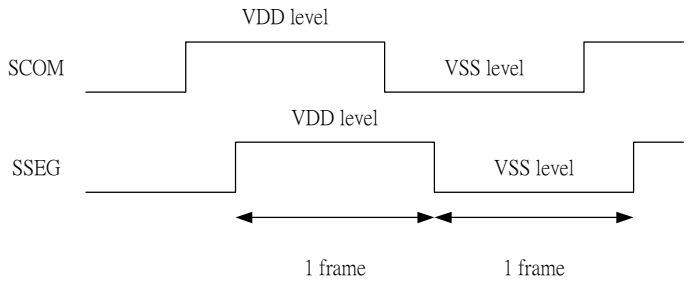
(At the time of reset:{ SPC1,SPC0}=0H, read address: 7H)

Mark shows "Don't care"

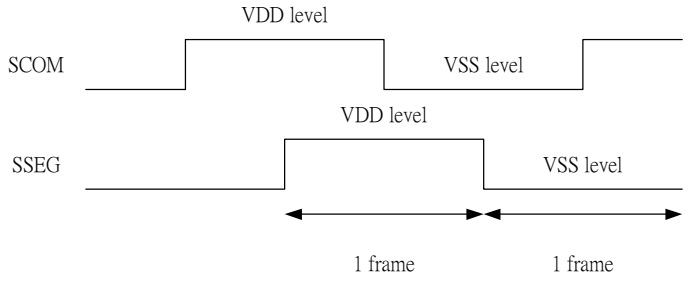
This command is used to select a signal to drive static pictograph.

SPC1	*SPC0*	*Signal for static pictograph*
0	0	VSS level is always output at SCOM and SSEG
0	1	Phase deviates by 45 degrees at SCOM and SSEG
1	0	Phase deviates by 90 degrees at SCOM and SSEG
1	1	Phase deviates by 135 degrees at SCOM and SSEG

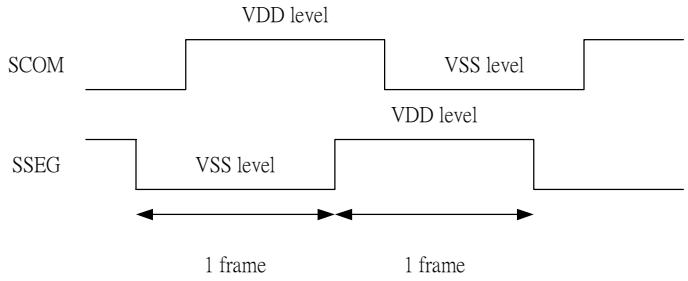
Drive waveform when (SPC1, SPC0) =(0, 1)



Drive waveform when (SPC1, SPC0) =(1, 0)



Drive waveform when (SPC1, SPC0) =(1, 1)



8.2.19 Display Select Control

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	PWM	※	※	※

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(At the time of reset: {PWM } = 0H, read address: 8H)

PWM

The PWM register selection the gradation display mode.

PWM = “0”: Variable display mode using 4 gradations selected from 16 gradations

PWM = “1”: 4-gradation fixed display mode

8.2.20 Electronic Volume Register Set

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	DV3	DV2	DV1	DV0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(Read address: AH)

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	※	DV6	DV5	DV4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(Read address: BH)

(At the time of reset: {DV6~DV0} = 00H)

※ Mark shows "Don't care"

The DV register can control V0 voltage.

The DV register has 7-bits, so can select 128 level voltage.

DV6	DV5	DV4	DV3	DV2	DV1	DV0	Output voltage
0	0	0	0	0	0	0	Smaller
0	0	0	0	0	0	1	:
			:				:
			:				:
1	1	1	1	1	1	0	:
1	1	1	1	1	1	1	Larger

The LCD driver voltage V0 is determined by VREF level, N times charge pump and electronic volume code equation.

When 4 times charge pump, the V0 voltage is equation (1)

V0 = 0.9 * VREF * [2 + (2 DV/127)] ----------(1)

When 3 times charge pump, the V0 voltage is equation (2)

V0 = 0.9 * VREF * [1 + (85 + 2 DV/169)] ----------(2)

When 2 times charge pump, the V0 voltage is equation (3)

V0 = 0.9 * VREF * [1 + (DV/127)] ----------(3)

(DV: DV6 to DV0 register values)

In order to prevent transient voltage from generating when an electronic volume code is set, the circuit design is such that the set value is not reflected as a level immediately after only the upper bits (DV6-DV4) of the electronic code have been set. The set value becomes valid when the lower bits (DV3-DV0) of the electronic control volume code have also been set.

8.2.21 Internal Register Read Address

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	RA3	RA2	RA1	RA0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(At the time of reset: {RA3, RA2, RA1, RA0} = 0H, Read address: CH)

The RA register set to specify the address for register read operation. The EM65100 has many registers and has register bank. Therefore, it is need 4-steps to read to read the specific register in maximum case.

(1) Write 02H to RE register for access to RA register.

(2) Writes specific register address to RA register.

(3) Write specific register bank to RE register.

(4) Read specific contents.

8.2.22 Resistance Ratio of CR Oscillator

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	※	RF2	RF1	RF0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(At the time of reset: {RF2, RF1, RF0} = 0H, read address: DH)

※ Mark shows "Don't care"

The RF registers can control resistance ratio of CR oscillator. Therefore frame frequency can change RF registers setting. When change RF registers value, should be need to check LCD display quality.

RF2	RF1	RF0	Operation
0	0	0	Initial Resistance Ratio
0	0	1	0.8 times of initial Resistance Ratio
0	1	0	0.9 times of initial Resistance Ratio
0	1	1	1.1 times of initial Resistance Ratio
1	0	0	1.2 times of initial Resistance Ratio
1	0	1	Prohibit Code
1	1	0	Prohibit Code
1	1	1	Prohibit Code

8.2.23 Extended power control

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	0	BF1	BF0	HPM	DIS

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

At the time of reset: {HPM, DIS} = 0H, {BF1,BF0}=0H;read address: EH)

※mark shows "Don't care"

The DIS register can control capacitors discharged that connected between the power supply V1-V4 for LCD drive voltage and VSS. V0 is discharged to VDD.

DIS = "0": Discharge OFF

DIS = "1": Discharge start

The HPM register is the power control for the power supply circuit for liquid crystal drive.

HPM = “H”: High power mode

HPM = “L”: Normal mode

BF1~BF0: The operating frequency in the booster is selected. When the boosting frequency is high, the driving ability of booster become high, but the current consumption is increased. Adjust the boosting frequency considering the external capacitors and the current consumption.

BF1	*BF0*	*Operating clock frequency in the booster*
0	0	1.5K Hz * 8
0	1	1.5K Hz * 4
1	0	1.5K Hz * 2
1	1	1.5 K Hz

9. Relationship between Setting and Common/Display RAM

The relationship between the COM pin numbers and the addresses in the Y-direction on the display RAM changes according to the SHIFT command. LCD Duty Set command. Display Starting Common Position Set command, and Display Starting Line Set command.

When "0" is selected for the display starting line:
The relationship between the COM pin and the addresses in the vertical direction of the display RAM (hereafter called MY) changes on an 15 dots basis according to the LCD Duty Set command and the Display Starting Common Position Set command. When the SHIFT bit is "0", the common position change in the forward direction. When "1" they change reverse direction. When "0" is selected as the values for LA6 to LA0 in the Display Starting Line Set command, the MY number corresponding to the display starting position is "0". The MY numbers are sequentially shifted backward when display occurs. In any case, the relations of COMA = MY67 and COMB = MY68 do not change.

When non-zero is selected for the display starting line:
The relationship between the COM pins and the addresses in the vertical direction on the display RAM, MY changes on an 15 dots basis according to the information in the LCD Duty Set command and Display Starting Common Position Set command. The common positions change in the forward when the SHIFT bit is "0", and change in the reverse direction when the SHIFT bit is "1". If non-zero is selected for the values for LA6 to LA0 by the Display Starting Line set command. the MY number corresponding to the display starting position shifts by the set value. The MY number shifts backward when display occurs. If it exceeds 66, it returns to 0, and the shifts sequentially. In any case, the relations of COMA = MY67 and COMB = MY68 do not change.

10. Absolute maximum ratings

10.1 Absolute maximum ratings

Item	*Symbol*	*Condition*	*Pin use*	*Rating*	*Unit*
Supply voltage (1)	VDD	Ta=25℃	VDD	-0.3 ~ + 4.0	V
Supply voltage (2)	Vci		Vci	-0.3 ~ + 4.0	V
Supply voltage (3)	Vcc		Vcc	-0.3 ~ + 13.0	V
Supply voltage (4)	V0		V0	-0.3 ~ + 13.0	V
Supply voltage (5)	V1,V2,V3,V4		V1,V2,V3,V4	-0.3 ~ V0+ 0.3	V
Input voltage	VI		*1	-0.3 ~ VDD+ 0.3	V
Storage temperature	Tstg			-45 ~ +125	℃

※1: D0~D7, CSB, RS, M86, P/S, WRB, RDB, CK, CKS, RESB, TEST, VREF Pins

10.2 Recommended operating conditions

Item	*Symbol*	*Application Pin*	*Min.*	*Max.*	*Unit*	*Note*
Supply voltage	VDD1	VDD	1.8	3.3	V	*1
	Vci	Vci	2.4	3.3	V	*2
Operating voltage	V0	V0	5	12	V	*3
	Vcc	Vcc		12	V	
	VREF	VREF	2.4	3.3	V	*4
Operating temperature	Topr		-30	85	℃	

※1 shows applying voltage to VSS pin.

※2 shows applying voltage to VSS pin. Usually, if applying voltage is same as VDD. Connect to VDD pin.

※3 shows the voltage relationship of V0>V1>V2>V3>V4>VSS is required.

※4 shows applying voltage to VSS pin.. In the case of using the voltage regulator. The voltage relationship of VREF≦Vci is required.

11.DC characteristics

VSS=0V , VDD = 1.8~3.3V , Ta = -30 ~85 ℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
High level input voltage	VIH		0.8VDD	0.9VDD	VDD	V	※ 1
Low level input voltage	VIL		0	0.1VDD	0.2VDD	V	※ 1
High level output current	IOH1	VOH = VDD-0.4V	-2.4	-3.2	-4.5	mA	※ 2
Low level output current	IOL1	VOL= 0.4V	2.4	3.2	4.5	mA	※ 2
Input leakage current	ILI	VI = VSS or VDD	-2	0	2	µA	※ 3
Output leakage current	ILO	VI = VSS or VDD	-2	0	2	µA	※ 4
LCD driver output resistance	RON	Δ |Von| = 0.5V, V0=10V	1.0	1.3	1.6	KΩ	※ 5
		Δ |Von| = 0.5V, V0=6V	1.2	1.7	2.2		
LCD driver output resistance	RON	Δ |Von| = 0.5V, VDD=3V	0.3	0.5	0.7	KΩ	※ 6
Standby current through VDD pin	ISTB	CK=0, CSB=VDD, Ta=25 ℃ , VDD=3V		5	15	µA	※ 7
Oscillator frequency (variable gradation mode)	fosc	VDD=3V , Ta=25℃, Rf setting = (Rf2,Rf1,Rf0)=(000)	124	186	248	KHz	※ 8
Oscillator frequency (4 gradation mode)	fosc	VDD=3V, Ta=25 ℃, Rf setting = (Rf2,Rf1,Rf0)=(000)	22	32	42	KHz	※9
Oscillator frequency (monochrome mode)	fosc	VDD=3V , Ta=25℃, Rf setting = (Rf2,Rf1,Rf0)=(000)	8	12	16	KHz	※10
Booster output voltage on Vcc pin	Vcc1	Four times boosting RL = 500KΩ (Vcc-VSS)	4*Vci *0.95			V	※11
	Vcc2	Three times boosting RL = 500KΩ (Vcc-VSS)	3*Vci *0.95			V	※12
	Vcc3	Two times boosting RL = 500KΩ(Vcc-VSS)	2*Vci *0.95			V	※13
Current consumption	IDD1	VDD = 3V, 4 times booster All ON pattern(gray), Display ON		100	130	µA	※14
	IDD2	VDD = 3V, 4 times booster Checker pattern(gray), Display ON		110	135	µA	※15
	IDD3	VDD = 3V, 3 times booster All ON pattern(gray), Display ON		75	100	µA	※16
	IDD4	VDD = 3V, 3 times booster Checker pattern(gray), Display ON		80	105	µA	※17
	IDD5	VDD = 3V, 4 times booster All ON pattern(mono), Display OFF	60	85	110	µA	※18

Relationship of oscillating frequency (fosc) and external clock frequency (fCK) to LCD frame frequency (fFLM) is each display mode

Original oscillating clock	Display mode	Ratio of display duty cycle (1/D)				Pin used
		1/69, 1/58, 1/50	1/42, 1/34, 1/26	1/18	1/10	
When use built-in oscillating circuit (fosc)	Variable gradation	fosc/(2*15*D)	fosc/(4*15*D)	fosc/(8*15*D)	fosc/(16*15*D)	FLM(internal)
	Simple gradation	fosc/(2*3*D)	fosc/(4*3*D)	fosc/(8*3*D)	fosc/(16*3*D)	
	Monochrome	fosc/(2*1*D)	fosc/(4*1*D)	fosc/(8*1*D)	fosc/(16*1*D)	
When use external clock from CK pin. (fCK)	Variable gradation	fCK/(2*15*D)	fCK /(4*15*D)	fCK /(8*15*D)	fCK /(16*15*D)	
	Simple gradation	fCK /(2*3*D)	fCK /(4*3*D)	fCK /(8*3*D)	fCK /(16*3*D)	
	Monochrome	fCK /(2*1*D)	fCK /(4*1*D)	fCK /(8*1*D)	fCK /(16*1*D)	

Pin used:

※ **1** D0-D7, CSB, RS, M86, RDB, WRB, CK, CKS, P/S, RESB, TEST pins.

※ **2** D0~D7 pins

※ **3** CSB, RS, M/S, M86, RDB, WRB, CK, CKS, P/S, RESB, TEST pins

※ **4** Applied when D0~D7 are in the state of high impedance.

※ **5** SEG0~SEG100. COM0~COM66, COMA, COMB pins Resistance when being applied 0.5V between each output pin and each power supply (V0, V1, V2, V3, V4) and when being applied 1/9 bias.

※ **6** SSEG, SCOM pins

※ **7** VDD pin, VDD pin current without load at the stoppage of original oscillating clock and at non-select (CSB=VDD)

※ **8** Oscillating frequency, when using the built-in oscillating circuit (variable gradation display mode)

※ **9** Oscillating frequency, when using the built-in oscillating circuit (4 gradation fixed display mode)

※ **10** Oscillating frequency, when using the built-in oscillating circuit (monochrome display mode)

※ **11** Vcc pin. When using the built-in oscillating circuit, the built-in power supply is used, and boosting 4 times is used, this pin is applied. Vci=2.4~3.3 V, The electronic control is preset (The code is (“1 1 1 1 1 1 1”)). Measuring conditions: bias=1/5~1/9, 1/69 duty, without load. RL=500 KΩ (between Vcc and VSS), C1=C2=1.0μF, DCON=AMPON=”1”

※ **12** Vcc pin. When using the built-in oscillating circuit, the built-in power supply is used, and boosting 3 times is used, this pin is applied. Vci=2.4~3.3 V, The electronic control is preset (The code is (“1 1 1 1 1 1 1”)). Measuring conditions: bias=1/5~1/9, 1/69 duty, without load. RL=500 KΩ (between Vcc and VSS), C1=C2=1.0μF, DCON=AMPON=”1”

※ **13** Vcc pin. When using the built-in oscillating circuit, the built-in power supply is used, and boosting 2 times is used, this pin is applied. Vci=2.4~3.3 V, The electronic control is preset (The code is (“1 1 1 1 1 1 1”)). Measuring conditions: bias=1/5~1/9, 1/69 duty, without load. RL=500 KΩ (between Vcc and VSS),

C1=C2=1.0μF, DCON=AMPON="1"

※ **14** VDD, Vci pin. When the built-in oscillating circuit and built-in power supply are used and there is no access from MPU. This pin is applied. Boosting 4 times is used the electronic control is preset (The code is ("1 1 1 1 1 1 1")). Display ALL ON pattern (on gray mode display mode) and LCD driver pin with no load. Measuring conditions: VDD=Vci=VREF, C1=C2=1.0μF, DCON=AMPON="1", (BF1,BF0)=1.5KHz.

※ **15** VDD, Vci pin. When the built-in oscillating circuit and built-in power supply are used and there is no access from MPU. This pin is applied. Boosting 4 times is used the electronic control is preset (The code is ("1 1 1 1 1 1 1")). Display a checkered pattern (on gray mode display mode) and LCD driver pin with no load. Measuring conditions: VDD=Vci=VREF, C1=C2=1.0μF, DCON=AMPON="1" , (BF1,BF0)=1.5KHz.

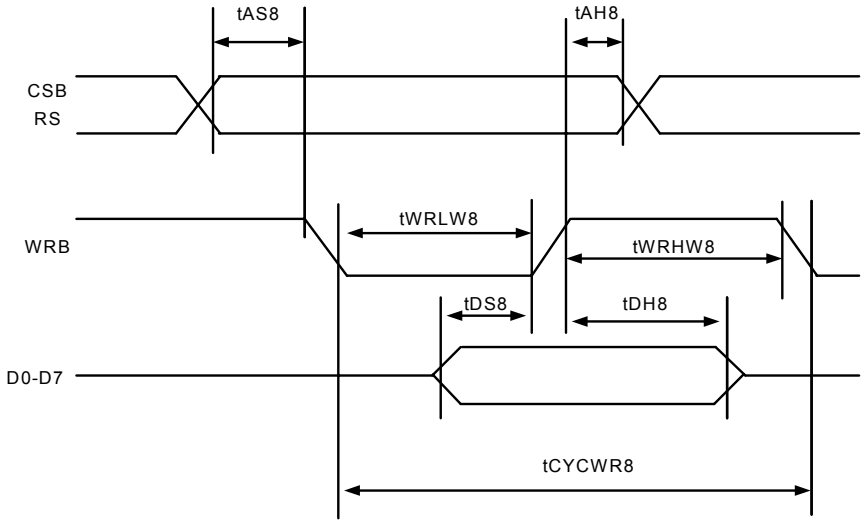
※ **16** VDD, Vci pin. When the built-in oscillating circuit and built-in power supply are used and there is no access from MPU. This pin is applied. Boosting 3 times is used the electronic control is preset (The code is ("1 1 1 1 1 1 1")). Display ALL ON pattern (on gray mode display mode) and LCD driver pin with no load. Measuring conditions: VDD=Vci=VREF, C1=C2=1.0μF, DCON=AMPON="1" , (BF1,BF0)=1.5KHz.

※ **17** VDD, Vci pin. When the built-in oscillating circuit and built-in power supply are used and there is no access from MPU. This pin is applied. Boosting 3 times is used the electronic control is preset (The code is ("1 1 1 1 1 1 1")). Display a checkered pattern (on gray mode display mode) and LCD driver pin with no load. Measuring conditions: VDD=Vci=VREF, C1=C2=1.0μF, DCON=AMPON="1" , (BF1,BF0)=1.5KHz.

※ **18** VDD, Vci pin. When the built-in oscillating circuit and built-in power supply are used and there is no access from MPU. This pin is applied. Boosting 4 times is used the electronic control is preset (The code is ("1 1 1 1 1 1 1")). Display OFF (on monochrome display mode) and LCD driver pin with no load. Measuring conditions: VDD=Vci=VREF, C1=C2=1.0μF, DCON=AMPON="1" , (BF1,BF0)=1.5KHz.

12. AC characteristic

(1) 80-family MCU write timing



VSS=0V, VDD = 2.7~3.3V , Ta = -30~+85℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Address hold time	tAH8		0			ns	CSB
Address setup time	tAS8		0			ns	RS
System cycle time in write	tCYCWR8		250			ns	WRB
Write pulse “L” width	tWRLW8		60			ns	(R/WB)
Write pulse “H” width	tWRHW8		185			ns	
Data setup time	tDS8		60			ns	D0~D7
Data hold time	tDH8		5			ns	

VSS=0V, VDD = 2.4~2.7V , Ta = -30~+85℃

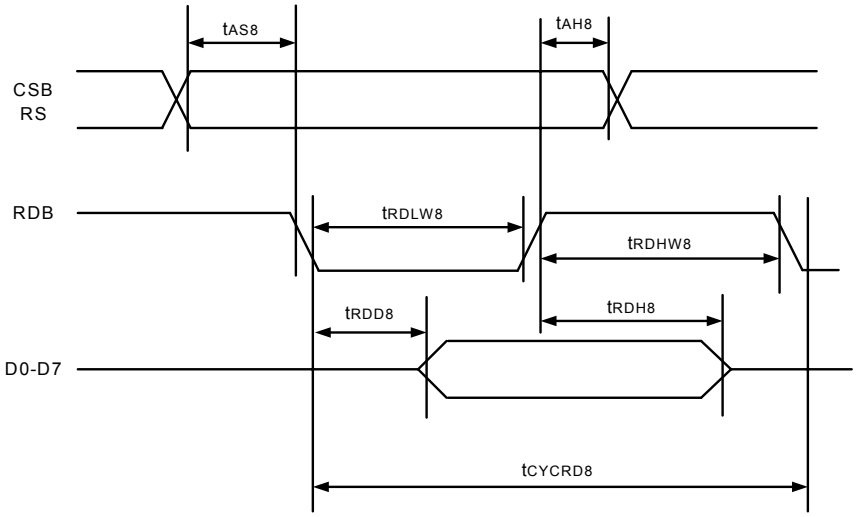
Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Address hold time	tAH8		0			ns	CSB
Address setup time	tAS8		0			ns	RS
System cycle time in write	tCYCWR8		330			ns	WRB
Write pulse “L” width	tWRLW8		80			ns	(R/WB)
Write pulse “H” width	tWRHW8		240			ns	
Data setup time	tDS8		80			ns	D0~D7
Data hold time	tDH8		10			ns	

VSS=0V, VDD = 2.4~3.3V , Ta = -30~+85℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Address hold time	tAH8		0			ns	CSB
Address setup time	tAS8		0			ns	RS
System cycle time in write	tCYCWR8		660			ns	WRB
Write pulse “L” width	tWRLW8		140			ns	(R/WB)
Write pulse “H” width	tWRHW8		500			ns	
Data setup time	tDS8		100			ns	D0~D7
Data hold time	tDH8		20			ns	

Note: All the timings must be specified relative to 20% and 80% of VDD voltage.

(2) 80-family MCU read timing



VSS=0V , VDD = 2.7~3.3V , Ta = -30~+85℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Address hold time	tAH8		0			ns	CSB
Address setup time	tAS8		0			ns	RS
System cycle time in read	tCYCRD8		450			ns	RDB(E)
Read pulse “L” width	tRDLW8		200			ns	
Read pulse “H” width	tRDHW8		185			ns	
Data setup time	tRDD8	CL = 80 pF			250	ns	D0~D7
Data hold time	tRDH8		10			ns	

VSS=0V , VDD = 2.4~2.7V , Ta = -30~+85℃

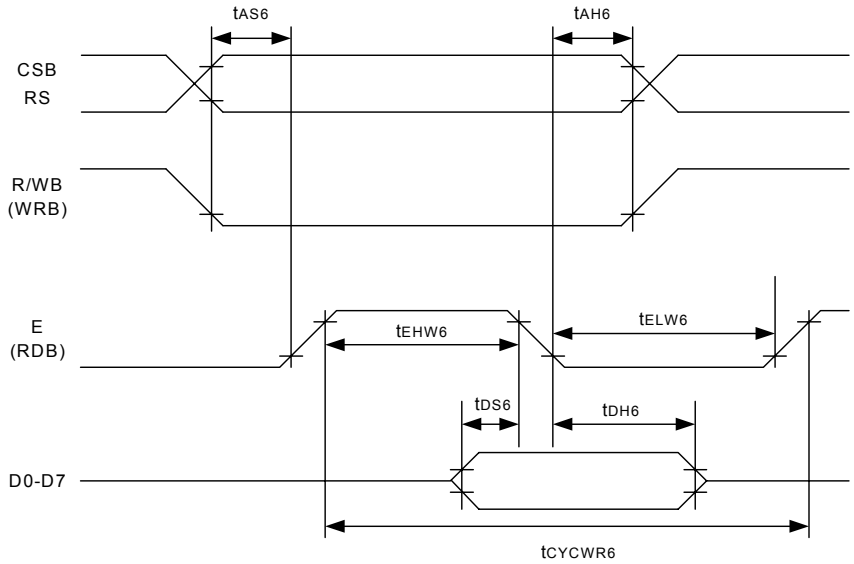
Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Address hold time	tAH8		0			ns	CSB
Address setup time	tAS8		0			ns	RS
System cycle time in read	tCYCRD8		600			ns	RDB(E)
Read pulse “L” width	tRDLW8		220			ns	
Read pulse “H” width	tRDHW8		240			ns	
Data setup time	tRDD8	CL = 80 pF			350	ns	D0~D7
Data hold time	tRDH8		10			ns	

VSS=0V , VDD = 1.8~2.4V , Ta = -30~+85℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Address hold time	tAH8		0			ns	CSB
Address setup time	tAS8		0			ns	RS
System cycle time in read	tCYCRD8		1000			ns	RDB(E)
Read pulse “L” width	tRDLW8		450			ns	
Read pulse “H” width	tRDHW8		500			ns	
Data setup time	tRDD8	CL = 80 pF			650	ns	D0~D7
Data hold time	tRDH8		10			ns	

Note: All the timings must be specified relative to 20% and 80% of VDD voltage.

(3) 68-family MCU write timing



VSS=0V , VDD = 2.7 ~3.3V , Ta = -30~+85℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Address hold time	tAH6		0			ns	CSB
Address setup time	tAS6		0			ns	RS
System cycle time in write	tCYCWR6		250			ns	RDB(E)
Write pulse “L” width	tELW6		60			ns	
Write pulse “H” width	tEHW6		185			ns	
Data setup time	tDS6		60			ns	D0~D7
Data hold time	tDH6		5			ns	

VSS=0V , VDD = 2.4 ~2.7V , Ta = -30~+85℃

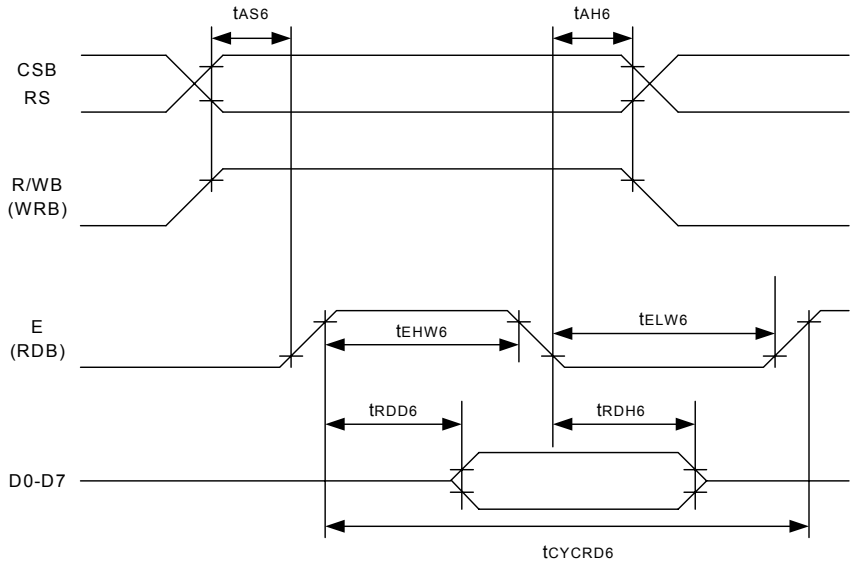
Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Address hold time	tAH6		0			ns	CSB
Address setup time	tAS6		0			ns	RS
System cycle time in write	tCYCWR6		330			ns	RDB(E)
Write pulse “L” width	tELW6		80			ns	
Write pulse “H” width	tEHW6		240			ns	
Data setup time	tDS6		80			ns	D0~D7
Data hold time	tDH6		10			ns	

VSS=0V , VDD = 1.8 ~2.4V , Ta = -30~+85℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Address hold time	tAH6		0			ns	CSB
Address setup time	tAS6		0			ns	RS
System cycle time in write	tCYCWR6		660			ns	RDB(E)
Write pulse “L” width	tELW6		140			ns	
Write pulse “H” width	tEHW6		500			ns	
Data setup time	tDS6		100			ns	D0~D7
Data hold time	tDH6		20			ns	

Note: All the timings must be specified relative to 20% and 80% of VDD voltage.

(4) 68-family MCU read timing



VSS=0V , VDD = 2.7~3.3V , Ta = -30~+85℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Address hold time	tAH6		0			ns	CSB
Address setup time	tAS6		0			ns	RS
System cycle time in write	tCYCRD6		450			ns	
Write pulse “L” width	tELW6		200			ns	RDB(E)
Write pulse “H” width	tEHW6		185			ns	
Data setup time	tRDD6	CL=80pF			250	ns	D0~D7
Data hold time	tRDH6		10			ns	

VSS=0V , VDD = 2.4~2.7V , Ta = -30~+85℃

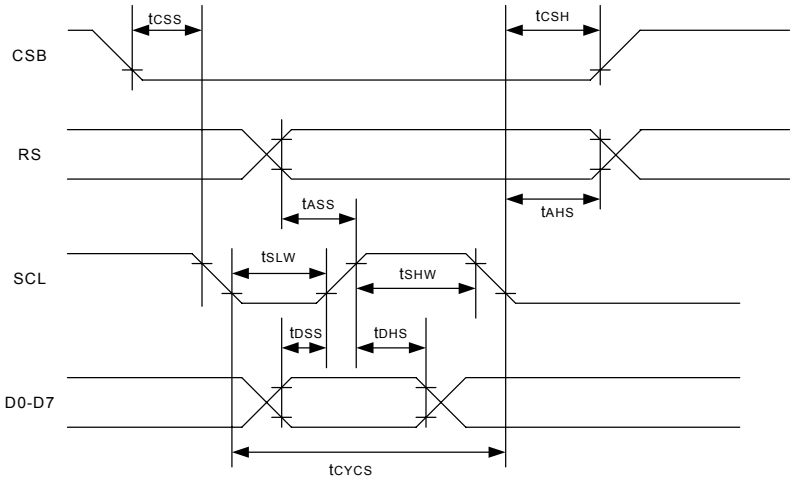
Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Address hold time	tAH6		0			ns	CSB
Address setup time	tAS6		0			ns	RS
System cycle time in write	tCYCRD6		600			ns	
Write pulse “L” width	tELW6		220			ns	RDB(E)
Write pulse “H” width	tEHW6		240			ns	
Data setup time	tRDD6	CL=80pF			350	ns	D0~D7
Data hold time	tRDH6		10			ns	

VSS=0V , VDD = 1.8~2.4V , Ta = -30~+85℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Address hold time	tAH6		0			ns	CSB
Address setup time	tAS6		0			ns	RS
System cycle time in write	tCYCRD6		1000			ns	
Write pulse “L” width	tELW6		450			ns	RDB(E)
Write pulse “H” width	tEHW6		500			ns	
Data setup time	tRDD6	CL=80pF			650	ns	D0~D7
Data hold time	tRDH6		10			ns	

Note: All the timings must be specified relative to 20% and 80% of VDD voltage.

(5) Serial interface timing diagram



VSS=0V , VDD = 2.7~3.3V , Ta = -30~+85℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Serial clock period	tCYCS		200			ns	SCL
SCL pulse “H” width	tSHW		80			ns	
SCL pulse “L” width	tSLW		80			ns	
Address setup time	tASS		40			ns	RS
Address hold time	tAHS		40			ns	
Data setup time	tDSS		80			ns	SDA
Data hold time	tDHS		80			ns	
CSB-SCL time	tCSS		40			ns	CSB
CSB hold time	tCSH		40			ns	

VSS=0V , VDD = 2.4~2.7V , Ta = -30~+85℃

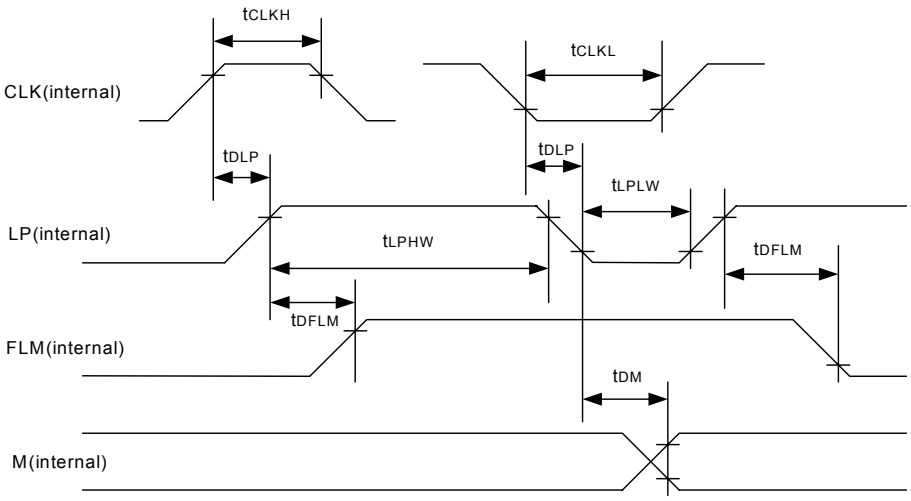
Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Serial clock period	tCYCS		250			ns	SCL
SCL pulse “H” width	tSHW		100			ns	
SCL pulse “L” width	tSLW		100			ns	
Address setup time	tASS		50			ns	RS
Address hold time	tAHS		50			ns	
Data setup time	tDSS		100			ns	SDA
Data hold time	tDHS		100			ns	
CSB-SCL time	tCSS		50			ns	CSB
CSB hold time	tCSH		50			ns	

VSS=0V , VDD = 1.8~2.4V , Ta = -30~+85℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Serial clock period	tCYCS		1000			ns	SCL
SCL pulse “H” width	tSHW		400			ns	
SCL pulse “L” width	tSLW		400			ns	
Address setup time	tASS		80			ns	RS
Address hold time	tAHS		80			ns	
Data setup time	tDSS		400			ns	SDA
Data hold time	tDHS		400			ns	
CSB-SCL time	tCSS		80			ns	CSB
CSB hold time	tCSH		80			ns	

Note: All the timings must be specified relative to 20% and 80% of VDD voltage.

(6) Display control timing



output timing VSS=0V , VDD = 2.4~3.3V , Ta = -30~+85℃

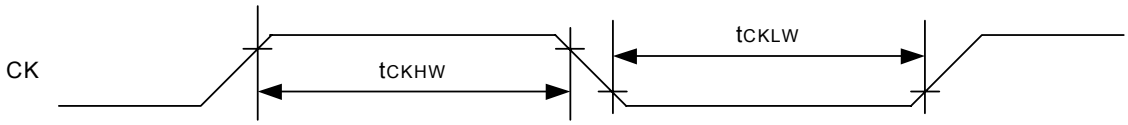
Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
LP delay time	tDLP	CL =15 pF	10		500	ns	LP(internal)
FLM delay time	tDFLM		10		500	ns	FLM(internal)
M delay time	tDM		10		500	ns	M(internal)

output timing VSS=0V , VDD = 1.8~2.4V , Ta = -30~+85℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
LP delay time	tDLP	CL =15 pF	10		1000	μs	LP(internal)
FLM delay time	tDFLM		10		1000	μs	FLM(internal)
M delay time	tDM		10		1000	μs	M(internal)

Note: All the timings must be specified relative to 20% and 80% of VDD voltage.

(7) Master clock input timing



VSS=0V , VDD = 2.4~3.3V , Ta = -30~+85℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
CK pulse "H" width (1)	tCKHW1		1.2		1.4	μs	CK
CK pulse "L" width (1)	tCKLW1		1.2		1.4	μs	※ 1
CK pulse "H" width (2)	tTCKHW2		5.4		6.5	μs	CK
CK pulse "L" width (2)	tCKLW2		5.4		6.5	μs	※ 2
CK pulse "H" width (3)	tCKHW3		38		45	μs	CK
CK pulse "L" width (3)	tCKLW3		38		45	μs	※ 3

VSS=0V , VDD = 1.8~2.4V , Ta = -30~+85℃

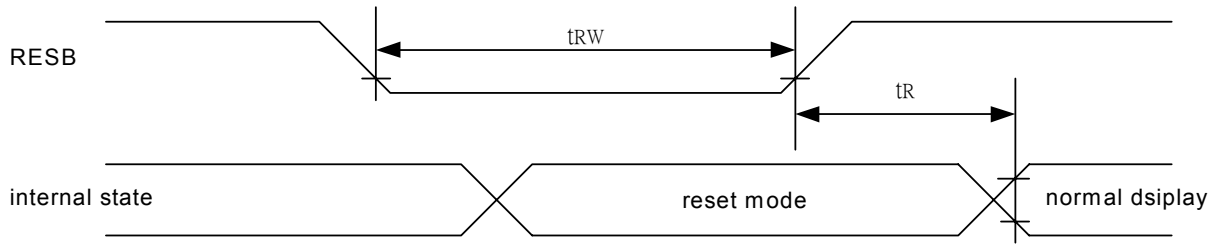
Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
CK pulse "H" width (1)	tCKHW1	Note1	1.2		1.4	μs	CK
CK pulse "L" width (1)	tCKLW1	Note1	1.2		1.4	μs	※ 1
CK pulse "H" width (2)	tCKHW2	Note2	5.4		6.5	μs	CK
CK pulse "L" width (2)	tCKLW2	Note2	5.4		6.5	μs	※ 2
CK pulse "H" width (3)	tCKHW3	Note3	3.8		4.5	μs	CK
CK pulse "L" width (3)	tCKLW3	Note3	3.8		4.5	μs	※ 3

※ 1 Applied when the gradation display mode.

※ 2 Applied when the simple gradation mode.

※ 3 Applied when the monochrome mode.

(8) Reset timing



VSS=0V, VDD = 2.4~3.3V, Ta = -30~+85℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Reset time	tR				1	μs	
Reset pulse “L” width	tRW		500			μs	RESB

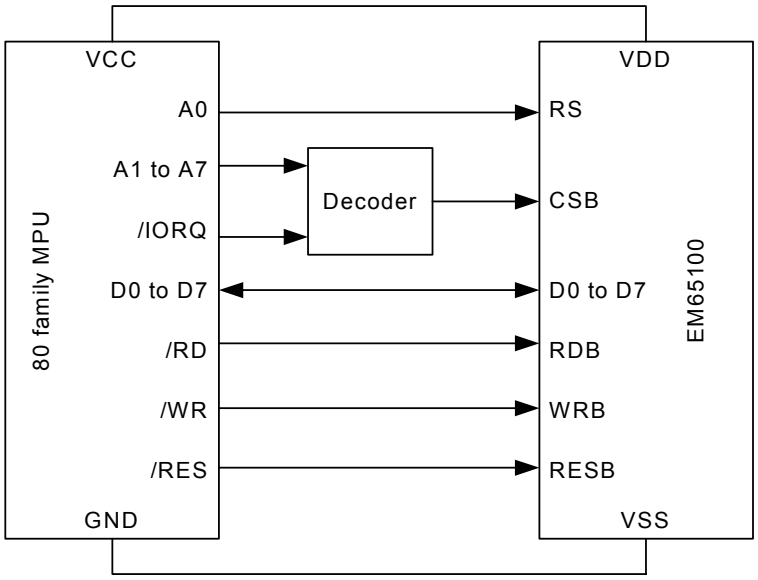
VSS=0V, VDD = 1.8~2.4V, Ta = -30~+85℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Reset time	tR				1.5	μs	
Reset pulse “L” width	tRW		500			μs	RESB

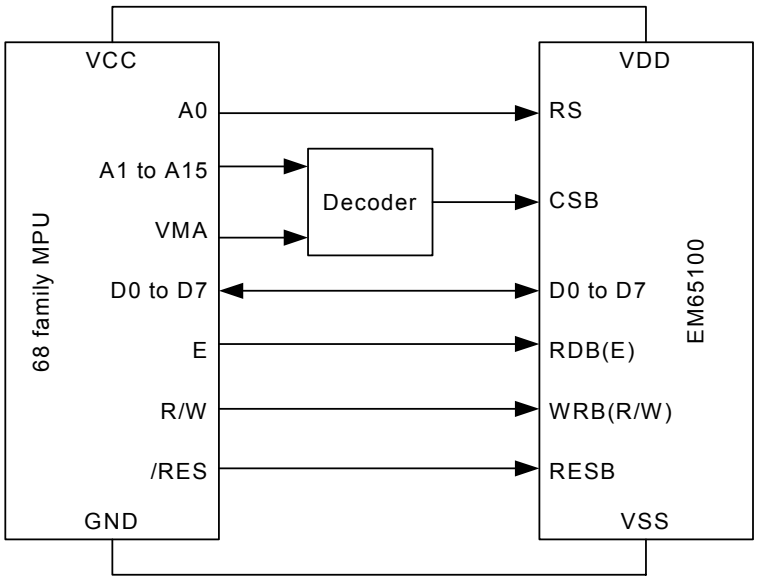
Note: All the timings must be specified relative to 20% and 80% of VDD voltage.

13. Application circuit

(1) Connection to 80-family MCU



(2) Connection to 68-family MCU



(3) Connection to the MCU with serial interface