文件名稱 DOC Title ：	文件編號 DOC NO ：TDS7011-02
EK7011CG DATA SHEET	版 本 REV ：1.5
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文件制/修訂一覽表 Revision History

版本 REV.	修訂日期 REV Date	生效日期 Eff. Date	修訂頁次 REV. Page	制/修訂項目/ 內容 Revise item / Content
0.2	2000/11/2	2000/1207		新增訂
1.1	2000/11/29	2000/1207	29	1. 增加Wafer thickness & Height of Bump的值
1.2	2000/12/6	2000/12/07	18	1. modify Input voltage condition
			29	2. Add COG application note
			34、36	3. Separate V_{SS} and V_{GND} pads
1.3	2001.2/22	2001/03/05	2	1. 刪除Pin Configuration的圖
			28	2. 晶片示意圖加上logo以辨識方向
			29	3. 修改Bump Height的值
			3,4,5,6,7,8,16 17,18,19,20,22 26	4. 將HV Ground 改成V_{GND}
1.4	2001/10/22	2001/10/24	16	1. 將Storeage temperature改成Operating temperature
			5	
1.5	2003/10/23	2003/10/28	32,33,34	1. 統一DATA SHEET與PAD LOCATION接腳名稱 LR改成L/R、Vdd:P改成Vdd、SC改成S/C EIO_2改成EIO2、D0改成DI0、D1改成DI1 D2改成DI2、D3改成DI3、D4改成DI4 D5改成DI5、D6改成DI6、D7改成DI7 CK改成XCK、DISPOFF 改成 $\overline{\text{DISPOFF}}$ PLP改成LP、EIO_1改成EIO1、 PMD改成MD、PFR 改成 FR

EUREKA Microelectronics, Inc.

EK7011CG

Rev. 1.5

DATA SHEET

160 Output Segment & Common LCD Driver

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EUREKA

160 Output Segment/Common LCD Driver

Description

The EK7011 is a 160 output segment/common LCD driver adaptable to drive a large scale dot matrix panel. It uses the Tape Carrier Package(TCP) to greatly reduce the size of the LCD module. EK7011 consumes very little power. Large LCD panels can be assembled by cascading EK7011s. In Segment Mode, the input data can be either 4-bit parallel or 8-bit parallel, selected by the Mode Select pin (MD).

Features

- CMOS process
- Logic power supply : 2.5V to 5.5V
- Low power consumption
- 160 LCD display output
- Supply voltage for LCD driver :15 to 40V
- Package : TCP, COG available

Features in Segment mode

- Shift clock frequency : 14MHz max. at V_{DD}=5V
- 4bit/8bit parallel input
- Automatic transfer of enable signal
- Automatic counting in the chip select mode. The internal clock stoped by automatically counting 160 of input data.

Features in Common mode

- Shift clock frequency : 4MHz max. at V_{DD}=5V
- Built-in 160-bit bidirectional shift register
- Single mode (160-bit shift register) or Dual Mode (two 80-bit shift registers) with these options:
  1. Y1 ⟶ Y160 Single mode
  2. Y160 ⟶ Y1 Single mode
  3. Y1 ⟶ Y80, Y81 ⟶ Y160 Dual mode
  4. Y160 ⟶ Y81, Y80 ⟶ Y1 Dual mode

Block Diagram

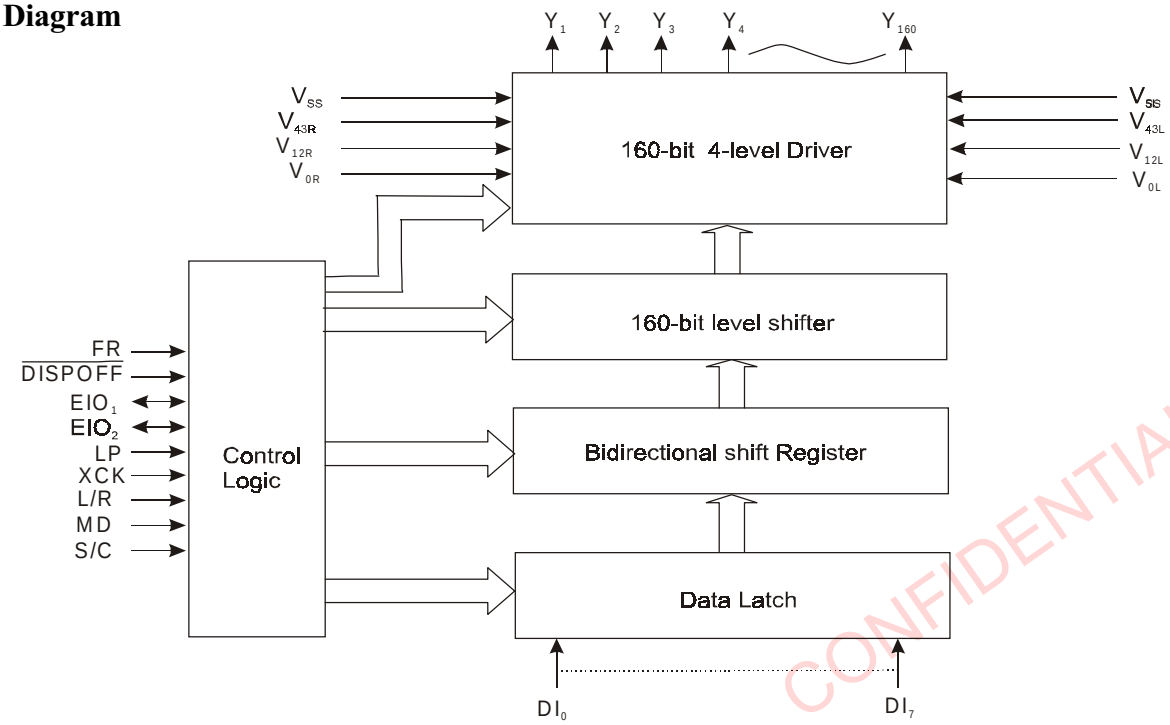

Fig.1