40 CH SEGMENT/COMMON DRIVER FOR DOT MATRIX LCD

DESCRIPTION

The AIP31065 is a LCD driver IC which is fabricated by low power CMOS technology. Basically this IC consists of 20 x 2 bit bi-directional shift register, 20 x 2 bit data latch and 20 x 2 bit driver. (refer to Fig 1) This IC can be used as common or segment driver.

FEATURES

- Dot matrix LCD driver with 40 channel output.
- Selects function to use common/segment drivers simultaneously.
- Input / Output signal
- Output: 20 x 2 channel waveform for LCD driving
- Input: Serial display data and control signal from the controller LSI.
  Bias voltage (V_1-V_6)
- Display driving bias: static - 1/5
- Power supply voltage: 2.7- 5.5V
- Supply voltage for display: 3.0 - 13.0V ($V_{LCD} = V_{DD} - V_{EE}$)
- CMOS Process
- Chip size: 2.360*1.905(mm* mm). The IC substrate should be connected to VDD in the PCB layout artwork.
- 64QFP or bare chip available

BLOCK DIAGRAM

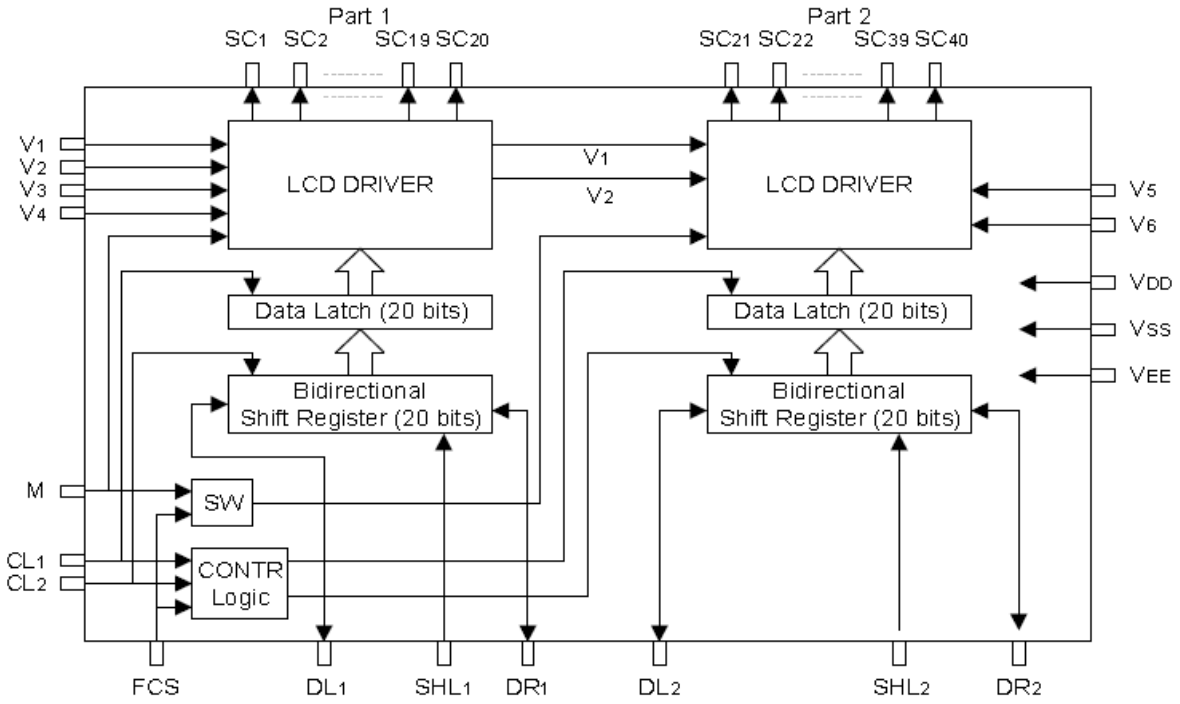


Fig.1

PIN CONFIGURATION

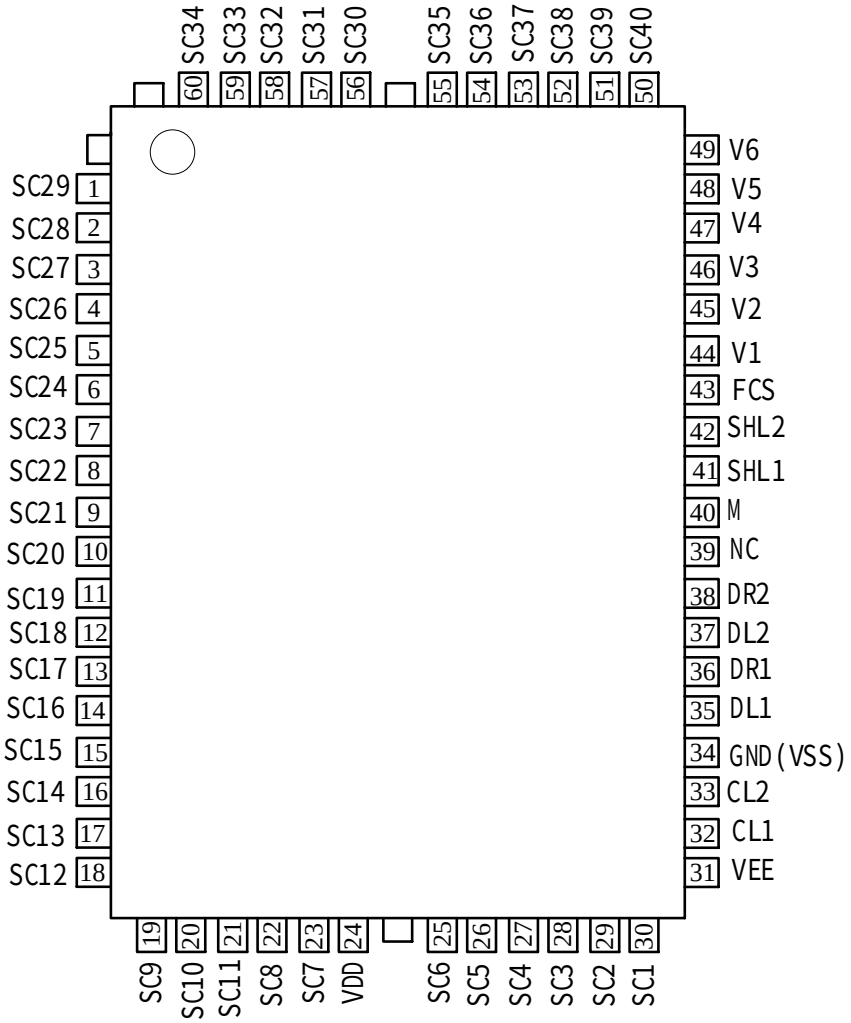


Fig.2

PIN DESCRIPTION

<table>
<tr><th>Pin (No.)</th><th>I/O</th><th colspan="2">Name</th><th>Description</th><th>Interface</th></tr>
<tr><td>V_{DD}(24)</td><td rowspan="3">Power</td><td colspan="2">Operating Voltage</td><td>For logical circuit (2.7 - 5.5V)</td><td rowspan="3">Power Supply</td></tr>
<tr><td>GND(34)</td><td colspan="2"></td><td>0V (GND)</td></tr>
<tr><td>V_{EE}(31)</td><td colspan="2">Negative Supply Voltage</td><td>For LCD driver circuit</td></tr>
<tr><td>V1, V2 (44,45)</td><td>I</td><td colspan="2">Bias Voltage</td><td>Bias voltage level for LCD drive (select level)</td><td>Power</td></tr>
<tr><td>SC_1 - SC_{20}</td><td>O</td><td rowspan="3">Part 1</td><td>LCD driver</td><td>LCD driver output</td><td>LCD</td></tr>
<tr><td>V3, V4 (46, 47)</td><td>I</td><td>Bias Voltage</td><td>Bias voltage level for LCD drive (non-select level)</td><td>Power</td></tr>
<tr><td>SHL1(41)</td><td>I</td><td>Data interface</td><td>Selection of the shift direction of Part 1 shift register
<table><tr><th>SHL1</th><th>DL1</th><th>DR1</th></tr><tr><td>V_{DD}</td><td>out</td><td>in</td></tr><tr><td>V_{SS}</td><td>in</td><td>out</td></tr></table></td><td>V_{DD} or V_{SS}</td></tr>
<tr><td>DL1, DR1 (35, 36)</td><td>I/O</td><td colspan="2">Data input/output of Part 1 shift register</td><td>Controller or AIP31065</td></tr>
<tr><td>SC_{21}- SC_{40}</td><td>O</td><td rowspan="3">Part 2</td><td>LCD driver</td><td>LCD driver output</td><td></td></tr>
<tr><td>V5, V6 (48, 49)</td><td>I</td><td>Bias Voltage</td><td>Bias voltage level for LCD drive (non-select level)</td><td>Power</td></tr>
<tr><td>SHL2(42)</td><td>I</td><td>Data interface</td><td>Selection of the shift direction of Part 2 shift register
<table><tr><th>SHL2</th><th>DL2</th><th>DR2</th></tr><tr><td>V_{DD}</td><td>out</td><td>in</td></tr><tr><td>V_{SS}</td><td>in</td><td>out</td></tr></table></td><td>V_{DD} or V_{SS}</td></tr>
<tr><td>DL2,DR2 (37, 38)</td><td>I/O</td><td colspan="2">Data input/output of Part 2 shift register</td><td>Controller or AIP31065</td></tr>
<tr><td>M (40)</td><td>I</td><td colspan="2">Alternated signal for LCD driver output</td><td rowspan="3"><table><tr><th>PART</th><th>FCS</th><th>CL1</th><th>CL2</th><th>M polartty</th></tr><tr><td rowspan="2">1</td><td>Vss</td><td rowspan="2">latch clock ↓</td><td rowspan="2">shift clock ↓</td><td rowspan="2">M</td></tr><tr><td>V_{DD}</td></tr><tr><td rowspan="2">2</td><td>Vss</td><td rowspan="2">latch clock ↑</td><td rowspan="2">shift clock ↑</td><td rowspan="2">$\overline{M}$</td></tr><tr><td>V_{DD}</td></tr></table>
Shift/latch clock of display data and polarity of M signal are changed by FCS signal.
By setting FCS to V_{DD} level, user can select the function that use Part 1 as segment driver and Part 2 as common driver simultaneously.</td><td rowspan="3">Controller</td></tr>
<tr><td>CL1,CL2 (32,33)</td><td>I</td><td colspan="2">Data shift /latch clock</td></tr>
<tr><td>FCS(43)</td><td>I</td><td colspan="2">Mode selection</td></tr>
<tr><td>NC(39)</td><td></td><td colspan="2"></td><td>No connection pin</td><td>NC</td></tr>
</table>

MAXIMUM ABSOLUTE LIMIT (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Operating Voltage	V_{DD}	- 0.3 to + 7.0	V
Driver Supply Voltage	V_{LCD}	V_{DD} - 15.0 to V_{DD}+ 0.3	V
Input Voltage 1	V_{IN1}	- 0.3 to V_{DD}+ 0.3	V
Input Voltage 2 (V_1 - V_6)	V_{IN2}	V_{DD}+ 0.3 to V_{EE} - 0.3	V
Operating Temperature	T_{OPR}	- 20 to + 70	°C
Storage Temperature	T_{SRG}	- 55 to + 125	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics (Ta=25℃，V_{DD}=5V±10%，V_{EE} = -5V±10%，V_{SS}=0V)

Characteristic	Symbol	Test condition	Min	Max	Unit	Applicable pin
Operating Current *	I_{DD}	fCL2= 400kHz	-	1	mA	-
Supply Current *	I_{EE}	fCL1= 1kHz	-	10	A	
Input High Voltage	V_{IH}	-	0.7VDD	VDD	V	CL1, CL2, DL1, DL2 , DR1, DR2, SHL1, SHL2 M, FCS
Input Low Voltage	V_{IL}		0	0.3VDD		
Input Leakage Current	I_{LKG}	VIN= 0-VDD	-5	5	A	
Output High Voltage	V_{OH}	IOH= -0.4mA	VDD-0.4	-	V	DL1, DL2, DR1, DR2
Output Low Voltage	V_{OL}	IOL= +0.4mA	-	0.4		
Voltage Descending	V_{D1}	I_{ON}= 0.1mA for one of SC1-SC40	-	1.1		V(V1-V6)-SC(SC1-SC40)
	V_{D2}	I_{ON}= 0.05mA for each SC1-SC40	-	1.5		
Leakage Current	I_V	VIN= VDD ～VEE (OutputSC1-SC40 :floating)	-10	10	A	V1-V6

AC Characteristics（Ta=25℃，V_{DD}=5V±10%，V_{EE} = -5V±10%，V_{SS}=0V）

Characteristic	Symbol	Test condition	Min	Max	Unit	Applicable pin
Data Shift Frequency	f_{CL}	-	-	400	kHz	CL2
Clock High Level Width	t_{WCKH}	-	800	-	ns	CL1, CL2
Clock Low Level Width	t_{WCKL}	-	800	-		CL2
Clock Set-up Time	t_{SL}	from CL2 to CL1	500	-		CL1, CL2
	t_{LS}	from CL1 to CL2	500	-		
Clock Rise/Fall Time	t_R/t_F	-	-	200		
Data Set-up Time	t_{SU}	-	300	-		DL1, DL2, DR1, DR2, FLM
Data Hold Time	t_{DH}	-	300	-		
Data Delay Time	t_D	C_L = 15pF	-	500		DL1, DL2, DR1, DR2

Time Characteristics

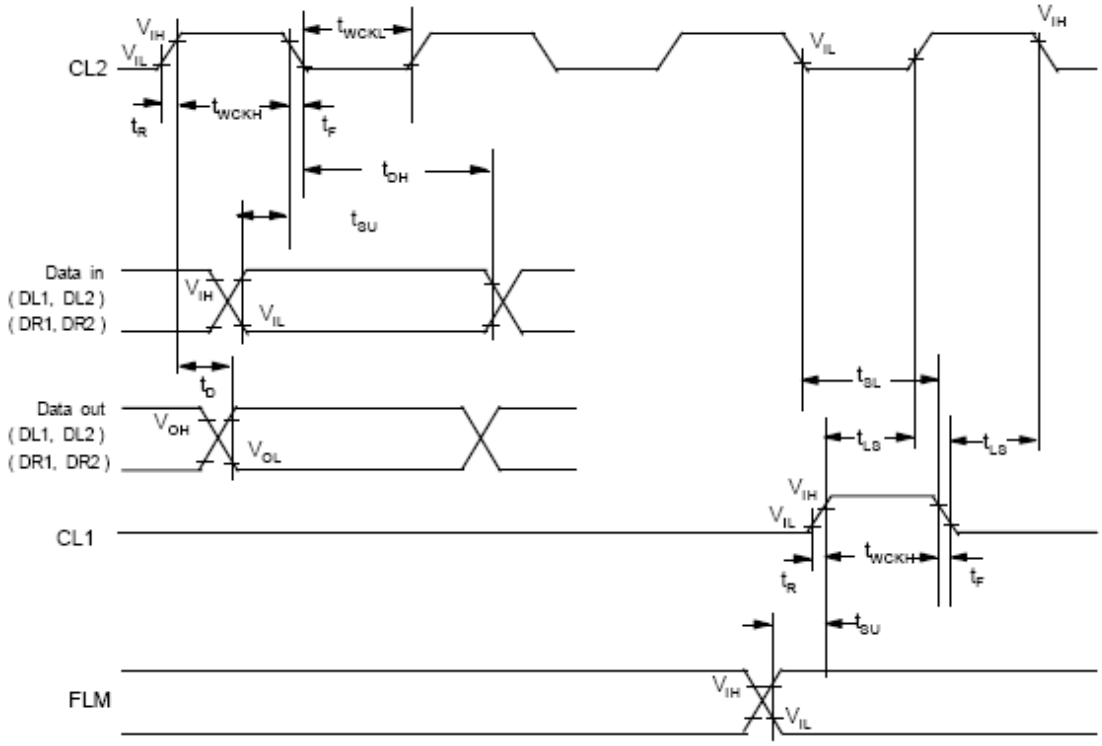


Fig 3. AC characteristics

Functional Description

1) To drive segment type

When the FCS is connected to Vss , AIP31065(SC1～SC40) is operated as segment driver.

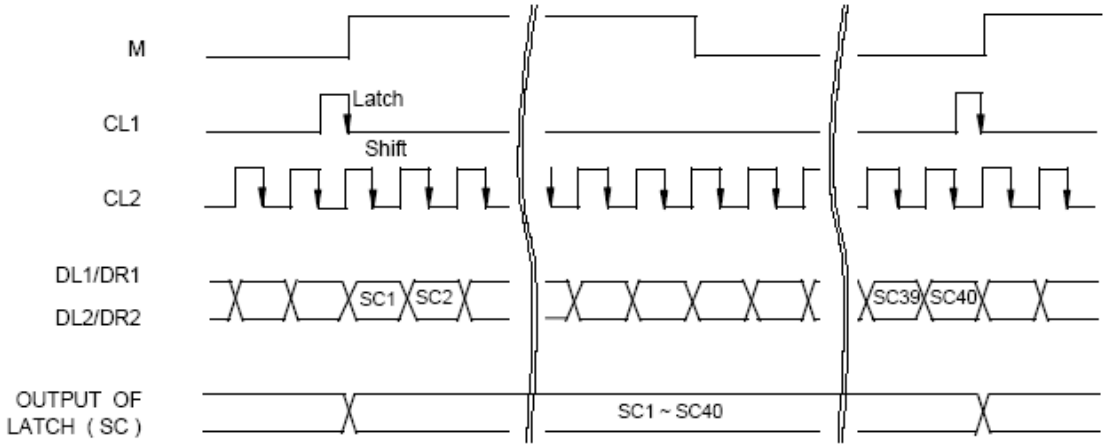


Fig 4. Segment Data Waveforms

2) To drive common type

When the FCS is connected to VDD, only part2 (SC21～SC40) of AIP31065 is operated as common driver.

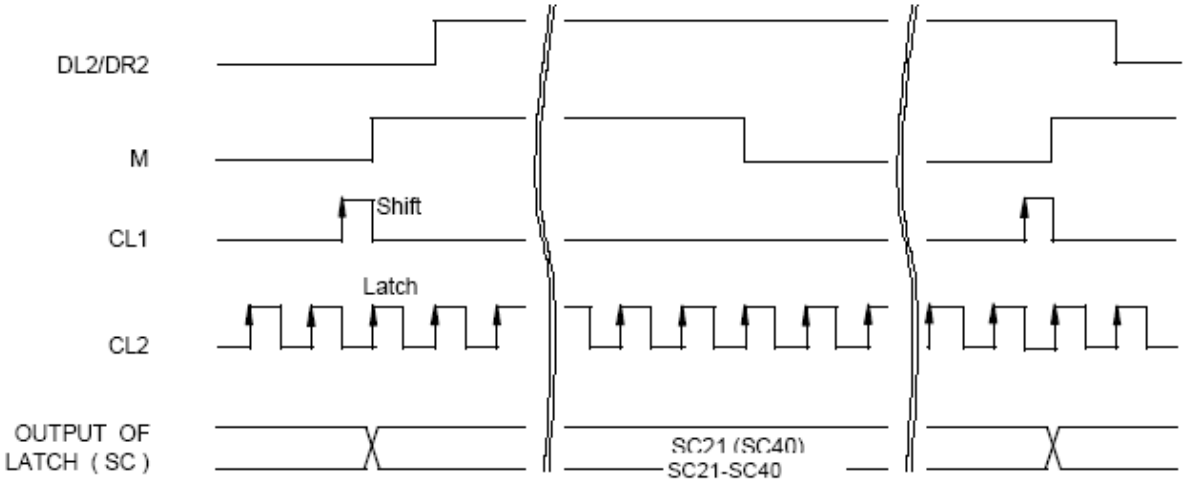


Fig 5. Common Data waveforms

LCD Output Waveforms

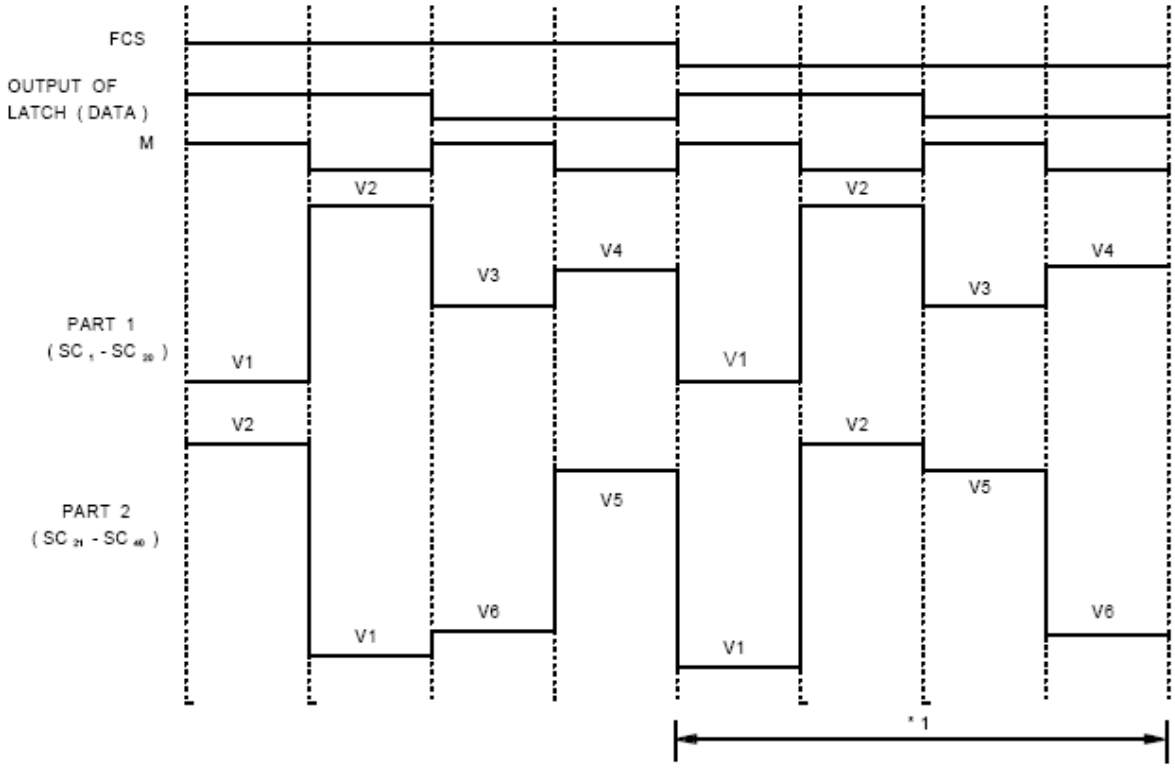
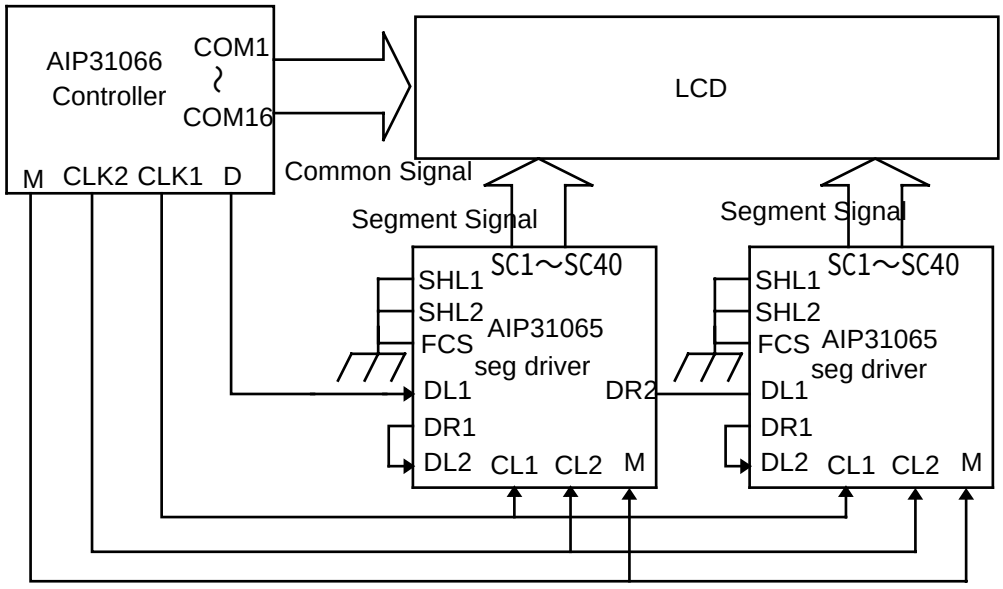


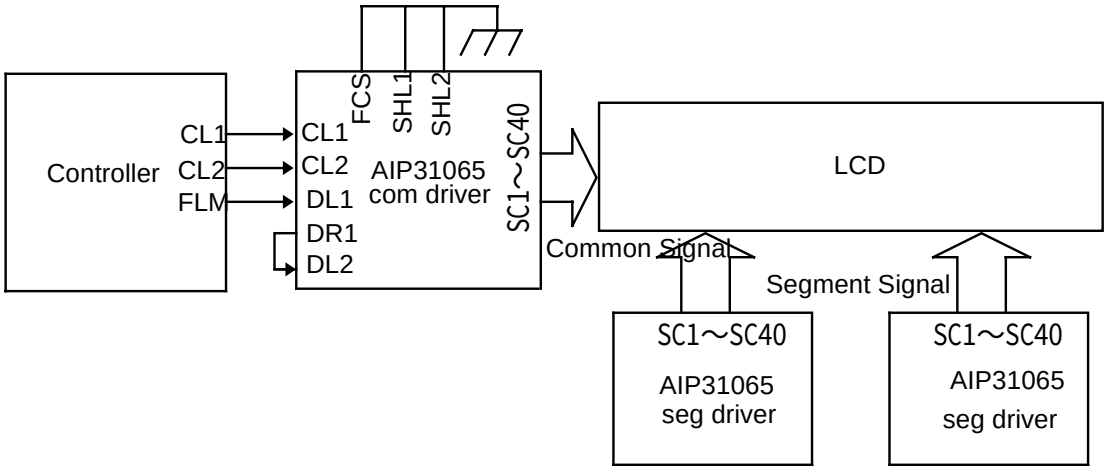
Fig. 6. Output waveform

APPLICATION CIRCUIT

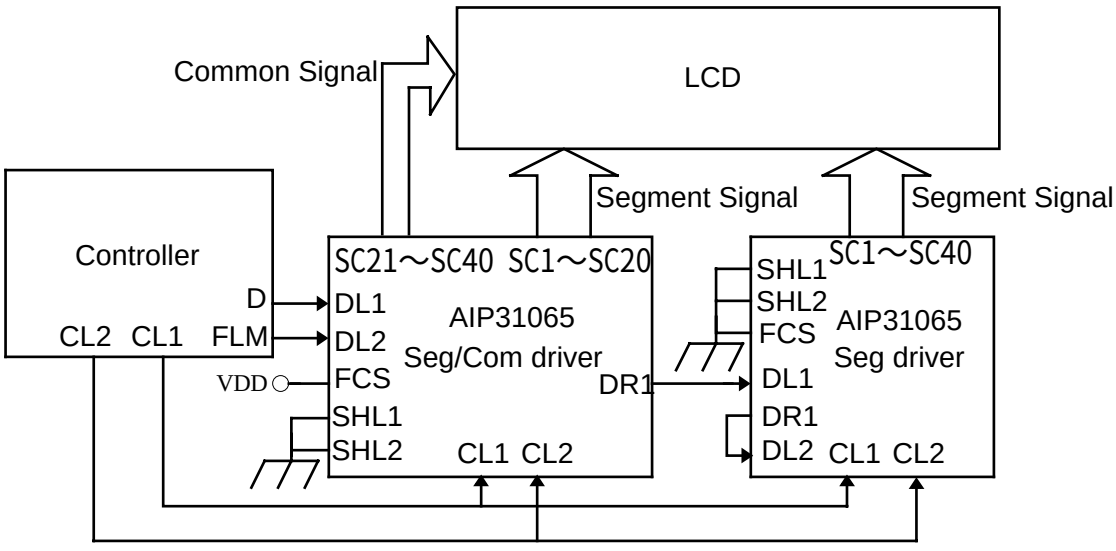
1) Segment Driver



2) Common Driver



3) Segment / Common Driver



Pad Coordinates