芯颖科技有限公司
CHIP WEALTH TECHNOLOGY LTD.

CH1115

128 X 64 Dot Matrix OLED/PLED Segment/Common Driver with Controller

Features

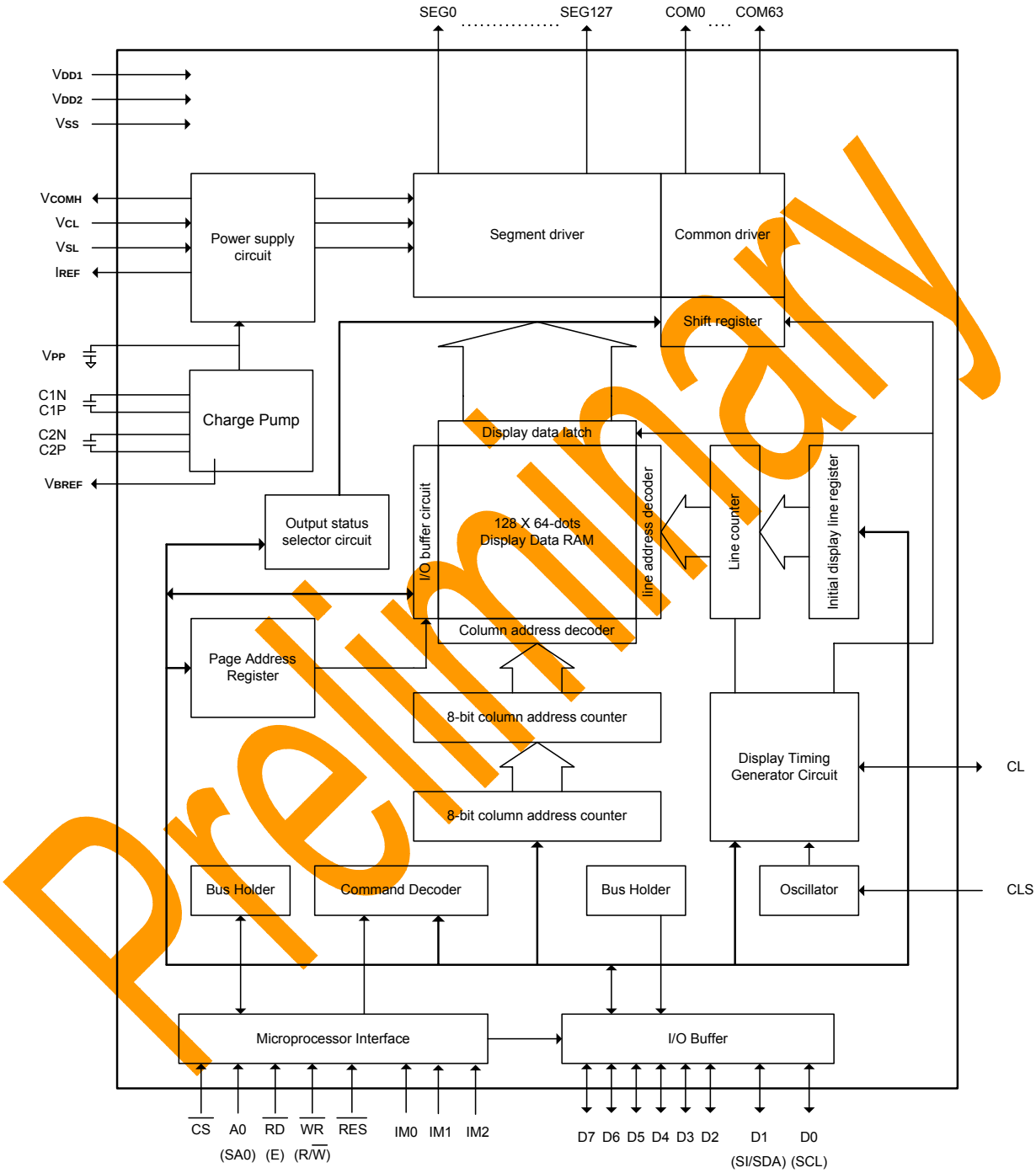
- Support maximum 128 X 64 dot matrix panel
- Embedded 128 X 64 bits SRAM
- Operating voltage:
  - Logic voltage supply: V_{DD1} = 1.65V - 3.5V
  - DC-DC voltage supply: V_{DD2} = 2.5V - 4.7V
  - OLED Operating voltage supply:
    External V_{PP} supply = 6.4V - 14.0V
    Internal V_{PP} generator = 7.4V – 10.0V
- Typical segment output current: 300μA
- Maximum segment output current: 500μA
- Typical common sink current: 38.4mA
- Maximum common sink current: 64mA
- 8-bit 6800-series parallel interface, 8-bit 8080-series parallel interface, serial 3-wire & 4-wire serial peripheral interface, 400KHz fast I^2C bus interface
- Programmable frame frequency and multiplexing ratio
- Continuous horizontal scroll
- Single screen horizontal scroll
- Internal or external I_{REF} selection
- Row non-overlap
- Breathing Display Effect
- Adjust I_{SEG} by pad(D2-D7)
- Row re-mapping and column re-mapping (ADC)
- Vertical scroll
- On-chip oscillator
- Programmable Internal charge pump circuit output
- 256-step contrast control on monochrome passive OLED panel
- Adaptive Power Save
- Low power consumption
  - Sleep mode: <5μA
  - VDD1=0V，VDD2=2.5V – 4.7V: <5μA
  - VDD1,2=0V，VPP=6.4V –14.0V: <5μA
- Wide range of operating temperatures: -40 to +85°C
- Available in COG form, thickness: 300μm

General Description

CH1115 is a single-chip CMOS OLED/PLED driver with controller for organic/polymer light emitting diode dot-matrix graphic display system. CH1115 consists of 128 segments, 64 commons that can support a maximum display resolution of 128 X 64. It is designed for Common Cathode type OLED panel.

CH1115 embeds with contrast control, display RAM oscillator and efficient DC-DC converter, which reduces the number of external components and power consumption. CH1115 is suitable for a wide range of compact portable applications, such as sub-display of mobile phone, calculator and MP3 player, etc.

Block Diagram



Pad Description

Power Supply

Symbol	I/O	Description
V_{DD1}	Supply	Power supply input: 1.65 - 3.5V
V_{DD2}	Supply	2.5 – 4.7V power supply pad for Power supply for charge pump circuit. This pin should be disconnected when V_{PP} is supplied externally
V_{SS}	Supply	Ground.
V_{SL}	Supply	This is a segment voltage reference pad. This pad should be connected to Vss externally.
V_{CL}	Supply	This is a common voltage reference pad. This pad should be connected to Vss externally.

OLED Driver Supplies

Symbol	I/O	Description
I_{REF}	O	This is a segment current reference pad. A resistor should be connected between this pad and Vss. Set the current at 18.75μA.
V_{COMH}	O	This is a pad for the voltage output high level for common signals. A capacitor should be connected between this pad and Vss.
V_{BREF}	NC	This is an internal voltage reference pad for booster circuit. Keep floating.
V_{PP}	P	OLED panel power supply. Generated by internal charge pump. Connect to capacitor. It could be supplied externally.
C1N, C1P	P	Connect to charge pump capacitor. These pins are not used and should be disconnected when Vpp is supplied externally.
C2P, C2N	P	Connect to charge pump capacitor. These pins are not used and should be disconnected when Vpp is supplied externally.

System Bus Connection Pads

<table>
<tr><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>CL</td><td>I/O</td><td>This pad is the system clock input. When internal clock is enabled, this pad should be Left open. The internal clock is output from this pad. When internal oscillator is disabled, this pad receives display clock signal from external clock source.</td></tr>
<tr><td>CLS</td><td>I</td><td>This is the internal clock enable pad.
CLS = “H”: Internal oscillator circuit is enabled.
CLS = “L”: Internal oscillator circuit is disabled (requires external input).
When CLS = “L”, an external clock source must be connected to the CL pad for normal operation.</td></tr>
<tr><td>IM0
IM1
IM2</td><td>I</td><td>These are the MPU interface mode select pads.
<table>
<tr><td></td><td>8080</td><td>I²C</td><td>6800</td><td>4-wire SPI</td><td>3-wire SPI</td></tr>
<tr><td>IM0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>IM1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>IM2</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
</table></td></tr>
<tr><td>$\overline{CS}$</td><td>I</td><td>This pad is the chip select input. When $\overline{CS}$ = “L”, then the chip select becomes active, and data/command I/O is enabled.</td></tr>
<tr><td>$\overline{RES}$</td><td>I</td><td>This is a reset signal input pad. When $\overline{RES}$ is set to “L”, the settings are initialized. The reset operation is performed by the $\overline{RES}$ signal level.</td></tr>
<tr><td>A0</td><td>I</td><td>This is the Data/Command control pad that determines whether the data bits are data or a command.
A0 = “H”: the inputs at D0 to D7 are treated as display data.
A0 = “L”: the inputs at D0 to D7 are transferred to the command registers.
In I²C interface, this pad serves as SA0 to distinguish the different address of OLED driver.</td></tr>
<tr><td>$\overline{WR}$
(R/$\overline{W}$)</td><td>I</td><td>This is a MPU interface input pad.
When connected to an 8080 MPU, this is active LOW. This pad connects to the 8080 MPU $\overline{WR}$ signal. The signals on the data bus are latched at the rising edge of the $\overline{WR}$ signal.
When connected to a 6800 Series MPU: This is the read/write control signal input terminal.
When R/$\overline{W}$ = “H”: Read.
When R/$\overline{W}$ = “L”: Write.</td></tr>
<tr><td>$\overline{RD}$
(E)</td><td>I</td><td>This is a MPU interface input pad.
When connected to an 8080 series MPU, it is active LOW. This pad is connected to the $\overline{RD}$ signal of the 8080 series MPU, and the data bus is in an output status when this signal is “L”.
When connected to a 6800 series MPU , this is active HIGH. This is used as an enable clock input of the 6800 series MPU.
When $\overline{RD}$ = “H”: Enable.
When $\overline{RD}$ = “L”: Disable.</td></tr>
<tr><td>D0 - D7
(SCL)
(SI/SDA)</td><td>I/O
I
I/O</td><td>This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus.
When the serial interface is selected, then D0 serves as the serial clock input pad (SCL) and D1 serves as the serial data input pad (SI). At this time, D2 to D7 are set to high impedance.
When the I²C interface is selected, then D0 serves as the serial clock input pad (SCL) and D1 serves as the serial data input pad (SDA). At this time, D2 to D7 are set to high impedance.</td></tr>
</table>

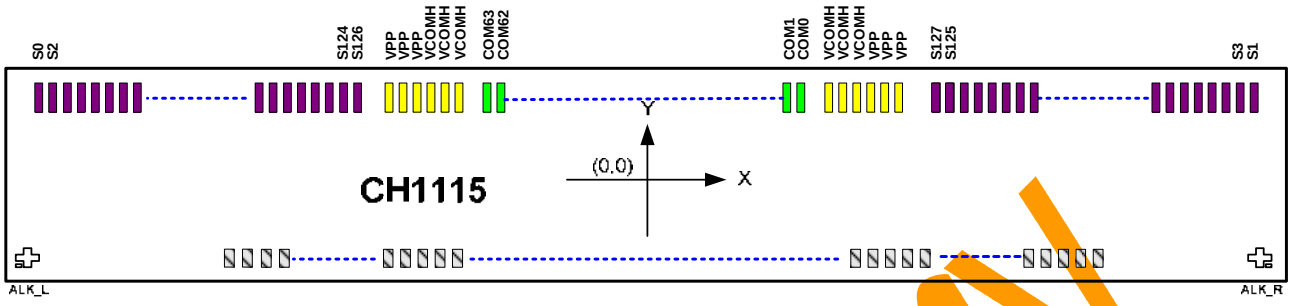
OLED Drive Pads

Symbol	I/O	Description
SEG 0,2, - 126	O	These pads are even Segment signal output for OLED display.
SEG1,3 - 127	O	These pads are odd Segment signal output for OLED display.
COM0 -63	O	These pads are Common signal output for OLED display.

Test Pads

Symbol	I/O	Description
TEST1-3	I	Test pad, internal pull low, no connection for user.
Dummy	-	These pads are not used. Keep floating.

Pad Configuration



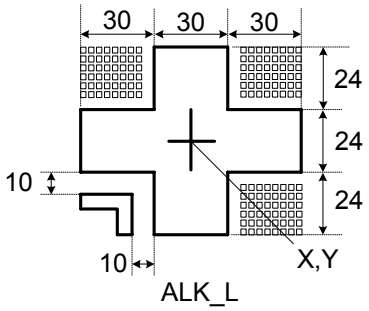
Chip Outline Dimensions

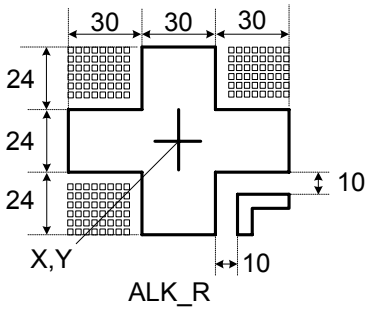
Item	Pad No.	Size (μm)	
		X	Y
Chip boundary	-	6440	684
Chip height	All pads	300	
Bump size	I/O	40	80
	SEG	15	110
	COM	15	110
		110	15
Pad pitch	COM	30	
	SEG	28.05	
	I/O	55	
Bump height	All pads	9±2	

Alignment Mark Location

NO	X	Y
ALK_L	-3157	-288
ALK_R	3157	-288

unit: μm





Functional Description

Microprocessor Interface Selection

The 8080-Parallel Interface, 6800-Parallel Interface, Serial Interface (SPI) or I^2C Interface can be selected by different selections of IM0~2 as shown in Table 1.

Table. 1

Interface	Config			Data signal								Control signal				
	IM0	IM1	IM2	D7	D6	D5	D4	D3	D2	D1	D0	E/$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	A0	$\overline{RES}$
6800	0	0	1	D7	D6	D5	D4	D3	D2	D1	D0	E	R/$\overline{W}$	$\overline{CS}$	A0	$\overline{RES}$
8080	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	A0	$\overline{RES}$
4-Wire SPI	0	0	0	Hz（Note1）						SI	SCL	Pull High or Low		$\overline{CS}$	A0	$\overline{RES}$
3-Wire SPI	1	0	0	Hz（Note1）						SI	SCL	Pull High or Low		$\overline{CS}$	Pull Low	$\overline{RES}$
I^2C	0	1	0	Hz（Note1）						SDA	SCL	Pull High or Low		Pull Low	SA0	$\overline{RES}$

Note1: When Serial Interface (SPI) or I^2C Interface is selected, D7~D2 is Hz. D7~ D2 is recommended to connect the V_{DD1} or V_{SS}. It is also allowed to leave D7~ D2 unconnected.

6800-series Parallel Interface

The parallel interface consists of 8 bi-directional data pads (D7-D0), R/$\overline{W}$, E, A0 and $\overline{CS}$ .It includes 2 forms.

Form 1: A falling edge of E input serve as READ latch signal while $\overline{CS}$ is kept low and R/$\overline{W}$ is kept high. A falling edge of E input serve as WRITE latch signal while $\overline{CS}$ is kept low and R/$\overline{W}$ is kept low. This is shown in Table.2 below.

Table.2-Control pins of 6800 interface (Form 1)

Function	$\overline{CS}$	A0	R/$\overline{W}$	E
Write command	L	L	L	↓
Read status	L	L	H	↓
Write data	L	H	L	↓
Read data	L	H	H	↓

1. ' ↓ 'stands for falling edge of signal.
2. ' H 'stands for high in signal, ' L ' stands for low in signal.

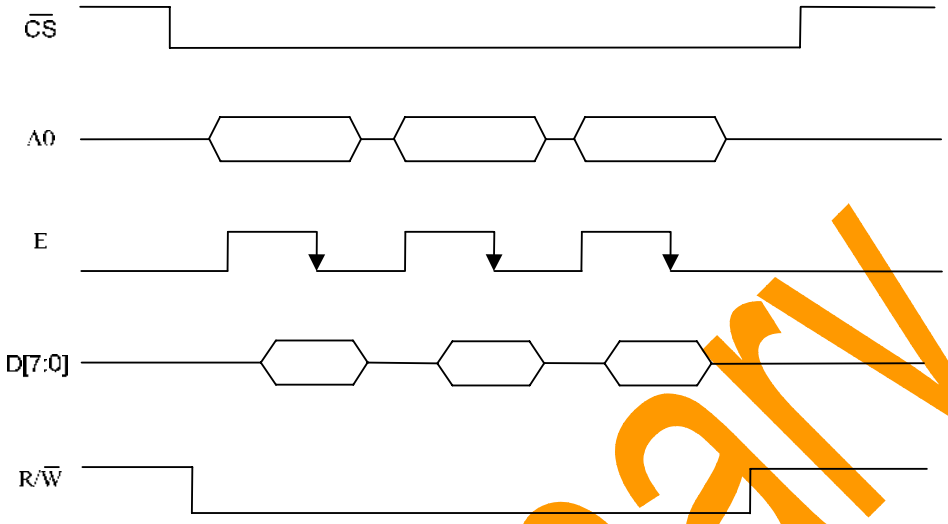


Figure. 1 Example of write procedure in 6800 parallel interface form 1

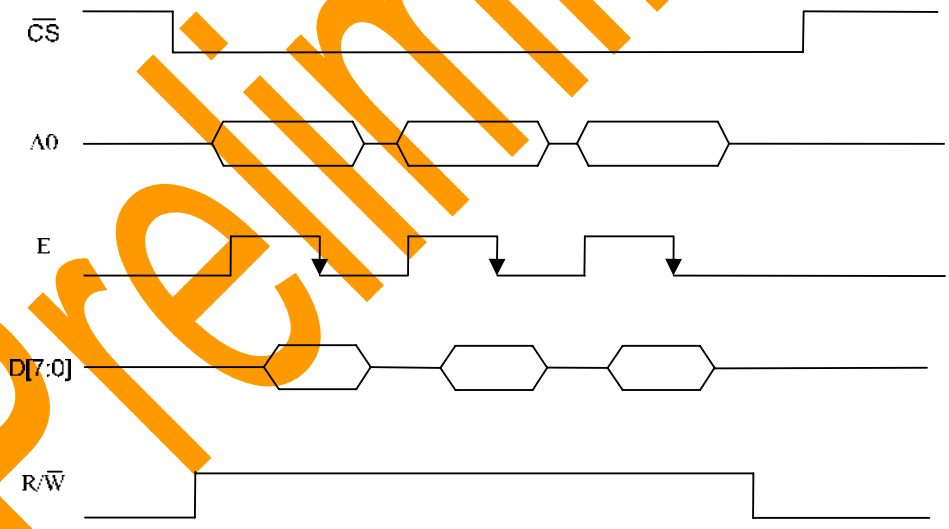


Figure. 2 Example of read procedure in 6800 parallel interface form 1

Form 2: A rising edge of $\overline{CS}$ input serve as READ latch signal while E is kept high and R/$\overline{W}$ is kept high. A rising edge of $\overline{CS}$ input serve as WRITE latch signal while E is kept high and R/$\overline{W}$ is kept low. A low in A0 indicates COMMAND read/write and high in A0 indicates DATA read/write. This is shown in Table.3 below.

Table.3-Control pins of 6800 interface (Form 2)

Function	**$\overline{CS}$**	**A0**	R/$\overline{W}$	**E**
Write command	↑	L	L	H
Read status	↑	L	H	H
Write data	↑	H	L	H
Read data	↑	H	H	H

Note:

1. ' ↓ 'stands for falling edge of signal.
2. ' H 'stands for high in signal, ' L ' stands for low in signal.

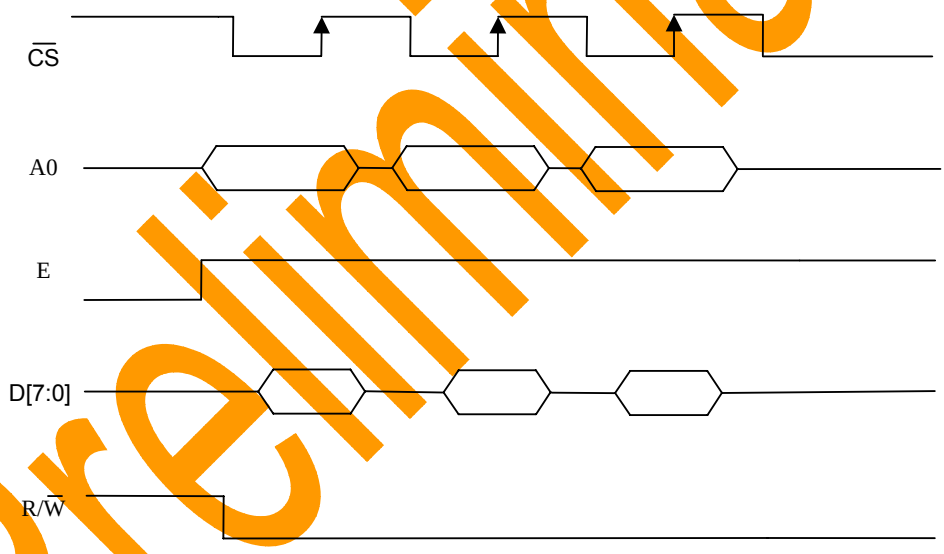


Figure. 3 Example of write procedure in 6800 parallel interface form 2

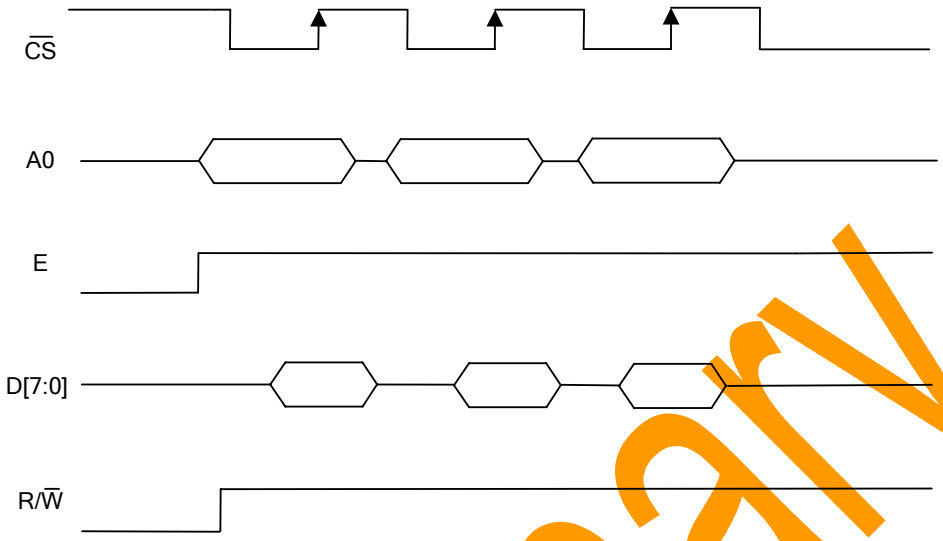


Figure. 4 Example of read procedure in 6800 parallel interface form 2

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing are internally performed, which require the insertion of a dummy read before the first actual display data read. This is shown in

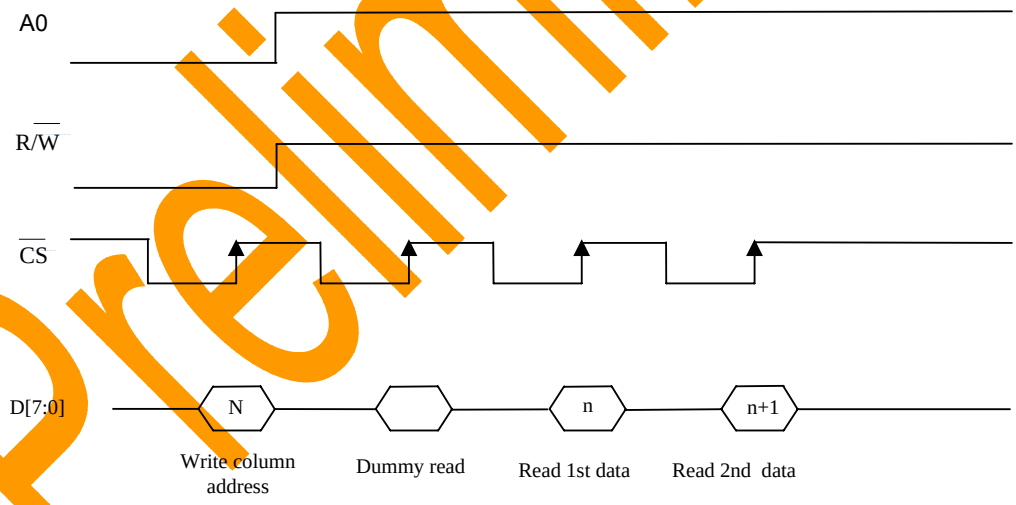


Figure. 5 Read data process–insertion of dummy read

8080-series Parallel Interface

The parallel interface consists of 8 bi-directional data pads (D7-D0), $\overline{WR}$, $\overline{RD}$, A0 and $\overline{CS}$. It includes 2 forms.

Form 1: A rising edge of $\overline{RD}$ input serve as data READ latch signal while $\overline{CS}$ is kept low. A rising edge of $\overline{WR}$ input serve as data READ latch signal while $\overline{CS}$ is kept low. A low in A0 indicates COMMAND read/write and high in A0 indicates DATA read/write. This is shown in Table.4 below.

Table.4-Control pins of 8080 interface (Form 1)

Function	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$
Write command	L	L	H	↑
Read status	L	L	↑	H
Write data	L	H	H	↑
Read data	L	H	↑	H

Note:

1. ' ↑ 'stands for rising edge of signal.
2. ' H 'stands for high in signal, ' L ' stands for low in signal.

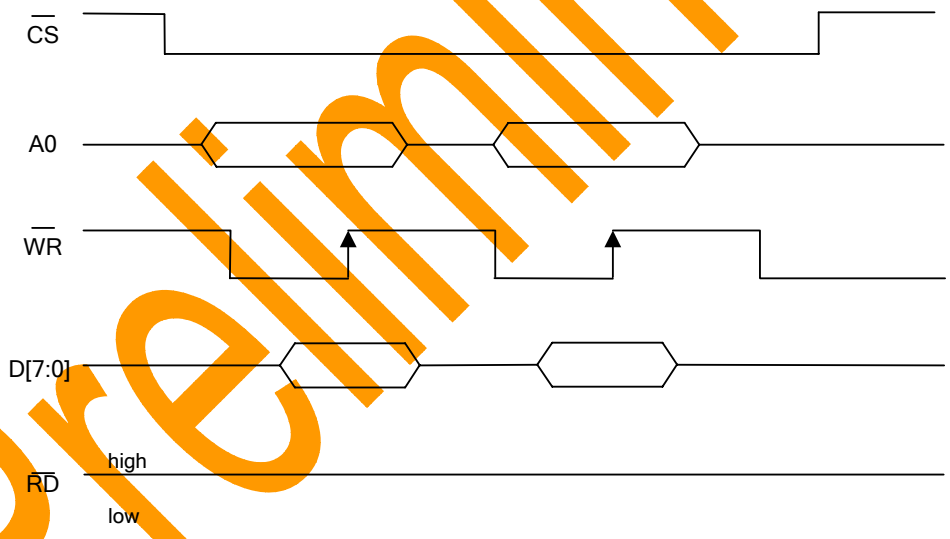


Figure. 6 Example of write procedure in 8080 parallel interface form 1

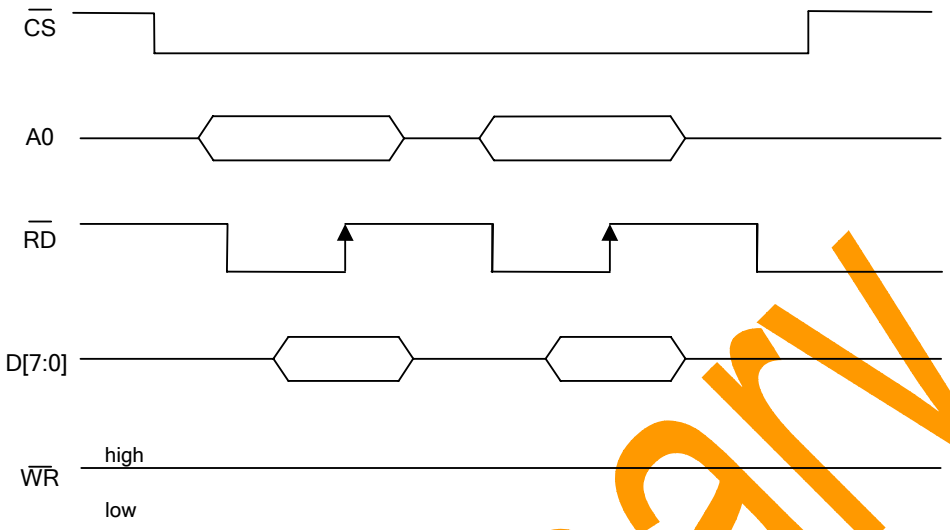


Figure.7 Example of read procedure in 8080 parallel interface form 1

Form 2: A rising edge of $\overline{CS}$ input serve as data READ latch signal while $\overline{RD}$ is kept low. A rising edge of $\overline{CS}$ input serve as data READ latch signal while $\overline{WR}$ is kept low. A low in A0 indicates COMMAND read/write and high in A0 indicates DATA read/write. This is shown in Table.5 below.

Table.5-Control pins of 8080 interface (Form 2)

Function	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$
Write command	↑	L	H	L
Read status	↑	L	L	H
Write data	↑	H	H	L
Read data	↑	H	L	H

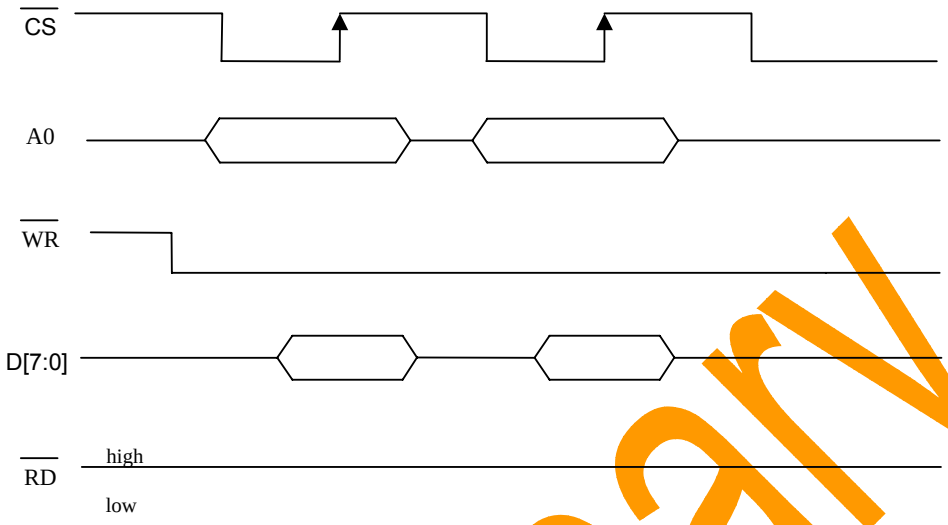


Figure.8 Example of write procedure in 8080 parallel interface form 2

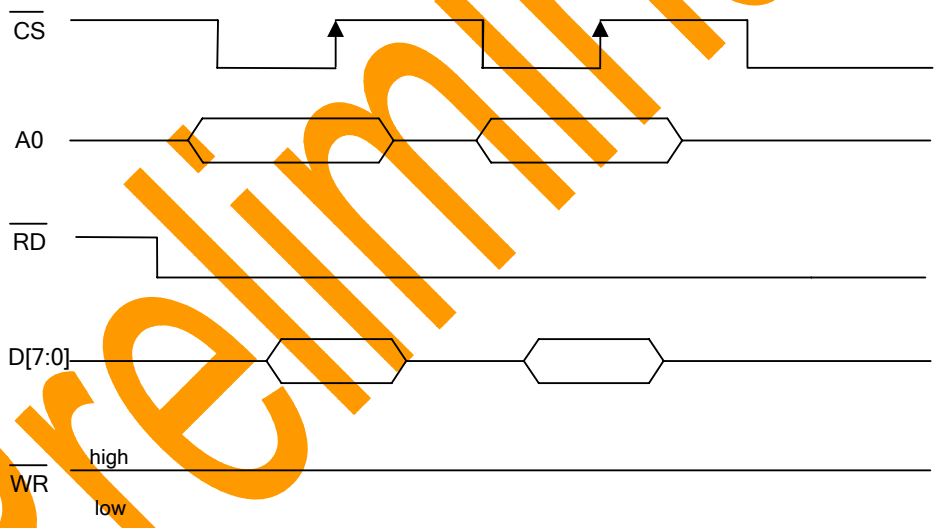


Figure.9 Example of read procedure in 8080 parallel interface form 2

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing are internally performed, which require the insertion of a dummy read before the first actual display data read. This is shown in

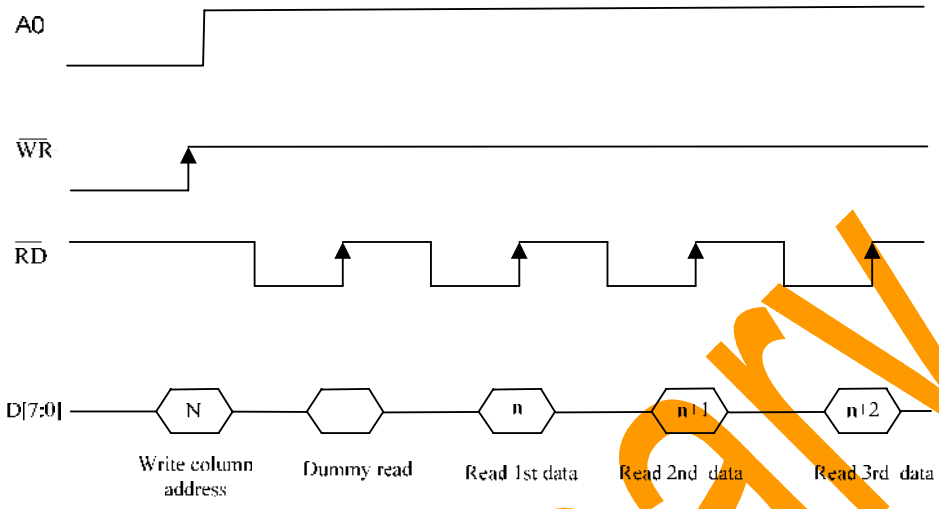


Figure.10 Read data process–insertion of dummy read

4 Wire Serial Interface (4-wire SPI)

The serial interface consists of serial clock SCL, serial data SI, A0 and $\overline{CS}$. SI is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, … and D0. A0 is sampled on every eighth clock and the data byte in the shift register is written to the display data RAM (A0=1) or command register (A0=0) in the same clock. See Figure .11

Table. 6

IM0	IM1	IM2	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0	D1	D2 to D7
0	0	0	4-wire SPI	$\overline{CS}$	A0	-	-	SCL	SI	(Hz)

Note: "-" pin must always be HIGH or LOW. D7~ D2 is recommended to connect the V_{DD1} or V_{SS}. It is also allowed to leave D7~ D2 unconnected.

The serial interface is initialized when $\overline{CS}$ is high. In this state, SCL clock pulse or SDI data have no effect. A falling edge on $\overline{CS}$ enables the serial interface and indicates the start of data transmission. The SPI is also able to work properly when the $\overline{CS}$ always keep low, but it is not recommended.

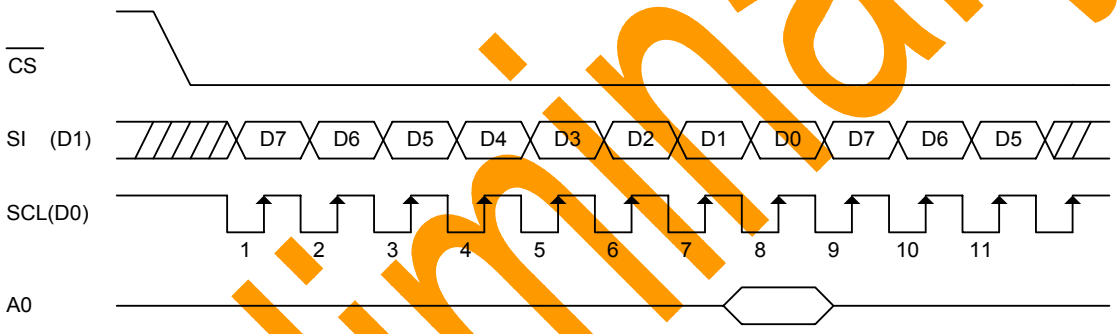


Figure .11 4-wire SPI data transfer

When the chip is not active, the shift registers and the counter are reset to their initial statuses.

Read is not possible while in serial interface mode.

Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend the operation be rechecked on the actual equipment.

3 Wire Serial Interface (3-wire SPI)

The 3 wire serial interface consists of serial clock SCL, serial data SI, and $\overline{CS}$. SI is shifted into an 9-bit shift register on every rising edge of SCL in the order of $D/\overline{C}$, D7, D6, … and D0. The $D/\overline{C}$ bit (first of the 9 bit) will determine the transferred data is written to the display data RAM ($D/\overline{C}$=1) or command register ($D/\overline{C}$=0).

Table. 7

IM0	IM1	IM2	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0	D1	D2 to D7
1	0	0	3-wire SPI	$\overline{CS}$	Pull Low	-	-	SCL	SI	(Hz)

Note: "-" pin must always be HIGH or LOW. D7~ D2 is recommended to connect the V_{DD1} or V_{SS}. It is also allowed to leave D7~ D2 unconnected.

The serial interface is initialized when $\overline{CS}$ is high. In this state, SCL clock pulse or SDI data have no effect. A falling edge on $\overline{CS}$ enables the serial interface and indicates the start of data transmission. The SPI is also able to work properly when the $\overline{CS}$ always keep low, but it is not recommended.

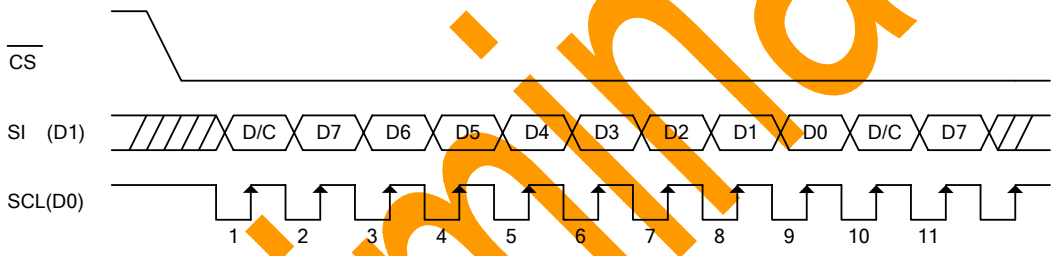


Figure. 12 3-wire SPI data transfer

When the chip is not active, the shift registers and the counter are reset to their initial statuses.

Read is not possible while in serial interface mode.

Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend the operation be rechecked on the actual equipment.

I^2C-bus Interface

The CH1115 can transfer data via a standard I^2C-bus and has slave mode only in communication. The command or RAM data can be written into the chip and the status and RAM data can be read out of the chip.

IM0	IM1	IM2	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0	D1	D2 to D7
0	1	0	I^2C Interface	Pull Low	SA0	-	-	SCL	SDA	(Hz)

Note: "-" pin must always be HIGH or LOW. D7~ D2 is recommended to connect the V_{DD1} or V_{SS}. It is also allowed to leave D7~ D2 unconnected.

$\overline{CS}$ signal could always pull low in I^2C-bus application.

Characteristics of the I^2C-bus

The I^2C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Note: The positive supply of pull-up resistor must equal to the value of V_{DD1}.

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

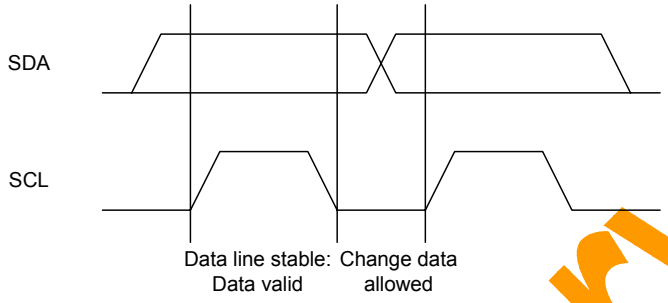


Figure. 13 Bit Transfer

Start and Stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).

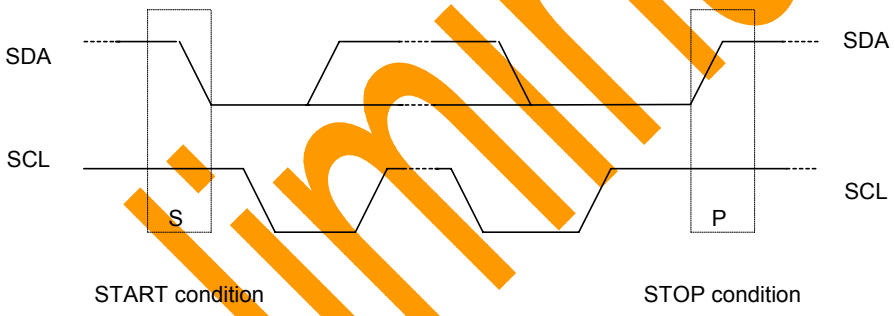


Figure. 14 Start and Stop conditions

System configuration

- Transmitter: The device that sends the data to the bus.
- Receiver: The device that receives the data from the bus.
- Master: The device that initiates a transfer, generates clock signals and terminates a transfer.
- Slave: The device addressed by a master.
- Multi-Master: More than one master can attempt to control the bus at the same time without corrupting the message
- Arbitration: Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.
- Synchronization: Procedure to synchronize the clock signals of two or more devices.

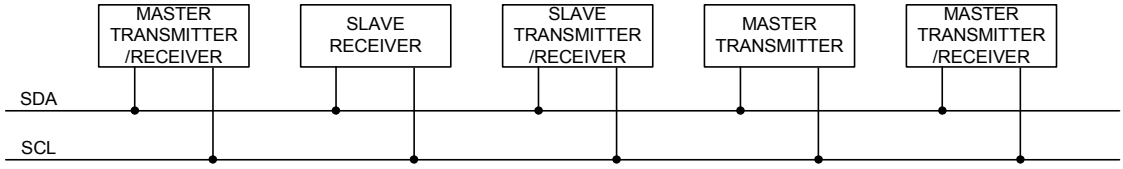


Figure. 15 System configuration

Acknowledge

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

Figure.16 Acknowledge

Protocol

The CH1115 supports both read and write access. The $R/\overline{W}$ bit is part of the slave address. Before any data is transmitted on the I^2C-bus, the device that should respond is addressed first. Two 7-bit slave addresses (0111100 and 0111101) are reserved for the CH1115. The least significant bit of the slave address is set by connecting the input SA0 to either logic 0(VSS) or 1 (VDD1). The I^2C-bus protocol is illustrated in Fig.16. The sequence is initiated with a START condition (S) from the I^2C-bus master that is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I^2C-bus transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves. A command word consists of a control byte, which defines Co and $D/\overline{C}$ (note1), plus a data byte (see Fig.16). The last control byte is tagged with a cleared most significant bit, the continuation bit Co. After a control byte with a cleared Co-bit, only data bytes will follow. The state of the $D/\overline{C}$-bit defines whether the data-byte is interpreted as a command or as RAM-data. The control and data bytes are also acknowledged by all addressed slaves on the bus. After the last control byte, depending on the $D/\overline{C}$ bit setting, either a series of display data bytes or command data bytes may follow. If the $D/\overline{C}$ bit was set to '1', these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended CH1115 device. If the $D/\overline{C}$ bit of the last control byte was set to '0', these command bytes will be decoded and the setting of the device will be changed according to the received commands. The acknowledgement after each byte is made only by the addressed slave. At the end of the transmission the I^2C-bus master issues a stop condition (P). If the $R/\overline{W}$ bit is set to one in the slave-address, the chip will output data immediately after the slave-address according to the $D/\overline{C}$ bit, which was sent during the last write access. If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

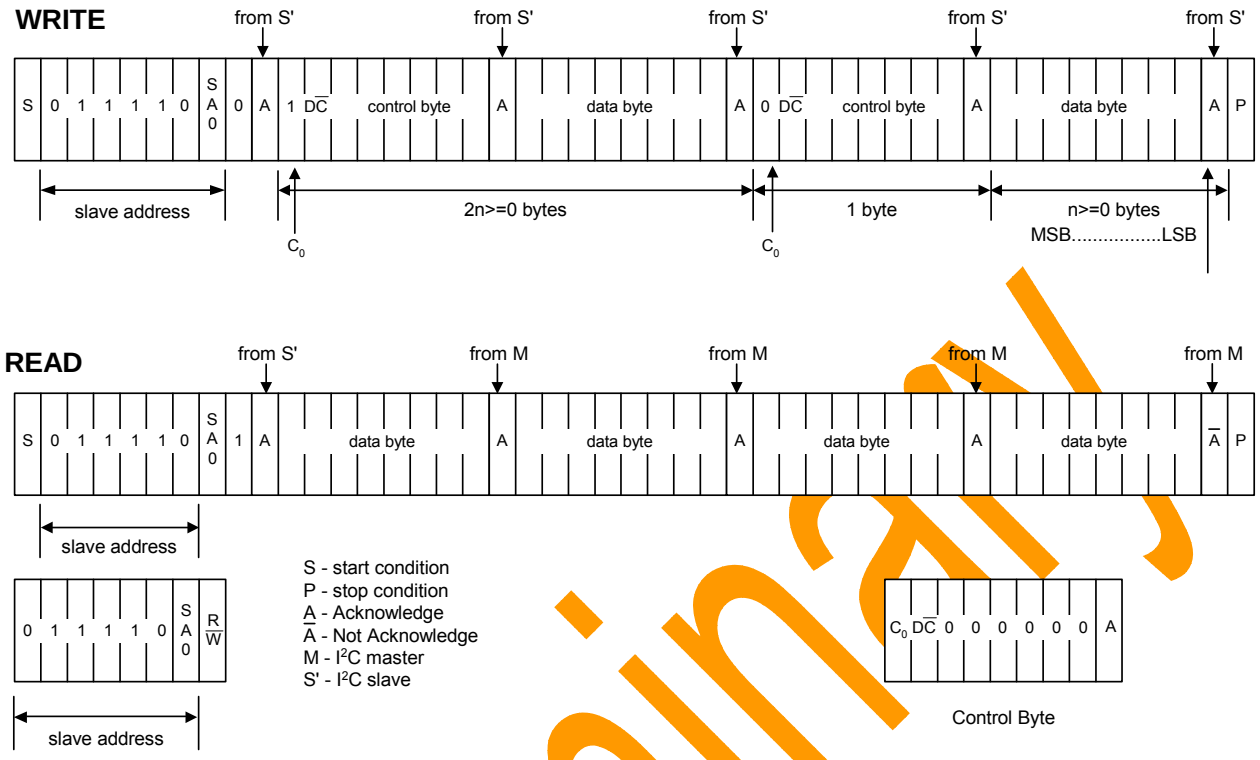


Figure.17 I²C Protocol

Note1:

1. Co= "0" : The last control byte , only data bytes to follow,
   Co= "1" : Next two bytes are a data byte and another control byte;
2. D/C = "0" : The data byte is for command operation,
   D/C = "1" : The data byte is for RAM operation.

Access to Display Data RAM and Internal Registers

This module determines whether the input data is interpreted as data or command. When A0 = "H", the inputs at D7 - D0 are interpreted as data and be written to display RAM. When A0 = "L", the inputs at D7 - D0 are interpreted as command, they will be decoded and be written to the corresponding command registers.

Display Data RAM

The Display Data RAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128 X 64 bits.

For mechanical flexibility, re-mapping on both segment and common outputs can be selected by software.

For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display.

The Page Address Circuit

As shown in Figure. 18, page address of the display data RAM is specified through the Page Address Set Command. The page address must be specified again when changing pages to perform access.

The Column Address

As shown in Figure.18, the display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/ write command. This allows the MPU display data to be accessed continuously. Because the column address is independent of the page address, when moving, for example, from page0 column 7FH to page 1 column 00H, it is necessary to re-specify both the page address and the column address.

Furthermore, as shown in Table. 8, the Column re-mapping (ADC) command (segment driver direction select command) can be used to reverse the relationship between the display data RAM column address and the segment output. Because of this, the constraints on the IC layout when the OLED module is assembled can be minimized.

Table. 8

Segment Output	SEG0		SEG128
ADC “0”	0 (H) →	Column Address	→ 7F (H)
ADC “1”	7F(H) ←	Column Address	← 0 (H)

The Line Address Circuit

The line address circuit, as shown in Figure.18, specifies the line address relating to the common output when the contents of the display data RAM are displayed. Using the display start line address set command, what is normally the top line of the display can be specified (this is the COM0 output when the common output mode is normal, and the COM63 output for CH1115, when the common output mode is reversed. The display area is a 64-line area for the CH1115 from the display start line address.

If the line addresses are changed dynamically using the display start line address set command, screen scrolling, page swapping, etc. that can be performed relationship between display data RAM and address (if initial display line is 1DH).

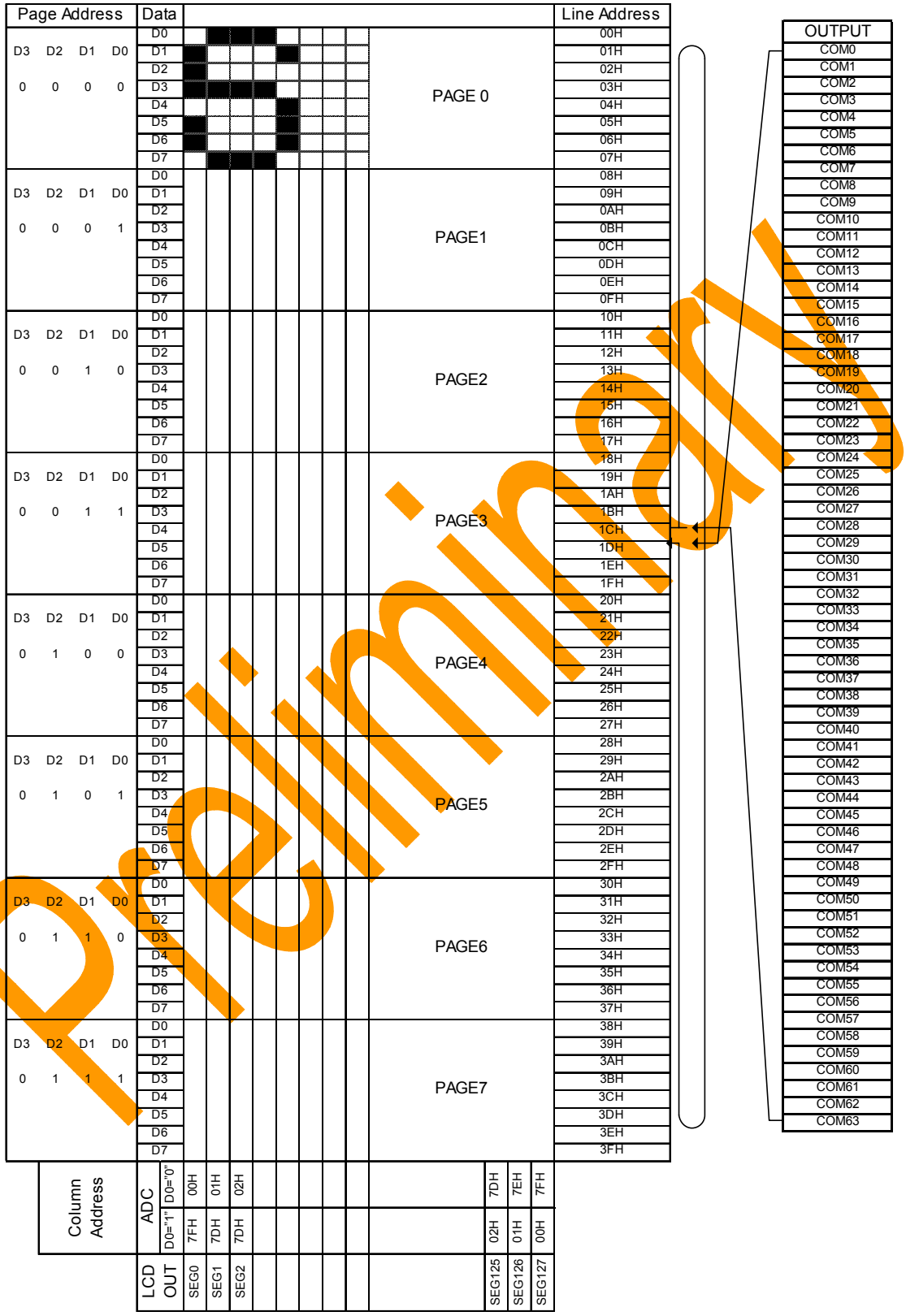

Page Address
Data
Line Address
OUTPUT
PAGE 0
PAGE1
PAGE2
PAGE3
PAGE4
PAGE5
PAGE6
PAGE7
Column Address
ADC
LCD OUT
Preliminary

Figure. 18

The Oscillator Circuit

This is a RC type oscillator (Figure.19) that produces the display clock. The oscillator circuit is only enabled when CLS = “H”. When CLS = “L”, the oscillation stops and the display clock is inputted through the CL terminal.

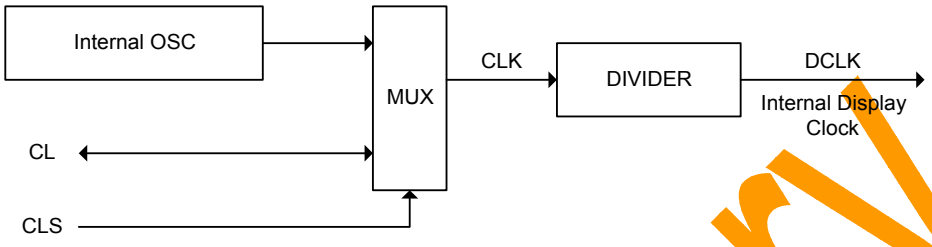


Figure.19

Charge Pump Regulator

This block accompanying only 2 external capacitors, is used to generate a 6.4V~10.0V voltage for OLED panel. This regulator can be turned ON/OFF by software command 8Bh setting.

Charge Pump output voltage control

This block is used to set the voltage value of charger pump output. The driving voltage can be adjusted from 6.4V up to 10.0V. This used to meet different demand of the panel.

Current Control and Voltage Control

This block is used to derive the incoming power sources into different levels of internal use voltage and current. VPP and VDD2 are external power supplies. I_{REF} is a reference current source for segment current drivers.

Common Drivers/Segment Drivers

Segment drivers deliver 128 current sources to drive OLED panel. The driving current can be adjusted up to 500μA with 256 steps. Common drivers generate voltage scanning pulses.

Reset Circuit

When the $\overline{RES}$ input falls to "L", these reenter their default state.
The default settings are shown below:

1. Display is OFF. Common and segment are in high impedance state.
2. 128 X 64 Display mode.
3. Normal segment and display data column address and row address mapping (SEG0 is mapped to column address 00H and COM0 mapped to row address 00H).
4. Shift register data clear in serial interface.
5. Display start line is set at display RAM line address 00H.
6. Column address counter is set at 0.
7. Normal scanning direction of the common outputs.
8. Contrast control register is set at 80H.
9. Internal DC-DC is selected.

Commands

The CH1115 uses a combination of A0, $\overline{RD}$ (E) and $\overline{WR}$ ($R/\overline{W}$) signals to identify data bus signals. As the chip analyzes and executes each command using internal timing clock only regardless of external clock, its processing speed is very high and its busy check is usually not required. The 8080 series microprocessor interface enters a read status when a low pulse is input to the $\overline{RD}$ pad and a write status when a low pulse is input to the $\overline{WR}$ pad. The 6800 series microprocessor interface enters a read status when a high pulse is input to the $R/\overline{W}$ pad and a write status when a low pulse is input to this pad. When a high pulse is input to the E pad, the command is activated. (For timing, see AC Characteristics.). Accordingly, in the command explanation and command table, $\overline{RD}$ (E) becomes 1(HIGH) when the 6800 series microprocessor interface reads status of display data. This is an only different point from the 8080 series microprocessor interface.

Taking the 8080 series, microprocessor interface as an example command will explain below.

When the serial interface is selected, input data starting from D7 in sequence.

Command Set

1. Set Lower Column Address: (00H - 0FH)
2. Set Higher Column Address: (10H – 1FH)

   Specifies column address of display RAM. Divide the column address into 4 higher bits and 4 lower bits. Set each of them into successions. When the microprocessor repeats to access to the display RAM, the column address counter is incremented during each access until address 127 is accessed. The page address is not changed during this time.

	A0	E / $\overline{RD}$	$R/\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
Higher bits	0	1	0	0	0	0	1	0	A6	A5	A4
Lower bits	0	1	0	0	0	0	0	A3	A2	A1	A0

A6	A5	A4	A3	A2	A1	A0	Display address
0	0	0	0	0	0	0	0(POR)
0	0	0	0	0	0	1	1
			:				:
1	1	1	1	1	1	1	127

Note: Don't use any commands not mentioned above.

3. Set Breathing Display Effect: (Double Bytes Command)

This command set Breathing Display Effect ON/OFF and Time Interval.

■ Breathing Light Set: (23H)

A0	$\frac{E}{RD}$	$\frac{R/W}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	0	1	1
0	1	0	ON/ OFF	*	*	A4	A3	A2	A1	A0

■ ON/OFF set:

When ON/OFF ="L", Breathing Light OFF. (POR)
When ON/OFF ="H", Breathing Light ON.

■ Breathing Display Effect Maximum Brightness Adjust Set: (A4 – A3)

A_4	A_3	Maximum Brightness (Contrast+1)
0	0	256(POR)
0	1	128
1	0	64
1	1	32

■ Breathing Display Effect Time Interval Set: (A2 – A0)

A_2	A_1	A_0	Time Interval step
0	0	0	1 Frames
0	0	1	2 Frames(POR)
0	1	0	3 Frames
:	:	:	:
1	1	0	7 Frames
1	1	1	8 Frames

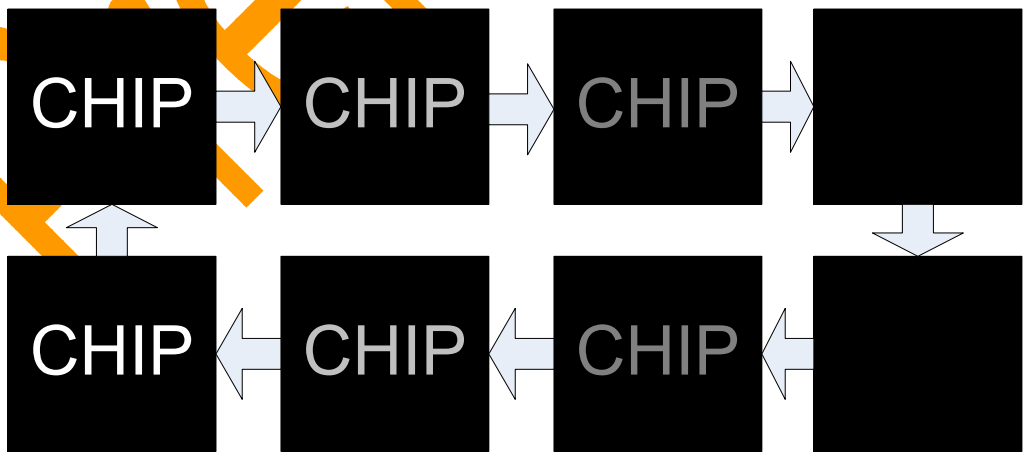


Figure.20

4. Additional Horizontal Scroll Setup: (Three Bytes Command)
This command consists of 3 consecutive bytes to set up the horizontal scroll parameters. It determined the scrolling start column position and end column position. The end column position must be larger than start column position.

■ Additional Horizontal Scroll Setup Mode Set: (24H)

A0	$\frac{E}{RD}$	$\frac{R/W}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	1	0	0
0	1	0	A7	A6	A5	A4	A3	A2	A1	A0
0	1	0	B7	B6	B5	B4	B3	B2	B1	B0

■ Start Column Position Set: (A7 – A0)

A0	$\frac{E}{RD}$	$\frac{R/W}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Column Position
0	1	0	*	0	0	0	0	0	0	0	0(POR)
0	1	0	*	0	0	0	0	0	0	1	1
0	1	0					:				:
0	1	0	*	1	1	1	1	1	1	0	126
0	1	0	*	1	1	1	1	1	1	1	127

■ End Column Position Set: (B7 – B0)

A0	$\frac{E}{RD}$	$\frac{R/W}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Column Position
0	1	0	*	0	0	0	0	0	0	0	0
0	1	0	*	0	0	0	0	0	0	1	1
0	1	0					:				:
0	1	0	*	1	1	1	1	1	1	0	126
0	1	0	*	1	1	1	1	1	1	1	127 (POR)

Note: "*" stands for "Don't care".

Please see the following figure for relationship of start column position and end column position.

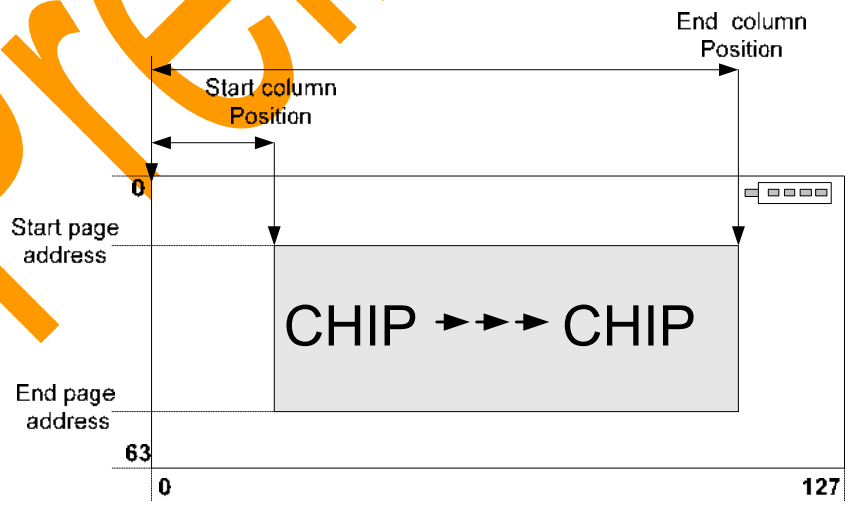


Figure.21

5. Horizontal Scroll Setup: (Four Bytes Command)

This command consists of 4 consecutive bytes to set up the horizontal scroll parameters. It determined the number of horizontal scroll per step , scrolling start page, time interval and end page.

Before issuing this command, the horizontal scroll must be deactivated (2EH). Otherwise, ram content may be corrupted.

■ Horizontal Scroll Setup Mode Set: (26H - 27H)

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	1	1	D
0	1	0	*	*	*	*	*	A2	A1	A0
0	1	0	*	*	*	*	*	B2	B1	B0
0	1	0	*	*	*	*	*	C2	C1	C0

D	Scroll Direction Set
0	Scroll Right(POR)
1	Scroll Left

■ Start Page Address Set: (A2 – A0)

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Start Page Address
0	1	0	*	*	*	*	*	0	0	0	0(POR)
0	1	0	*	*	*	*	*	0	0	1	1
0	1	0					:				:
0	1	0	*	*	*	*	*	1	1	0	6
0	1	0	*	*	*	*	*	1	1	1	7

■ Time Interval Set: (B2 – B0)

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Time Interval
0	1	0	*	*	*	*	*	0	0	0	6 frames(POR)
0	1	0	*	*	*	*	*	0	0	1	32 frames
0	1	0	*	*	*	*	*	0	1	0	64 frames
0	1	0	*	*	*	*	*	0	1	1	128 frames
0	1	0	*	*	*	*	*	1	0	0	3 frames
0	1	0	*	*	*	*	*	1	0	1	4 frames
0	1	0	*	*	*	*	*	1	1	0	5 frames
0	1	0	*	*	*	*	*	1	1	1	2 frames

■ End Page Address Set: (C2 – C0)

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	End Page Address
0	1	0	*	*	*	*	*	0	0	0	0
0	1	0	*	*	*	*	*	0	0	1	1
0	1	0					:				:
0	1	0	*	*	*	*	*	1	1	0	6
0	1	0	*	*	*	*	*	1	1	1	7 (POR)

Note: "*" stands for "Don't care".

6. Set Scroll Mode: (28H – 2BH)

Control continuous or single screen scroll.

A0	$\overline{RD}$ E	$\overline{WR}$ R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	1	0	D1	D0

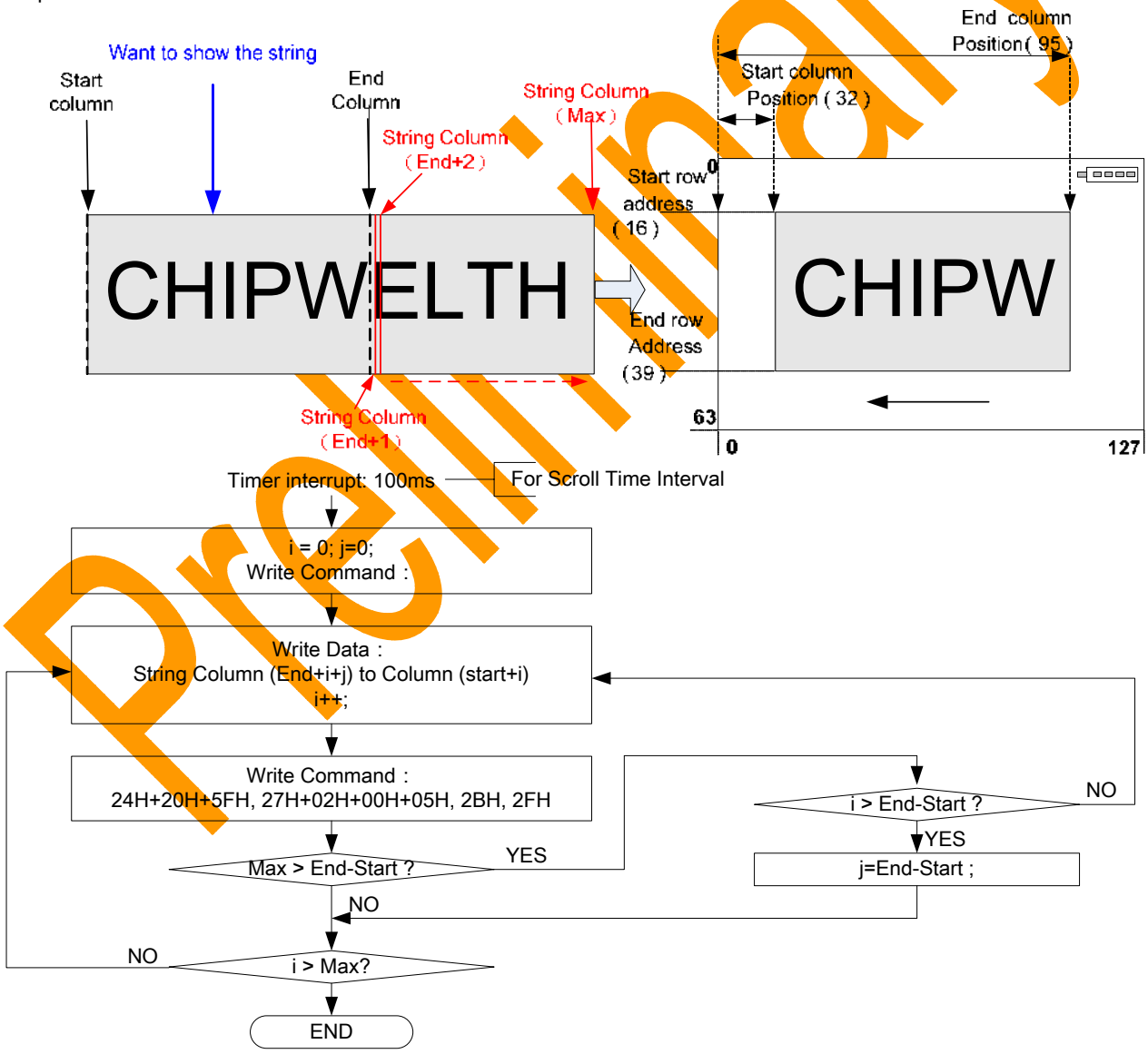
D1	D0	Scroll mode
0	0	Continuous horizontal/vertical scroll(default)
0	1	Single Screen scroll
1	x	1 Column scroll mode

■ Single column scroll mode

The display scroll one column after the 2BH+2FH commands are written.

The scroll is end after the 2EH command is written.

Example:



7. Set Deactivate /Activate Horizontal Scroll: (2EH - 2FH)

Stop or start motion of horizontal scrolling. This command should only be issued after horizontal scroll setup parameters (24H/26H/27H/28H/29H/2CH/2DH) are defined.

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	1	1	1	D

When D="L", Stop motion of horizontal scroll. (POR)
When D="H", Start motion of horizontal scroll.

Note: The following actions are prohibited after the horizontal scroll is activated

- Changing additional horizontal scroll setup parameters.
- Changing horizontal scroll setup parameters.
- Changing scroll mode setup parameters.

After the deactivate horizontal scroll issued, the display of screen is reset to original status.

8. Set Pump voltage value: (30H~33H)

Specifies output voltage (V_{PP}) of the internal charger pump.

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	1	0	0	A1	A0

A1	A0	Pump output voltage (V_{PP})
0	0	10.0
0	1	7.4
1	0	8.0(Power on)
1	1	9.0

9. Set Display Start Line: (40H - 7FH)

Specifies line address (refer to Figure. 18) to determine the initial display line or COM0. The RAM display data becomes the top line of OLED screen. It is followed by the higher number of lines in ascending order, corresponding to the duty cycle. When this command changes the line address, the smooth scrolling or page change takes place.

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	A5	A4	A3	A2	A1	A0

A5	A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
			:			:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

10. Set Contrast Control Register: (Double Bytes Command)

This command is to set contrast setting of the display. The chip has 256 contrast steps from 00 to FF. The segment output current increases as the contrast step value increases.

Segment output current setting: ISEG = (α+1)/256 X I_{REF} X scale factor

Where: α is contrast step; Scale factor = 16.

■ The Contrast Control Mode Set: (81H)

When this command is input, the contrast data register set command becomes enabled. Once the contrast control mode has been set, no other command except for the contrast data register command can be used. Once the contrast data set command has been used to set data into the register, then the contrast control mode is released.

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1
0	1	0	A7	A6	A5	A4	A3	A2	A1	A0

■ Contrast Data Register Set: (00H – FFH)

By using this command to set eight bits of data to the contrast data register; the OLED segment output assumes one of the 256 current levels.

When this command is input, the contrast control mode is released after the contrast data register has been set.

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	I_{SEG}
0	1	0	0	0	0	0	0	0	0	0	Small
0	1	0	0	0	0	0	0	0	0	1	
0	1	0	0	0	0	0	0	0	1	0	
0	1	0					:				:
0	1	0	1	0	0	0	0	0	0	0	POR
0	1	0					:				:
0	1	0	1	1	1	1	1	1	1	0	
0	1	0	1	1	1	1	1	1	1	1	Large

When the contrast control function is not used, set the D7 - D0 to 1000,0000.

11. I_{REF} Resistor Set and Adjust I_{SEG} by PAD: (Double Bytes Command)

I_{REF} can be controlled by external resister or internal resister.

■ I_{REF} Resister Set: (82H)

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	1	0
0	1	0	ON/ OFF	*	*	*	*	D	A1	A0

When D = “L”, External resistor is selected(POR).

When D = “H”, Internal resistor is selected.

■ Internal Resistor Set: (A1 – A0)

A1	A0	Resistor (K)
0	0	510(POR)
0	1	310
1	0	220
1	1	180

When VPP=9V, Contrast=255, I_{REF} Resistor & IREF Table(Just for reference):

I_{REF} Resistor (K)	I_{REF} (uA)	I_{SEG} (uA)
360	12.50	200
160	18.75	300
70	25.0	400
30	31.25	500

■ Adjust I_{SEG} by PAD[6:2]

When ON/OFF = “L”, Disable I_{SEG} adjust. (POR).

When ON/OFF = “H”, Enable I_{SEG} adjust.

I_{SEG} change with the value of D2-D6 pin.

Step number		D6	D5	D4	D3	D2	I_{SEG} adjust
Up	0	0	0	0	0	0	0%
	1	0	0	0	0	1	3%
	2	0	0	0	1	0	6%
	3	0	0	0	1	1	9%
	4	0	0	1	0	0	12%
	5	0	0	1	0	1	15%
	6	0	0	1	1	0	18%
	7	0	0	1	1	1	21%
	8	0	1	0	0	0	24%
	9	0	1	0	0	1	27%
	10	0	1	0	1	0	30%
	11	0	1	0	1	1	33%
	12	0	1	1	0	0	36%
	13	0	1	1	0	1	39%
	14	0	1	1	1	0	42%
	15	0	1	1	1	1	45%
	0	1	0	0	0	0	0%

Down	1	1	0	0	0	1	-3%
	2	1	0	0	1	0	-6%
	3	1	0	0	1	1	-9%
	4	1	0	1	0	0	-12%
	5	1	0	1	0	1	-15%
	6	1	0	1	1	0	-18%
	7	1	0	1	1	1	-21%
	8	1	1	0	0	0	-24%
	9	1	1	0	0	1	-27%
	10	1	1	0	1	0	-30%
	11	1	1	0	1	1	-33%
	12	1	1	1	0	0	-36%
	13	1	1	1	0	1	-39%
	14	1	1	1	1	0	-42%
	15	1	1	1	1	1	0%

Note1: When 8080/6800 interface is used, I_{SEG} adjust is disabled.

Note2: When I_{SEG} adjust is used, Contrast value should be set to 0x80.

Example: up step 9, Pin[D6:D2]=[01001]

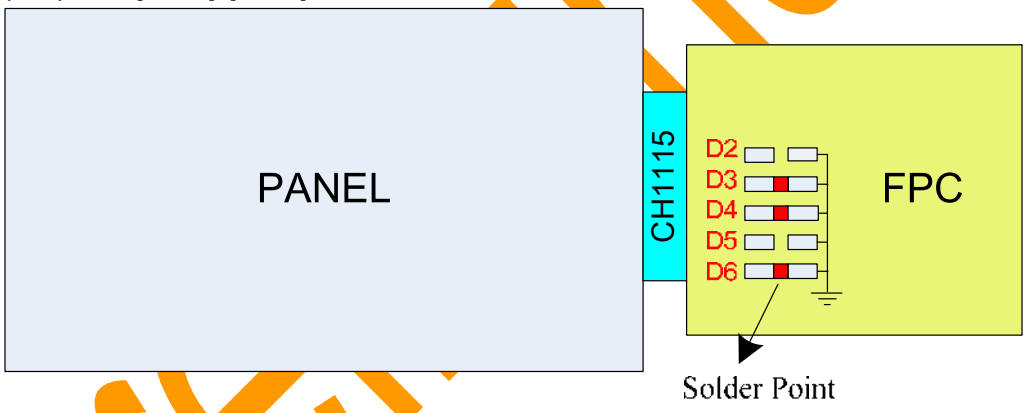


Figure.22

12. Set Segment Re-map: (A0H - A1H)

Change the relationship between RAM column address and segment driver. The order of segment driver output pads can be reversed by software. This allows flexible IC layout during OLED module assembly. For details, refer to the column address section of Figure. 18. When display data is written or read, the column address is incremented by 1 as shown in Figure.18.

A0	$\frac{E}{RD}$	$\frac{R/W}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	ADC

When ADC = “L”, the right rotates (normal direction). (POR)

When ADC = “H”, the left rotates (reverse direction).

13. Set SEG pads hardware configuration: (A2H – A3H)

This command is to set the SEG signals pad configuration to match the OLED panel hardware layout.

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	1	D

When D = “L”, Even on the left. (POR)

When D = “H”, Even on the right.

Please see the following figure for Set Segment Re-map and SEG pads hardware configuration.

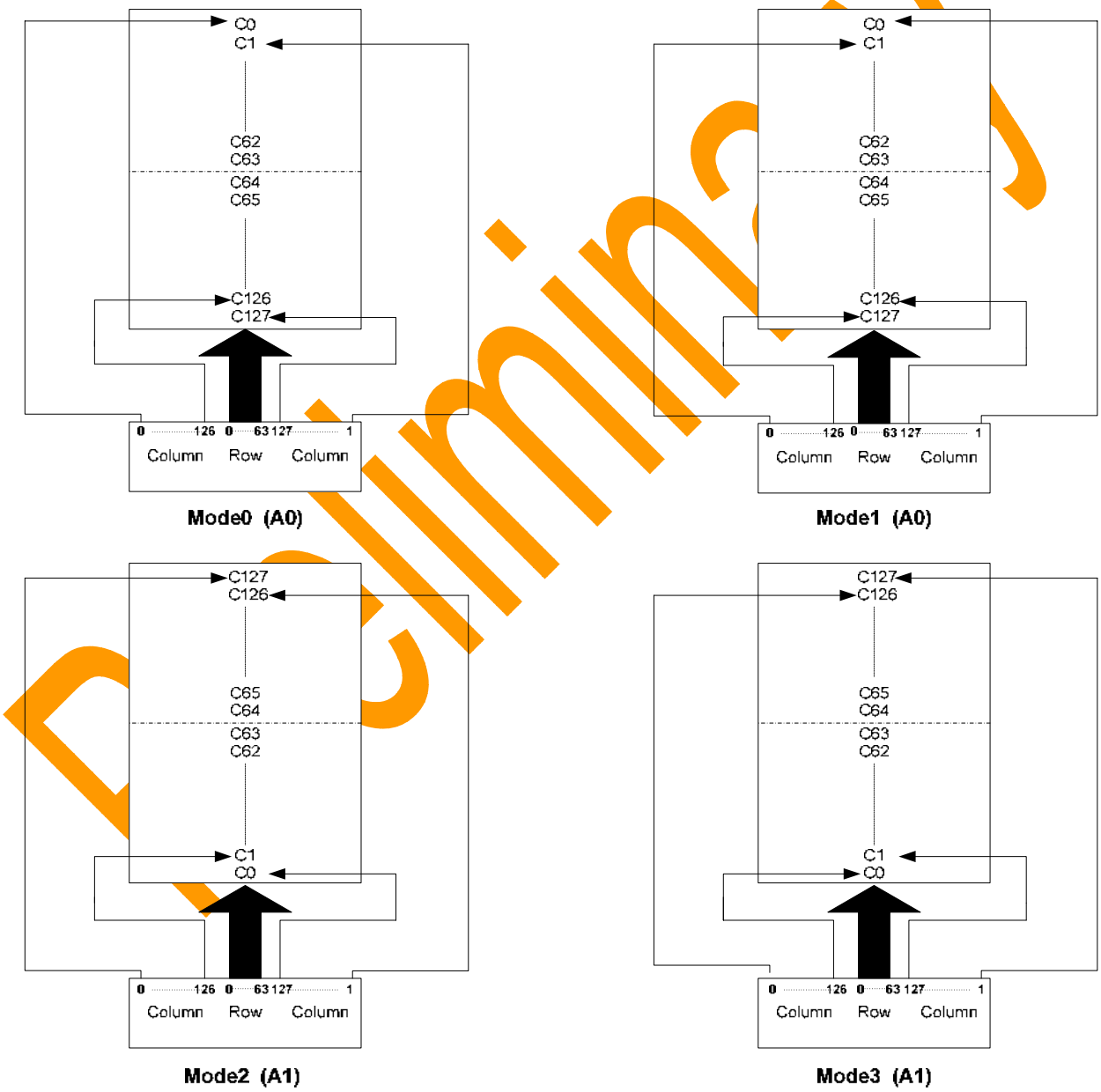


Figure.23

14. Set Entire Display OFF/ON: (A4H - A5H)

Forcibly turns the entire display on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held.

This command has priority over the normal/reverse display command.

A0	$\overline{RD}$ E	$\overline{WR}$ R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D

When D = “L”, the normal display status is provided. (POR)

When D = “H”, the entire display ON status is provided.

15. Set Normal/Reverse Display: (A6H -A7H)

Reverses the display ON/OFF status without rewriting the contents of the display data RAM.

A0	$\overline{RD}$ E	$\overline{WR}$ R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	1	D

When D = “L”, the RAM data is high, being OLED ON potential (normal display). (POR)

When D = “H”, the RAM data is low, being OLED ON potential (reverse display)

16.Set Multiplex Ration: (Double Bytes Command)

This command switches default 64 multiplex modes to any multiplex ratio from 1 to 64. The output pads COM0-COM63 will be switched to corresponding common signal.

■ Multiplex Ration Mode Set: (A8H)

A0	$\overline{RD}$ E	$\overline{WR}$ R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	0	0

■ Multiplex Ration Data Set: (00H - 3FH)

A0	$\overline{RD}$ E	$\overline{WR}$ R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	Multiplex Ratio
0	1	0	*	*	0	0	0	0	0	0	1
0	1	0	*	*	0	0	0	0	0	1	2
0	1	0	*	*	0	0	0	0	1	0	3
0	1	0					:				:
0	1	0	*	*	1	1	1	1	1	0	63
0	1	0	*	*	1	1	1	1	1	1	64 (POR)

17. Set DC-DC OFF/ON: (Double Bytes Command)

This command is to control the DC-DC voltage converter. The converter will be turned on by issuing this command then display ON command. The panel display must be off while issuing this command.

■ DC-DC Control Mode Set: (ADH)

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	0	1

■ DC-DC ON/OFF Mode Set: (8AH - 8BH)

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	1	0	1	D

When D = “L”, DC-DC is disabled.

When D = “H”, DC-DC will be turned on when display on. (POR)

Table. 9

DC-DC STATUS	DISPLAY ON/OFF STATUS	Description
0	0	Sleep mode
0	1	External V_{PP} must be used.
1	0	Sleep mode
1	1	Built-in DC-DC is used, Normal Display

18. Display OFF/ON: (AEH - AFH)

Alternatively turns the display on and off.

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	D

When D = “L”, Display OFF OLED. (POR)

When D = “H”, Display ON OLED.

When the display OFF command is executed, power saver mode will be entered.

Sleep mode:

This mode stops every operation of the OLED display system, and can reduce current consumption nearly to a static current value if no access is made from the microprocessor. The internal status in the sleep mode is as follows:

1) Stops the oscillator circuit and DC-DC circuit.
2) Stops the OLED drive and outputs Hz as the segment/common driver output.
3) Holds the display data and operation mode provided before the start of the sleep mode.
4) The MPU can access to the built-in display RAM.

19. Set Page Address: (B0H - B7H)

Specifies page address to load display RAM data to page address register. Any RAM data bit can be accessed when its page address and column address are specified. The display remains unchanged even when the page address is changed.

A0	$\frac{E}{RD}$	$\frac{R/W}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	A_3	A_2	A_1	A_0

A_3	A_2	A_1	A_0	Page address
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7

Note: Don't use any commands not mentioned above for user.

20. Set Common Output Scan Direction: (C0H - C8H)

This command sets the scan direction of the common output allowing layout flexibility in OLED module design. In addition, the display will have immediate effect once this command is issued. That is, if this command is sent during normal display, the graphic display will be vertically flipped.

A0	$\frac{E}{RD}$	$\frac{R/W}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	0	D	*	*	*

When D = "L", Scan from COM0 to COM [N -1]. (POR)

When D = "H", Scan from COM [N -1] to COM0.

21. Set Display Offset: (Double Bytes Command)

This is a double byte command. The next command specifies the mapping of display start line to one of COM0-63 (it is assumed that COM0 is the display start line, that equals to 0). For example, to move the COM16 towards the COM0 direction for 16 lines, the 6-bit data in the second byte should be given by 010000. To move in the opposite direction by 16 lines, the 6-bit data should be given by (64-16), so the second byte should be 100000.

■ Display Offset Mode Set: (D3H)

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	0	0	1	1

■ Display Offset Data Set: (00H~3FH)

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	COMx
0	1	0	*	*	0	0	0	0	0	0	0 (POR)
0	1	0	*	*	0	0	0	0	0	1	1
0	1	0	*	*	0	0	0	0	1	0	2
0	1	0					:				:
0	1	0	*	*	1	1	1	1	1	0	62
0	1	0	*	*	1	1	1	1	1	1	63

Note: "*" stands for "Don't care"

22. Set Display Clock Divide Ratio/Oscillator Frequency: (Double Bytes Command)

This command is used to set the frequency of the internal display clocks (DCLKs). It is defined as the divide ratioused to divide the oscillator frequency. POR is 8. Frame frequency is determined by divide ratio, number of display clocks per row, MUX ratio and oscillator frequency.

■ Divide Ratio/Oscillator Frequency Mode Set: (D5H)

A0	$\overline{RD}$ E	$\overline{WR}$ R / W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	0	1	0	1
0	1	0	A_7	A_6	A_5	A_4	*	*	A_1	A_0

A1 - A0 defines the divide ration of the display clocks (DCLK).

A_1	A_0	Divide Ration
0	0	8(POR)
0	1	16
1	0	3
1	1	4

A7 - A4 sets the oscillator frequency. Oscillator frequency increase with the value of A[7:4] and vice versa.

A7	A6	A5	A4	Oscillator Frequency of fOSC
0	0	0	0	-17.1%
0	0	0	1	-13.3%
0	0	1	0	-10.3%
0	0	1	1	-7.0%
0	1	0	0	-3.6%
0	1	0	1	fOSC (POR)
0	1	1	0	+3.0%
0	1	1	1	+6.2%
1	0	0	0	+8.6%
1	0	0	1	+11.2%
1	0	1	0	+13.8%
1	0	1	1	+16.3%
1	1	0	0	+18.6%
1	1	0	1	+20.7%
1	1	1	0	+22.8%
1	1	1	1	+25.1%

23. Set Adaptive Power Save: (D6H - D7H)

This command sets Adaptive Power Save.

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	0	1	1	D

When D = “L”, Normal.

When D = “H”, Adaptive Power Save (POR).

24. Set Discharge/Pre-charge Period: (Double Bytes Command)

This command is used to set the duration of the Discharge/Pre-charge period. The interval is counted in number of DCLK. POR is 6 DCLKs.

■ Pre-charge Period Mode Set: (D9H)

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	1	0	0	1

■ Discharge/Pre-charge Period Data Set: (00H - FFH)

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

Pre-charge Period Adjust: (A3 - A0)

A_3	A_2	A_1	A_0	Pre-charge Period
0	0	0	0	0 DCLK (Note)
0	0	0	1	3 DCLKs
0	0	1	0	6 DCLKs (POR)
		:		:
1	1	1	0	42 DCLKs
1	1	1	1	45 DCLKs

Discharge Period Adjust: (A7 - A4)

A_7	A_6	A_5	A_4	Discharge Period
0	0	0	0	INVALID
0	0	0	1	3 DCLKs
0	0	1	0	6 DCLKs (POR)
		:		:
1	1	1	0	42 DCLKs
1	1	1	1	45 DCLKs

Note:

When set A[3:0]=0, the period for display will increase 6 DCLKs. And there is no pre-charge period so that it will save power consumption.

25. Set VCOM Deselect Level: (Double Bytes Command)

This command is to set the common pad output voltage level at deselect stage.

■ VCOM Deselect Level Mode Set: (DBH)

A0	$\overline{RD}$ E	$\overline{WR}$ R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	1	0	1	1

■ VCOM Deselect Level Data Set: (00H - FFH)

A0	$\overline{RD}$ E	$\overline{WR}$ R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

$V_{COM} = \beta \times V_{REF} = (0.430 + A[7:0] \times 0.006415) \times V_{REF}$

A[7:0]	β	A[7:0]	β
00H	0.430	20H	0.635
01H	0.436	21H	0.642
02H	0.442	22H	0.648
03H	0.449	23H	0.654
04H	0.456	24H	0.661
05H	0.462	25H	0.667
06H	0.468	26H	0.674
07H	0.475	27H	0.680
08H	0.481	28H	0.687
09H	0.488	29H	0.693
0AH	0.494	2AH	0.699
0BH	0.501	2BH	0.706
0CH	0.507	2CH	0.712
0DH	0.513	2DH	0.719
0EH	0.520	2EH	0.725
0FH	0.526	2FH	0.731
10H	0.533	30H	0.738
11H	0.539	31H	0.744
12H	0.525	32H	0.751
13H	0.552	33H	0.757
14H	0.558	34H	0.764
15H	0.565	35H	0.770 (POR)
16H	0.571	36H	0.776
17H	0.578	37H	0.783
18H	0.584	38H	0.789
19H	0.590	39H	0.796
1AH	0.596	3AH	0.802
1BH	0.603	3BH	0.808
1CH	0.610	3CH	0.815
1DH	0.616	3DH	0.821
1EH	0.622	3EH	0.828
1FH	0.629	3FH	0.834
40H - FEH	1	FF	External

Note: V_{COM} voltage must be less than VPP voltage.

26. Set row non-overlap/SEG Hiz Period: (Double Bytes Command).

This command is used to set the duration of the row non-overlap /SEG Hiz Period period.

■ row non-overlap /SEG Hiz Period Set: (DCH)

A0	$\overline{RD}$ E	$\overline{WR}$ R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	1	1	0	0

■ Row non-overlap /SEG Hiz Period Data Set: (00H - FFH)

A0	$\overline{RD}$ E	$\overline{WR}$ R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	A7	A6	A5	A4	A3	A2	A1	A0

Row non-overlap Period Adjust: (A4 - A0)

A4	A3	A2	A1	A0	Row non-overlap Period
0	0	0	0	0	0 DCLK
0	0	0	0	1	3 DCLKs(POR)
0	0	0	1	0	6 DCLKs
:	:	:	:	:	:
1	1	1	1	0	90 DCLKs
1	1	1	1	1	93 DCLKs

SEG Hiz Period Adjust: (A7 – A5)

A7	A6	A5	Front
0	0	0	0 DCLK (POR)
1	0	0	1DCLK
1	1	1	2 DCLKs

Please see the following figure for Dis-charge/Pre-charge/Row non-overlap/SEG Hiz.

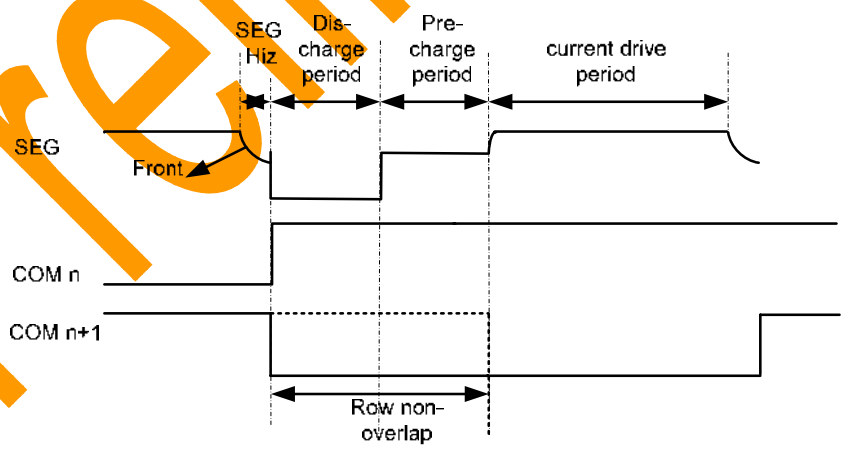


Figure.24

27. Read-Modify-Write: (E0H)

A pair of Read-Modify-Write and End commands must always be used. Once read-modify-write is issued, column address is not incremental by read display data command but incremental by write display data command only. It continues until End command is issued. When the End is issued, column address returns to the address when read-modify-write is issued. This can reduce the microprocessor load when data of a specific display area is repeatedly changed during cursor blinking or others.

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

Cursor display sequence:

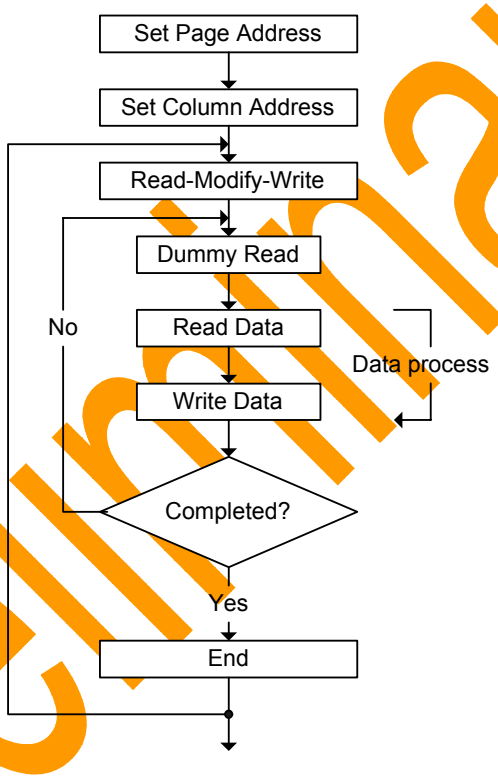


Figure. 25

28. End: (EEH)

Cancels Read-Modify-Write mode and returns column address to the original address (when Read-Modify-Write is issued.)

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

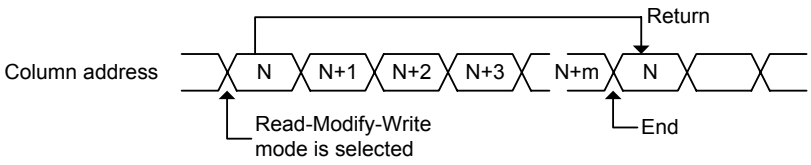


Figure. 26

29. NOP: (E3H)

Non-Operation Command.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

30. Write Display Data

Write 8-bit data in display RAM. As the column address is incremental by 1 automatically after each write, the microprocessor can continue to write data of multiple words.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write RAM data							

31. Read Status

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	-	ON/OFF	ID					

ON/OFF: Indicates whether the display is on or off. When goes low the display turns on. When goes high, the display turns off. This is the opposite of Display ON/OFF command.

ID： These bits contain the information of the chip. The output bits 010101 (it means CH1115).

Note: D/$\overline{C}$ or A0 must be set to low before reading status.

32. Read Display Data

Reads 8-bit data from display RAM area specified by column address and page address. As the column address is increment by 1 automatically after each write, the microprocessor can continue to read data of multiple words. A single dummy read is required immediately after column address being setup. Refer to the display RAM section of FUNCTIONAL DESCRIPTION for details. Note that no display data can be read via the serial interface.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read RAM data							

Note: D/$\overline{C}$ or A0 must be set to high before reading display data.

Command Table

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
1. Set Column Address 4 lower bits	0	1	0	0	0	0	0	Lower column address				Sets 4 lower bits of column address of display RAM in register. (POR = 00H)
2. Set Column Address 4 higher bits	0	1	0	0	0	0	1	Higher column address				Sets 4 higher bits of column address of display RAM in register. (POR = 10H)
3. Set Breathing Light and Blinking	0	1	0	0	0	1	0	0	0	1	1	This command is to control breathing light. (POR = 01H)
	0	1	0	ON/ OFF	*	*	*	A4	A2	A1	A0	
4. Additional Horizontal Scroll Setup Mode Set	0	1	0	0	0	1	0	0	1	0	0	This command consists of 3 consecutive bytes to set up the horizontal scroll parameters. It determined the scrolling start column position(POR=00H) and end column position(POR=7FH).
	0	1	0	*	Start Column Address							
	0	1	0	*	End Column Address							
5. Horizontal Scroll Setup	0	1	0	0	0	1	0	0	1	1	D	This command consists of 4 consecutive bytes to set up the horizontal scroll parameters. It determined scroll mode, scroll start page(POR=00H), time interval(POR=00H) between each scroll step in terms of frame frequency, and end page(POR=07H).
	0	1	0	*	*	*	*	*	Start Page Address			
	0	1	0	0	*	*	*	*	Time Interval			
	0	1	0	0	*	*	*	*	End Page Address			
6. Set Scroll Mode	0	1	0	0	0	1	0	1	1	0	D	This command is to Control continuous or Single screen scroll. (POR=2CH)
7. Set Deactivate / Activate Horizontal Scroll	0	1	0	0	0	1	0	1	1	1	D	Stop(0) or Start(1) motion of horizontal scrolling. (POR=2EH)
8. Set Pump voltage value	0	1	0	0	0	1	1	0	0	Pump voltage value		This command is to control the DC-DC voltage output value and select pump mode. (POR=32H)
9. Set Display Start Line	0	1	0	0	1	Line address						Specifies RAM display line for COM0. (POR = 40H)
10.The Contrast Control Mode Set	0	1	0	1	0	0	0	0	0	0	1	This command is to set Contrast Setting of the display. The chip has 256 contrast steps from 00 to FF. (POR = 80H)
Contrast Data Register Set	0	1	0	Contrast Data								

11. I_{REF} Resistor Set and Adjust I_{SEG} by PAD	0	1	0	1	0	0	0	0	0	1	0	This command is to set internal or external I_{REF} resistor and Adjust I_{SEG} by PAD. (POR=00H)
	0	1	0	ON/ OFF	*	*	*	*	D	A1	A0	
12. Set Segment Re-map (ADC)	0	1	0	1	0	1	0	0	0	0	ADC	The right (0) or left (1) rotation. (POR = A0H)
13. Set SEG pads hardware configuration	0	1	0	1	0	1	0	0	0	1	D	The EVEN left (0) or right (1) rotation. (POR = A2H)
14. Set Entire Display OFF/ON	0	1	0	1	0	1	0	0	1	0	D	Selects normal display (0) or Entire Display ON (1). (POR = A4H)
15. Set Normal/ Reverse Display	0	1	0	1	0	1	0	0	1	1	D	Normal indication (0) when low, but reverse indication (1) when high. (POR = A6H)
16.Multiplex Ration Mode Set	0	1	0	1	0	1	0	1	0	0	0	This command switches default 63 multiplex mode to any multiplex ratio from 1 to 64. (POR = 3FH)
Multiplex Ration Data Set	0	1	0	*	*	Multiplex Ratio						
17. DC-DC Control Mode Set	0	1	0	1	0	1	0	1	1	0	1	This command is to control the DC-DC voltage DC-DC will be turned on when display on converter (1) or DC-DC OFF (0). (POR = 8BH)
DC-DC ON/OFF Mode Set	0	1	0	1	0	0	0	1	0	1	D	
18. Display OFF/ON	0	1	0	1	0	1	0	1	1	1	D	Turns on OLED panel (1) or turns off (0). (POR = AEH)
19. Set Page Address	0	1	0	1	0	1	1	Page Address				Specifies page address to load display RAM data to page address register. (POR = B0H)

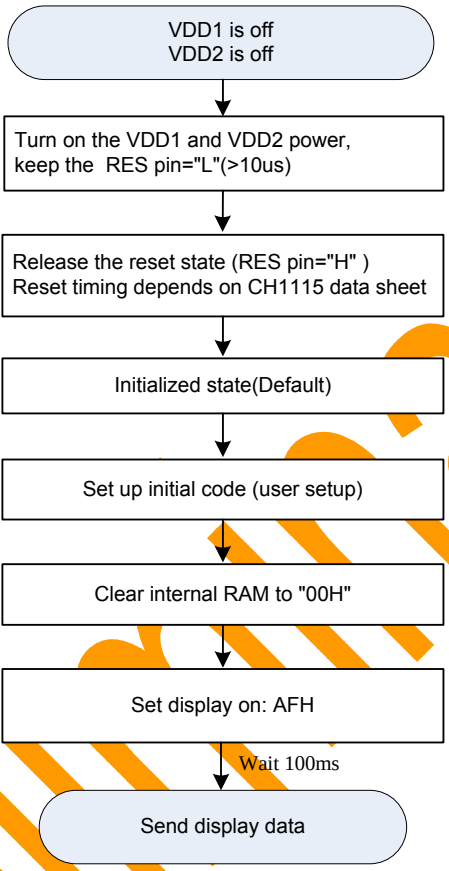
Command Table (Continued)

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
20. Set Common Output Scan Direction	0	1	0	1	1	0	0	D	*	*	*	Scan from COM0 to COM [N - 1] (0) or Scan from COM [N -1] to COM0 (1). (POR = C0H)
21. Display Offset Mode Set	0	1	0	1	1	0	1	0	0	1	1	This is a double byte command which specifies the mapping of display start line to one of COM0-63. (POR = 00H)
Display Offset Data Set	0	1	0	*	*	COMx						
22. Set Display Divide Ratio/Oscillator Frequency Mode Set	0	1	0	1	1	0	1	0	1	0	1	This command is used to set the frequency of the internal display clocks. (POR = 50H)
Divide Ratio/Oscillator Frequency Data Set	0	1	0	Oscillator Frequency				*	*	Divide Ratio		
23. Set Adaptive Power Save	0	1	0	1	1	0	1	0	1	1	D	This command sets Adaptive Power Save ON/OFF (POR = D7H)
24. Dis-charge / Pre-charge Period Mode Set	0	1	0	1	1	0	1	1	0	0	1	This command is used to set the duration of the dis-charge and pre-charge period. (POR = 22H)
Dis-charge /Pre-charge Period Data Set	0	1	0	Dis-charge Period				Pre-charge Period				
25. VCOM Deselect Level Mode Set	0	1	0	1	1	0	1	1	0	1	1	This command is to set the common pad output voltage level at deselect stage. (POR = 35H)
VCOM Deselect Level Data Set	0	1	0	VCOM (β X V_{REF})								
26.Set row non-overlap /SEG Hiz Period	0	1	0	1	1	0	1	1	1	0	0	This command is to set Line overlap/SEG Hiz Period (POR = 01H)
	0	1	0	SEG Hiz Period			Row non-overlap Period					
27. Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Read-Modify-Write start.
28. End	0	1	0	1	1	1	0	1	1	1	0	Read-Modify-Write end.
29. NOP	0	1	0	1	1	1	0	0	0	1	1	Non-Operation Command
30. Write Display Data	1	1	0	Write RAM data								
31. Read Status	0	0	1	BUSY	ON/ OFF	*	*	*	0	0	0	
32. Read Display Data	1	0	1	Read RAM data								

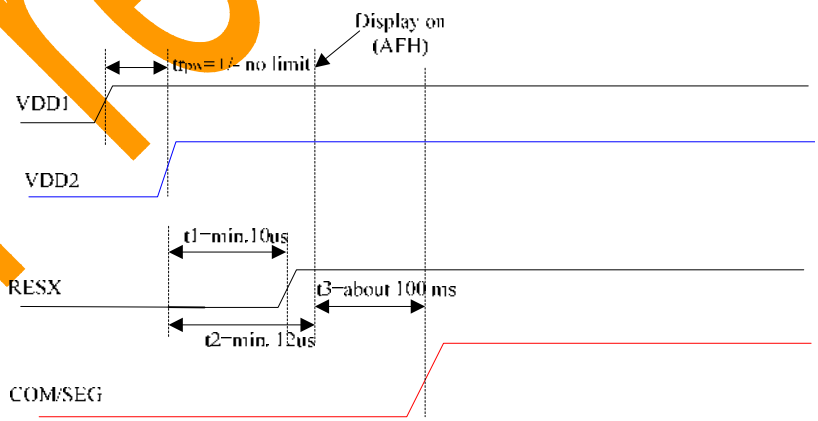
Note: Do not use any other command, or the system malfunction may result.

1. Power On and Initialization

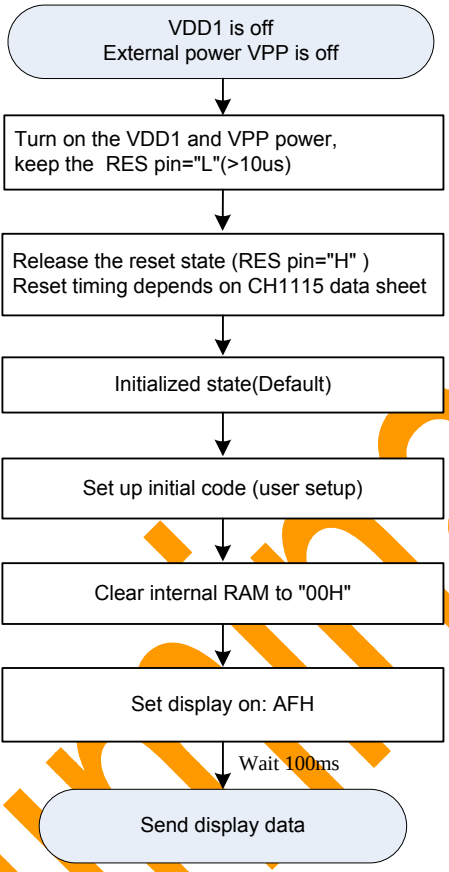
1.1. Built-in DC-DC pump power is being used immediately after turning on the power:



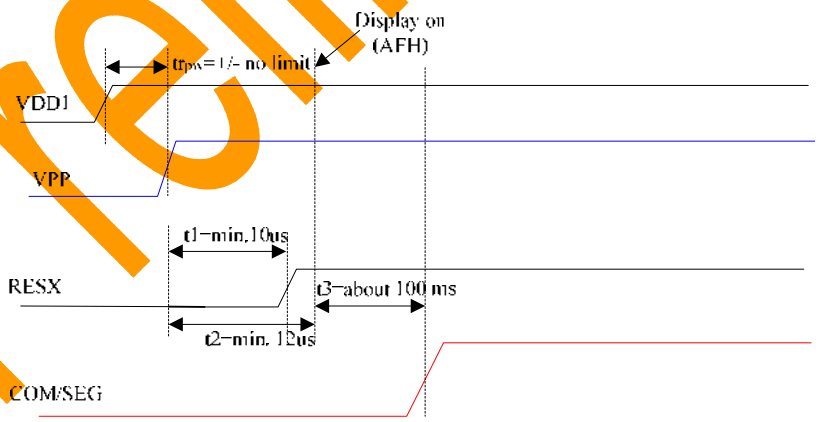
Power on sequence：



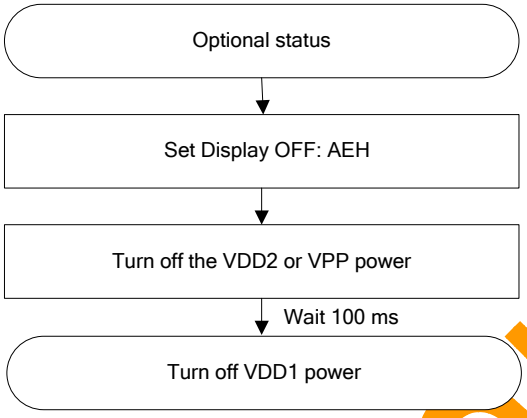
1.2. External power is being used immediately after turning on the power:



Power on sequence:



1.3. Power Off



Power off sequence：

Absolute Maximum Rating*

DC Supply Voltage (V_{DD1}) . . . . . -0.3V to +3.6V

DC Supply Voltage (V_{DD2}) . . . . . -0.3V to +4.8V

DC Supply Voltage (V_{PP}) . . . . . -0.3V to +14.5V

Input Voltage . . . . . -0.3V to V_{DD1} + 0.3V

Operating Ambient Temperature . . . . . -40°C to +85°C

Storage Temperature . . . . . -55°C to +125°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

DC Characteristics (Vss = 0V, V_{DD1} = 1.65 - 3.5V T_A =+25°C, unless otherwise specified)

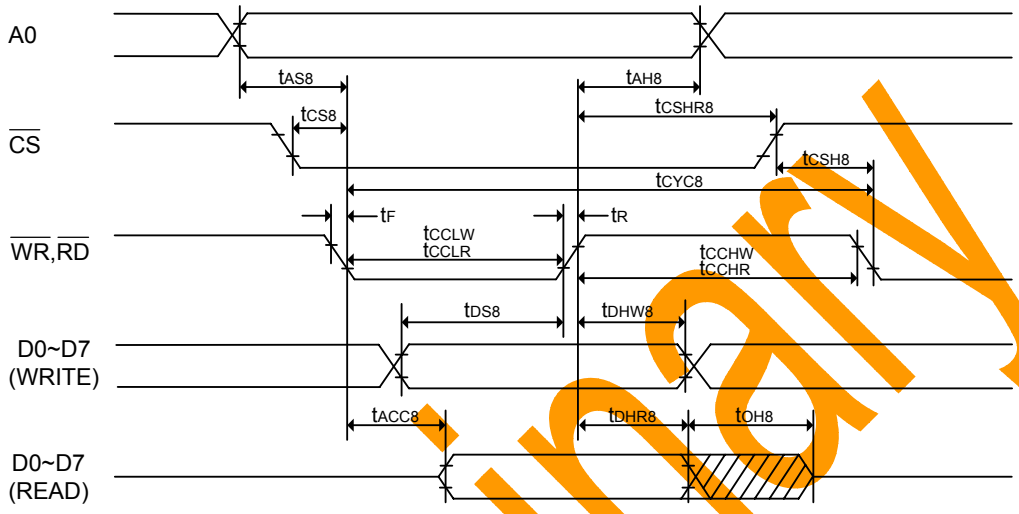
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{DD1}	Operating voltage	1.65	-	3.5	V	
V_{DD2}	Operating voltage	2.5	-	4.7	V	
V_{PP} (External)	OLED Operating voltage	6.4		14.0	V	
Vpp (Internal)	Charge Pump Output Voltage	7.0	7.4	-	V	VDD2=2.9V~4.7V,7.4V Mode, Maximum output loading =12mA (I_{REF} = -18.75μA, Contrast α = 256)
		7.6	8.0	-	V	VDD2=3.5V~4.7V,8.0V Mode, Maximum output loading =18mA (I_{REF} = -18.75μA, Contrast α = 256)
		8.5	9.0	-	V	VDD2=3.7V~4.7V,9.0V Mode, Maximum output loading =18mA (I_{REF} = -18.75μA, Contrast α = 256)
		9.5	10.0	-	V	VDD2=4.2V~4.7V,10.0V Mode, Maximum output loading =18mA (I_{REF} = -18.75μA, Contrast α = 256)
I_{DD1}	Dynamic current consumption 1	-	-	600	μA	V_{DD1} = 3V, V_{DD2} = 3.7V, I_{REF} = -18.75μA, Contrast α = 256, Internal charge pump OFF, Display ON, display data = All ON, No panel attached.
I_{DD2}	Dynamic current consumption 2	-	-	3.5	mA	V_{DD1} = 3V, V_{DD2} =3.7V, I_{REF} = -18.75μA, Contrast α = 256, internal charge pump ON, Display ON, Display data = All ON, No panel attached.
I_{PP}	OLED dynamic current consumption	-	-	1.5	mA	V_{DD1} = 3V, V_{DD2} = 3.7V, V_{PP} =9V(external), I_{REF} = -18.75μA, Contrast α = 256, Display ON, display data = All ON, No panel attached. Connect charge pump capacitor
I_{SP}	Sleep mode current consumption in V_{DD1} & V_{DD2}	-	-	5	μA	During sleep, T_A = +25°C, V_{DD1} = 3.0V, V_{DD2} = 3.0V.
	Sleep mode current consumption in V_{PP}	-	-	5	μA	During sleep, T_A = +25°C, V_{PP} = 9V (External)
I_{SEG}	Segment output current	-	-300	-	μA	V_{DD1} = 3V, V_{PP} = 9V, I_{REF} = -18.75μA, R_{LOAD} = 20kΩ, Display ON. Contrast α = 256.
		-	-37.5	-	μA	V_{DD1} = 3V, V_{PP} = 9V, I_{REF} = -18.75μA, R_{LOAD} = 20kΩ, Display ON. Contrast α = 32.
ΔI_{SEG1}	Segment output current uniformity	-	-	±3	%	ΔI_{SEG1} = (I_{SEG} - I_{MID})/I_{MID} X 100% I_{MID} = (I_{MAX} + I_{MIN})/2 I_{SEG} [0:127] at contrast α = 256.
ΔI_{SEG2}	Adjacent segment output current uniformity	-	-	±2	%	ΔI_{SEG2} = (I_{SEG}[N] - I_{SEG}[N+1])/(I_{SEG}[N] + I_{SEG}[N+1]) X 100% I_{SEG} [0:127] at contrast α = 256.

DC Characteristics (Continued)

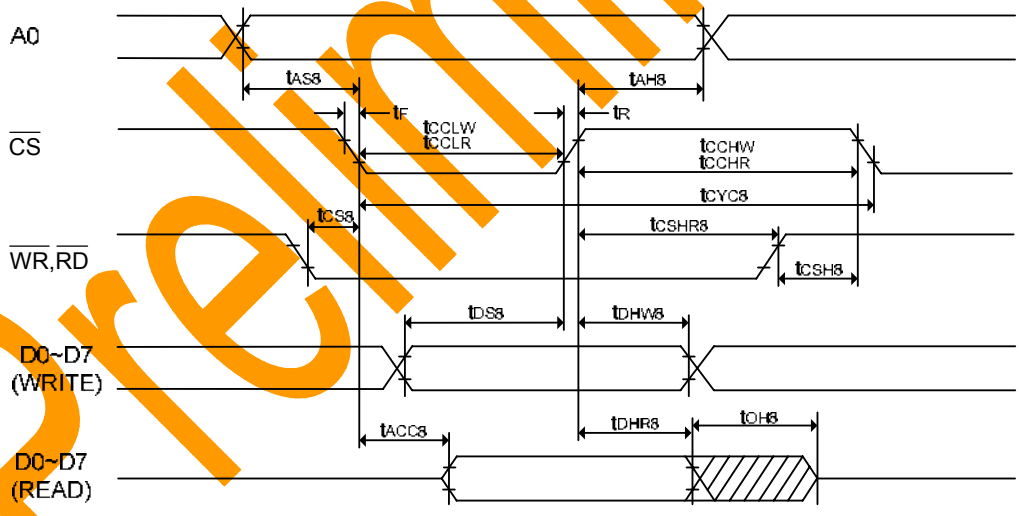
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IHC}	High-level input voltage	0.8 X V_{DD1}	-	V_{DD1}	V	A0, D0 - D7, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS}$, CLS, CL, IM0~2 and $\overline{RES}$.
V_{ILC}	Low-level input voltage	V_{SS}	-	0.2 X V_{DD1}	V	
V_{OHC}	High-level output voltage	0.8 X V_{DD1}	-	V_{DD1}	V	I_{OH} = -0.5mA (D0 - D7, and CL).
V_{OLC}	Low -level output voltage	V_{SS}	-	0.2 X V_{DD1}	V	I_{OL} = 0.5mA (D0, D2 - D7, and CL)
V_{OLCS}	SDA low -level output voltage	V_{SS}	-	0.2 X V_{DD1}	V	VDD1<2V; I_{OL}=3mA (SDA)
				0.4		VDD1>2V
I_{LI}	Input leakage current	-1.0	-	1.0	μA	V_{IN} = V_{DD1} or V_{SS} (A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS}$, CLS, IM0~2 and $\overline{RES}$).
I_{Hz}	Hz leakage current	-1.0	-	1.0	μA	When the D0 - D7, and CL are in high impedance.
f_{OSC}	Oscillation frequency	-	8	-	MHz	T_A = +25°C.
f_{FRM}	Frame frequency for 64 Commons	-	96	-	Hz	When fosc = 8MHz, Divide ratio = 8, common width = 162 DCLKs.
R_{ON1}	Common switch resistance	-	16	-	Ω	Vpp=9V,Vcom= GND +0.4V
R_{ON2}	Common switch resistance	-	500	-	Ω	Vpp=9V,VCOM=0.770×Vpp-0.4V

AC Characteristics

(1) System buses Read/Write characteristics 1 (For the 8080 Series Interface MPU)



8080-series parallel interface cycle (Form1)



8080-series parallel interface cycle (Form2)

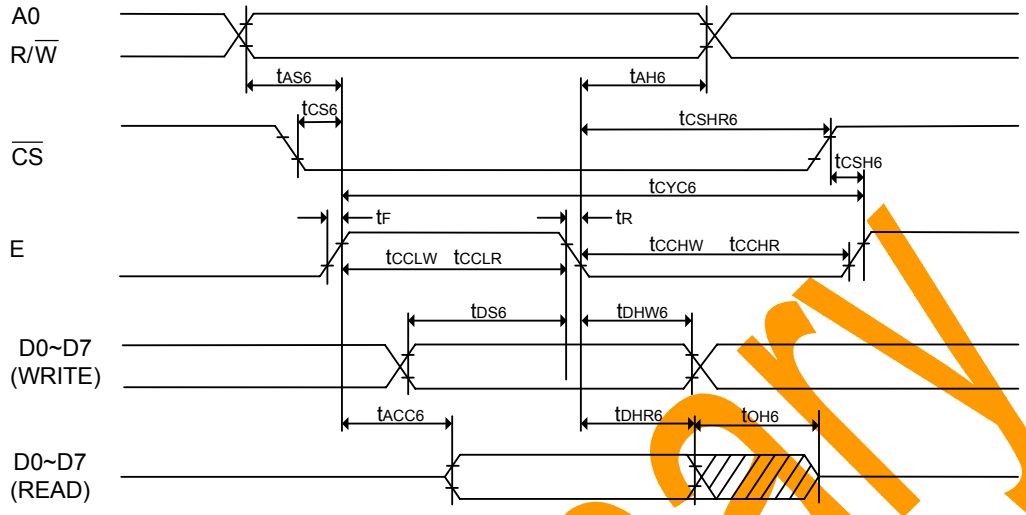
(VDD1 = 1.65 - 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYC8}	System cycle time	600	-	-	ns	
t_{AS8}	Address setup time	0	-	-	ns	
t_{AH8}	Address hold time	0	-	-	ns	
t_{DS8}	Data setup time	80	-	-	ns	
t_{DHW8}	Write Data hold time	20	-	-	ns	
t_{DHR8}	Read Data hold time	20	-	-	ns	
T_{OH8}	Output disable time	-	-	140	ns	C_L = 100pF
t_{ACC8}	$\overline{RD}$ access time	-	-	280	ns	C_L = 100pF
t_{CCLW}	Control L pulse width (WR)	300	-	-	ns	
t_{CCLR}	Control L pulse width (RD)	300	-	-	ns	
t_{CCHW}	Control H pulse width (WR)	300	-	-	ns	
t_{CCHR}	Control H pulse width (RD)	300	-	-	ns	
t_R	Rise time	-	-	30	ns	
t_F	Fall time	-	-	30	ns	
t_{CS8}	Chip select setup time	0	-	-	ns	
t_{CSH8}	Chip select hold time	40	-	-	ns	
t_{CSHR8}	Chip select hold time to read signal	40	-	-	ns	

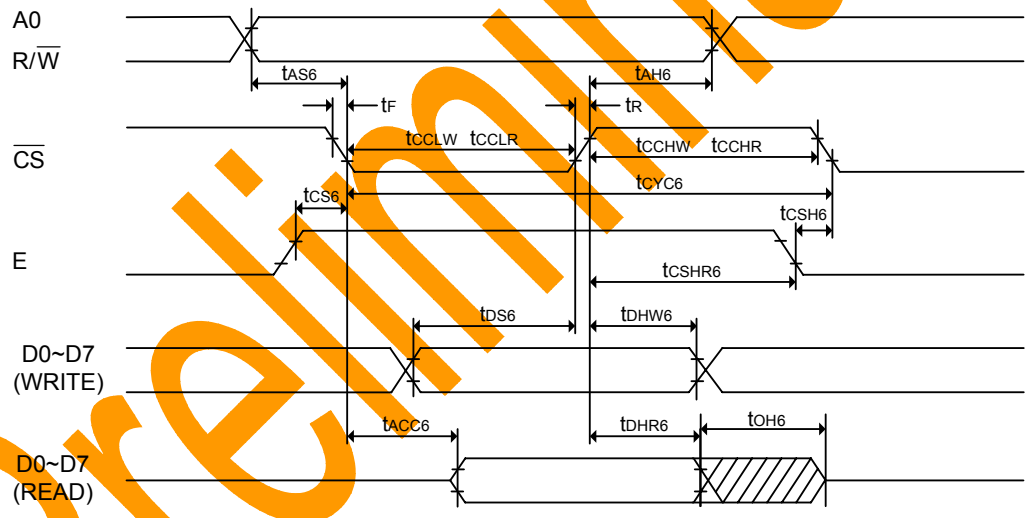
(V_{DD1} = 2.4 - 3.5V, T_A = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYC8}	System cycle time	300	-	-	ns	
t_{AS8}	Address setup time	0	-	-	ns	
t_{AH8}	Address hold time	0	-	-	ns	
t_{DS8}	Data setup time	40	-	-	ns	
t_{DHW8}	Write Data hold time	10	-	-	ns	
t_{DHR8}	Read Data hold time	10	-	-	ns	
t_{OH8}	Output disable time	-	-	70	ns	C_L = 100pF
t_{ACC8}	$\overline{RD}$ access time	-	-	140	ns	C_L = 100pF
t_{CCLW}	Control L pulse width (WR)	150	-	-	ns	
t_{CCLR}	Control L pulse width (RD)	150	-	-	ns	
t_{CCHW}	Control H pulse width (WR)	150	-	-	ns	
t_{CCHR}	Control H pulse width (RD)	150	-	-	ns	
t_R	Rise time	-	-	15	ns	
t_F	Fall time	-	-	15	ns	
t_{CS8}	Chip select setup time	0	-	-	ns	
t_{CSH8}	Chip select hold time	20	-	-	ns	
t_{CSHR8}	Chip select hold time to read signal	20	-	-	ns	

(2) System buses Read/Write Characteristics 2 (For the 6800 Series Interface MPU)



6800-series parallel interface cycle (Form1)



6800-series parallel interface cycle (Form2)

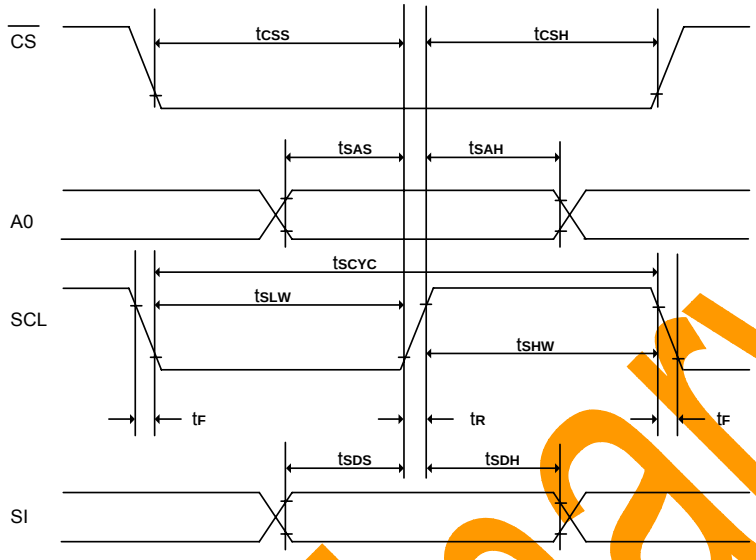
(V_{DD1} = 1.65 - 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYC6}	System cycle time	600	-	-	ns	
t_{AS6}	Address setup time	0	-	-	ns	
t_{AH6}	Address hold time	0	-	-	ns	
t_{DS6}	Data setup time	80	-	-	ns	
t_{DHW6}	Write Data hold time	20	-	-	ns	
t_{DHR6}	Read Data hold time	20	-	-	ns	
t_{OH6}	Output disable time	-	-	140	ns	C_L = 100pF
t_{ACC6}	Access time	-	-	280	ns	C_L = 100pF
t_{EWHW}	Enable H pulse width (Write)	300	-	-	ns	
t_{EWHR}	Enable H pulse width (Read)	300	-	-	ns	
t_{EWLW}	Enable L pulse width (Write)	300	-	-	ns	
t_{EWLR}	Enable L pulse width (Read)	300	-	-	ns	
t_R	Rise time	-	-	30	ns	
t_F	Fall time	-	-	30	ns	
t_{CS6}	Chip select setup time	0	-	-	ns	
t_{CSH6}	Chip select hold time	40	-	-	ns	
t_{CSHR6}	Chip select hold time to read signal	40	-	-	ns	

(V_{DD1} = 2.4 - 3.5V, T_A = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYC6}	System cycle time	300	-	-	ns	
t_{AS6}	Address setup time	0	-	-	ns	
t_{AH6}	Address hold time	0	-	-	ns	
t_{DS6}	Data setup time	40	-	-	ns	
t_{DHW6}	Write Data hold time	10	-	-	ns	
t_{DHR6}	Read Data hold time	10	-	-	ns	
t_{OH6}	Output disable time	-	-	70	ns	C_L = 100pF
t_{ACC6}	Access time	-	-	140	ns	C_L = 100pF
t_{EWHW}	Enable H pulse width (Write)	150	-	-	ns	
t_{EWHR}	Enable H pulse width (Read)	150	-	-	ns	
t_{EWLW}	Enable L pulse width (Write)	150	-	-	ns	
t_{EWLR}	Enable L pulse width (Read)	150	-	-	ns	
t_R	Rise time	-	-	15	ns	
t_F	Fall time	-	-	15	ns	
t_{CS6}	Chip select setup time	0	-	-	ns	
t_{CSH6}	Chip select hold time	20	-	-	ns	
t_{CSHR6}	Chip select hold time to read signal	20	-	-	ns	

(3) System buses Write characteristics 3 (For 4 wire SPI)



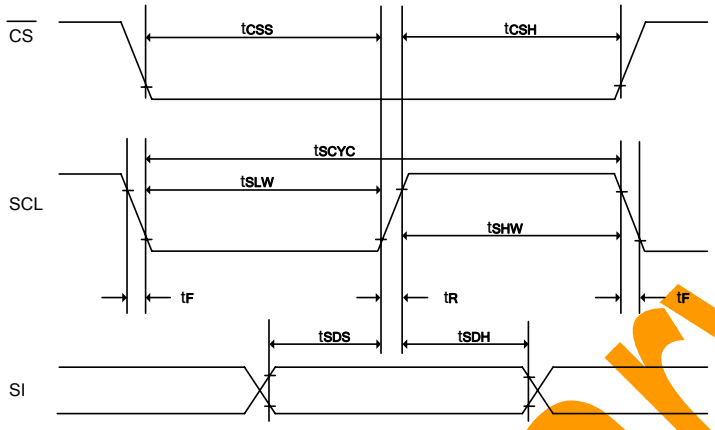
(V_{DD1} = 1.65 - 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tSCYC	Serial clock cycle	100	-	-	ns	
tSAS	Address setup time	60	-	-	ns	
tSAH	Address hold time	60	-	-	ns	
tSDS	Data setup time	40	-	-	ns	
tSDH	Data hold time	40	-	-	ns	
tCSS	$\overline{CS}$ setup time	90	-	-	ns	
tCSH	$\overline{CS}$ hold time time	24	-	-	ns	
tSHW	Serial clock H pulse width	40	-	-	ns	
tSLW	Serial clock L pulse width	40	-	-	ns	
tR	Rise time	-	-	6	ns	
tF	Fall time	-	-	6	ns	

(V_{DD1} = 2.4 - 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tSCYC	Serial clock cycle	50	-	-	ns	
tSAS	Address setup time	30	-	-	ns	
tSAH	Address hold time	30	-	-	ns	
tSDS	Data setup time	20	-	-	ns	
tSDH	Data hold time	20	-	-	ns	
tCSS	$\overline{CS}$ setup time	45	-	-	ns	
tCSH	$\overline{CS}$ hold time time	12	-	-	ns	
tSHW	Serial clock H pulse width	20	-	-	ns	
tSLW	Serial clock L pulse width	20	-	-	ns	
tR	Rise time	-	-	3	ns	
tF	Fall time	-	-	3	ns	

(4) System buses Write characteristics 4(For 3 wire SPI)



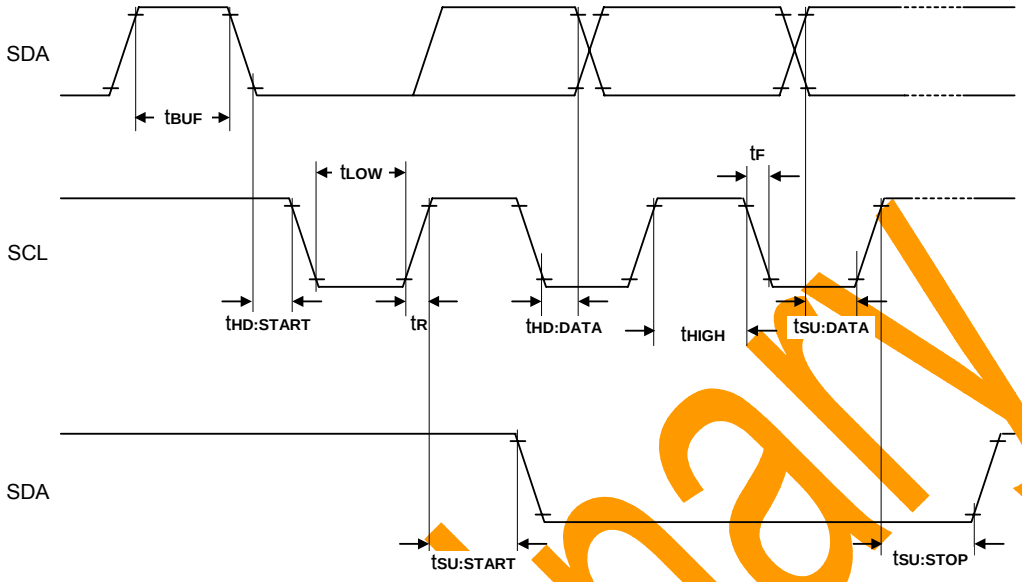
(V_{DD1} = 1.65 - 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tSCYC	Serial clock cycle	100	-	-	ns	
tSDS	Data setup time	40	-	-	ns	
tSDH	Data hold time	40	-	-	ns	
tCSS	$\overline{CS}$ setup time	90	-	-	ns	
tCSH	$\overline{CS}$ hold time time	24	-	-	ns	
tSHW	Serial clock H pulse width	40	-	-	ns	
tSLW	Serial clock L pulse width	40	-	-	ns	
tR	Rise time	-	-	6	ns	
tF	Fall time	-	-	6	ns	

(V_{DD1} = 2.4 - 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tSCYC	Serial clock cycle	50	-	-	ns	
tSDS	Data setup time	20	-	-	ns	
tSDH	Data hold time	20	-	-	ns	
tCSS	$\overline{CS}$ setup time	45	-	-	ns	
tCSH	$\overline{CS}$ hold time time	12	-	-	ns	
tSHW	Serial clock H pulse width	20	-	-	ns	
tSLW	Serial clock L pulse width	20	-	-	ns	
tR	Rise time	-	-	3	ns	
tF	Fall time	-	-	3	ns	

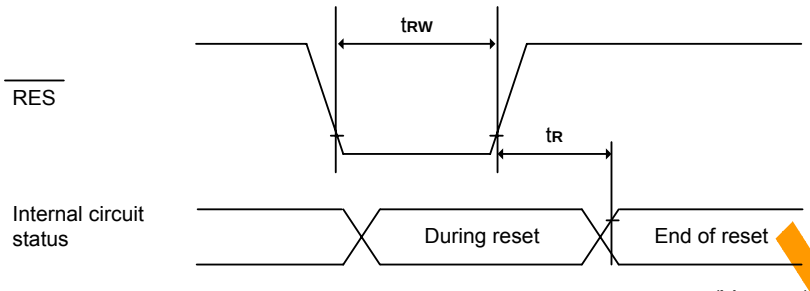
(5) I²C interface characteristics



(V_{DD1} = 1.65 - 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
f_{SCL}	SCL clock frequency	DC	-	400	kHz	
T_{LOW}	SCL clock Low pulse width	1.3	-	-	uS	
T_{HIGH}	SCL clock H pulse width	0.6	-	-	uS	
$T_{SU:DATA}$	data setup time	100	-	-	nS	
$T_{HD:DATA}$	data hold time	0	-	0.9	uS	
T_R	SCL，SDA rise time	20+0.1Cb	-	300	nS	
T_F	SCL，SDA fall time	20+0.1Cb	-	300	nS	
Cb	Capacity load on each bus line	-	-	400	pF	
$T_{SU:START}$	Setup timefor re-START	0.6	-	-	uS	
$T_{HD:START}$	START Hold time	0.6	-	-	uS	
$T_{SU:STOP}$	Setup time for STOP	0.6	-	-	uS	
T_{BUF}	Bus free times between STOP and START condition	1.3	-	-	uS	

(6) Reset Timing



(V_{DD1} = 1.65 - 3.5V, T_A = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_R	Reset time	-	-	2.0	µs	
t_{RW}	Reset low pulse width	20.0	-	-	µs	

(V_{DD1} = 2.4 - 3.5V, T_A = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_R	Reset time	-	-	1.0	µs	
t_{RW}	Reset low pulse width	10.0	-	-	µs	

Application Circuit (for reference only)

Reference Connection to MPU:

1. 8080 series interface: (Internal oscillator, Built-in DC-DC)

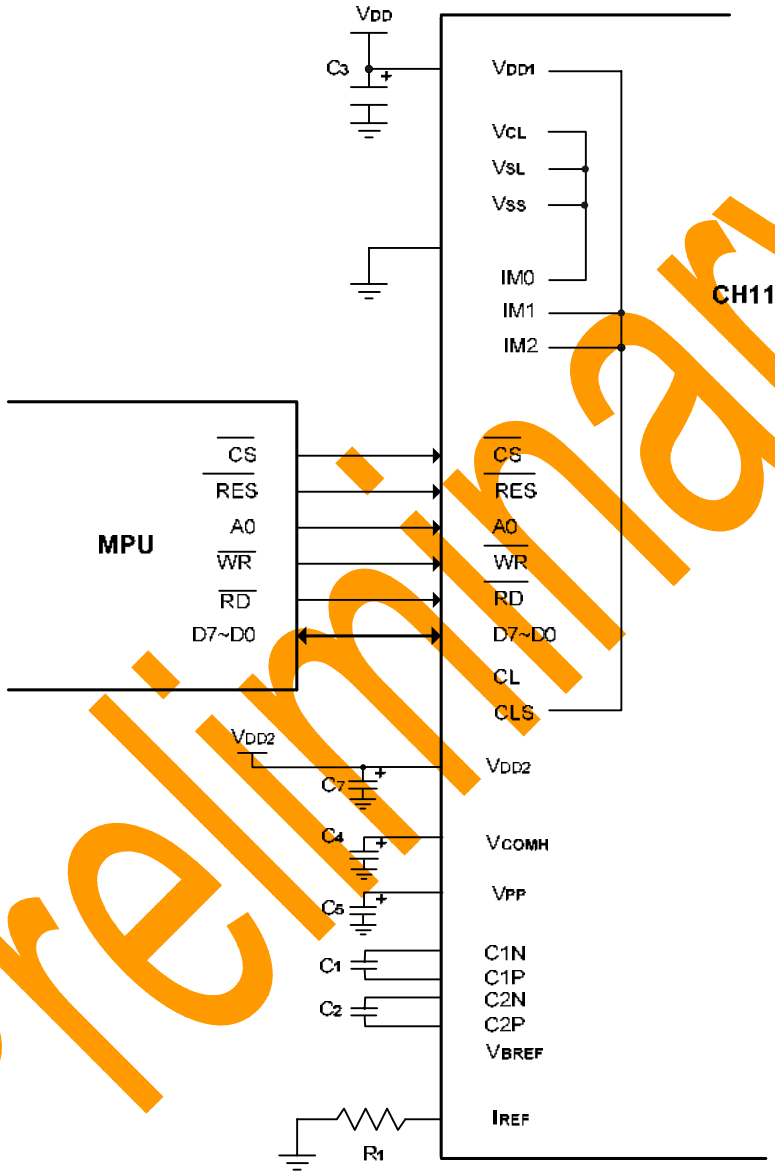


Figure. 27

Note:

C3 - C5 ,C7: 4.7μF. C1, C2 : 0.22μF.
R1: about 310kΩ（ISEG=300uA）, R1 = (Voltage at IREF - Vss)/IREF

2. 6800 Series Interface: (Internal oscillator, Built-in DC-DC)

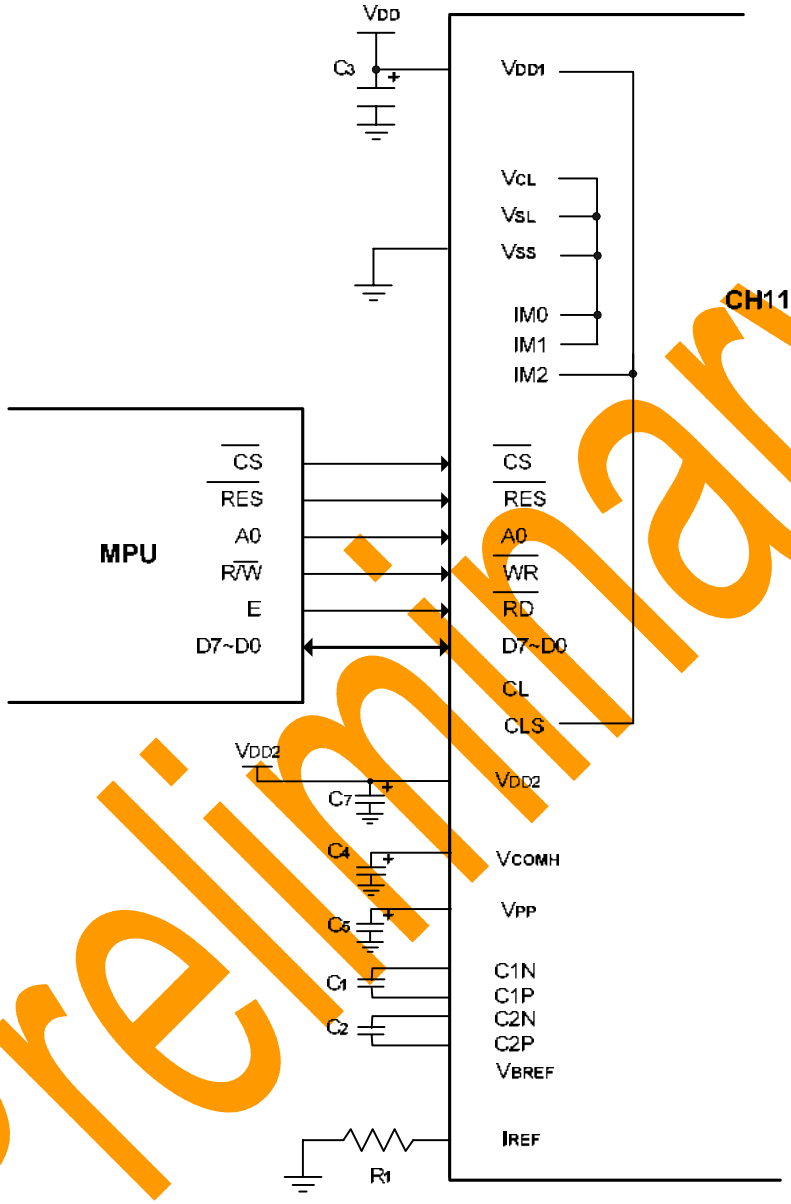


Figure. 28

Note:
C3 - C5, C7: 4.7μF. C1, C2 : 0.22μF
R1: about 310kΩ（ISEG=300uA）, R1 = (Voltage at IREF - Vss)/IREF

3. Serial Interface(3-wire or 4-wire SPI): (Internal oscillator, External V_{PP} , Max 14.0V)

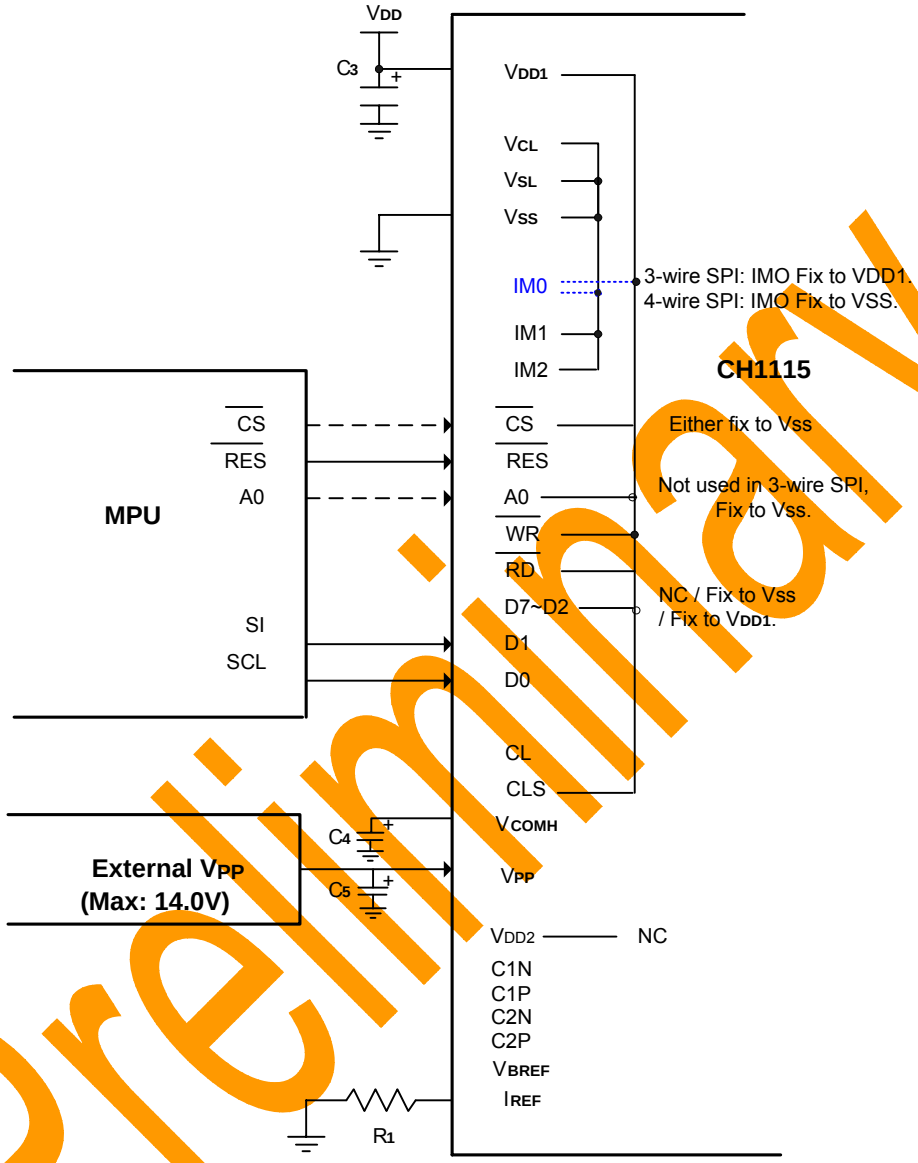


Figure. 29

Note:

C_3 - C_5: 4.7μF

R_1: about 310kΩ（ISEG=300uA）, R_1 = (Voltage at I_{REF} - V_{SS})/I_{REF}

$\overline{WR}$ and $\overline{RD}$ are not used in SPI mode, should fix to VSS or VDD1.

$\overline{CS}$ can fix to VSS in SPI mode.

4. **I²C Interface: (Internal oscillator, Built-in DC-DC)**

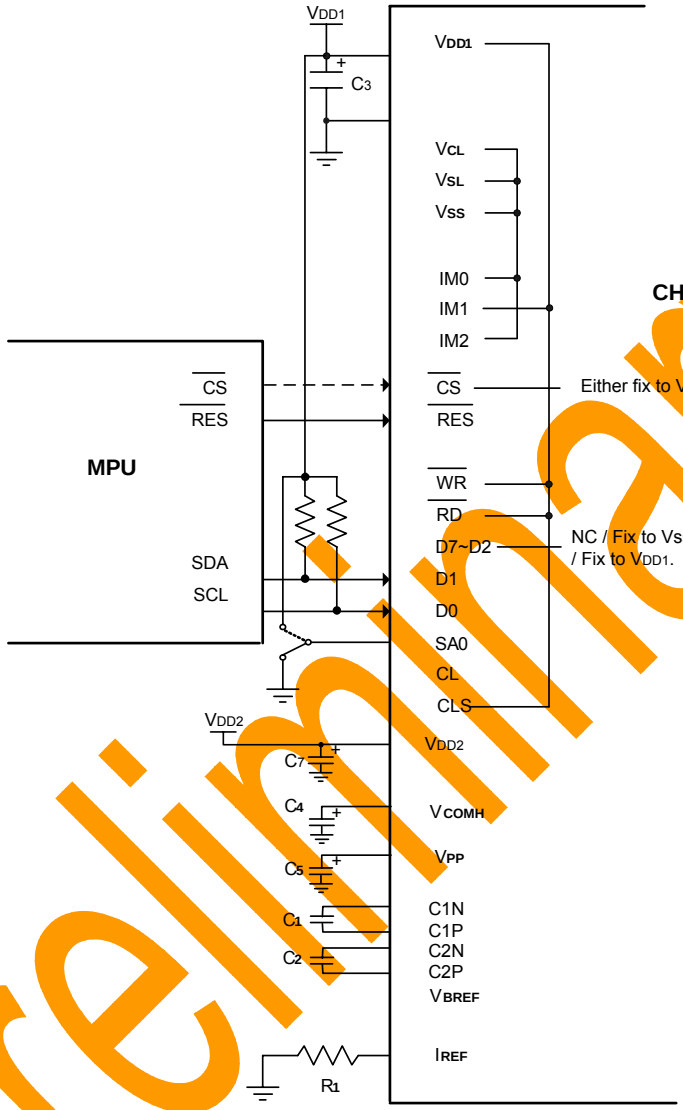


Figure. 30

Note:

C_3 - C_5, C_7: 4.7μF. C_1, C_2: 0.22μF.

R_1: about 310kΩ（ISEG=300uA）, R_1 = (Voltage at I_{REF} - V_{SS})/I_{REF}

The least significant bit of the slave address is set by connecting the input SA0 to either logic 0(VSS) or 1 (VDD1).

$\overline{WR}$ and $\overline{RD}$ are not used in I²C mode, should fix to VSS or VDD1.

$\overline{CS}$ can fix to VSS in I²C mode.

The positive supply of pull-up resistor must equal to the value of V_{DD1}.

Ordering Information

Part No.	Package
CH1115G	Gold bump on chip tray

SPEC Revision History

Version	Content	Date
0.0	Original	Nov.2016
0.1	Page 28: Add single column scroll Page 31: Modify IREF Resistor & IREF Table Page 36: Modify Oscillator Frequency of f_{OSC} Page 39: Modify Adaptive Power Save POR value Page 40: Add VCOMH external Page 41: Row non-overlap default 3 Dclks Page 50: Modify V_{DD2} voltage range Page 50: Modify Charge Pump Output Voltage Page 51: Add RON1 and RON2 dc character Page 51: Modify f_{OSC} and f_{FRM} (Page 50)	Aug.2017