



# **ORIENT DISPLAY**

**MAKE THINGS POSSIBLE**

## Specification for LCD Module

### AMC1602IR-B-Y6WFDY-STL

Revision A0



AM	Orient Display
C	Character Type
1602	16 Characters x 02 Lines
I	Serial I, Module Dimension 85.0 x 30.0 x 14.0 (MAX)
R	RoHS Compliant
B	COB Type
Y	STN Positive Yellow Green Dark Character on Yellow Green Background
6	6 o'clock Viewing Direction
W	Top: -20~+70°C; Tstr: -30~+80°C
F	Transflective
D	LED Backlight
Y	Yellow Green Backlight
/	Controller <a href="#">ST7066U-0A</a> Or Compatible
/	Parallel Interface



DOCUMENT REVISION HISTORY:

DATE	PAGE	DESCRIPTION
2023.10.	-	First release

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# **1. Precautions in use of LCD Modules**

- (1) Avoid applying excessive shocks to the module or making any alterations or modifications to it.
- (2) Don't make extra holes on the printed circuit board, modify its shape or change the components of LCD module.
- (3) Don't disassemble the LCM.
- (4) Don't operate it above the absolute maximum rating.
- (5) Don't drop, bend or twist LCM.
- (6) Soldering: only to the I/O terminals.
- (7) Storage: please storage in anti-static electricity container and clean environment.

# **2. General Specification**

<b>Item</b>	<b>Dimension</b>	<b>Unit</b>
Number of Characters	16 characters x 2 Lines	—
Module dimension(With LED Backlight )	85.0 x 30.0 x 14.0 (MAX)	mm
View area	64.5x15.5	mm
Active area	56.20x11.50	mm
Dot size	0.55x 0.65	mm
Dot pitch	0.60 x 0.70	mm
Character size	2.95 x 5.55	mm
Character pitch	3.55 x 5.95	mm
LCD type	STN, Yellow-Green, Transflective	
Duty	1/16	
View direction	6 o'clock	
Backlight Type	Yellow-Green LED Backlight	

### **3. Absolute Maximum Ratings**

Item		Symbol	Min	Max	Unit
Input Voltage		$V_I$	-0.3	$V_{DD}+0.3$	V
Supply Voltage For Logic		$V_{DD}-V_{SS}$	-0.3	7.0	V
Supply Voltage For LCD		$V_{DD}-V_0$	$V_{dd}-10.0$	0	V
Wide Temperature LCM	Operating Temp.	$T_{op}$	-20	70	°C
	Storage Temp.	$T_{str}$	-30	80	°C

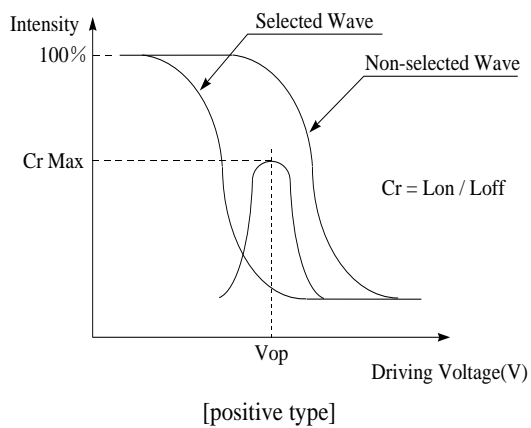
### **4. Electrical Characteristics**

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	$V_{DD}-V_{SS}$	—	4.5	5.0	5.5	V
Supply Voltage For LCD	$V_{DD}-V_0$	$T_a=25^{\circ}\text{C}$	3.6	4.1	4.6	V
Input High Volt.	$V_{IH}$	—	$0.7 V_{DD}$	—	$V_{DD}$	V
Input Low Volt.	$V_{IL}$	—	-0.3	—	0.6	V
Supply Current	$I_{DD}$	$V_{DD}=5\text{V}$	0.8	1.2	1.5	mA
Supply Voltage of Yellow-green backlight	$V_{LED}$	Forward current =120 mA Number of LED die 2x12= 24	3.9	4.1	4.3	V

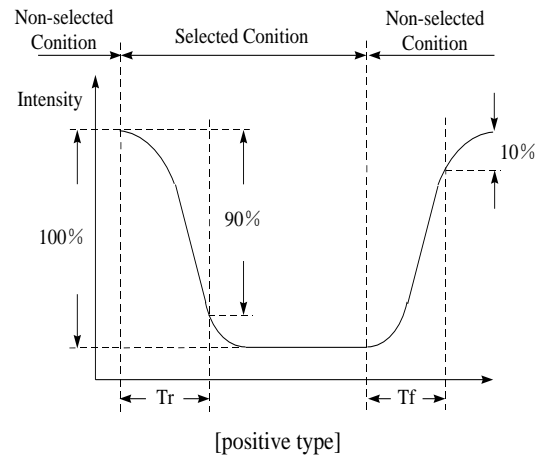
# 5. Optical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
View Angle	(V) $\theta$	$CR \geq 2$	-20	—	35	deg
	(H) $\phi$	$CR \geq 2$	-30	—	30	deg
Contrast Ratio	CR	—	—	3	—	—
Response Time	T rise	—	—	—	250	ms
	T fall	—	—	—	250	ms

## Definition of Operation Voltage (Vop)



## Definition of Response Time (Tr, Tf)



### Conditions :

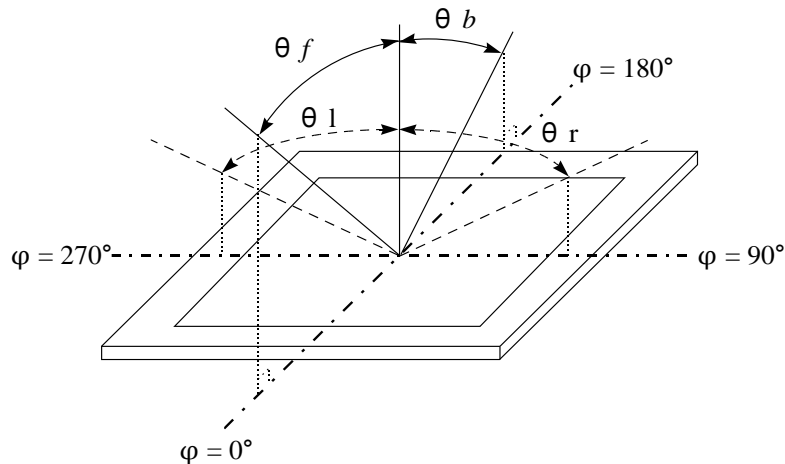
Operating Voltage : Vop

Viewing Angle( $\theta$  ,  $\phi$ ) :  $0^\circ$  ,  $0^\circ$

Frame Frequency : 64 HZ

Driving Waveform : 1/N duty , 1/a bias

### Definition of viewing angle( $CR \geq 2$ )

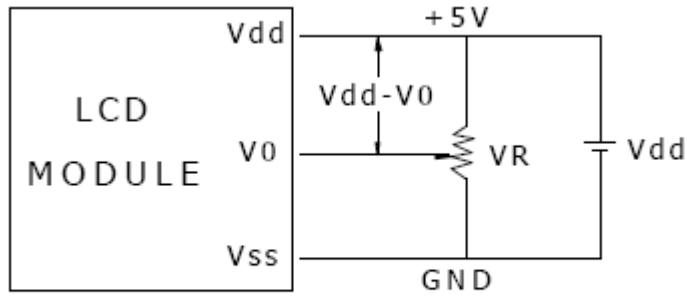


## **6. Interface Pin Function**

<b>Pin No.</b>	<b>Symbol</b>	<b>Level</b>	<b>Description</b>
1	DB0	H/L	Data bit 0
2	DB1	H/L	Data bit 1
3	DB2	H/L	Data bit 2
4	DB3	H/L	Data bit 3
5	DB4	H/L	Data bit 4
6	DB5	H/L	Data bit 5
7	DB6	H/L	Data bit 6
8	DB7	H/L	Data bit 7
9	E	H,H→L	Chip enable signal
10	R/W	H/L	H: Read(MPU→Module) L: Write(MPU→Module)
11	RS	H/L	H: DATA, L: Instruction code
12	V0	(Variable)	Operating voltage for LCD
13	V <sub>SS</sub>	0V	Ground
14	V <sub>DD</sub>	5.0V	Supply Voltage for logic
15	LED(+)		Anode of LED Backlight
16	LED(-)		Cathode of LED Backlight

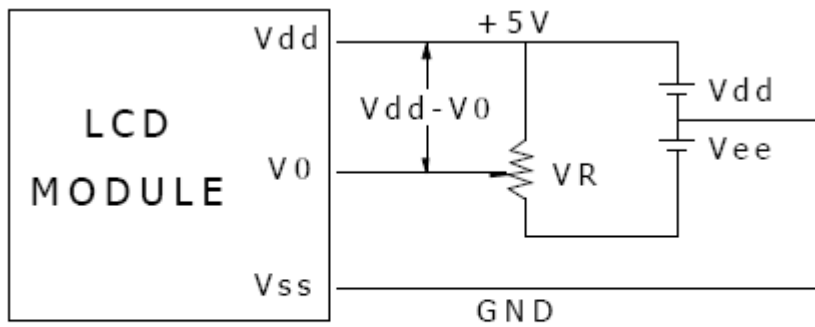
## **7. POWER SUPPLY**

### **SINGLE SUPPLY VOLTAGE TYPE**



Vdd-V0: LCD Driving Voltage  
VR: 10K - 20K

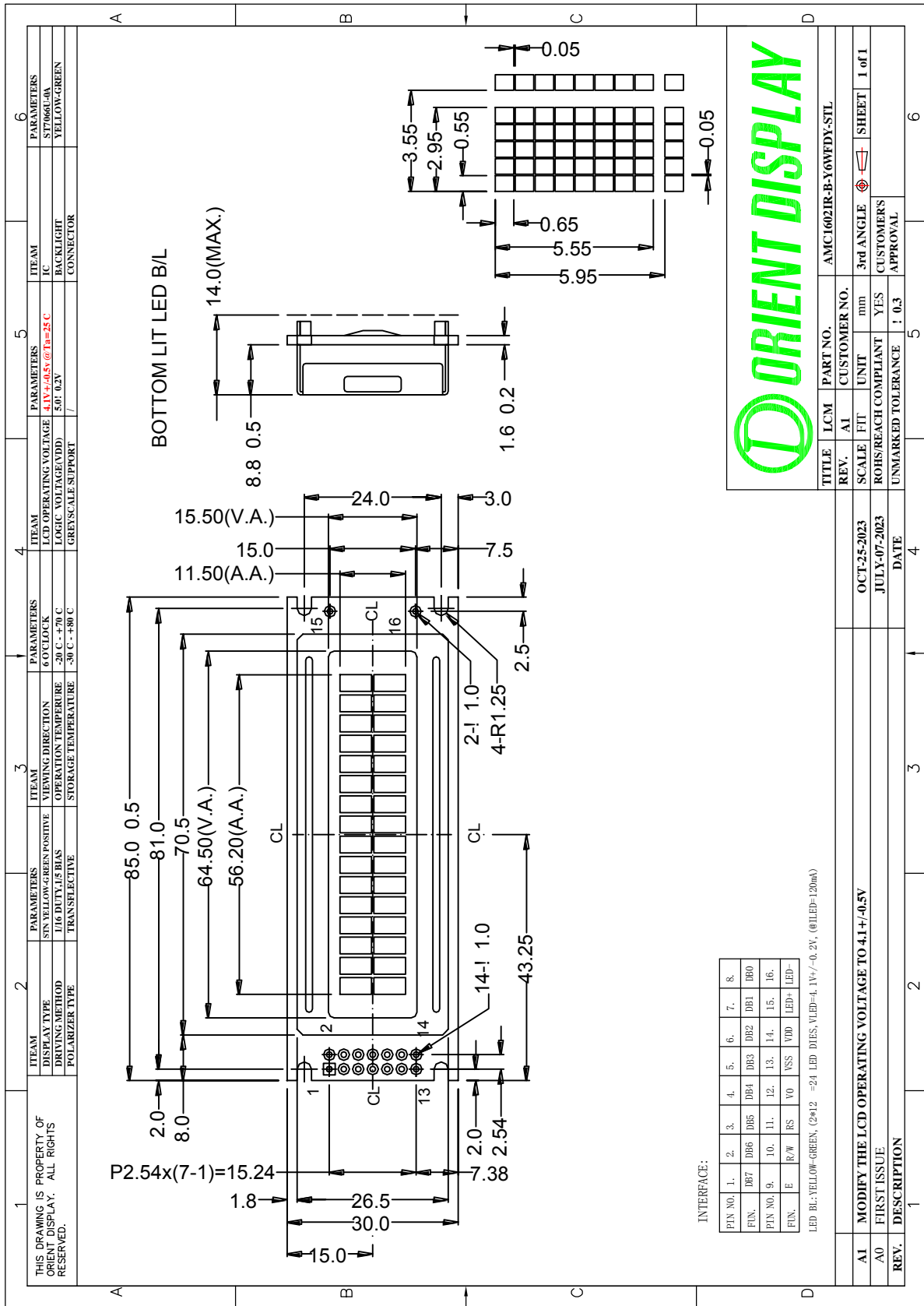
### **DUAL SUPPLY VOLTAGE TYPE**



Vdd-V0: LCD Driving Voltage  
VR: 10K - 20K



# 8. Contour Drawing & Block Diagram



## 9. Function Description

The LCD display Module is built in a LSI controller, the controller has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as display clear and cursor shift, and address information for display data RAM (DDRAM) and character generator (CGRAM). The IR can only be written from the MPU. The DR temporarily stores data to be written or read from DDRAM or CGRAM. When address information is written into the IR, then data is stored into the DR from DDRAM or CGRAM. By the register selector (RS) signal, these two registers can be selected.

RS	R/W	Operation
0	0	IR write as an internal operation (display clear, etc.)
0	1	Read busy flag (DB7) and address counter (DB0 to DB7)
1	0	Write data to DDRAM or CGRAM (DR to DDRAM or CGRAM)
1	1	Read data from DDRAM or CGRAM (DDRAM or CGRAM to DR)

### Busy Flag (BF)

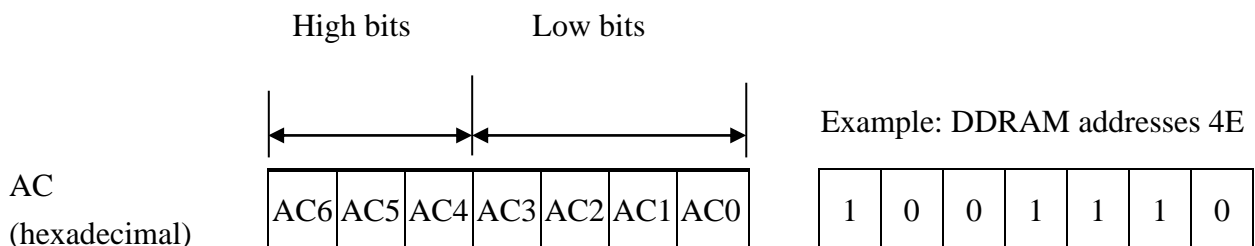
When the busy flag is 1, the controller LSI is in the internal operation mode, and the next instruction will not be accepted. When RS=0 and R/W=1, the busy flag is output to DB7. The next instruction must be written after ensuring that the busy flag is 0.

### Address Counter (AC)

The address counter (AC) assigns addresses to both DDRAM and CGRAM

### Display Data RAM (DDRAM)

This DDRAM is used to store the display data represented in 8-bit character codes. Its extended capacity is 80×8 bits or 80 characters. Below figure is the relationships between DDRAM addresses and positions on the liquid crystal display.



## Display position DDRAM address

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

2-Line by 16-Character Display

### **Character Generator ROM (CGROM)**

The CGROM generate  $5 \times 8$  dot or  $5 \times 10$  dot character patterns from 8-bit character codes. See Table 2.

### **Character Generator RAM (CGRAM)**

In CGRAM, the user can rewrite character by program. For  $5 \times 8$  dots, eight character patterns can be written, and for  $5 \times 10$  dots, four character patterns can be written.

Write into DDRAM the character code at the addresses shown as the left column of table 1. To show the character patterns stored in CGRAM.

# Relationship between CGRAM Addresses, Character Codes (DDRAM) and Character patterns

**Table 1.**

For 5 \* 8 dot character patterns

Character Codes ( DDRAM data )		CGRAM Address		Character Patterns ( CGRAM data )				
7 6 5 4 3 2 1 0		5 4 3 2 1 0		7 6 5 4 3 2 1 0				
High Low		High Low		High Low				
0 0 0 0 * 0 0 0		0 0 0	0 0 0	* * *		Character pattern( 1 )		
			0 0 1	* * *			0 0 0	Cursor pattern
			0 1 0	* * *			0 0 0	
			0 1 1	* * *			0 0 0	
			1 0 0	* * *			0 0 0	
			1 0 1	* * *			0 0 0	
			1 1 0	* * *			0 0 0	
			1 1 1	* * *			0 0 0	
			0 0 0	* * *			0 0 0	
			0 0 1	* * *			0 0 0	
0 1 0	* * *	0 0 0	Character pattern( 2 )					
0 1 1	* * *	0 0 0						
1 0 0	* * *	0 0 0						
0 0 0 0 * 0 0 1		0 0 1	1 0 0	* * *	0 0 0	Cursor pattern		
			1 0 1	* * *	0 0 0			
			1 1 0	* * *	0 0 0			
			1 1 1	* * *	0 0 0			
			0 0 0	* * *				
			0 0 1	* * *				
			1 0 0	* * *				
			1 0 1	* * *				
			1 1 0	* * *				
			1 1 1	* * *				
			1 1 1	* * *				

For 5 \* 10 dot character patterns

Character Codes ( DDRAM data )		CGRAM Address		Character Patterns ( CGRAM data )		
7 6 5 4 3 2 1 0		5 4 3 2 1 0		7 6 5 4 3 2 1 0		
High Low		High Low		High Low		
0 0 0 0 * 0 0 0		0 0	0 0 0 0	* * *	0 0 0 0 0	Character pattern
			0 0 0 1	* * *	0 0 0 0 0	
			0 0 1 0	* * *	0 0 0 0 0	
			0 0 1 1	* * *	0 0 0 0 0	
			0 1 0 0	* * *	0 0 0 0 0	
			0 1 0 1	* * *	0 0 0 0 0	
			0 1 1 0	* * *	0 0 0 0 0	
			0 1 1 1	* * *	0 0 0 0 0	
			1 0 0 0	* * *	0 0 0 0 0	
			1 0 0 1	* * *	0 0 0 0 0	
1 0 1 0	* * *	0 0 0 0 0	Cursor pattern			
			1 1 1 1	* * *	* * * * *	

■ : " High "

# 10. Character Generator ROM Pattern

Table.2

ST7066U

Table 4 Correspondence between Character Codes and Character Patterns (ROM Code: 0A)

NO.7066-0A

b7-b4 b3-b0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	CG RAM (1)			0	1	P	^	P				-	9	E	Q	P
0001	(2)	!	1	A	Q	a	9			.	7	7	4	ä	q	
0010	(3)	"	2	B	R	b	r			7	4	7	×	β	θ	
0011	(4)	#	3	C	S	c	s			7	0	7	E	ε	σ	
0100	(5)	\$	4	D	T	d	t			\	I	1	7	μ	σ	
0101	(6)	%	5	E	U	e	u			.	7	7	1	ε	0	
0110	(7)	&	6	F	V	f	v			7	0	2	3	p	Σ	
0111	(8)	'	7	G	W	g	w			7	7	×	7	g	π	
1000	(1)	(	8	H	X	h	x			4	0	*	7	7	×	
1001	(2)	)	9	I	Y	i	y			9	7	7	7	7	7	
1010	(3)	*	:	J	Z	j	z			ε	0	0	7	j	7	
1011	(4)	+	:	K	L	k	l			×	7	ε	0	×	7	
1100	(5)	,	<	L	7	l	l			7	0	7	7	7	7	
1101	(6)	-	=	M	7	m	7			ε	×	7	7	7	7	
1110	(7)	.	>	N	^	n	7			ε	ε	7	7	7	7	
1111	(8)	/	?	O	L	o	ε			7	7	7	7	7	7	7

# 11. Instruction Table

Instruction Table:

Instruction	Instruction Code										Description	Description Time (270KHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM. and set DDRAM address to "00H" from AC	1.52 ms
Return Home	0	0	0	0	0	0	0	0	1	x	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.52 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	37 us
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	D=1:entire display on C=1:cursor on B=1:cursor position on	37 us
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	x	x	Set cursor moving and display shift control bit, and the direction, without changing DDRAM data.	37 us
Function Set	0	0	0	0	1	DL	N	F	x	x	DL:interface data is 8/4 bits N:number of line is 2/1 F:font size is 5x11/5x8	37 us
Set CGRAM address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter	37 us
Set DDRAM address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter	37 us
Read Busy flag and address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0 us
Write data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM)	37 us
Read data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM)	37 us

**Note:**

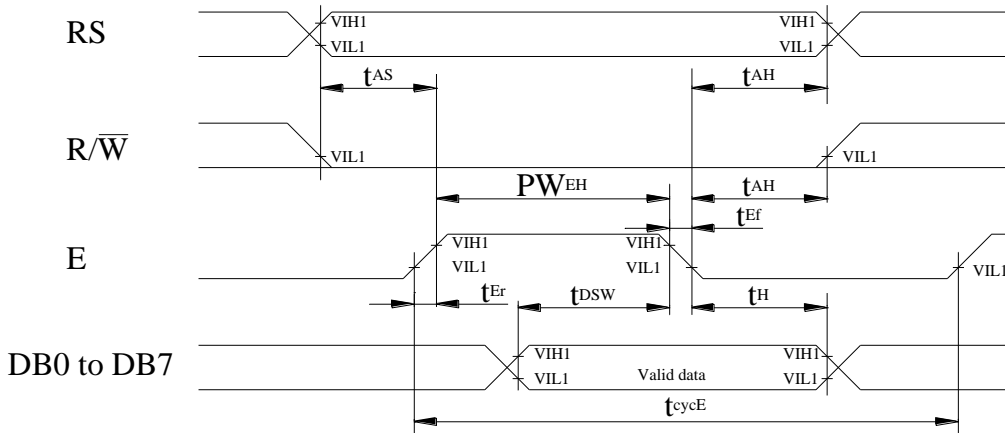
Be sure the ST7066U is not in the busy state (BF = 0) before sending an instruction from the MPU to the ST7066U. If an instruction is sent without checking the busy flag, the time between the first instruction and next instruction will take much longer than the instruction time itself. Refer to Instruction Table for the list of each instruction execution time.

\* "—" : don't care



# 12. Timing Characteristics

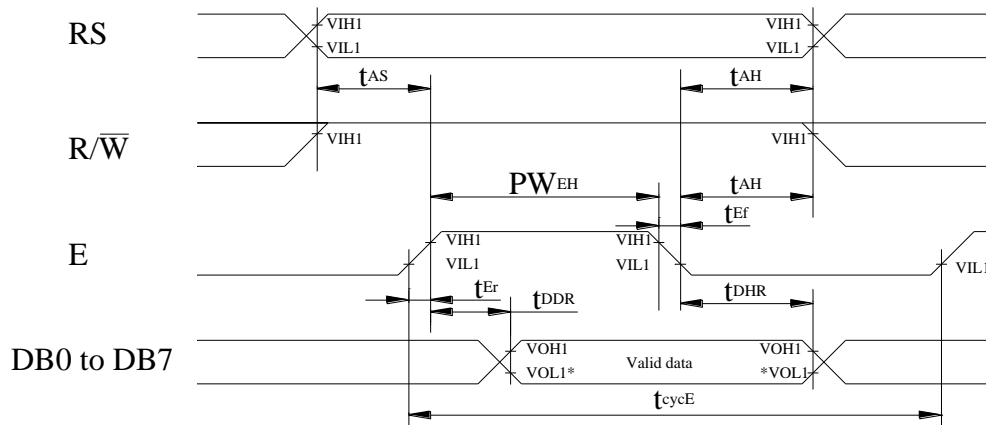
## 12.1 Write Operation



T<sub>a</sub>=25°C, V<sub>DD</sub>=5.0± 0.5V

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
<i>Internal Clock Operation</i>						
f <sub>OSC</sub>	OSC Frequency	R = 91KΩ	190	270	350	KHz
<i>External Clock Operation</i>						
f <sub>EX</sub>	External Frequency	-	125	270	410	KHz
	Duty Cycle	-	45	50	55	%
T <sub>R</sub> , T <sub>F</sub>	Rise/Fall Time	-	-	-	0.2	μs
<i>Write Mode (Writing data from MPU to ST7066U)</i>						
T <sub>C</sub>	Enable Cycle Time	Pin E	1200	-	-	ns
T <sub>PW</sub>	Enable Pulse Width	Pin E	140	-	-	ns
T <sub>R</sub> , T <sub>F</sub>	Enable Rise/Fall Time	Pin E	-	-	25	ns
T <sub>AS</sub>	Address Setup Time	Pins: RS,RW,E	0	-	-	ns
T <sub>AH</sub>	Address Hold Time	Pins: RS,RW,E	10	-	-	ns
T <sub>DSW</sub>	Data Setup Time	Pins: DB0 - DB7	40	-	-	ns
T <sub>H</sub>	Data Hold Time	Pins: DB0 - DB7	10	-	-	ns

## 12.2 Read Operation



NOTE: \*VOL1 is assumed to be 0.8V at 2 MHz operation.

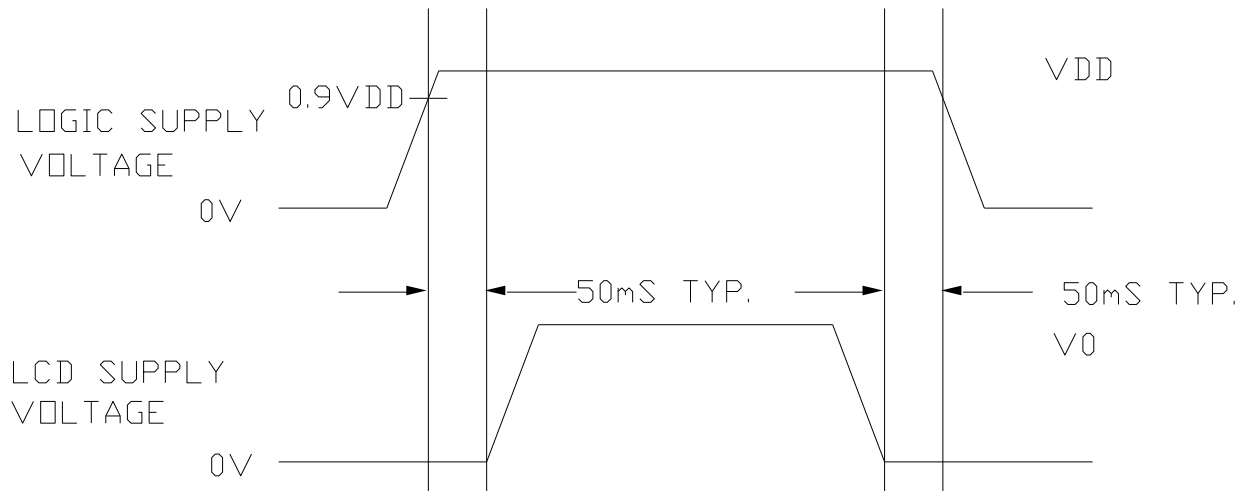
$T_a=25^\circ\text{C}$ ,  $V_{DD}=5.0\pm 0.5\text{V}$

Read Mode (Reading Data from ST7066U to MPU)						
$T_C$	Enable Cycle Time	Pin E	1200	-	-	ns
$T_{PW}$	Enable Pulse Width	Pin E	140	-	-	ns
$T_{R,T_F}$	Enable Rise/Fall Time	Pin E	-	-	25	ns
$T_{AS}$	Address Setup Time	Pins: RS,RW,E	0	-	-	ns
$T_{AH}$	Address Hold Time	Pins: RS,RW,E	10	-	-	ns
$T_{DDR}$	Data Setup Time	Pins: DB0 - DB7	-	-	100	ns
$T_H$	Data Hold Time	Pins: DB0 - DB7	10	-	-	ns

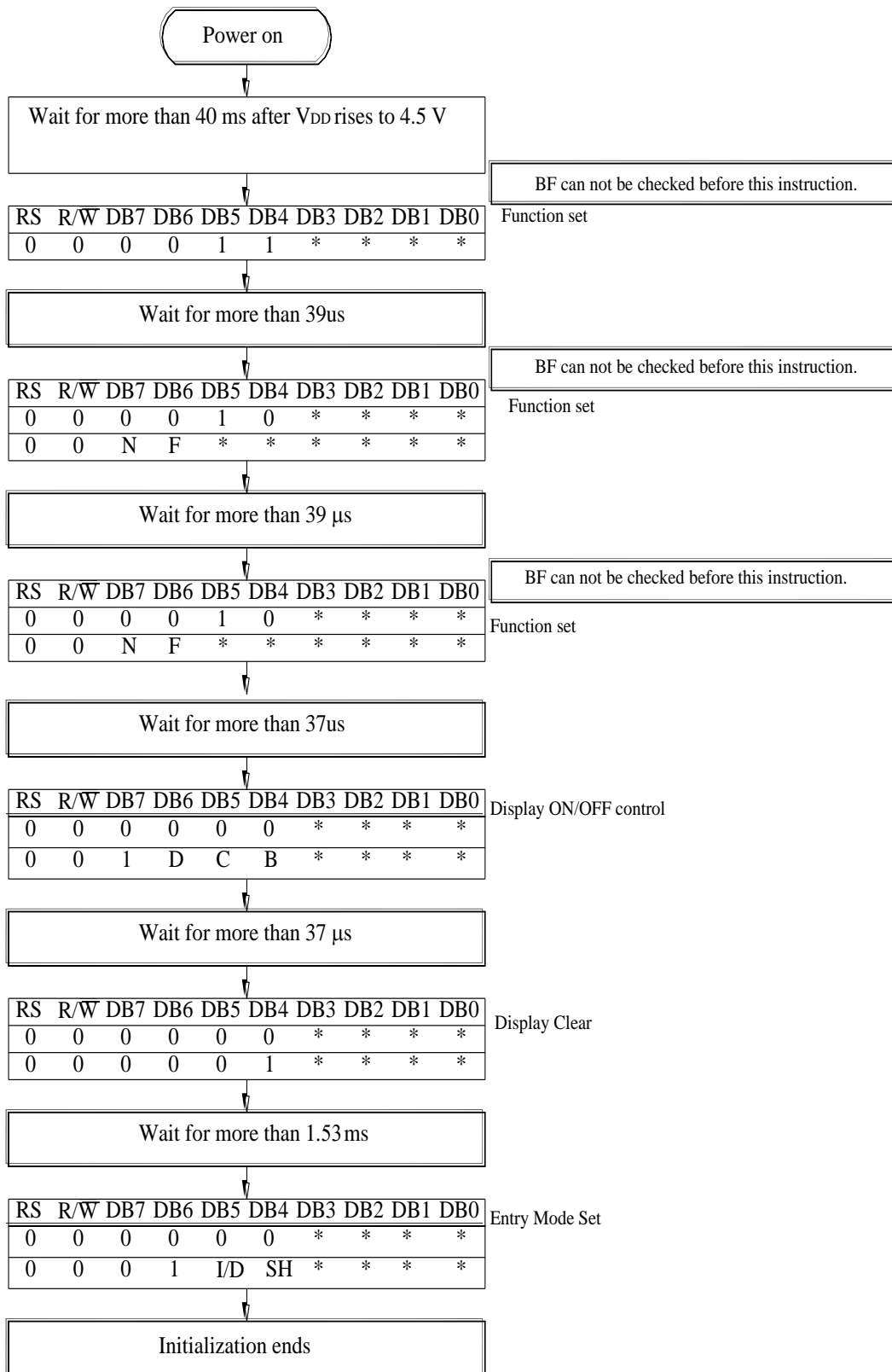


### 12.3 Timing Diagram of VDD Against V0.

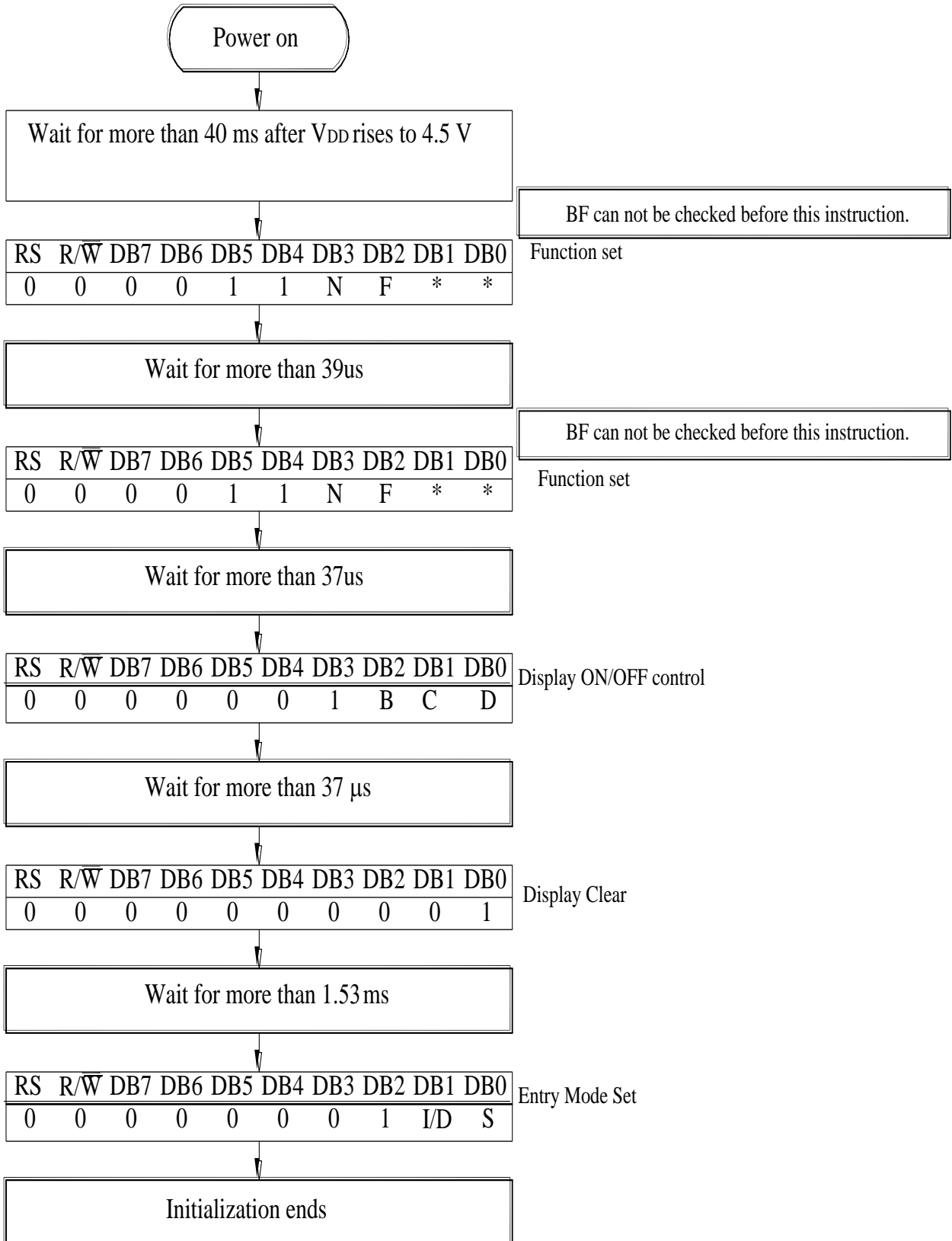
Power on sequence shall meet the requirement of Figure 4, the timing diagram of VDD against V0.



# 13. Initializing of LCM



4-Bit Inerface



8-Bit Ineterface

# 14. Quality Assurance

## Screen Cosmetic Criteria

Item	Defect	Judgment Criterion	Partition																				
1	Spots	<p>A)Clear</p> <table border="1"> <thead> <tr> <th>Size: d mm</th> <th>Acceptable Qty in active area</th> </tr> </thead> <tbody> <tr> <td><math>d \leq 0.1</math></td> <td>Disregard</td> </tr> <tr> <td><math>0.1 &lt; d \leq 0.2</math></td> <td>6</td> </tr> <tr> <td><math>0.2 &lt; d \leq 0.3</math></td> <td>2</td> </tr> <tr> <td><math>0.3 &lt; d</math></td> <td>0</td> </tr> </tbody> </table> <p>Note: Including pin holes and defective dots which must be within one pixel size.</p> <p>B)Unclear</p> <table border="1"> <thead> <tr> <th>Size: d mm</th> <th>Acceptable Qty in active area</th> </tr> </thead> <tbody> <tr> <td><math>d \leq 0.2</math></td> <td>Disregard</td> </tr> <tr> <td><math>0.2 &lt; d \leq 0.5</math></td> <td>6</td> </tr> <tr> <td><math>0.5 &lt; d \leq 0.7</math></td> <td>2</td> </tr> <tr> <td><math>0.7 &lt; d</math></td> <td>0</td> </tr> </tbody> </table>	Size: d mm	Acceptable Qty in active area	$d \leq 0.1$	Disregard	$0.1 < d \leq 0.2$	6	$0.2 < d \leq 0.3$	2	$0.3 < d$	0	Size: d mm	Acceptable Qty in active area	$d \leq 0.2$	Disregard	$0.2 < d \leq 0.5$	6	$0.5 < d \leq 0.7$	2	$0.7 < d$	0	Minor
Size: d mm	Acceptable Qty in active area																						
$d \leq 0.1$	Disregard																						
$0.1 < d \leq 0.2$	6																						
$0.2 < d \leq 0.3$	2																						
$0.3 < d$	0																						
Size: d mm	Acceptable Qty in active area																						
$d \leq 0.2$	Disregard																						
$0.2 < d \leq 0.5$	6																						
$0.5 < d \leq 0.7$	2																						
$0.7 < d$	0																						
2	Bubbles in Polarizer	<table border="1"> <thead> <tr> <th>Size: d mm</th> <th>Acceptable Qty in active area</th> </tr> </thead> <tbody> <tr> <td><math>d \leq 0.3</math></td> <td>Disregard</td> </tr> <tr> <td><math>0.3 &lt; d \leq 1.0</math></td> <td>3</td> </tr> <tr> <td><math>1.0 &lt; d \leq 1.5</math></td> <td>1</td> </tr> <tr> <td><math>1.5 &lt; d</math></td> <td>0</td> </tr> </tbody> </table>	Size: d mm	Acceptable Qty in active area	$d \leq 0.3$	Disregard	$0.3 < d \leq 1.0$	3	$1.0 < d \leq 1.5$	1	$1.5 < d$	0	Minor										
Size: d mm	Acceptable Qty in active area																						
$d \leq 0.3$	Disregard																						
$0.3 < d \leq 1.0$	3																						
$1.0 < d \leq 1.5$	1																						
$1.5 < d$	0																						
3	Scratch	In accordance with spots cosmetic criteria. When the light reflects on the panel surface, the scratches are not to be remarkable.	Minor																				
4	Allowable Density	Above defects should be separated more than 30mm each other.	Minor																				
5	Coloration	Not to be noticeable coloration in the viewing area of the LCD panels. Back-light type should be judged with back-light on state only.	Minor																				

# 15. Reliability

## Content of Reliability Test

Environmental Test			
Test Item	Content of Test	Test Condition	Applicable Standard
High Temperature storage	Endurance test applying the high storage temperature for a long time.	80°C 96hrs	—
Low Temperature storage	Endurance test applying the high storage temperature for a long time.	-30°C 96hrs	—
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70°C 96hrs	—
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20°C 96hrs	—
High Temperature/ Humidity Storage	Endurance test applying the high temperature and high humidity storage for a long time.	60°C,90%RH 96hrs	—
High Temperature/ Humidity Operation	Endurance test applying the electric stress (Voltage & Current) and temperature / humidity stress to the element for a long time.	60°C,90%RH 96hrs	—
Temperature Cycle	Endurance test applying the low and high temperature cycle. <div style="text-align: center;"> <p style="margin: 0;">-30°C    25°C    80°C</p> <p style="margin: 0;">30min    5min    30min</p> <p style="margin: 0;">1 cycle</p> </div>	-30°C→80°C 10 cycles	—
Mechanical Test			
Vibration test	Endurance test applying the vibration during transportation and using.	50Hz→3mm p-p Total 0.5hrs	—

\*\*\*Supply voltage for logic system=5V. Supply voltage for LCD system =Operating voltage at 25°C