



**SPECIFICATION  
FOR  
LCD MODULE**

**MODULE NO: AFK320480A0-3.5INTM  
REVISION NO: V01**

Customer's Approval:

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	SIGNATURE	DATE
PREPARED BY (RD ENGINEER)		
CHECKED BY		
APPROVED BY		



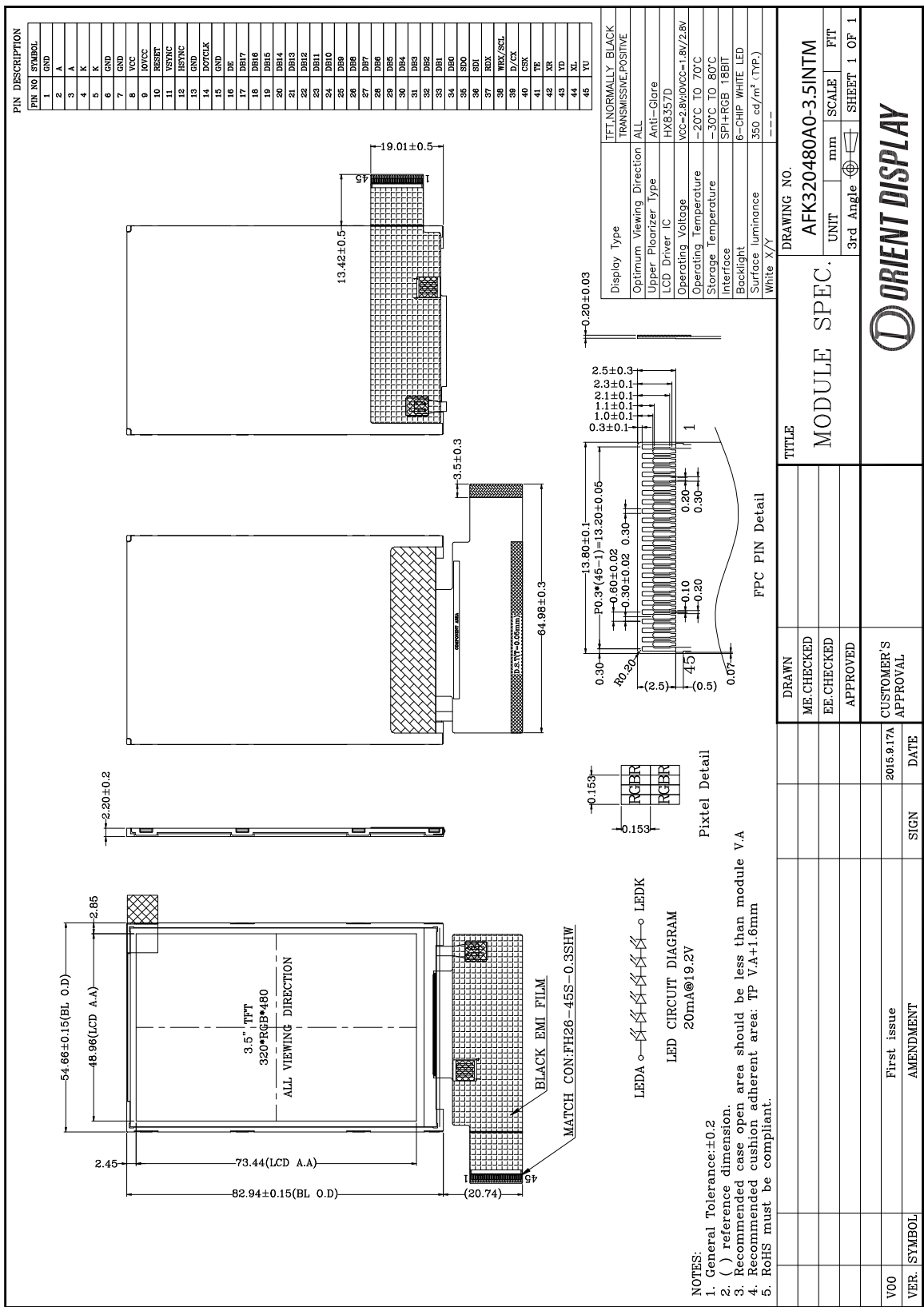
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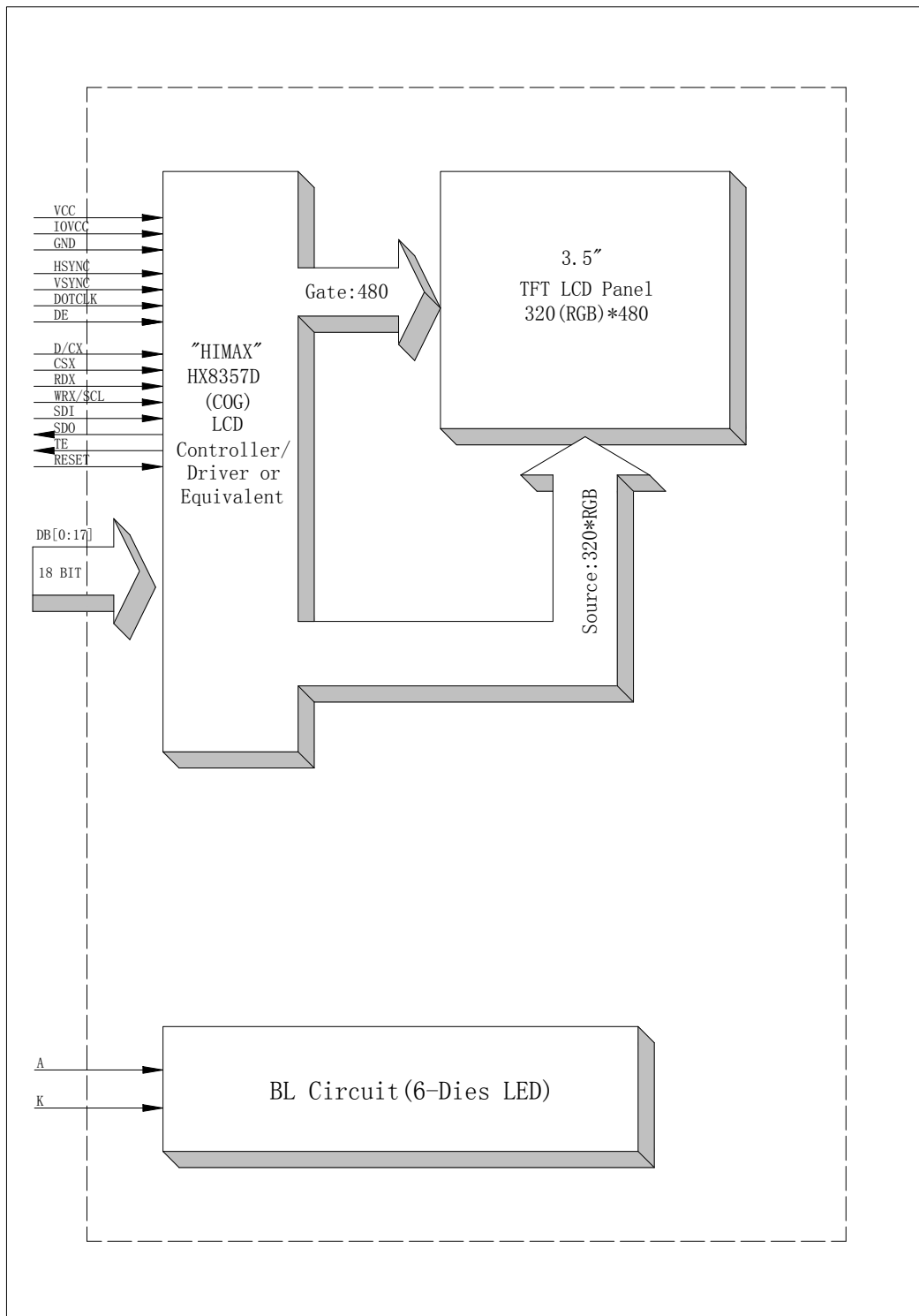
# 1. General Specification

<b>Item</b>	<b>Contents</b>	<b>Unit</b>
LCD TYPE	TFT/TRANSMISSIVE	
MODULE SIZE (W*H*T)	54.66*82.94*2.2	MM
ACTIVE SIZE (W*H)	48.96*73.44	MM
PIXEL PITCH (W*H)	0.153*0.153	MM
NUMBER OF DOTS	320*480	
DIVER IC	HX8357D	
INTERFACE TYPE	SPI+18BIT RGB	
TOP POLARIZER TYPE	ANTI-GLARE	
RECOMMEND VIEWING DIRECTION	ALL	O'CLOCK
GRAY SCALE INVERSION DIRECTION	--	O'CLOCK
COLORS	262K	
BACKLIGHT TYPE	6-DIES WHITE LED	
TOUCH PANEL TYPE	WITHOUT	

# 2. Mechanical Drawing



### 3. Block Diagram



## 4. Interface Pin Function

Pin No.	Symbol	Description
1	GND	Power ground.
2	A	Anode of LED backlight.
3	A	Anode of LED backlight.
4	K	Cathode of LED backlight.
5	K	Cathode of LED backlight.
6	GND	Power ground.
7	GND	Power ground.
8	VCC	Power supply for analog voltage.
9	IOVCC	Power supply for logic voltage.
10	RESET	Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied.
11	VSYNC	Vertical synchronizing signal in RGB interface. If this pin is not used, connect it to GND.
12	HSYNC	Horizontal synchronizing signal in RGB interface. If this pin is not used, connect it to GND.
13	GND	Power ground.
14	DOTCLK	Data enable signal in RGB interface. If this pin is not used, connect it to GND.
15	GND	Power ground.
16	DE	A data ENABLE signal in RGB mode. If this pin is not used, connect it to GND.
17~34	DB17~DB0	Data bus.
35	SDO	Serial data output. If SDO_EN=0, SDO is not use. If SDO_EN=1, SDO is serial data output. If not used, please let it open.
36	SDI	Serial data input pin and output pin in serial bus system interface. The data is inputted on the rising edge of the SCL signal. If not used, please let it open.
37	RDX	MPU mode: Serves as a read signal and read data at the low level. If this pin is not used, connect it to IOVCC or GND.
38	WRX/SCL	MPU mode: Serves as a write signal and write data at the low level. SPI mode: it servers as SCL (Serial Clock) If this pin is not used, connect it to IOVCC or GND.
39	D/CX	MPU, SPI-4 line: Data / Command Selection pin. If this pin is not used, connect it to IOVCC or GND.
40	CSX	Chip select signal. Low: chip can be accessed; High: chip cannot be accessed. If this pin is not used, connect it to IOVCC.
41	TE	Tearing effect output. If not used, please open this pin.

42	NC	NO CONNECT
43	NC	NO CONNECT
44	NC	NO CONNECT
45	NC	NO CONNECT



## 5. Absolute Maximum Ratings

<b>Parameter</b>	<b>Symbol</b>	<b>Min</b>	<b>Max</b>	<b>Unit</b>
Supply voltage for analog	VCC	-0.3	4.6	V
Supply voltage for logic	IOVCC	-0.3	4.6	V
Supply current (One LED)	I <sub>LED</sub>		30	mA
Operating temperature	T <sub>OP</sub>	-20	+70	°C
Storage temperature	T <sub>ST</sub>	-30	+80	°C

## 6. Electrical Characteristics

### 6.1 Input Power

Item	Symbol	Min	Typ.	Max	Unit	Applicable terminal
Supply Voltage for Analog	VCC	2.5	2.8	3.3	V	
Supply Voltage for Logic	IOVCC	1.65	1.8/2.8	3.3	V	
Input Voltage	V <sub>IL</sub>	GND	-	0.3IOVCC	V	
	V <sub>IH</sub>	0.8 IOVCC	-	IOVCC		
Input leakage Current	I <sub>LKG</sub>	-1		1	μA	

### 6.2 Backlight Driving Conditions

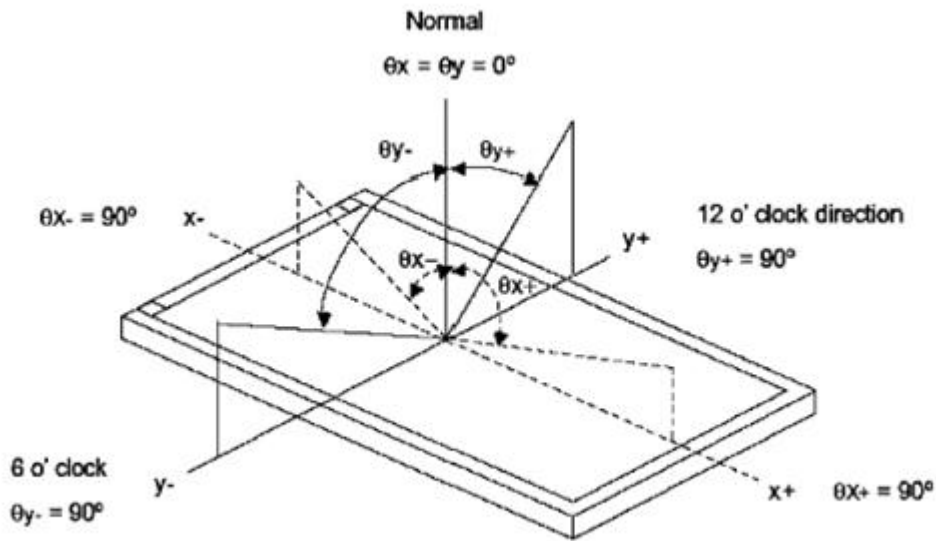
Item	Symbol	Value			Unit	Remark
		Min.	Typ.	Max.		
Voltage for LED Backlight	V <sub>F</sub>	18.0	19.2	20.4	V	I <sub>L</sub> =20mA
Current for LED Backlight	I <sub>L</sub>		20	30	mA	
Power Consumption	P		0.384		W	
LED Life Time		30,000			Hr	Note

**Note:** Brightness to be decreased to 50% of the initial value at ambient temperature TA=25°C

## 7. Optical Characteristics

ITEM	SYMBOL	CONDITIONS	SPECIFICATIONS			UNIT	NOTE
			MIN	TYP.	MAX		
Luminance	L	$I_L = 20\text{mA}$		350		$\text{Cd/m}^2$	
Contrast Ratio	CR	$\theta = 0^\circ$		700			
Response Time	$T_{\text{ON}}$	$25^\circ\text{C}$		30		ms	
	$T_{\text{OFF}}$						
CIE Color Coordinate	Red	$X_R$	Viewing normal angle				
		$Y_R$					
	Green	$X_G$					
		$Y_G$					
	Blue	$X_B$					
		$Y_B$					
	White	$X_W$			0.327		
		$Y_W$			0.354		
Viewing Angle	Hor.	$\theta_{X+}$	$CR \geq 10$		80	Degree	
		$\theta_{X-}$			80		
	Ver.	$\theta_{Y+}$			80		
		$\theta_{Y-}$			80		
Uniformity	Un			80		%	

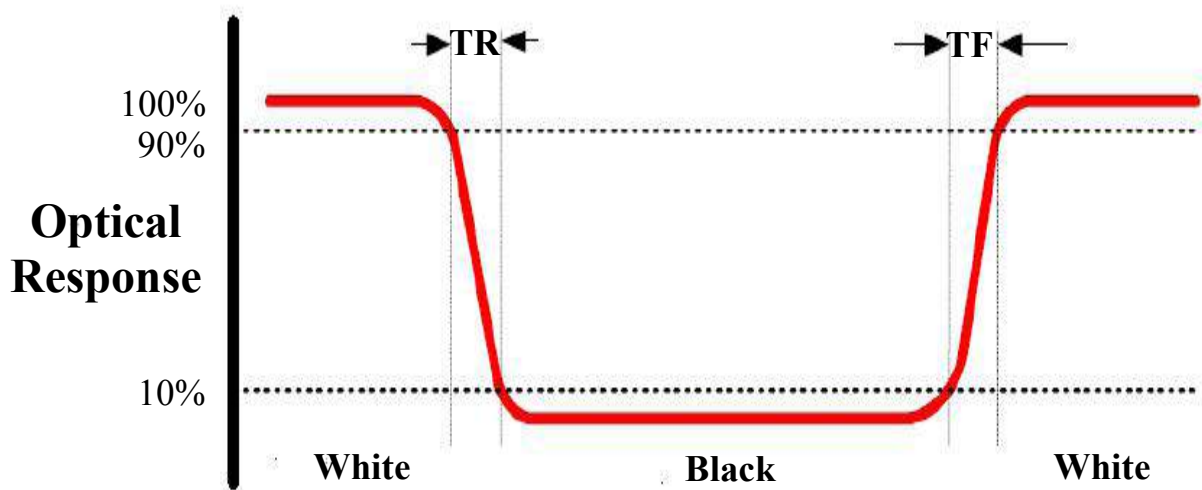
**Note 1: Definition of Viewing Angle  $\theta_x$  and  $\theta_y$ :**



**Note 2: Definition of contrast ratio CR:**

$$CR = \frac{\text{Luminance of white state}}{\text{Luminance of black state}}$$

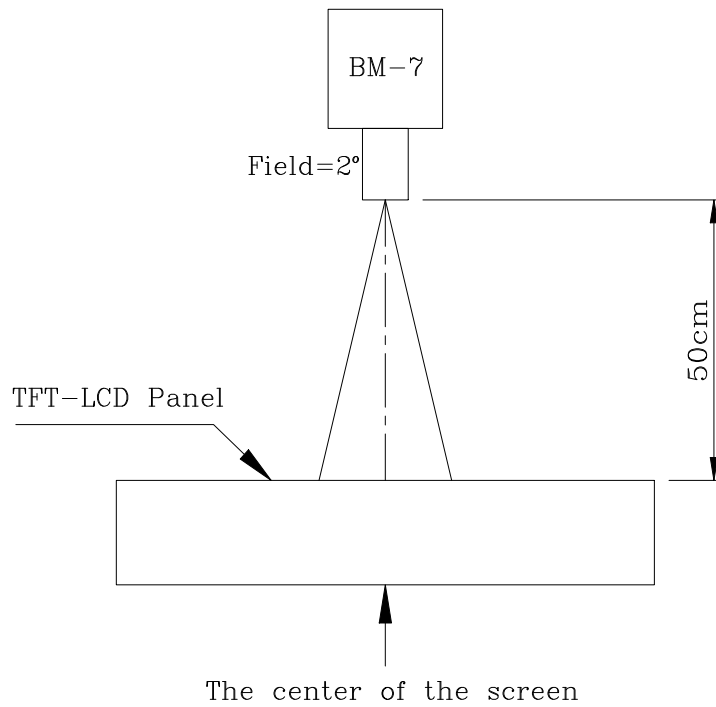
**Note 3: Definition of Response Time ( $T_r, T_f$ )**



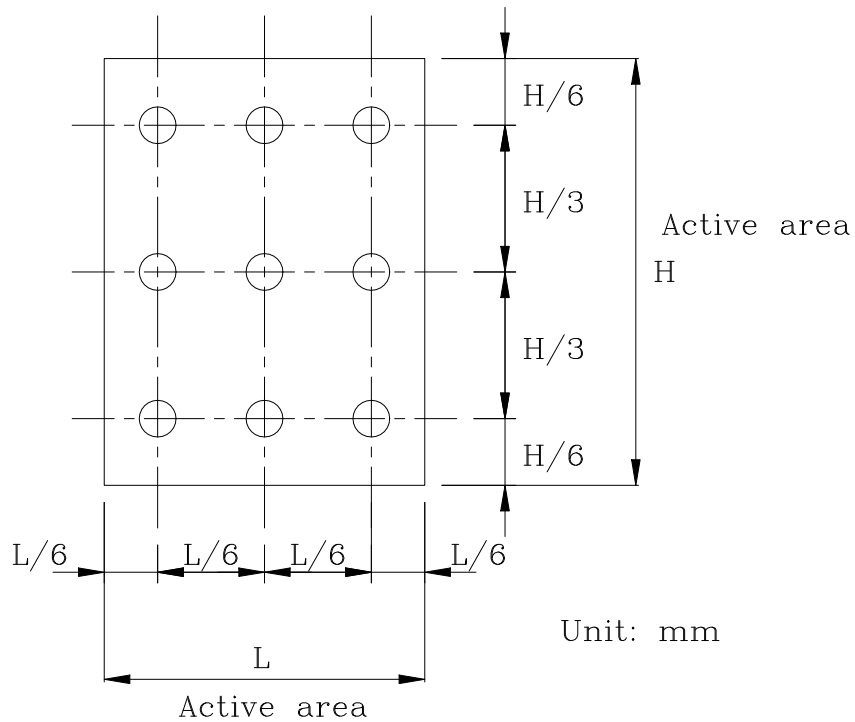
#### Note 4: Definition of Luminance

##### ①The Brightness Test Equipment Setup

Field=2° (As measuring “black” image, field=2° is the best testing condition)



##### ②The Brightness Test Point Setup



# 8. Timing Characteristics

## 8.1 MPU interface characteristic

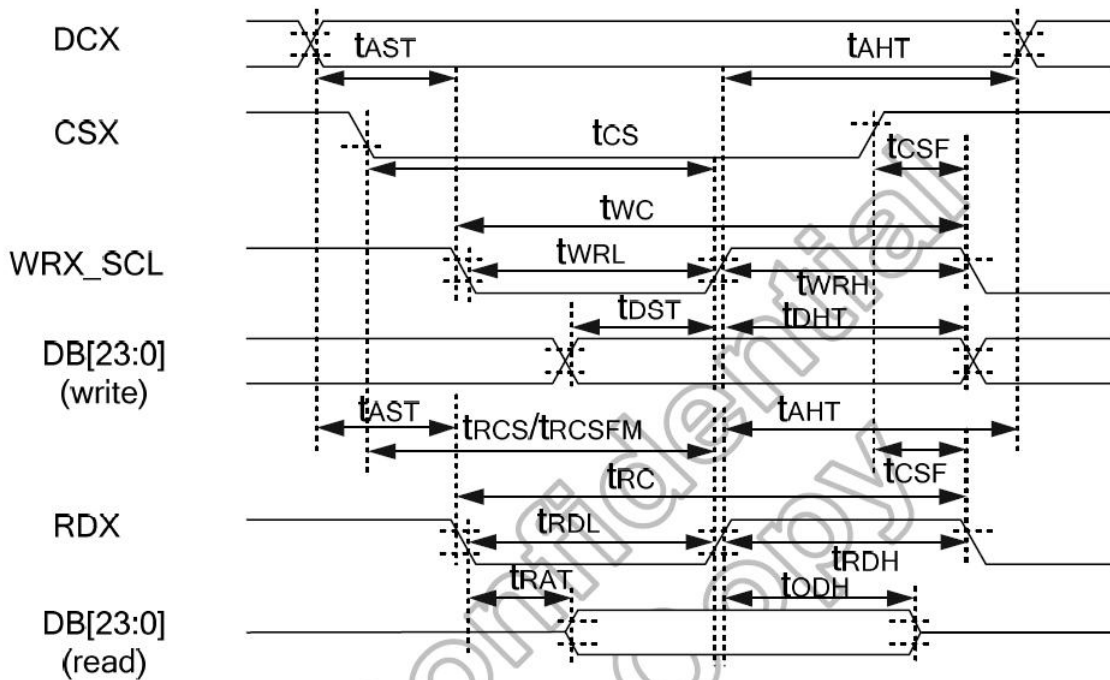


Figure 8.1:MPU interface characteristics

(GND=0V, IOVCC=1.8V, VCI=2.8V,  $T_A=25^\circ\text{C}$ , Sleep Out states)

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
DCX	$t_{AST}$	Address setup time	0	-	ns	-
	1	Address hold time (Write/Read)	10	-		
CSX	$t_{CS}$	Chip select setup time (Write)	10	-	ns	-
	$t_{RCS}$	Chip select setup time (Read register)	45	-		
	$t_{RCSFM}$	Chip select setup time (GRAM)	355	-		
	$t_{CSF}$	Chip select wait time (Write/Read)	10	-		
WRX_SCL	$t_{WC}$	Write cycle (write register)	50	-	ns	-
	$t_{WC}$	Write cycle (write GRAM@SLPOUT)	47	-		
	$t_{WC}$	Write cycle (write GRAM@SLPIN)	100	-		
	$t_{WRH}$	Control pulse "H" duration	15	-		
	$t_{WRL}$	Control pulse "L" duration	15	-		
RDX	$t_{RC}$	Read cycle (read register)	160	-	ns	-
	$t_{RC}$	Read cycle (GRAM)	450	-		
	$t_{RDH}$	Control pulse "H" duration	90	-		
	$t_{RDH}$	Control pulse "L" duration(read register)	35	-		
	$t_{RDH}$	Control pulse "L" duration(GRAM)	345	-		
DB[23:0]	$t_{DST}$	Data setup time	10	-	ns	For maximum $C_L=30\text{pF}$ For minimum $C_L=8\text{pF}$
	$t_{DHT}$	Data hold time	10	-		
	$t_{RAT}$	Read access time(read register)	-	40		
	$t_{RAT}$	Read access time(GRAM)	-	340		
	$t_{ODH}$	Output disable time	20	80		

Table 8.1: MPU interface characteristics

**Note:** The input signal rise time and fall time ( $t_r$ ,  $t_f$ ) is specified at 15 ns or less.  
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

## 8.2 SPI interface characteristics

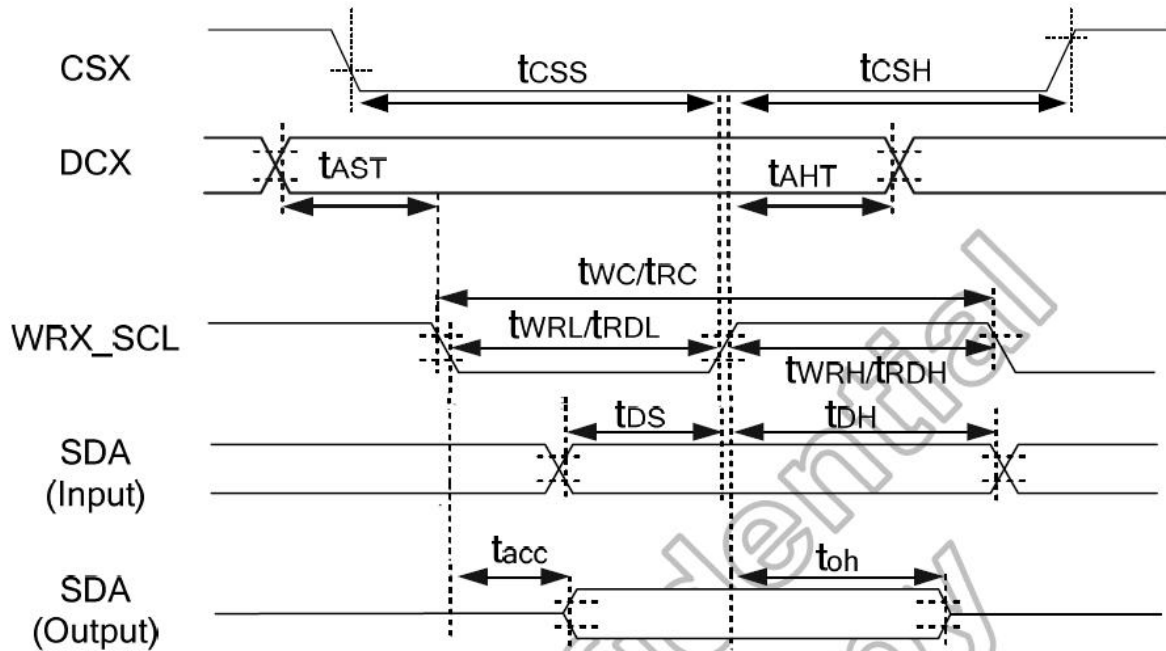


Figure 8.2: SPI interface characteristics

(GND=0V, IOVCC=1.8V, VCI=2.8V,  $T_A=25^\circ\text{C}$ , Sleep Out states)

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
CSX	$t_{cSS}$	Chip select setup time (Write)	15	-	ns	-
	$t_{cSS}$	Chip select setup time (Read)	60	-		
	$t_{cSH}$	Chip select hold time (Write)	15	-		
	$t_{cSH}$	Chip select hold time (Read)	65	-		
DCX	$t_{AST}$	Address setup time	0	-	ns	-
	I	Address hold time (Write/Read)	10	-		
WRX_SCL (Write)	$t_{wC}$	Write cycle	66	-	ns	-
	$t_{wRH}$	Control pulse "H" duration	15	-		
	$t_{wRL}$	Control pulse "L" duration	15	-		
WRX_SCL (Read)	$t_{rC}$	Read cycle	150	-	ns	-
	$t_{rDH}$	Control pulse "H" duration	60	-		
	$t_{rDL}$	Control pulse "L" duration	60	-		
SDA (Input)	$t_{DS}$	Data setup time	10	-	ns	For maximum $C_L=30\text{pF}$ For minimum $C_L=8\text{pF}$
	$t_{DH}$	Data hold time	10	-		
SDA (Output)	$t_{acc}$	Read access time	10	50	ns	
	$t_{oh}$	Output disable time	15	50		

Table 8.2: SPI interface characteristics

**Note:** The input signal rise time and fall time ( $t_r$ ,  $t_f$ ) is specified at 15 ns or less.  
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

### 8.3 RGB interface characteristics

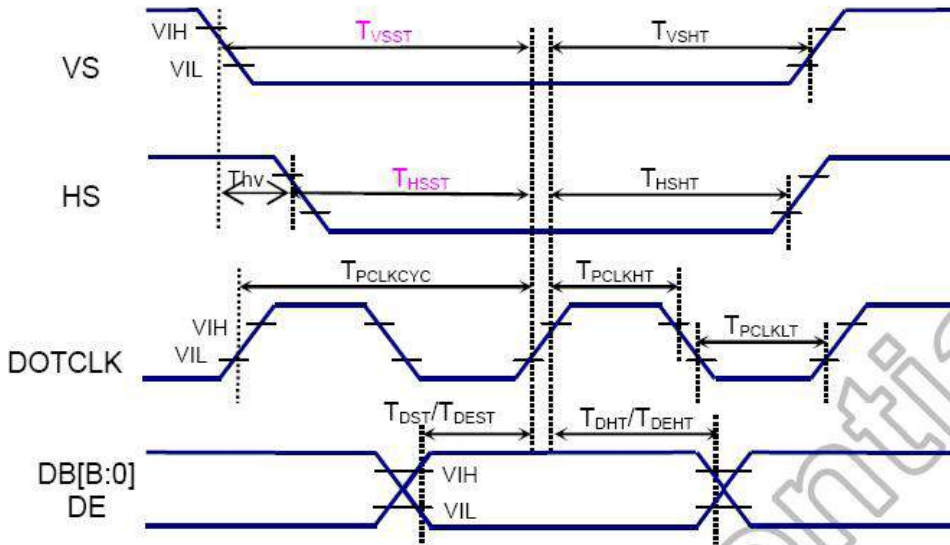


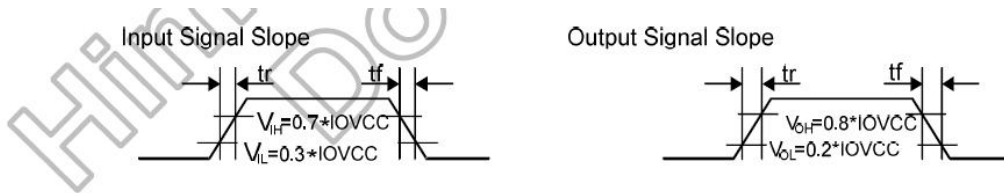
Figure 8.3: RGB interface characteristics

(GND=0V, IOVCC=1.8V, VCI=2.8V, TA=25°C, Sleep Out states)

Item	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Pixel low pulse width	$T_{CLKLT}$	-	15	-	-	ns
Pixel high pulse width	$T_{CLKHT}$	-	15	-	-	ns
Vertical Sync. Set-up time	$T_{VSST}$	-	15	-	-	ns
Vertical Sync. Hold time	$T_{VSHT}$	-	15	-	-	ns
Horizontal Sync. Set-up time	$T_{HSST}$	-	15	-	-	ns
Horizontal Sync. Hold time	$T_{HSHT}$	-	15	-	-	ns
Data Enable set-up time	$T_{DEST}$	-	15	-	-	ns
Data Enable hold time	$T_{DEHT}$	-	15	-	-	ns
Data set-up time	$T_{DST}$	-	15	-	-	ns
Data hold time	$T_{DHT}$	-	15	-	-	ns
Phase difference of sync signal falling edge	$Thv$	-	0	-	320	Dotclk

Table 8.3: RGB interface characteristics

**Note:** The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.





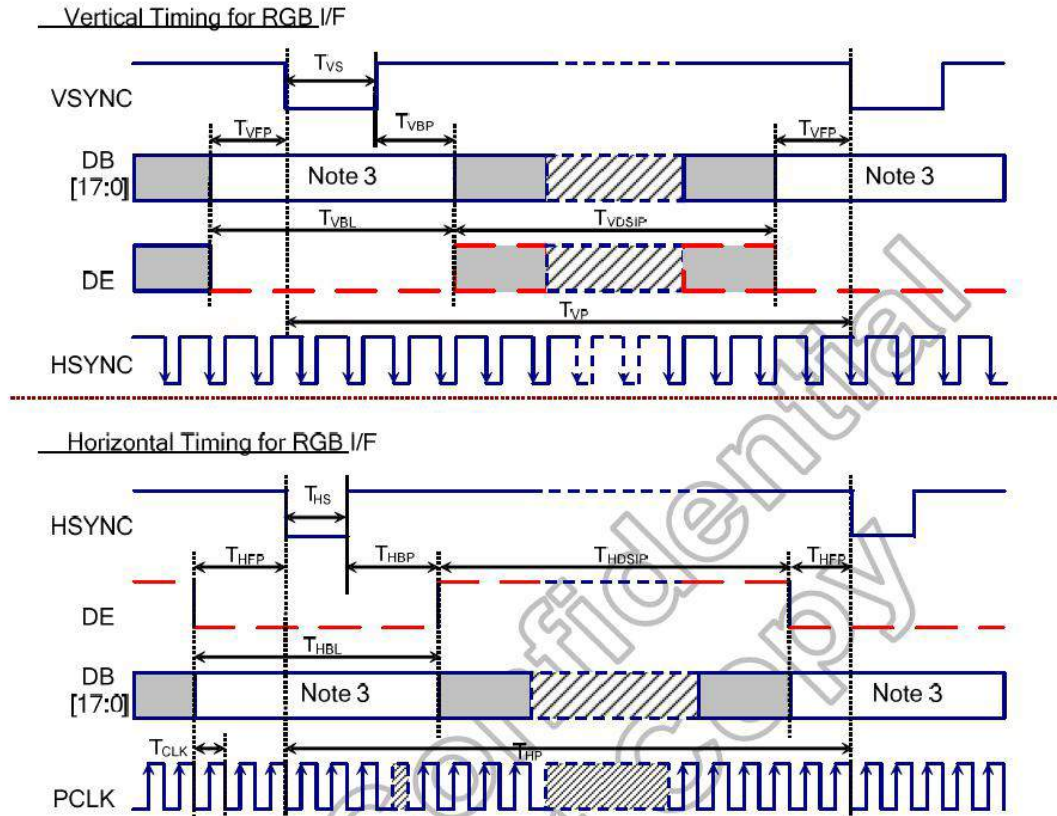


Figure 8.4: General timings for RGB I/F-2

Item	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
<b>Vertical Timing</b>						
Vertical cycle period	$T_{VP}$	-	486	-	-	HS
Vertical low pulse width	$T_{VS}$	-	2	-	-	HS
Vertical front porch	$T_{VFP}$	-	2	-	-	HS
Vertical back porch	$T_{VBP}$	-	2	-	-	HS
Vertical blanking period	$T_{VBL}$	$T_{VS} + T_{VBP} + T_{VFP}$	6	-	-	HS
Vertical active area	$T_{VDISP}$	-	-	480	-	HS
			-		-	HS
			-		-	HS
Vertical refresh rate	$T_{VRR}$	Frame rate	50	60	70	Hz
<b>Horizontal Timing</b>						
Horizontal cycle period	$T_{HP}$	-	335	-	-	DOTCLK
Horizontal low pulse width	$T_{HS}$	-	5	-	-	DOTCLK
Horizontal front porch	$T_{HFP}$	-	5	-	-	DOTCLK
Horizontal back porch	$T_{HBP}$	-	5	-	-	DOTCLK
Horizontal blanking period	$T_{HBL}$	$T_{HS} + T_{HBP} + T_{HFP}$	15	-	-	DOTCLK
Horizontal active area	$T_{HDISP}$	-	-	320	-	DOTCLK
Pixel clock cycle	$f_{CLKCYC}$	-	9	-	-	MHz
TVRR=60Hz						

Table 8.4: RGB interface characteristics-2

**Note:** (1) IOVCC=1.65 to 3.3V, VCI=2.3 to 3.3V, VSSA=VSSD=0V, Ta=-30 to 70°C (to +85°C no damage)

(2) Data lines can be set to "High" or "Low" during blanking time – Don't care.

(3) HP is multiples of PCLK.

## 8.4 Reset input timing

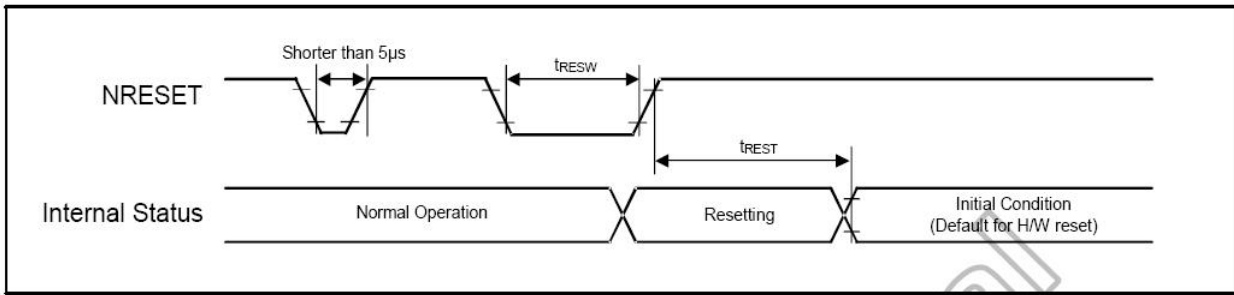


Figure 8.5: Reset input timing

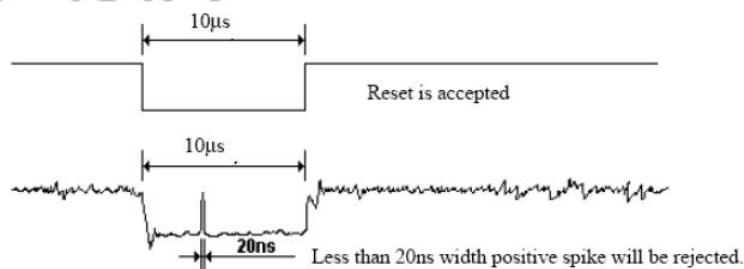
Symbol	Parameter	Related Pins	Spec.			Note	Unit
			Min.	Typ.	Max.		
tRESW	Reset low pulse width <sup>(1)</sup>	NRESET	10	-	-	-	µs
tREST	Reset complete time <sup>(2)</sup>	-	5	-	-	When reset applied during SLPIN mode	ms
		-	120	-	-	When reset applied during SLPOUT mode	ms

Table 8.5: Reset input timing

Note: (1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the following table.

NRESET Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

- (2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which Maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.
- (3) During Reset Complete Time, ID and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of NRESET.
- (4) Spike Rejection also applies during a valid reset pulse as shown as below:



01. It is necessary to wait 5msec after releasing NRESET before sending commands. Also Sleep Out command cannot be sent for 120msec.

## 9. Standard Specification for Reliability

### 9.1 Standard Specification for Reliability of LCD Module

No.	Item	Description
01	High temperature operation	The sample should be allowed to stand at 70°C for 120 hours under driving condition and then returning it to normal temperature condition, and allowing it stand for 2 hours.
02	Low temperature operation	The sample should be allowed to stand at -20°C for 120 hours under driving condition and then returning it to normal temperature condition, and allowing it stand for 2 hours.
03	High temperature storage	The sample should be allowed to stand at 80°C for 240 hours under no-load condition, and then returning it to normal temperature condition, and allowing it stand for 2 hours.
04	Low temperature storage	The sample should be allowed to stand at -30°C for 240 hours under no-load condition, then returning it to normal temperature condition, and allowing it stand for 2 hours.
05	Moisture storage	The sample should be allowed to stand at 60°C,90%RH MAX for 240 hours under no-load condition, then taking it out and drying it at normal temperature for 2 hours.
06	Thermal shock storage	The sample should be allowed to stand the following 10 cycles : -30°C for 30 minutes → normal temperature for 5 minutes → +80°C for 30 minutes → normal temperature for 5 minutes, as one cycle.
07	Packing vibration	Frequency range : 10Hz ~ 55Hz Amplitude of vibration : 1.5mm Sweep time: 12 min X,Y,Z 2 hours for each direction.
08	Packing drop test	According to ASTM-D-5327.
09	Electrical Static Discharge	Air: ±4KV 150pF/330Ω 5 times
		Contact: ±2KV 150pF/330Ω 5 time

\*Sample size for each test item is 3~5pcs

## 9.2 Testing Conditions and Inspection Criteria

For the final test, the testing sample must be stored at room temperature for 24 hours. After the tests listed in Table 9.2, standard specifications for reliability will be executed in order to ensure stability.

No.	Item	Test Model	In section Criteria
01	Current Consumption	Refer To Specification	The current consumption should conform to the product specification.
02	Contrast	Refer To Specification	After the tests have been executed, the contrast must be larger than half of its initial value prior to the tests.
03	Appearance	Visual inspection	Defect free.

## 9.3 MTBF

MTBF	Functions, performance, appearance, etc. shall be free from remarkable deterioration within 50,000 hours under ordinary operating and storage conditions room temperature ( $25\pm 5^{\circ}\text{C}$ ), normal humidity ( $50\pm 10\%$ RH), and in area not exposed to direct sun light.
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# 10. Specification of Quality Assurance

This standard of Quality Assurance confirms to the quality of LCD module products supplied by ODNA.

## 10.1 Quality Test

Before delivering, the supplier should conduct the following tests to confirm the quality of products.

- Electrical-Optical Characteristics: According to the individual specification to test the product.
- Appearance Characteristics: According to the individual specification to test the product.
- Reliability Characteristics: According to the definition of reliability on the specification for testing products.

## 10.2 Delivery Test

Before delivering, the supplier should conduct the delivery test.

- Test method: According to MIL-STD105E.General Inspection Level II take a single Time.
- The defects classify of AQL as following:  
Major defect: AQL = 0.65  
Minor defect: AQL = 2.5  
Total defects: AQL = 2.5

## 10.3 Non-conforming Analysis & Deal With Manners

### 10.3.1 Non-conforming Analysis

- Purchaser should provide the data detail of non-conforming sample and the non-conforming.
- After receiving the data detail from purchaser, the analysis of non-conforming should be finished within two weeks.
- If the analysis can't be finished on time, supplier must notice purchaser 3 days in advance.

### 10.3.2 Disposition of non-conforming

- If any product defect be found during assembling, supplier must change the good for every defect after confirmation.
- Both supplier and customer should analyze the reason and discuss the disposition of non-conforming when the reason of nonconforming is not sure.

## 10.4 Agreement items

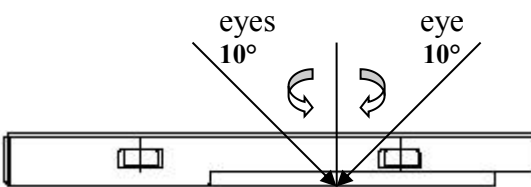
Both parties should negotiate together when the following problems happen.

- There is any problem of standard of quality assurance, and both sides should agree that it must be modified.
- There is any argument item which does not record in the standard of quality assurance.
- Any other special problem.

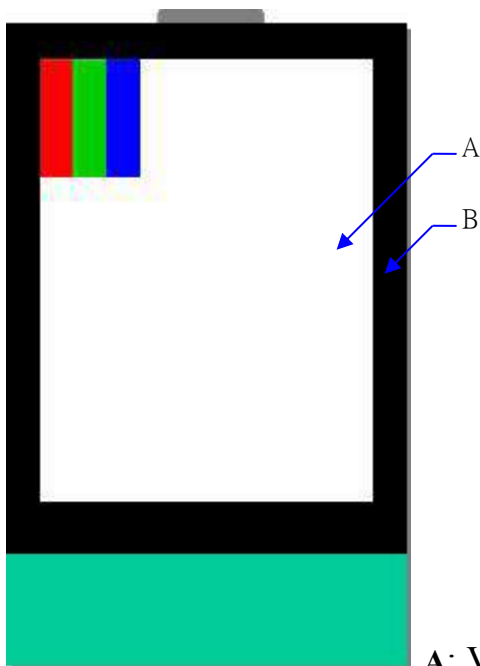
## 10.5 Standard of The Product Appearance Test

### 10.5.1 Manner of appearance test

- The test must be under 20W × 2 or 40W fluorescent light, and the distance of view must be at 30±5cm.
- When test the model of transmissive product must add the reflective plate.
- The test direction is base on around 10° of vertical line.
- Temperature: 25±5°C Humidity: 60±10%RH



- Definition of area:

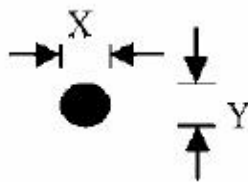
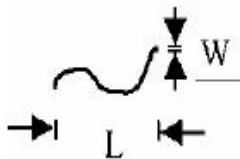


A: Viewing area B: Outside viewing area

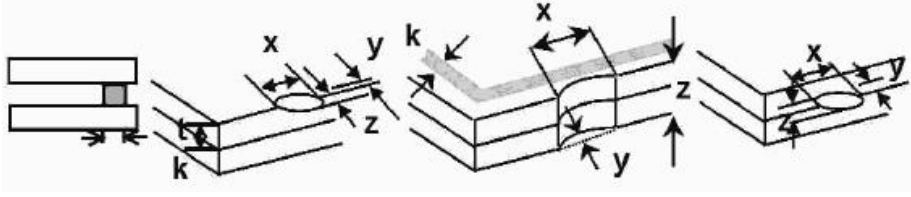
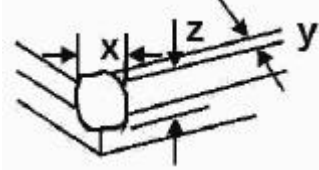
### **10.5.2 Basic principle**

- When the standard can not be described, AQL will be applied.
- The sample of the lowest acceptable quality level must be negotiated by both supplier and customer when any dispute happened.
- New item must be added on time when it is necessary.

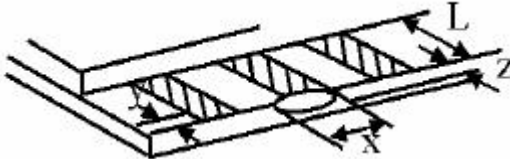
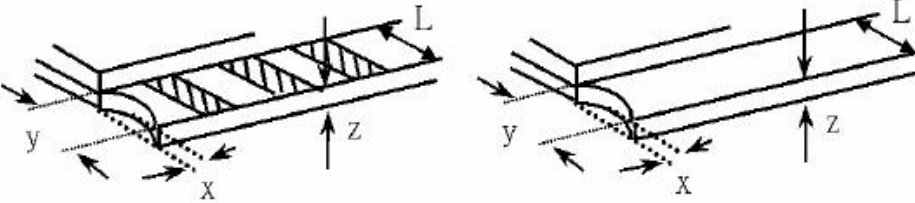
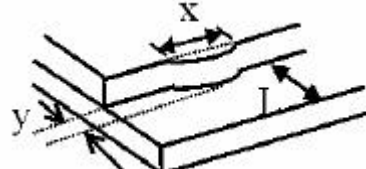
## 10.6 Inspection Specification

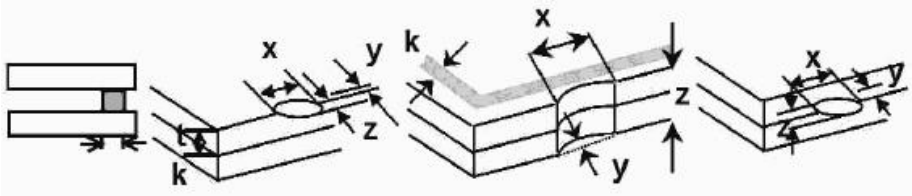
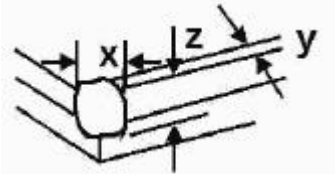
NO.	Item	Criterion	AQL												
01	Electrical Testing	1.1 Missing vertical, horizontal segment, segment contrast defect. 1.2 Missing character, dot or icon. 1.3 Display malfunction. 1.4 No function or no display. 1.5 Current consumption exceeds product specifications. 1.6 LCD viewing angle defect. 1.7 Mixed product types. 1.8 Flicker	0.65												
02	Black or White spots or Bright spots or Color spots on LCD (Display only)	2.1 White and black or color spots on display $\leq 0.25\text{mm}$ , no more than Five spots. 2.2 Densely spaced: No more than three spots within 3mm.	2.5												
03	LCD and Touch Panel black spots, white spots, contamination (non – display)	3.1 Round type: As following drawing $\Phi = (X+Y) / 2$  <table border="1" data-bbox="821 1086 1348 1332"> <thead> <tr> <th>Size(mm)</th> <th>Acceptable Q'ty</th> </tr> </thead> <tbody> <tr> <td><math>\Phi \leq 0.10</math></td> <td>Accept no dense</td> </tr> <tr> <td><math>0.10 &lt; \Phi \leq 0.20</math></td> <td>2</td> </tr> <tr> <td><math>0.20 &lt; \Phi \leq 0.25</math></td> <td>2</td> </tr> <tr> <td><math>0.25 &lt; \Phi \leq 0.30</math></td> <td>1</td> </tr> <tr> <td><math>0.30 &lt; \Phi</math></td> <td>0</td> </tr> </tbody> </table> <p>* Densely spaced: No more than two spots within 3mm.</p>	Size(mm)	Acceptable Q'ty	$\Phi \leq 0.10$	Accept no dense	$0.10 < \Phi \leq 0.20$	2	$0.20 < \Phi \leq 0.25$	2	$0.25 < \Phi \leq 0.30$	1	$0.30 < \Phi$	0	2.5
		Size(mm)	Acceptable Q'ty												
$\Phi \leq 0.10$	Accept no dense														
$0.10 < \Phi \leq 0.20$	2														
$0.20 < \Phi \leq 0.25$	2														
$0.25 < \Phi \leq 0.30$	1														
$0.30 < \Phi$	0														
3.2 Line type: (As following drawing)  <table border="1" data-bbox="726 1489 1348 1758"> <thead> <tr> <th>Length(mm)</th> <th>Width(mm)</th> <th>Acceptable Q'ty</th> </tr> </thead> <tbody> <tr> <td>---</td> <td><math>W \leq 0.02</math></td> <td>Accept no dense</td> </tr> <tr> <td><math>L \leq 3.0</math></td> <td><math>0.02 &lt; W \leq 0.05</math></td> <td rowspan="2">2</td> </tr> <tr> <td><math>L \leq 2.5</math></td> <td><math>0.03 &lt; W \leq 0.08</math></td> </tr> <tr> <td>---</td> <td><math>0.08 &lt; W</math></td> <td>Rejection</td> </tr> </tbody> </table> <p>* Densely spaced: No more than two lines within 3mm.</p>	Length(mm)	Width(mm)	Acceptable Q'ty	---	$W \leq 0.02$	Accept no dense	$L \leq 3.0$	$0.02 < W \leq 0.05$	2	$L \leq 2.5$	$0.03 < W \leq 0.08$	---	$0.08 < W$	Rejection	2.5
Length(mm)	Width(mm)	Acceptable Q'ty													
---	$W \leq 0.02$	Accept no dense													
$L \leq 3.0$	$0.02 < W \leq 0.05$	2													
$L \leq 2.5$	$0.03 < W \leq 0.08$														
---	$0.08 < W$	Rejection													

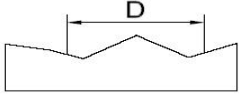
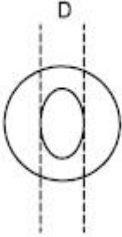


NO.	Item	Criterion		AQL	
04	Polarizer bubbles	If bubbles are visible, judge using black spot specifications, not easy to find, must check in specify direction	Size $\Phi$ (mm)	Acceptable Q'ty	2.5
			$\Phi \leq 0.20$	Accept no dense	
			$0.20 < \Phi \leq 0.50$	3	
			$0.50 < \Phi \leq 1.00$	2	
			$1.00 < \Phi$	0	
			Total Q'ty	3	
05	Scratches	Follow NO.3 -2 Line Type.			
06	Chipped glass	Symbols: x: Chip length    y: Chip width    z: Chip thickness k: Seal width    t: Glass thickness    a: LCD side length L: Electrode pad length 6.1 General glass chip: 6.1.1 Chip on panel surface and crack between panels:		2.5	
					
		z: Chip thickness	y: Chip width		x: Chip length
		$Z \leq 1/2t$	Not over viewing area		$x \leq 1/8a$
		$1/2t < z \leq 2t$	Not exceed 1/3k		$x \leq 1/8a$
		⊙ Unit: mm ⊙ If there are 2 or more chips, x is the total length of each chip			
6.1.2 Corner crack:					
					
z: Chip thickness	y: Chip width		x: Chip length		
$Z \leq 1/2t$	Not over viewing area		$x \leq 1/8a$		
$1/2t < z \leq 2t$	Not exceed 1/3k		$x \leq 1/8a$		
⊙ Unit: mm ⊙ If there are 2 or more chips, x is the total length of each chip					

NO.	Item	Criterion	AQL
08	Cracked glass	The LCD with extensive crack is not acceptable.	2.5
09	Backlight elements	9.1 Illumination source flickers when lit. 9.2 Spots or scratches that appear when lit must be judged. Using LCD spot, lines and contamination standards. 9.3 Backlight doesn't light or color is wrong.	2.5 2.5 0.65
10	Bezel	Bezel must comply with product specifications.	2.5
11	PCB、COB	11.1 COB seal may not have pinholes larger than 0.2mm or contamination. 11.2 COB seal surface may not have pinholes through to the IC. 11.3 The height of the COB should not exceed the height indicated in the assembly diagram. 11.4 There may not be more than 2mm of sealant outside the seal area on PCB. And there should be no more than three places. 11.5 Parts on PCB must be the same as on the production characteristic chart, There should be no wrong parts, missing parts or excess parts. 11.6 The jumper on the PCB should conform to the product characteristic chart.	2.5 2.5 2.5 2.5 0.65 0.65
12	FPC	12.1 FPC terminal damage $\cong$ 1/2 FPC terminal width and can not affect the function , we judge accept. 12.2 FPC alignment hole damage $\cong$ 1/2 alignment area and can not affect the function , we judge accept.	2.5 2.5
13	Soldering	13.1 No cold solder joints, missing solder connections, oxidation or icicle. 13.2 No short circuits in components on PCB or FPC.	2.5 0.65

NO.	Item	Criterion	AQL																
07	Glass crack	<p>Symbols:  x: Chip length    y: Chip width    z: Chip thickness  k: Seal width    t: Glass thickness    a: LCD side length  L: Electrode pad length</p> <p>7.2 Protrusion over terminal:  7.2.1 Chip on electrode pad:</p>  <table border="1" data-bbox="558 784 1236 929"> <tr> <td>y: Chip width</td> <td>x: Chip length</td> <td>z: Chip thickness</td> </tr> <tr> <td><math>y \leq 0.5\text{mm}</math></td> <td><math>x \leq 1/8a</math></td> <td><math>0 &lt; z \leq t</math></td> </tr> </table> <p>7.2.2  Non-conductive portion:</p>  <table border="1" data-bbox="558 1299 1236 1444"> <tr> <td>y: Chip width</td> <td>x: Chip length</td> <td>z: Chip thickness</td> </tr> <tr> <td><math>y \leq L</math></td> <td><math>x \leq 1/8a</math></td> <td><math>0 &lt; z \leq t</math></td> </tr> </table> <p>⊙ If there chipped area touches the ITO terminal, over 2/3 of the ITO must remain and be inspected according to electrode terminal specifications.  ⊙ If the product will be heat sealed by the customer, the alignment mark must not be damaged.</p> <p>7.2.3 Substrate protuberance and internal crack</p>  <table border="1" data-bbox="885 1769 1324 1915"> <tr> <td>y: width</td> <td>x: length</td> </tr> <tr> <td><math>y \leq 1/3L</math></td> <td><math>X \leq a</math></td> </tr> </table>	y: Chip width	x: Chip length	z: Chip thickness	$y \leq 0.5\text{mm}$	$x \leq 1/8a$	$0 < z \leq t$	y: Chip width	x: Chip length	z: Chip thickness	$y \leq L$	$x \leq 1/8a$	$0 < z \leq t$	y: width	x: length	$y \leq 1/3L$	$X \leq a$	2.5
y: Chip width	x: Chip length	z: Chip thickness																	
$y \leq 0.5\text{mm}$	$x \leq 1/8a$	$0 < z \leq t$																	
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y: width	x: length																		
$y \leq 1/3L$	$X \leq a$																		

NO.	Item	Criterion	AQL												
14	Touch Panel Chipped glass	<p>Symbols:  x: Chip length    y: Chip width    z: Chip thickness  k: Seal width    t: Touch Panel Total thickness    a: LCD side length  L: Electrode pad length</p> <p>14.1 General glass chip:  14.1.1 Chip on panel surface and crack between panels:</p>  <table border="1" data-bbox="451 790 1270 1008"> <tr> <td>z: Chip thickness</td> <td>y: Chip width</td> <td>x: Chip length</td> </tr> <tr> <td><math>Z \leq t</math></td> <td><math>\leq 1/2 k</math> and not over viewing area</td> <td><math>x \leq 1/8a</math></td> </tr> </table> <p>⊙ Unit: mm  ⊙ If there are 2 or more chips, x is the total length of each chip</p> <p>14.1.2 Corner crack:</p>  <table border="1" data-bbox="451 1384 1270 1601"> <tr> <td>z: Chip thickness</td> <td>y: Chip width</td> <td>x: Chip length</td> </tr> <tr> <td><math>z \leq t</math></td> <td><math>\leq 1/2 k</math> and not over viewing area</td> <td><math>x \leq 1/8a</math></td> </tr> </table> <p>⊙ Unit: mm  ⊙ If there are 2 or more chips, x is the total length of each chip</p>	z: Chip thickness	y: Chip width	x: Chip length	$Z \leq t$	$\leq 1/2 k$ and not over viewing area	$x \leq 1/8a$	z: Chip thickness	y: Chip width	x: Chip length	$z \leq t$	$\leq 1/2 k$ and not over viewing area	$x \leq 1/8a$	2.5
z: Chip thickness	y: Chip width	x: Chip length													
$Z \leq t$	$\leq 1/2 k$ and not over viewing area	$x \leq 1/8a$													
z: Chip thickness	y: Chip width	x: Chip length													
$z \leq t$	$\leq 1/2 k$ and not over viewing area	$x \leq 1/8a$													

NO.	Item	Criterion	AQL										
15	Touch Panel(Fish eye、dent and bubble on film)	<table border="1" data-bbox="456 371 987 577"> <thead> <tr> <th>SIZE(mm)</th> <th>Acceptable Q'ty</th> </tr> </thead> <tbody> <tr> <td><math>\Phi \leq 0.2</math></td> <td>Accept no dense</td> </tr> <tr> <td><math>0.2 &lt; D \leq 0.4</math></td> <td>5</td> </tr> <tr> <td><math>0.4 &lt; D \leq 0.5</math></td> <td>2</td> </tr> <tr> <td><math>0.5 &lt; D</math></td> <td>0</td> </tr> </tbody> </table>  	SIZE(mm)	Acceptable Q'ty	$\Phi \leq 0.2$	Accept no dense	$0.2 < D \leq 0.4$	5	$0.4 < D \leq 0.5$	2	$0.5 < D$	0	2.5
SIZE(mm)	Acceptable Q'ty												
$\Phi \leq 0.2$	Accept no dense												
$0.2 < D \leq 0.4$	5												
$0.4 < D \leq 0.5$	2												
$0.5 < D$	0												
16	Touch Panel Newton ring	Newton ring dimension $\leq 1/2$ touch panel area and not affect font and line distortion( $\leq 2.5\%$ ) , it is acceptable.	2.5										
17	Touch Panel Linearity	Less than 2.5% is acceptable.	2.5										
18	LCD Ripple	Touch the touch panel , can not see the LCD ripple. Pen: R 1.0mm silicon rubber. Operation Force: 80g	2.5										
19	General appearance	<p>19.1 Pin type must match type in specification sheet.</p> <p>19.2 LCD pin loose or missing pins.</p> <p>19.3 Product packaging must the same as specified on packaging specification sheet.</p> <p>19.4 Product dimension and structure must conform to product specification sheet.</p>	<p>0.65</p> <p>0.65</p> <p>0.65</p> <p>0.65</p>										

# 11. Handling Precaution

## 11.1 Handling of LCM

- Avoid external shock.
- Don't apply excessive force on the surface.
- Liquid in LCD is hazardous substance, do not lick or swallow. When the liquid is attaching to your hand, skin, cloth, etc., wash it thoroughly and immediately.
- Don't operate it above the absolute maximum rating.
- Don't disassemble the LCM.
- The operators should wear protections whenever he/she comes into contact with the module. Never touch any of the conductive parts such as the LSI pads, the copper leads on the PCB and the interface terminals with any parts of the human body.
- The modules should be kept in antistatic bags or other containers resistant to static for storage.
- The module is coated with a film to protect the display surface, be careful when peeling off this protective film since static electricity may be generated.

## 11.2 Storage

- Store it in an ambient temperature of  $25\pm 10^{\circ}\text{C}$ , and in a relative humidity of  $50\pm 10\%\text{RH}$ . Don't expose to sunlight or fluorescent light.
- Store it in a clean environment, free from dust, active gas, and solvent.
- Store it in anti-static electricity container.
- Store it without any physical load.

## 11.3 Soldering

- Use only soldering irons with proper grounding and no leakage.
- Iron: no higher than  $280\pm 10^{\circ}\text{C}$  and less than 3 sec during hand soldering.
- Rewiring: no more than 2 times.

# 12. Packing Method

----TBD