RAiO

RA8808

128x64 Driver

for Dot Matrix LCD

Specification

Version 1.2

December 15, 2009

RAiO Technology Inc.

Update History		
Version	**Date**	**Description**
1.0	March 26, 2009	Preliminary version
1.1	October 23, 2009	Update Section 6-3-3 LCD Driver
1.2	December 15, 2009	1. Add Section 6-3-4 Temperature Compensation. 2. Updata Figure 8-2、Figure 8-3.

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1. Overview

The RA8808 is a LCD driver LSI with 128(Segment) x 64(Common) driver output for dot matrix liquid crystal graphic display systems. This device consists of the display RAM,128-bit segment drivers, 64-bit common drivers and decoder logic. It has the internal display RAM for storing the display data transferred from an 8-bit 8080/6800 micro controller or 3-wire-SPI/IIC controller and generates the dot matrix liquid crystal driving signals corresponding to stored data.

2. Features

- Dot matrix LCD segment driver with 128 channel output, and common driver with 64 channel output
- Internal timing generator circuit for dynamic display
- Selection of master/slave mode for combine two RA8808 controller to support 256x64 dot Matrix
- Applicable LCD common duty: 1/48, 1/64
- Support 6800/8080 8-bit parallel MPU interface
- Support 3-wires SPI and IIC serial MPU interface.
- Two 512 bytes (4096-bits) Display SRAM
- LCD driving voltage: 8V ~17V
- Built-in 2X~4X Voltage Booster and Voltage Follower
- Power supply voltage: +2.7V ~ 5.5V
- High voltage CMOS process
- Bare gold bump chip available

3. Pin Configuration

3-1 Block Diagram

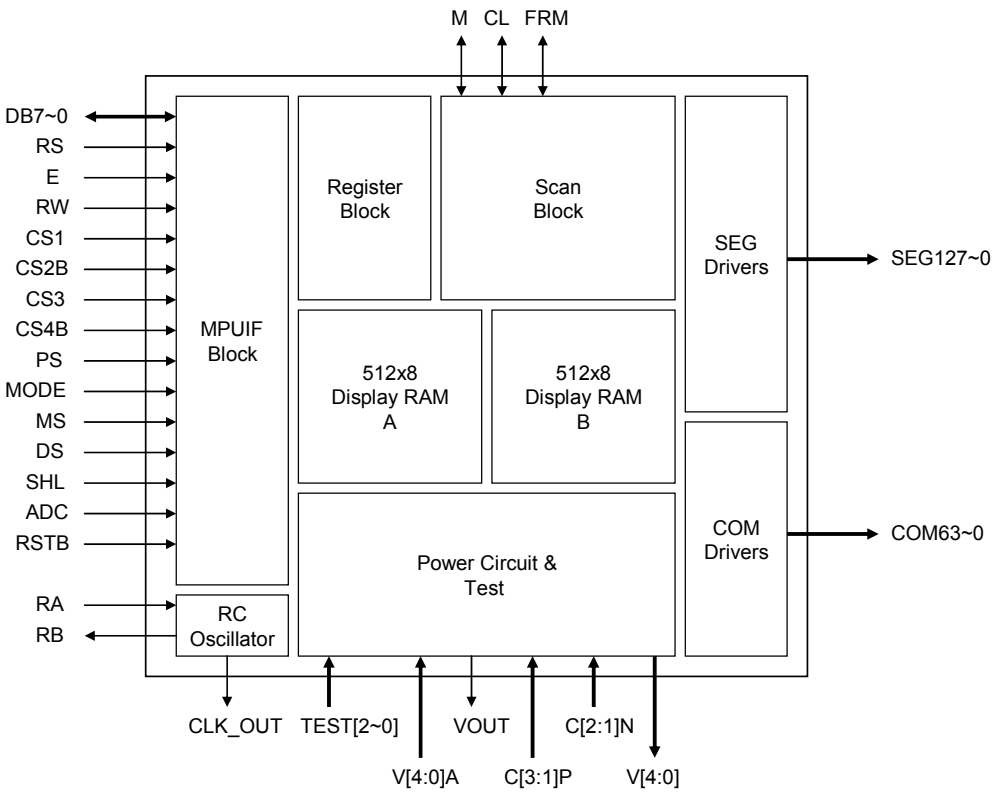


Figure 3-1 : RA8808 Block Diagram

3-2 PAD Diagram

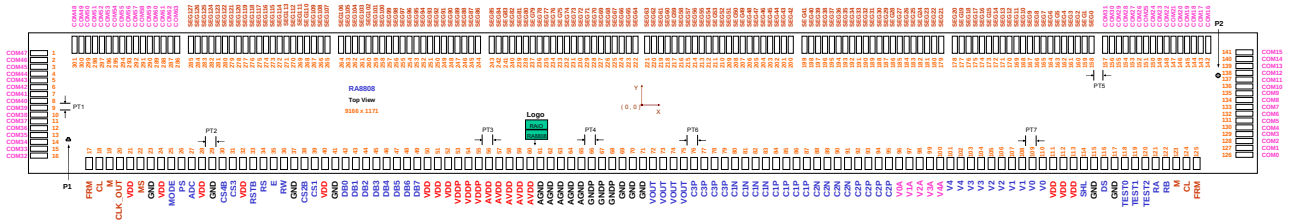
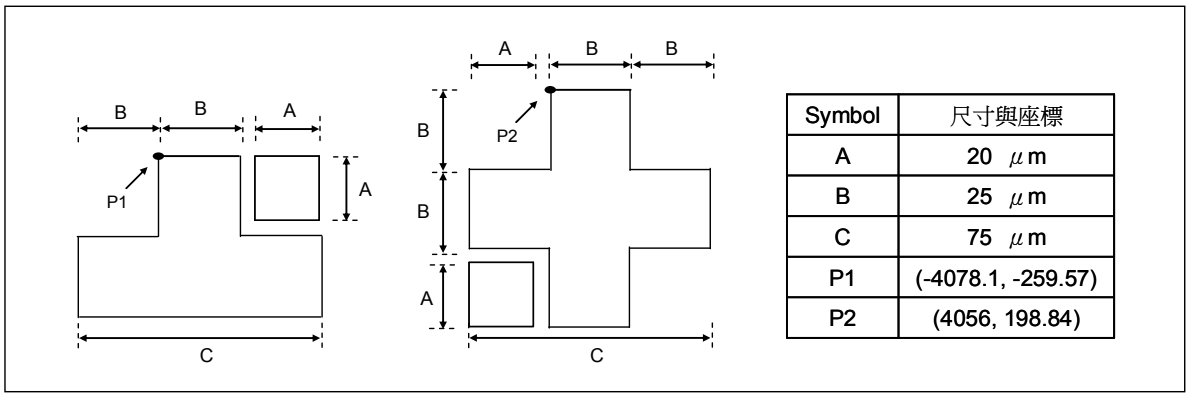


Figure 3-2 : RA8808 PAD Diagram

Table 3-1 : Bump Size and Pitch

Chip Size	9166 μm x 1171 μm	
Bump Size	PAD 1~16, PAD 126~141 (COM Pads)	66 μm x 22 μm
	PAD 142~301 (SEG/COM Pads)	22 μm x 66 μm
	PAD 17~125 (MCU/Power Pads)	37 μm x 46 μm
Bump Pitch	PT1 : PAD 1~16, PAD 126~141, PAD 142~157, PAD 158~178, PAD 179~199, PAD 200~221, PAD 222~243 , PAD 244~264, PAD 265~285, PAD 286~301	48 μm
	PT2 : PAD 17~55, PAD 56~65, PAD 66~75, PAD 76~108, PAD 76~108, PAD 109~125	72 μm
	PT3 : PAD 55~56	76.6 μm
	PT4: PAD 65~66	77.02 μm
	PT5: PAD 157~158, PAD 178~179, PAD 199~200, PAD 221~222, PAD 243~244, PAD 264~265, PAD 285~286	96 μm
	PT6: PAD 75~76	102.3 μm
	PT7: PAD 108~109	112 μm
Bump Height	15 ± 3 μm	



Symbol	尺寸與座標
A	20 μm
B	25 μm
C	75 μm
P1	(-4078.1, -259.57)
P2	(4056, 198.84)

Figure 3-3 : Fixed Point Dimension

3-3 PAD Center Coordinates

Pad No.	Pad Name	X	Y
1	COM47	-4439.51	384.62
2	COM46	-4439.51	336.62
3	COM45	-4439.51	288.62
4	COM44	-4439.51	240.62
5	COM43	-4439.51	192.62
6	COM42	-4439.51	144.62
7	COM41	-4439.51	96.62
8	COM40	-4439.51	48.62
9	COM39	-4439.51	0.62
10	COM38	-4439.51	-47.38
11	COM37	-4439.51	-95.38
12	COM36	-4439.51	-143.38
13	COM35	-4439.51	-191.38
14	COM34	-4439.51	-239.38
15	COM33	-4439.51	-287.38
16	COM32	-4439.51	-335.38
17	FRM	-3928	-464.37
18	CL	-3856	-464.37
19	M	-3784	-464.37
20	CLK_OUT	-3712	-464.37
21	VDD	-3640	-464.37
22	MS	-3568	-464.37
23	GND	-3496	-464.37
24	VDD	-3424	-464.37
25	MODE	-3352	-464.37
26	PS	-3280	-464.37
27	ADC	-3208	-464.37
28	VDD	-3136	-464.37
29	GND	-3064	-464.37
30	CS4B	-2992	-464.37
31	CS3	-2920	-464.37

Pad No.	Pad Name	X	Y
32	VDD	-2848	-464.37
33	RSTB	-2776	-464.37
34	RS	-2704	-464.37
35	E	-2632	-464.37
36	RW	-2560	-464.37
37	GND	-2488	-464.37
38	CS2B	-2416	-464.37
39	CS1	-2344	-464.37
40	VDD	-2272	-464.37
41	GND	-2200	-464.37
42	DB0	-2128	-464.37
43	DB1	-2056	-464.37
44	DB2	-1984	-464.37
45	DB3	-1912	-464.37
46	DB4	-1840	-464.37
47	DB5	-1768	-464.37
48	DB6	-1696	-464.37
49	DB7	-1624	-464.37
50	VDD	-1552	-464.37
51	VDD	-1480	-464.37
52	VDD	-1408	-464.37
53	VDDP	-1336	-464.37
54	VDDP	-1264	-464.37
55	VDDP	-1192	-464.37
56	AVDD	-1115.4	-464.37
57	AVDD	-1043.4	-464.37
58	AVDD	-971.4	-464.37
59	AVDD	-899.4	-464.37
60	AVDD	-827.4	-464.37
61	AGND	-755.4	-464.37
62	AGND	-683.4	-464.37

Pad No.	Pad Name	X	Y
63	AGND	-611.4	-464.37
64	AGND	-539.4	-464.37
65	AGND	-467.4	-464.37
66	GNDP	-390.38	-464.37
67	GNDP	-318.38	-464.37
68	GNDP	-246.38	-464.37
69	GND	-174.38	-464.37
70	GND	-102.38	-464.37
71	GND	-30.38	-464.37
72	VOUT	41.62	-464.37
73	VOUT	113.62	-464.37
74	VOUT	185.62	-464.37
75	VOUT	257.62	-464.37
76	C3P	359.92	-464.37
77	C3P	431.92	-464.37
78	C3P	503.92	-464.37
79	C3P	575.92	-464.37
80	C1N	647.92	-464.37
81	C1N	719.92	-464.37
82	C1N	791.92	-464.37
83	C1N	863.92	-464.37
84	C1P	935.92	-464.37
85	C1P	1007.92	-464.37
86	C1P	1079.92	-464.37
87	C1P	1151.92	-464.37
88	C2N	1223.92	-464.37
89	C2N	1295.92	-464.37
90	C2N	1367.92	-464.37
91	C2N	1439.92	-464.37
92	C2P	1511.92	-464.37
93	C2P	1583.92	-464.37

Pad No.	Pad Name	X	Y
94	C2P	1655.92	-464.37
95	C2P	1727.92	-464.37
96	V0A	1799.92	-464.37
97	V1A	1871.92	-464.37
98	V2A	1943.92	-464.37
99	V3A	2015.92	-464.37
100	V4A	2087.92	-464.37
101	V4	2159.92	-464.37
102	V4	2231.92	-464.37
103	V3	2303.92	-464.37
104	V3	2375.92	-464.37
105	V2	2447.92	-464.37
106	V2	2519.92	-464.37
107	V1	2591.92	-464.37
108	V1	2663.92	-464.37
109	V0	2775.92	-464.37
110	V0	2847.92	-464.37
111	VDD	2919.92	-464.37
112	VDD	2991.92	-464.37
113	VDD	3063.92	-464.37
114	SHL	3135.92	-464.37
115	GND	3207.92	-464.37
116	DS	3279.92	-464.37
117	GND	3351.92	-464.37
118	TEST0	3423.92	-464.37
119	TEST1	3495.92	-464.37
120	TEST2	3567.92	-464.37
121	RA	3639.92	-464.37
122	RB	3711.92	-464.37
123	M	3783.92	-464.37
124	CL	3855.92	-464.37

Pad No.	Pad Name	X	Y
125	FRM	3927.92	-464.37
126	COM0	4439.51	-335.38
127	COM1	4439.51	-287.38
128	COM2	4439.51	-239.38
129	COM3	4439.51	-191.38
130	COM4	4439.51	-143.38
131	COM5	4439.51	-95.38
132	COM6	4439.51	-47.38
133	COM7	4439.51	0.62
134	COM8	4439.51	48.62
135	COM9	4439.51	96.62
136	COM10	4439.51	144.62
137	COM11	4439.51	192.62
138	COM12	4439.51	240.62
139	COM13	4439.51	288.62
140	COM14	4439.51	336.62
141	COM15	4439.51	384.62
142	COM16	3984	442.07
143	COM17	3936	442.07
144	COM18	3888	442.07
145	COM19	3840	442.07
146	COM20	3792	442.07
147	COM21	3744	442.07
148	COM22	3696	442.07
149	COM23	3648	442.07
150	COM24	3600	442.07
151	COM25	3552	442.07
152	COM26	3504	442.07
153	COM27	3456	442.07
154	COM28	3408	442.07
155	COM29	3360	442.07

Pad No.	Pad Name	X	Y
156	COM30	3312	442.07
157	COM31	3264	442.07
158	SEG0	3168	442.07
159	SEG1	3120	442.07
160	SEG2	3072	442.07
161	SEG3	3024	442.07
162	SEG4	2976	442.07
163	SEG5	2928	442.07
164	SEG6	2880	442.07
165	SEG7	2832	442.07
166	SEG8	2784	442.07
167	SEG9	2736	442.07
168	SEG10	2688	442.07
169	SEG11	2640	442.07
170	SEG12	2592	442.07
171	SEG13	2544	442.07
172	SEG14	2496	442.07
173	SEG15	2448	442.07
174	SEG16	2400	442.07
175	SEG17	2352	442.07
176	SEG18	2304	442.07
177	SEG19	2256	442.07
178	SEG20	2208	442.07
179	SEG21	2112	442.07
180	SEG22	2064	442.07
181	SEG23	2016	442.07
182	SEG24	1968	442.07
183	SEG25	1920	442.07
184	SEG26	1872	442.07
185	SEG27	1824	442.07
186	SEG28	1776	442.07

Pad No.	Pad Name	X	Y
187	SEG29	1728	442.07
188	SEG30	1680	442.07
189	SEG31	1632	442.07
190	SEG32	1584	442.07
191	SEG33	1536	442.07
192	SEG34	1488	442.07
193	SEG35	1440	442.07
194	SEG36	1392	442.07
195	SEG37	1344	442.07
196	SEG38	1296	442.07
197	SEG39	1248	442.07
198	SEG40	1200	442.07
199	SEG41	1152	442.07
200	SEG42	1056	442.07
201	SEG43	1008	442.07
202	SEG44	960	442.07
203	SEG45	912	442.07
204	SEG46	864	442.07
205	SEG47	816	442.07
206	SEG48	768	442.07
207	SEG49	720	442.07
208	SEG50	672	442.07
209	SEG51	624	442.07
210	SEG52	576	442.07
211	SEG53	528	442.07
212	SEG54	480	442.07
213	SEG55	432	442.07
214	SEG56	384	442.07
215	SEG57	336	442.07
216	SEG58	288	442.07
217	SEG59	240	442.07

Pad No.	Pad Name	X	Y
218	SEG60	192	442.07
219	SEG61	144	442.07
220	SEG62	96	442.07
221	SEG63	48	442.07
222	SEG64	-48	442.07
223	SEG65	-96	442.07
224	SEG66	-144	442.07
225	SEG67	-192	442.07
226	SEG68	-240	442.07
227	SEG69	-288	442.07
228	SEG70	-336	442.07
229	SEG71	-384	442.07
230	SEG72	-432	442.07
231	SEG73	-480	442.07
232	SEG74	-528	442.07
233	SEG75	-576	442.07
234	SEG76	-624	442.07
235	SEG77	-672	442.07
236	SEG78	-720	442.07
237	SEG79	-768	442.07
238	SEG80	-816	442.07
239	SEG81	-864	442.07
240	SEG82	-912	442.07
241	SEG83	-960	442.07
242	SEG84	-1008	442.07
243	SEG85	-1056	442.07
244	SEG86	-1152	442.07
245	SEG87	-1200	442.07
246	SEG88	-1248	442.07
247	SEG89	-1296	442.07
248	SEG90	-1344	442.07

Pad No.	Pad Name	X	Y
249	SEG91	-1392	442.07
250	SEG92	-1440	442.07
251	SEG93	-1488	442.07
252	SEG94	-1536	442.07
253	SEG95	-1584	442.07
254	SEG96	-1632	442.07
255	SEG97	-1680	442.07
256	SEG98	-1728	442.07
257	SEG99	-1776	442.07
258	SEG100	-1824	442.07
259	SEG101	-1872	442.07
260	SEG102	-1920	442.07
261	SEG103	-1968	442.07
262	SEG104	-2016	442.07
263	SEG105	-2064	442.07
264	SEG106	-2112	442.07
265	SEG107	-2208	442.07
266	SEG108	-2256	442.07
267	SEG109	-2304	442.07
268	SEG110	-2352	442.07
269	SEG111	-2400	442.07
270	SEG112	-2448	442.07
271	SEG113	-2496	442.07
272	SEG114	-2544	442.07
273	SEG115	-2592	442.07
274	SEG116	-2640	442.07
275	SEG117	-2688	442.07
276	SEG118	-2736	442.07
277	SEG119	-2784	442.07
278	SEG120	-2832	442.07
279	SEG121	-2880	442.07

Pad No.	Pad Name	X	Y
280	SEG122	-2928	442.07
281	SEG123	-2976	442.07
282	SEG124	-3024	442.07
283	SEG125	-3072	442.07
284	SEG126	-3120	442.07
285	SEG127	-3168	442.07
286	COM63	-3264	442.07
287	COM62	-3312	442.07
288	COM61	-3360	442.07
289	COM60	-3408	442.07
290	COM59	-3456	442.07
291	COM58	-3504	442.07
292	COM57	-3552	442.07
293	COM56	-3600	442.07
294	COM55	-3648	442.07
295	COM54	-3696	442.07
296	COM53	-3744	442.07
297	COM52	-3792	442.07
298	COM51	-3840	442.07
299	COM50	-3888	442.07
300	COM49	-3936	442.07
301	COM48	-3984	442.07

4. Pin Description

4-1 MPU Interface

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>DB0~DB7</td><td>I/O</td><td>
In Parallel Mode :
Data Bus
These are data bus for data transfer between MPU(6800/8080) and RA8808.
In Serial Mode :
<table>
<tr><th>Pin</th><th>Description</th></tr>
<tr><td>DB7</td><td rowspan="2">These pins are not used and must be connected to low.</td></tr>
<tr><td>DB6</td></tr>
<tr><td>DB5</td><td rowspan="3">In IIC Interface :
These pins are used as the IIC device address input. (SA[2:0])
In SPI Interface :
These pins are not used and must be connected to high or low.</td></tr>
<tr><td>DB4</td></tr>
<tr><td>DB3</td></tr>
<tr><td>DB2</td><td>In IIC Interface :
This pin is not used and must be connected to low.
In SPI Interface :
This pin is used as Chip selection, active low. (ZCS)</td></tr>
<tr><td>DB1</td><td>In IIC Interface :
This pin is used as Bi-direction serial Data.(SDA)
In SPI Interface :
This pin is used as Bi-direction serial Data.(SDA)</td></tr>
<tr><td>DB0</td><td>In IIC Interface :
This pin is used as serial clock.(SCL)
In SPI Interface :
This pin is used as serial clock.(SCK)</td></tr>
</table>
</td></tr>
<tr><td>E</td><td>I</td><td>
In Parallel Mode :
Enable or Read Control
When use 6800 series interface, this pin is used as Enable, active high.
When use 8080 series interface, this pin is used as data read, active low.
In Serial Mode :
This pin is not used and must be connected to low.
</td></tr>
<tr><td>RW</td><td>I</td><td>
In Parallel Mode :
Read-Write Control or Write Control
When use 6800 series interface, this pin is used as data read/write control. Active high for read and active low for write.
When use 8080 series interface, this pin is used as data write, active low.
In Serial Mode :
This pin is not used and must be connected to low.
</td></tr>
<tr><td>RS</td><td>I</td><td>
In Parallel Mode :
Data or Instruction
RS = H ➔ DB0~DB7 : Display RAM data
RS = L ➔ DB0~DB7 : Instruction data
In Serial Mode :
This pin is not used and must be connected to low.
</td></tr>
</table>

<table>
<tr><td>CS1
CS2B</td><td>I</td><td>In Parallel Mode :
Chip selection for left side (Note *)
In order to interface left side data for input or output, the terminals have to be
CS1 = H, CS2B = L.
In Serial Mode :
These pins are not used and must be connected to high or low.</td></tr>
<tr><td>CS3
CS4B</td><td>I</td><td>In Parallel Mode :
Chip selection for right side (Note *)
In order to interface right side data for input or output, the terminals have to be
CS3 = H, CS4B = L.
In Serial Mode :
These pins are not used and must be connected to high or low.</td></tr>
<tr><td>RSTB</td><td>I</td><td>Reset Signal
When RSTB = L,
_ON/OFF register becomes set by 0. (display off)
_Display start line register becomes set by 0.(Z-address 0 set, display from line 0)
After releasing reset, this condition can be changed only by instruction.</td></tr>
<tr><td>PS</td><td>I</td><td>Parallel/Serial MPU Interface Selection
<table>
<tr><th>PS</th><th>Parallel/Serial</th></tr>
<tr><td>H</td><td>Parallel</td></tr>
<tr><td>L</td><td>Serial</td></tr>
</table></td></tr>
<tr><td>MODE</td><td>I</td><td>MPU Interface Selection(Combine with PS)
<table>
<tr><th>PS</th><th>MODE</th><th>MPU Interface</th></tr>
<tr><td>H</td><td>H</td><td>6800 series</td></tr>
<tr><td>H</td><td>L</td><td>8080 series</td></tr>
<tr><td>L</td><td>H</td><td>3-wire SPI</td></tr>
<tr><td>L</td><td>L</td><td>IIC</td></tr>
</table></td></tr>
</table>

Note :

Because the two sides are independent for display the data, they must have their own chip selections. Please refer to the figure below :

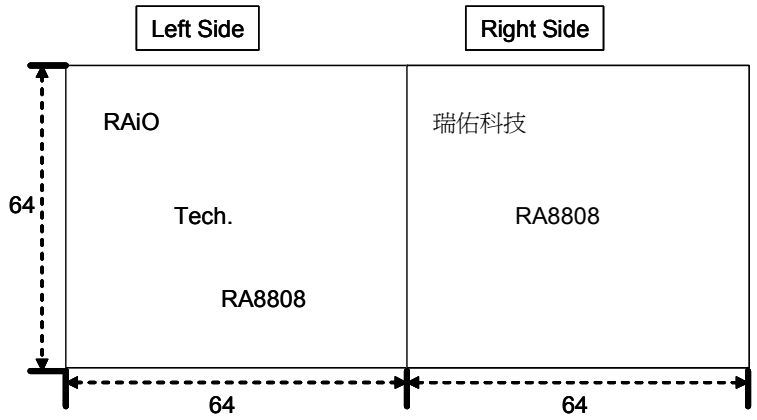


Figure 4-1

4-2 LCD Panel Interface

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>SEG0~
SEG127</td><td>O</td><td>LCD Segment Driver Output
Display RAM data 1 : On, Display RAM data 0 : Off
Relation of display RAM & M :
<table>
<tr><th>M</th><th>Data</th><th>Output Level</th></tr>
<tr><td>L</td><td>L</td><td>V2</td></tr>
<tr><td>L</td><td>H</td><td>V0</td></tr>
<tr><td>H</td><td>L</td><td>V3</td></tr>
<tr><td>H</td><td>H</td><td>GND</td></tr>
</table></td></tr>
<tr><td>COM0~
COM63</td><td>O</td><td>Common Signal Output for LCD Driving
Relation of common signal & M :
<table>
<tr><th>M</th><th>Common Signal</th><th>Output Level</th></tr>
<tr><td>L</td><td>L</td><td>V1</td></tr>
<tr><td>L</td><td>H</td><td>GND</td></tr>
<tr><td>H</td><td>L</td><td>V4</td></tr>
<tr><td>H</td><td>H</td><td>V0</td></tr>
</table></td></tr>
<tr><td>M</td><td>I/O</td><td>Alternating Signal Input for LCD Driving.
The input/output selection is determined by MS.</td></tr>
<tr><td>CL</td><td>I/O</td><td>Display Synchronous Signal
Display data is latched at rising time of the CL signal and increments the Z-address counter at CL falling time.
The input/output selection is determined by MS.</td></tr>
<tr><td>FRM</td><td>I/O</td><td>Synchronous Control Signal
Presets the 6-bit Z counter and synchronizes the common signal with the frame signal when the frame signal becomes high.
The input/output selection is determined by MS.</td></tr>
<tr><td>MS</td><td>I</td><td>Master/Slave Mode Selection
<table>
<tr><th>MS</th><th>Master/Slave Mode</th></tr>
<tr><td>H</td><td>Master</td></tr>
<tr><td>L</td><td>Slave</td></tr>
</table>
When in Master mode, M, CL, FRM are output pins.
When in Slave mode, M, CL, FRM are input pins. (Note *)</td></tr>
</table>

Note :

Because RA8808 support two RA8808 chips combination for display, it can support maximum display range 256x64. The combination condition just refer to the figure below :

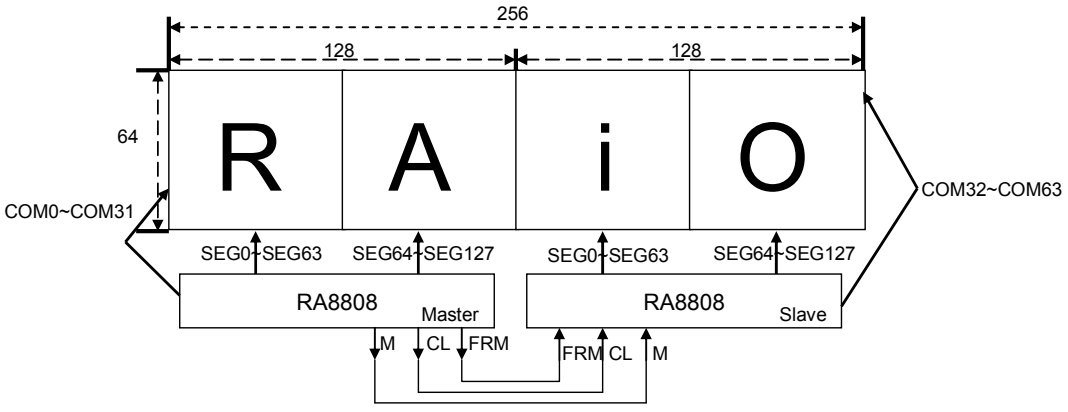
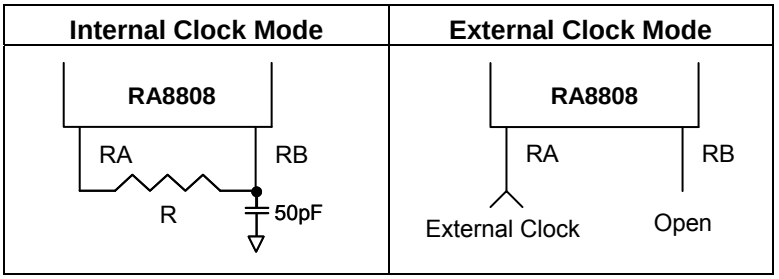


Figure 4-2

4-3 Clock

Pin Name	I/O	Description
RA	I	In internal clock mode, this pin connects to external resistor for RC circuit. In external clock mode, this pin is an input of external clock. 
RB	O	In internal clock mode, this pin connects to external resistor for RC circuit. In external clock mode, this pin must keep floating.
CLK_OUT	O	Internal system clock output for cascade application or others for user.

4-4 Power

Pin Name	I/O	Description
VOUT	O	**Regulator Voltage Output**
VDD VDDP	P	**Digital Power**
GND GNDP	P	**Digital Ground**
AVDD	P	**Analog Power**
AGND	P	**Analog Ground**
C1N C1P	I	**Capacitor Input** These are used to connect a capacitor for internal Booster.
C2N C2P	I	**Capacitor Input** These are used to connect a capacitor for internal Booster.
C3P	I	**Capacitor Input** These are used to connect a capacitor for internal Booster.
V0A~V4A	I	**Voltage Input**
V0~V4	O	**Voltage Source of LCD Driver** The relationship of the power is V0 > V1 > V2 > V3 > V4 > GND

4-5 MISC

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>ADC</td><td>I</td><td>Selection of Segment Data Direction
<table><tr><th>ADC</th><th>Common Data Shift Direction</th></tr><tr><td>H</td><td>SEG0 ➔ SEG1 … ➔SEG127</td></tr><tr><td>L</td><td>SEG127 ➔ SEG126 … ➔ SEG0</td></tr></table></td></tr>
<tr><td>SHL</td><td>I</td><td>Selection of Common Data Shift Direction
<table><tr><th>SHL</th><th>Common Data Shift Direction</th></tr><tr><td>H</td><td>COM0 ➔ COM1 … ➔COM63</td></tr><tr><td>L</td><td>COM63 ➔ COM62 … ➔ COM0</td></tr></table></td></tr>
<tr><td>DS</td><td>I</td><td>Selection of Display Duty
<table><tr><th>DS</th><th>Duty</th></tr><tr><td>H</td><td>1/64</td></tr><tr><td>L</td><td>1/48</td></tr></table></td></tr>
<tr><td>TEST0
TEST1
TEST2</td><td>I</td><td>These pins must contact to GND in normal mode.</td></tr>
</table>

5. Electrical Characteristics

5-1 Maximum Absolute Limit

Table 5-1

Characteristic	Symbol	Value	Unit	Note
Operation voltage	VDD	-0.3 - +7.0	V	
Driver supply voltage	VB	-0.3 - VDD+0.3	V	
	VLCD	8~17	V	
Operation temperature	VOPR	-30 - +85	°C	
Storage temperature	VSTG	-55 - +125	°C	

5-2 DC Characteristics

Table 5-2

(VDD = +5V / +3.3V ± 10%, VSS = 0V, Ta = -30 to +80°C)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit	Note
Input high voltage	V_{IH1}	–	0.7_{VDD}	–	V_{DD}	V	(1)
	V_{IH2}	–	$0.55V_{DD}$	–	V_{DD}	V	(2)
Input low voltage	V_{IL1}	–	0	–	$0.3V_{DD}$	V	(1)
	V_{IL2}	–	0	–	$0.2V_{DD}$	V	(2)
Output high voltage	V_{OH}	I_{OH} = 1.2mA	$0.8V_{DD}$	–	–	V	
Output low voltage	V_{OL}	I_{OL} = 1.6mA	–	–	$0.2V_{DD}$	V	
Input leakage current	I_{LKG}	$V_{IN} = V_{SS} \sim V_{DD}$	-1.0	–	1.0	uA	(3)
Operating current	I_{DD1}	Display with display off	–	1.1	--	mA	(4)
	I_{DD2}	Static display with data	–	1.3	--	mA	(4)
On resistance	R_{ON}	V_{DD}-V_{SS} = 15V I_{LOAD} = ± 0.1mA	–	–	1.5	kΩ	(5)

Note :

1. RSTB.
2. CL, FRM, M, MODE, PS, ADC, SHL, DS, CS1, CS2B, CS3, CS4B, E, RW, RS, DB0 - DB7
3. Except M, CL, FRM
4. VDD= 5V, 128x64 COG module, FCLK = 448kHz, frame frequency = 72.6Hz, booster setting with 4X, V0/V1/V2/V3/V4 = 8.80 / 7.74 / 6.77 / 1.94 / 0.97, display data = 0x55.
5. V0 > V1 = V0 - 1/9 (V0-V_{SS}) > V2 = V0 - 2/9 (V0-V_{SS}) > V3 = V_{SS} + 2/9 (V0-V_{SS}) > V4 = V0 + 1/9 (V0- V_{SS}) > V_{SS}

5-3 AC Characteristics

Table 5-3 : 6800 Interface

Description	Symbol	Min	Typ	Max	Unit
E cycle	tC	1000	–	–	ns
E high level width	tWH	450	–	–	ns
E low level width	tWL	450	–	–	ns
E rise time	tR	–	–	25	ns
E fall time	tF	–	–	25	ns
Address set-up time	tASU	140	–	–	ns
Address hold time	tAH	10	–	–	ns
Data set-up time	tDSU	200	–	–	ns
Data delay time	tD	–	–	320	ns
Data hold time (write)	tDHW	10	–	–	ns
Data hold time (read)	tDHR	20	–	–	ns

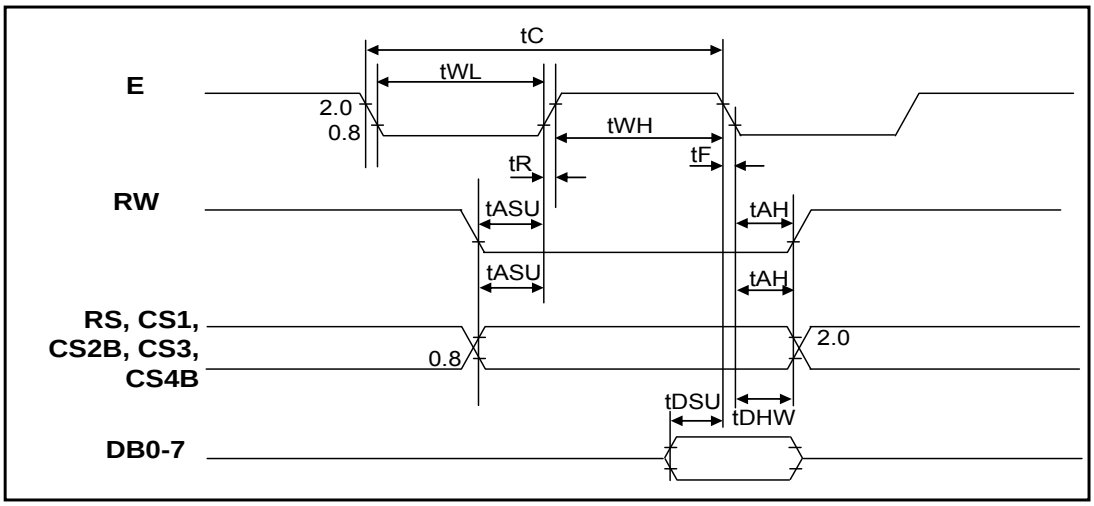


Figure 5-1 : MPU 6800 Write Timing

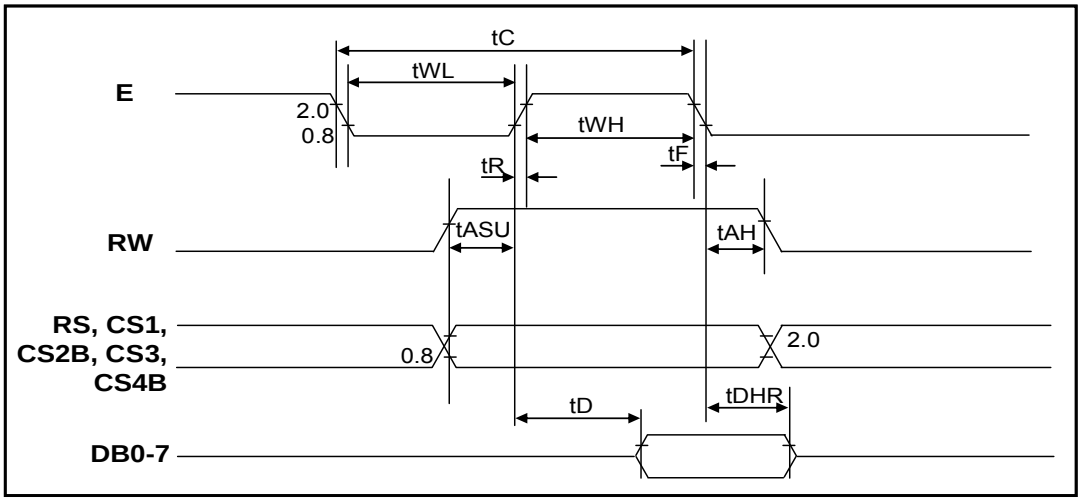


Figure 5-2 : MPU 6800 Read Timing

Table 5-4 : 8080 Interface

Description	Symbol	Rating		Unit	Condition
		Min.	Max.		
Cycle time	tCYC8	1000	--	ns	tc = one system clock period
Strobe Pulse width	tCC8	50	--	ns	
Address setup time	tAS8	0	--	ns	
Address hold time	tAH8	20	--	ns	
Data setup time	tDS8	30	--	ns	
Data hold time	tDH8	20	--	ns	
Data output access time	tACC8	0	20	ns	
Data output hold time	tOH8	0	10	ns	

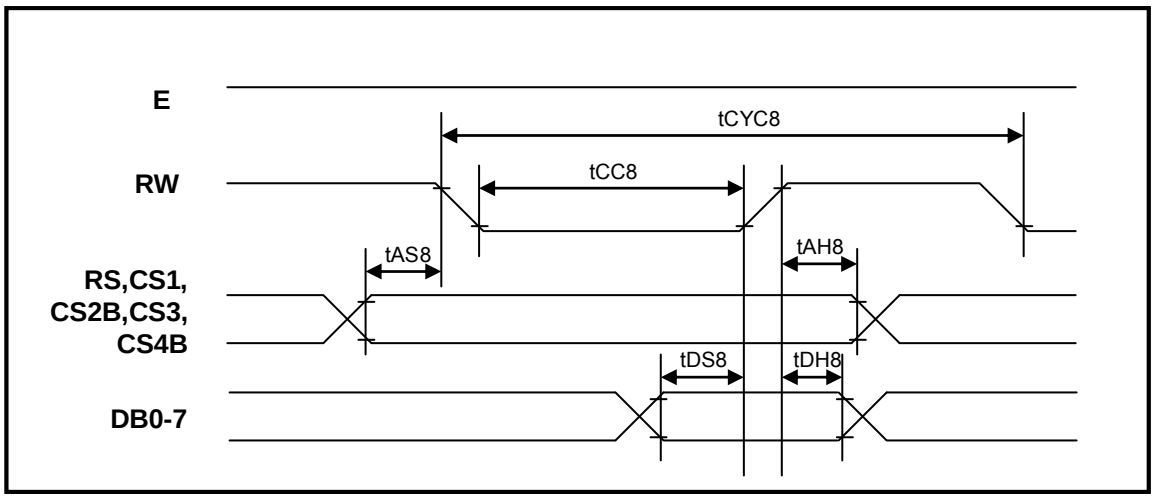


Figure 5-3 : MPU 8080 Write Timing

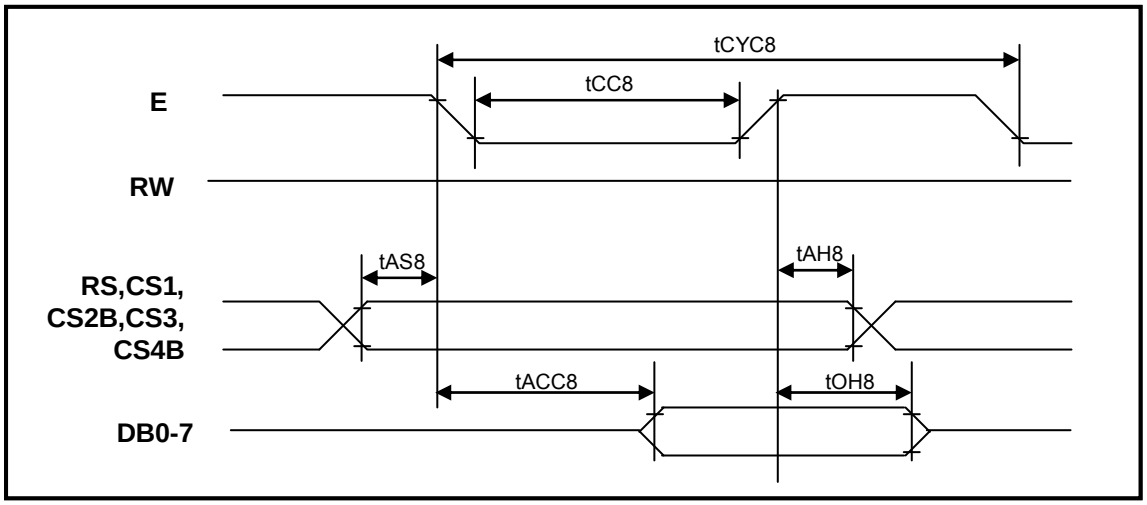


Figure 5-4 : MPU 8080 Read Timing

Table 5-5 : 3-Wire SPI Interface

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Access Time	ZCS	tCYC3		3.6		ms
ZCS Setup Time		tCSH3		20		ns
Clock Low Pulse Width	SCK	tCKL3		100		
Clock High Pulse Width		tCKH3		100		
Data Setup Time	SDA	tDS3		20		
Data Hold Time		tDH3		10		

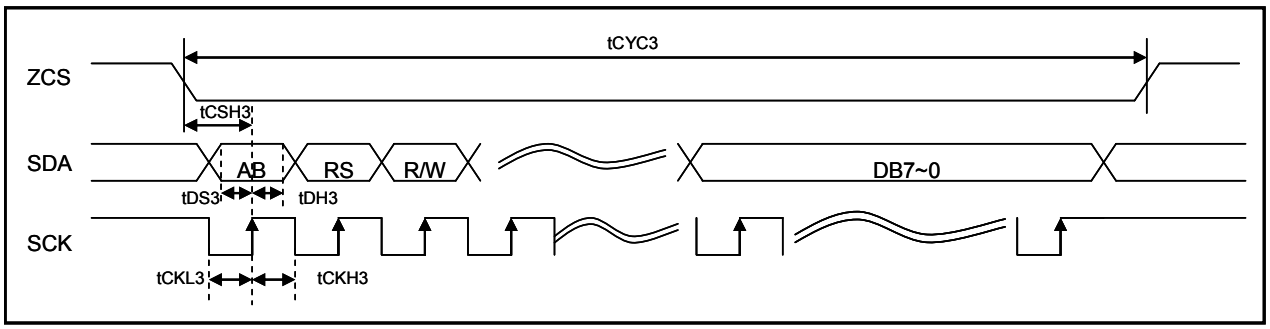


Figure 5-5 : 3-Wire SPI Timing

Table 5-6 : IIC Interface

Item	Signal	Symbol	Rating		Unit
			Min.	Max.	
SCL Clock Frequency	SCL	fSCL	100	400	KHz
Bus Free Time Between STOP and START	SCL/SDA	tBUF	1	-	μs
Low Period of SCL Clock	SCL	tLOW	200	-	ns
High Period of SCL Clock	SCL	tHIGH	200	-	ns
Data Setup Time	SCL/SDA	tDSIIC	100	-	ns
Data Hold Time	SCL/SDA	tDHIIC	100	-	ns

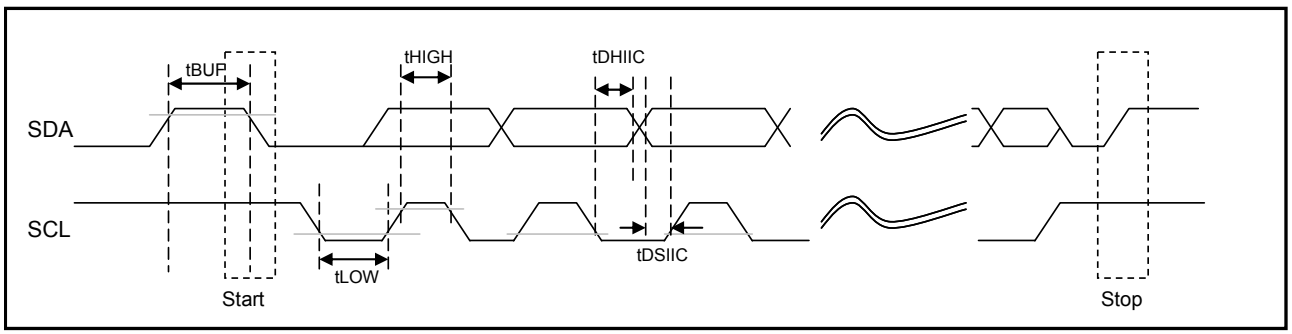


Figure 5-6 : IIC Timing

6. Operating Principles and Methods

6-1 MPU Interface

6-1-1 6800 Interface

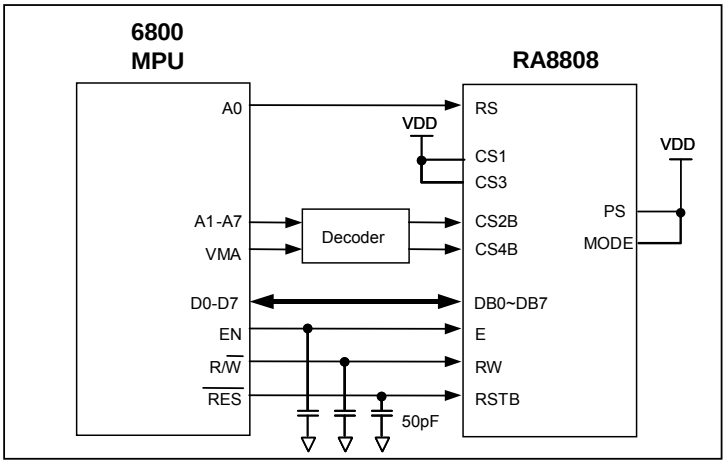


Figure 6-1 : 6800 (8-bit) MPU Interface

The RA8808 supports 6800 MPU interface. The Register/Status Read/Write and Memory read/Write waveform just like the below figure :

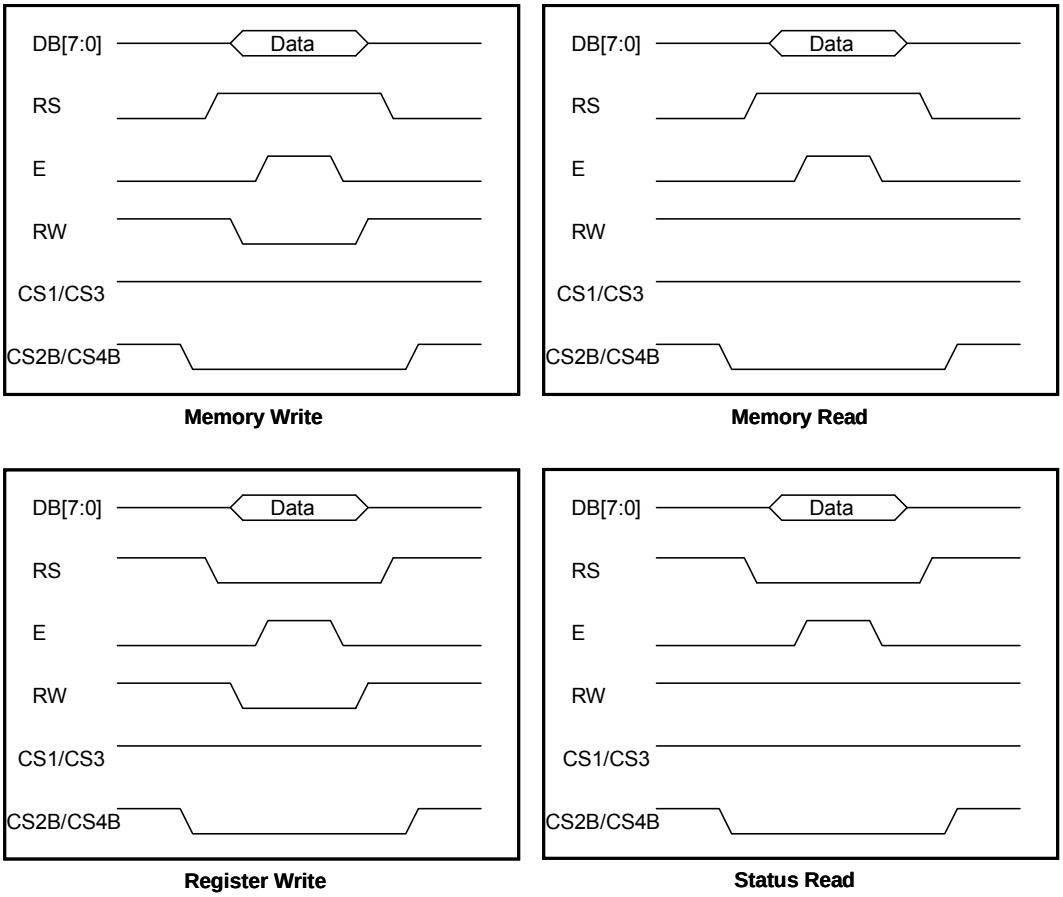


Figure 6-2 : 6800 Interface

6-1-2 8080 Interface

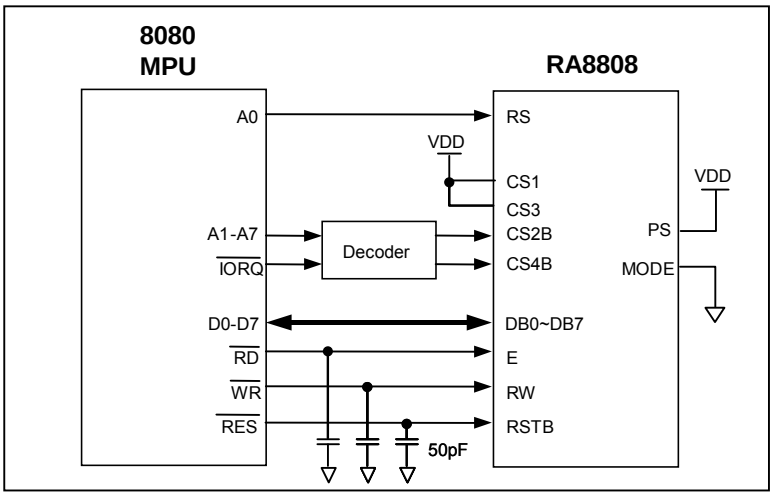


Figure 6-3 : 8080 (8-bit) MPU Interface

The RA8808 also support 8080 MPU interface. The Register/Status Read/Write and Memory read/Write waveform just like the below figure:

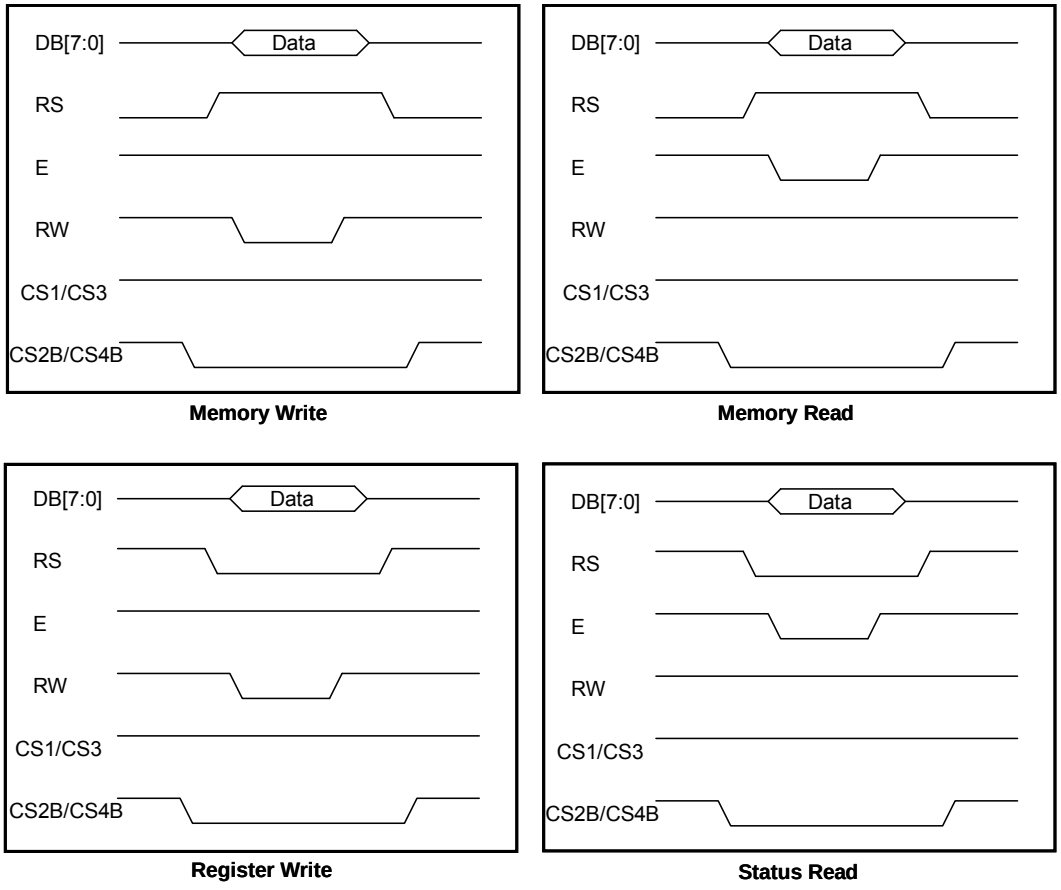


Figure 6-4 : 8080 Interface

6-1-3 3-Wire SPI Interface

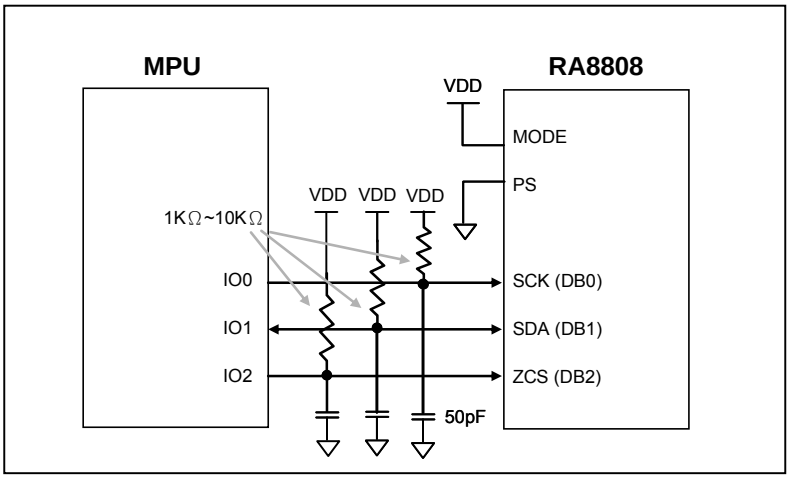


Figure 6-5 : The MPU Interface Diagram of 3-Wire SPI

The SPI is available through the chip select line (ZCS), serial transfer clock line (SCK), serial input/output line (SDA). The SPI can be configured in command/memory write mode or status/memory read mode by setting most three bits of first byte. Before a data transmission begins, ZCS which is low active must be set to low until the transmission is finished. When the SPI module is in command/memory write mode (Figure 6-6), a byte is received from the controller to RA8808 via SDA under the control of the SCK from the controller. When the SPI module is in status/memory read mode (Figure 6-7), a byte is sent from RA8808 to the controller via SDA under the control of the SCK from the controller.

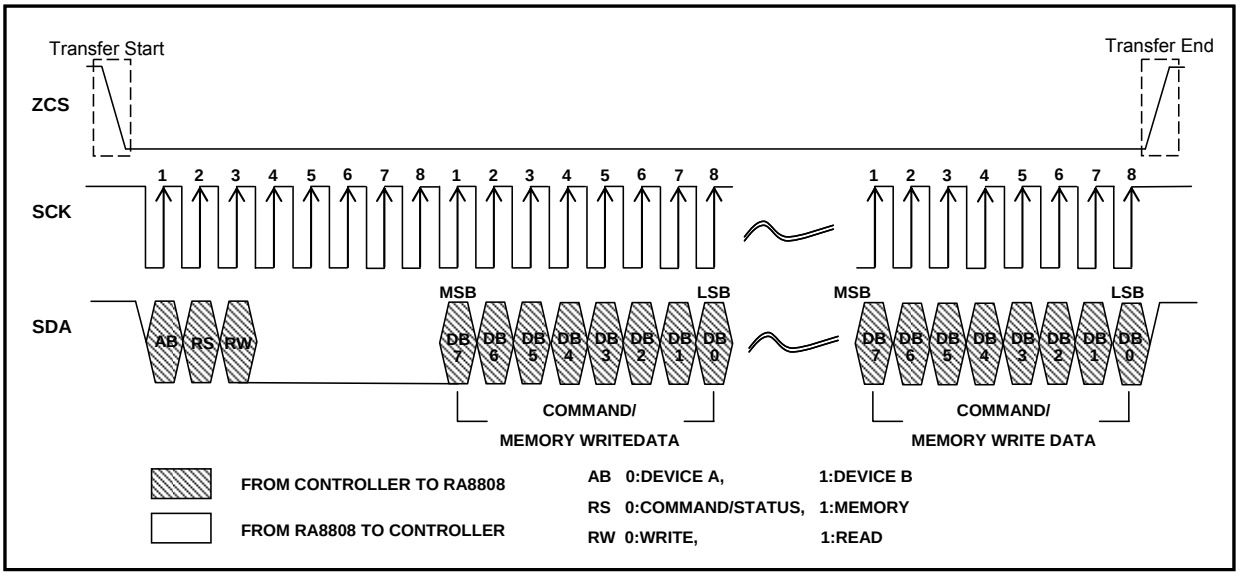


Figure 6-6 : Command/Memory Write on SPI-Bus

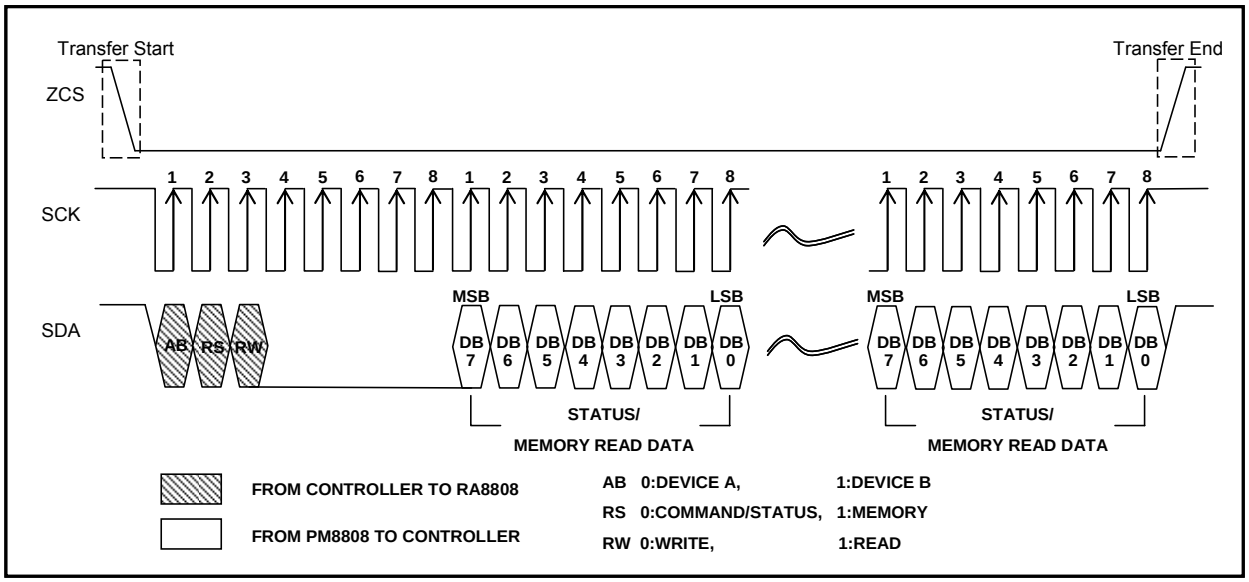


Figure 6-7 : Status/Memory Read on SPI-Bus

6-1-4 IIC Interface

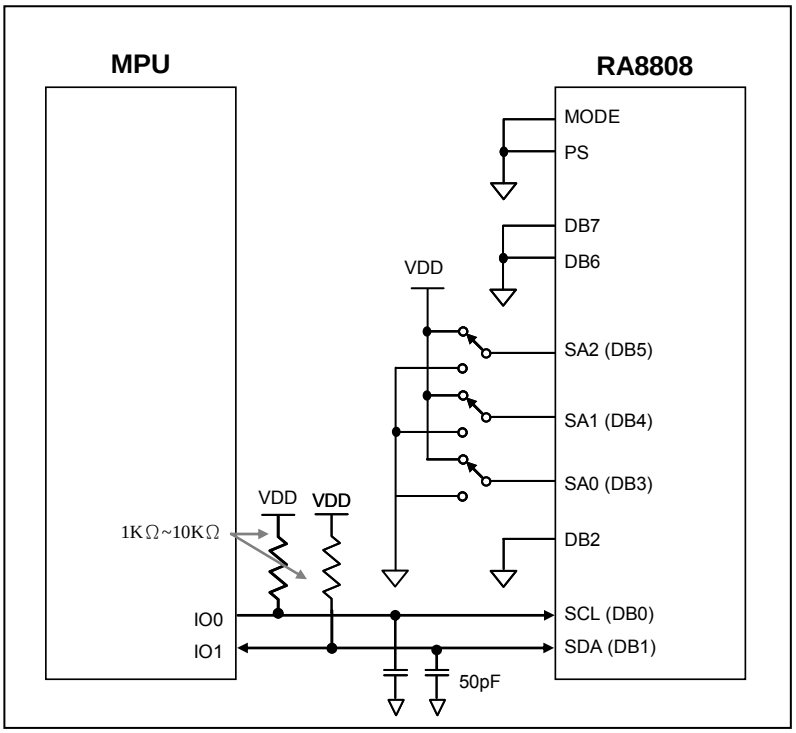


Figure 6-8 : The MPU Interface Diagram of IIC

The IIC is available through the serial transfer clock line (SCL) and the serial input/output(SDA). The IIC can be configured in command/memory write mode or status/memory read mode by setting first byte that including device ID (Table 6-1), read bit and write bit. When the IIC module is in command/memory write mode (Figure 6-9), a byte that from the controller to PM8808 is received via SDA under the control of the SCL from the controller and RA8808 sends a acknowledge signal at ninth SCL clock. When the SPI module is in status/memory read mode (Figure 6-10), a byte that from RA8808 to the controller is sent via SDA under the control of the SCL from the controller and the controller sends a acknowledge signal to PM8808 after receiving a byte data.

Table 6-1 : IIC DEVICE ID

Device ID					
BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00b		SA[2:0] SLAVE ADDRESS			0 : DEVICE A 1 : DEVICE B
For Example : If you set slave address 000b, the Device A ID will be 10_0000b and the Device B ID will be 10_0001b.					

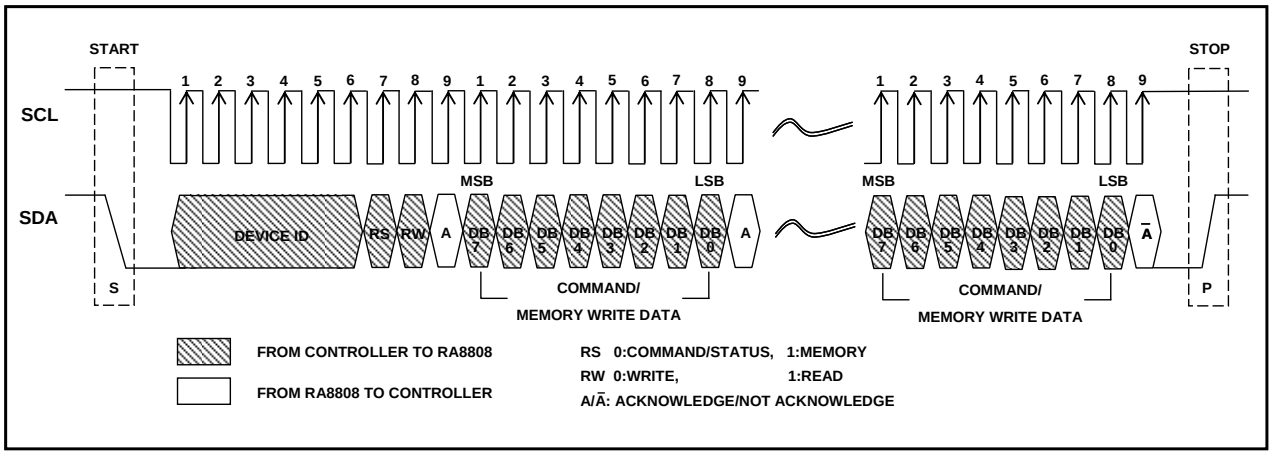


Figure 6-9 : Command/Memory Write on IIC-Bus

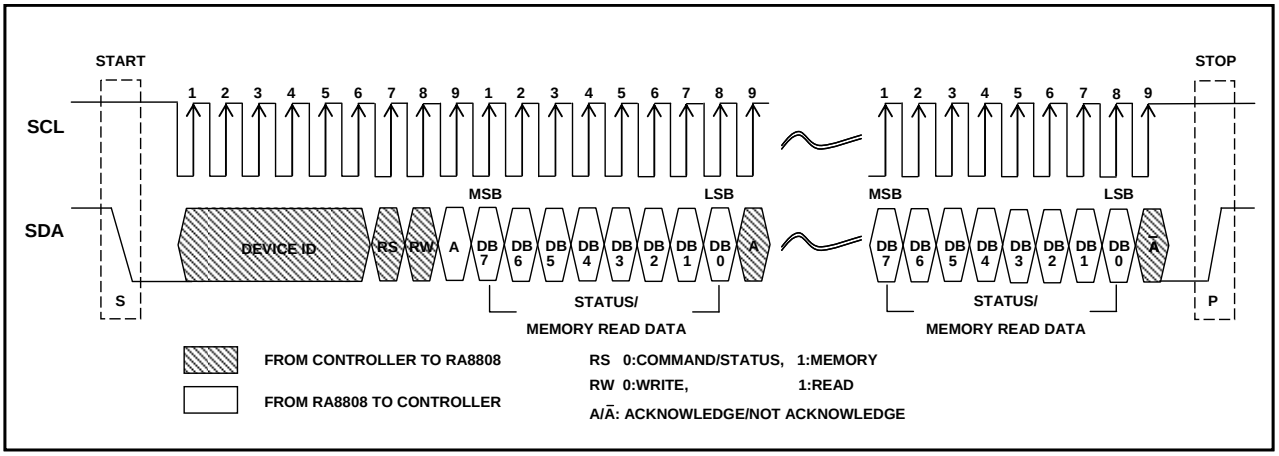


Figure 6-10 : Status/Memory Read on IIC-Bus

6-2 RC Oscillator

The RC Oscillator generates system clock of the RA8808 by the oscillation resister R and capacitor C. The capacitor C is embedded. Resistor R must be connected between RA and RB pins when use internal clock mode. The FRM, CL, M are generated by the frequency(system clock) from the oscillation circuit. If VDD = 5V, for generating 440KHz system clock(FRM frequency ~70Hz), RA and RB pins must be connected to a 51KΩ resistor. The oscillation circuit is as following:

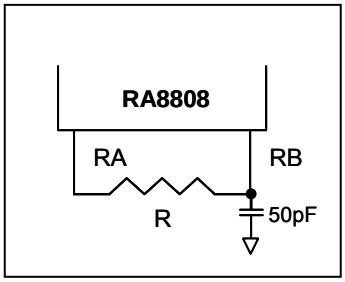


Figure 6-11 : Internal Clock Mode

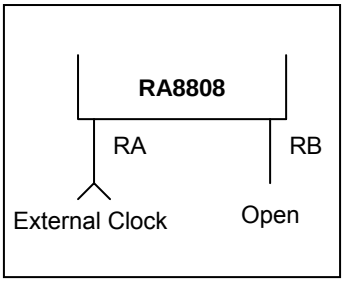


Figure 6-12 : External Clock Mode

6-3 LCD Driver and Power Supply Circuit

The LCD Driver power system operation method is descripted the bellow Figure 6-13. The power supply system is a low power consumption circuit for dot matrix LCD.

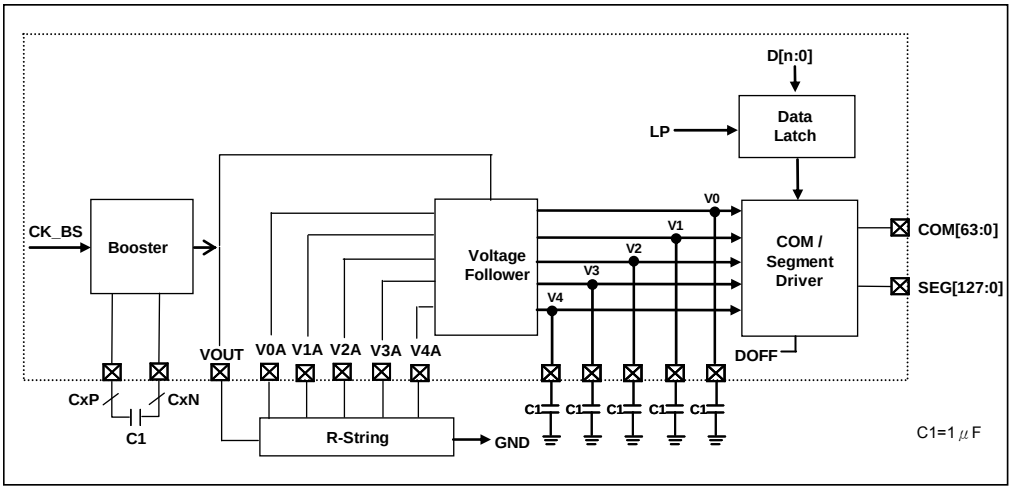


Figure 6-13 : LCD Driver and Power Supply Circuit Block

6-3-1 Booster Circuit

The power supply circuit is consist of Boosters, internal voltage follower. The booster can produce 2X, 3X, 4X step-up of "VDD - GND" voltage levels. When VOUT is equal to 2 × VDD, the capacitor 1uF is connected to C1P and C1N pin. When VOUT is equal to 3 × VDD, the capacitor 1uF is additional connected to C2P and C2N pin. When VOUT is equal to 4 × VDD, the capacitor 1uF is additional connected to C3P and C1N pin. The application circuit for booster can refer the description of Figure 6-14. Note to the maximum rating voltage in the booster application circuit carefully.

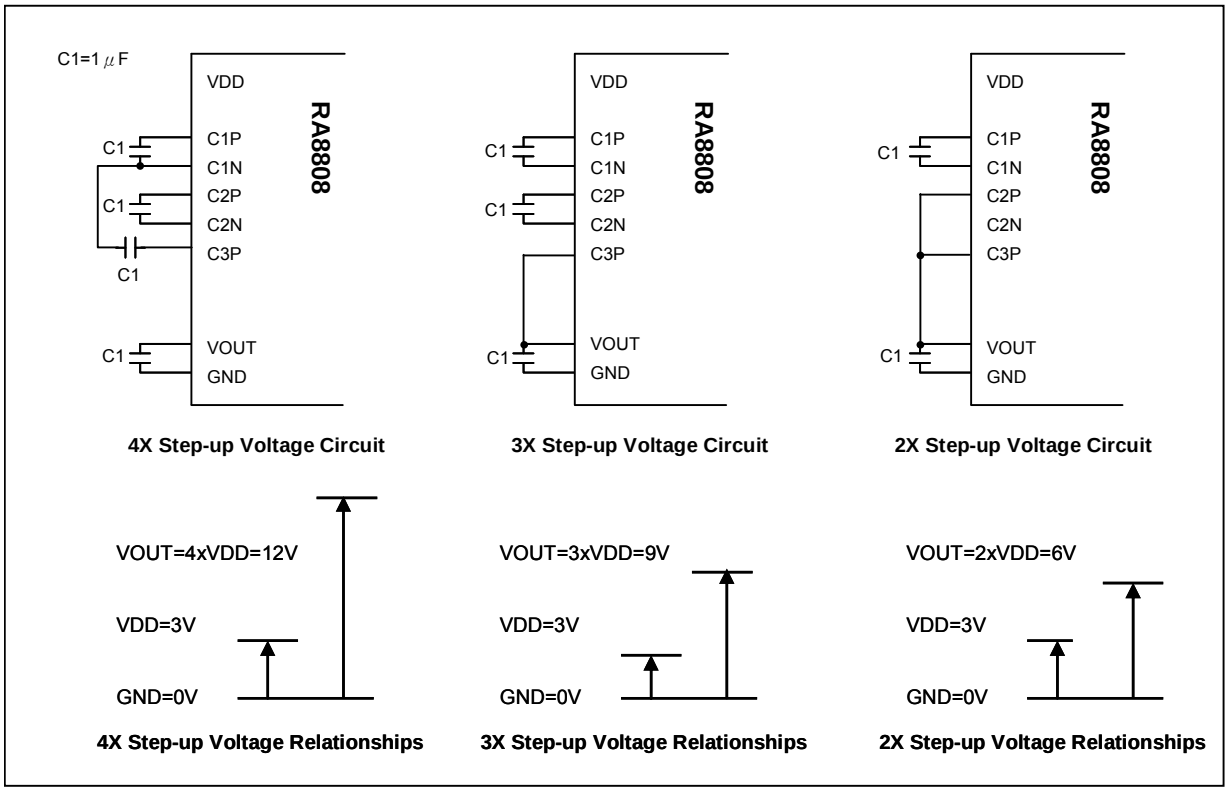


Figure 6-14 : Application Circuit of Booster

Normally, if use the internal Driver Power, then the application circuit is follow Figure 6-13. If use external VOUT, that means do not use the internal Booster, then the connection is show as Figure 6-15.

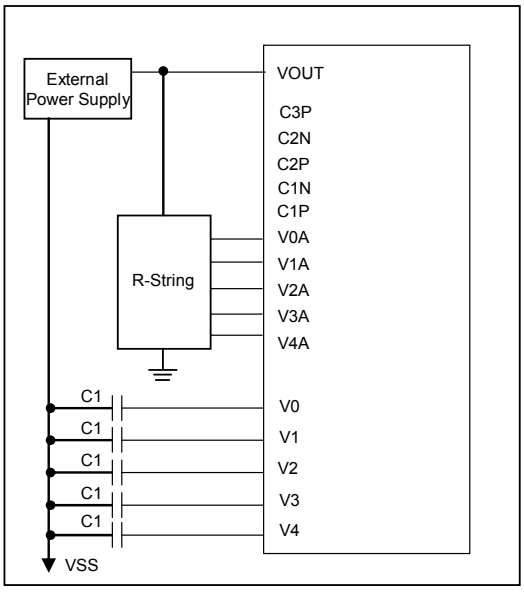


Figure 6-15 : External VOUT

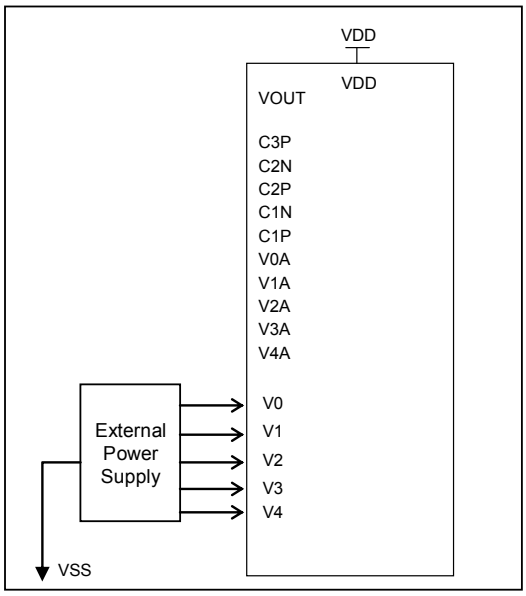


Figure 6-16 : Use External Voltage Follower

6-3-2 Voltage Follower

The internal Voltage Follower provides V0~V4 power for LCD Driver circuit. Of course, the user could select internal or external Voltage Follower. The relationship of V0~V4 and VOUT is as following:

VOUT > V0 > V1 > V2 > V3 > V4 > GND

Figure 6-13 shows the circuit of using internal Voltage Follower. For external V0~V4, the connection is show as Figure 6-16.The internal voltage follower is included to V0,V1,V2,V3,V4 for differential input voltages V0A,V1A,V2A,V3A,V4A.

6-3-3 LCD Driver

The Segment/Common Driver of RA8808 is used to latch the data of pre-stage, then send to Level Shifter for combination. The combined data will follow the Timing Generator to control the switchs then pass the V0~V4 to Common and Segment.

The LCD Bias of RA8808 is adjustable by external R-string so that user can adjust the display quality.Please refer to Figure 8-2 and Figure 8-3.

6-3-4 Temperature Compensation

The temperature compensation of RA8808 is achieved by external circuit. Please refer to the Figure 6-17, R1 and R3 + R2//RT of voltage divider decided to transistor VB; R2//RT for the temperature compensation, characteristics such as Figure 6-18.

※The following information is for reference only. When using different LCD specifications or different characteristics of the parts (ex: Q, R, RT, ...), you may need to adjust R1, R2, R3, RT resistance according to the actual application.

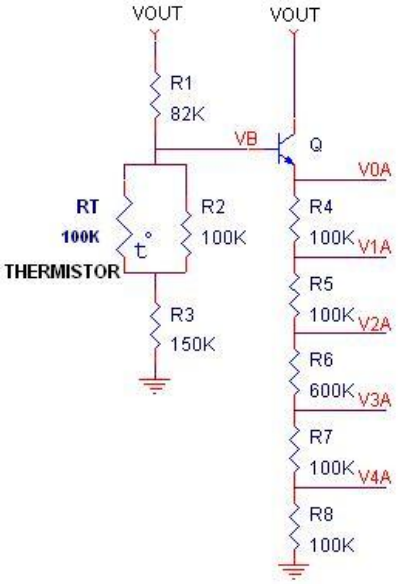


Figure 6-17 : The Reference Circuit of Temperature Compensation

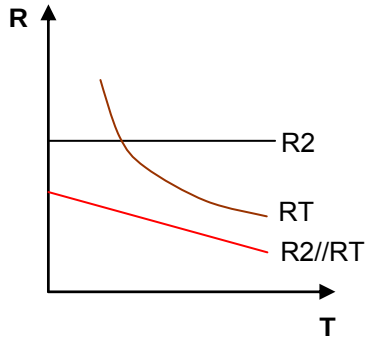


Figure 6-18 : The Characteristic of Temperature Compensation

6-4 I/O Buffer

6-4-1 In Parallel Mode

Input buffer controls the status between the enable and disable of chip. Unless the CS1 and CS2B(Left side chip) or the CS3 and CS4B(Right side chip) are in active mode, input or output of data and instruction does not execute. Therefore internal state is not change. But RSTB, ADC can operate regardless CS1 and CS2B or CS3 and CS4B.

6-4-2 In Serial Mode

Input buffer also controls the status between the enable and disable of chip. Unless the serial data is decoded and the status is DEVICE A(Left side chip) or DEVICE B(Right side chip), input or output of data and instruction does not execute. Therefore internal state is not change. Just the same, RSTB, ADC can operate regardless the status DEVICE A or DEVICE B.

6-5 Input Register

6-5-1 In Parallel Mode

Input register is provided to interface with MPU which is different operating frequency. Input register stores the data temporarily before writing it into display RAM. When CS1 and CS2B or CS3 and CS4B are in the active mode, RW and RS select the input register, the data from MPU is written into input register. And then, write it into display RAM. Data latched for falling of the E signal when in 6800 series MPU IF or rising of the RW signal when in 8080 series MPU IF and write automatically into the display data RAM by internal operation.

6-5-2 In Serial Mode

Input register is provided to interface with MPU which is different operating frequency. Input register stores the data temporarily before writing it into display RAM. When serial data is decoded and the status is DEVICE A or DEVICE B and RW and RS select the input register, the data from MPU is written into input register. And then, write it into display RAM automatically by internal operation.

6-6 Output Register

6-6-1 In Parallel Mode

Output register stores the data temporarily from display data RAM when CS1 and CS2B or CS3 and CS4B are in active mode and RW=H and RS=H when in 6800 series MPU IF or E=L and RS=H when in 8080 series MPU IF, stored data in display data RAM is latched in output register. When CS1 and CS2B or CS3 and CS4B are in active mode and RW=H and RS=L when in 6800 series MPU IF or E=L and RS=L when in 8080 series MPU IF, status data (busy check) can read out. To read the contents of display data RAM, twice access of read instruction is needed. In first access, data in display data RAM is latched into output register. In second access, MPU can read data which is latched. That is, to read the data in display data RAM, it needs dummy read. But status read is not needed dummy read.

Table 6-2

MPU / RS	6800	8080	Function
L	RW = L	RW = L	Instruction write
	RW = H	E = L	Status read (busy check)
H	RW = L	RW = L	Data write (from input register to display data RAM)
	RW = H	E = L	Data read (from display data RAM to output register)

6-6-2 In Serial Mode

Output register stores the data temporarily from display data RAM when the status is DEVICE A or DEVICE B and RW=H and RS=H, stored data in display data RAM is latched in output register. When the status is DEVICE A or DEVICE B RW=H and RS=L, status data (busy check) can read out. To read the contents of display data RAM, twice access of read instruction is needed. In first access, data in display data RAM is latched into output register. In second access, MPU can read data which is latched. That is, to read the data in display data RAM, it needs dummy read. But status read is not needed dummy read.

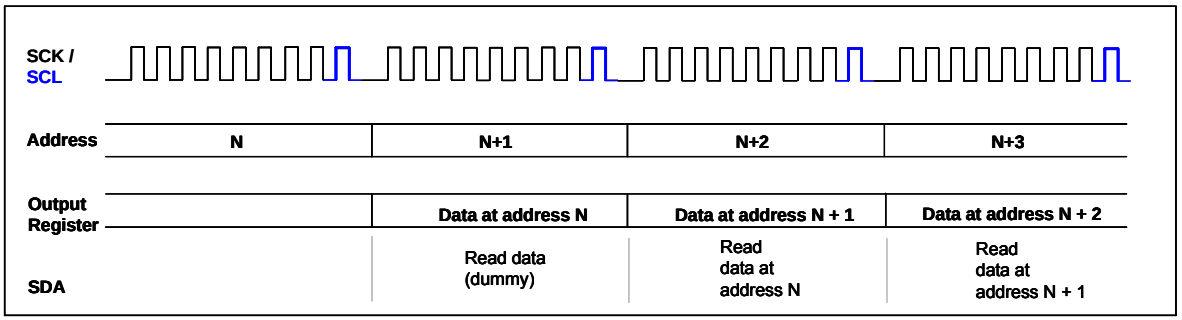


Figure 6-19 : Serial Mode Read Cycle

6-7 Reset

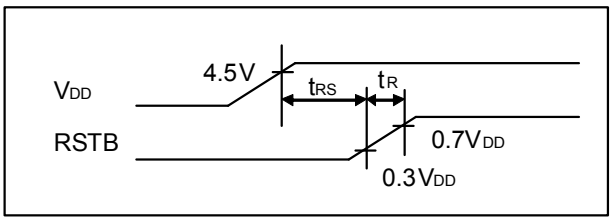
The system can be initialized by setting RSTB terminal at low level when turning power on, receiving instruction from MPU.
When RSTB becomes low, following procedure is occurred.

_ Display off
_ Display start line register become set by 0. (Z-address 0)

While RSTB is low, No instruction except status read can be accepted. Therefore, execute other instructions after making sure that DB4 = 0 (clear RSTB) and DB7 = 0 (ready) by status read instruction. The Conditions of power supply at initial power up are shown in Table 6-3.

Table 6-3 : Power Supply Initial Conditions

Item	Symbol	Min	Typ	Max	Unit
Reset Time	t_{RS}	1.0	-	-	μs
Rise Time	t_R	-	-	200	ns



6-8 Busy Flag

Busy Flag indicates that RA8808 is operating or no operating. When busy flag is high, RA8808 is in internal operating. When busy flag is low, RA8808 can accept the data or instruction. DB7 indicates busy flag of the RA8808.

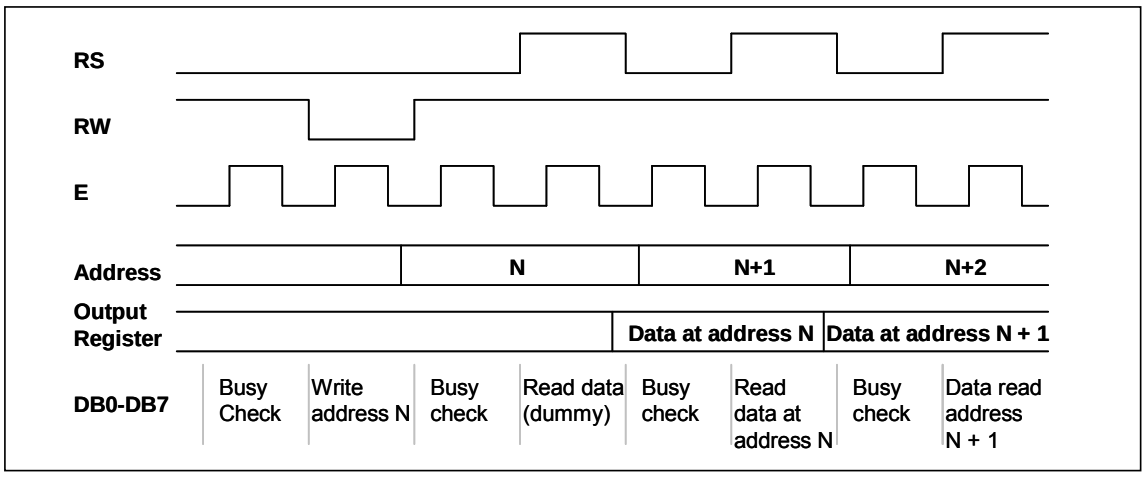


Figure 6-20 : MPU Read Cycle

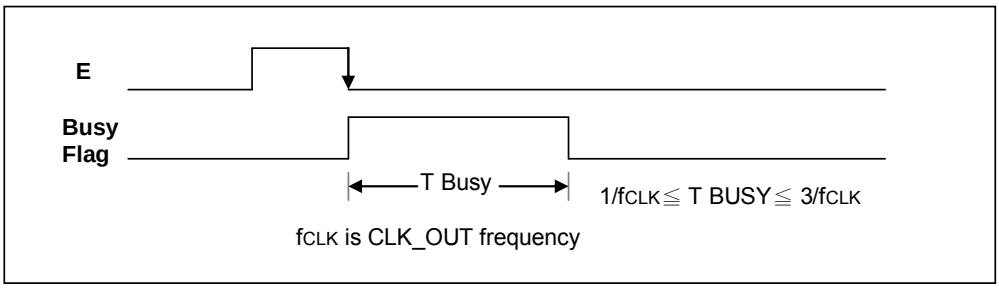


Figure 6-21 : Busy Flag

6-9 Display ON/OFF Flip – Flop

The display on/off flip-flop makes on/off the liquid crystal display. When flip-flop is reset (logical low), selective voltage or non selective voltage appears on segment output terminals. When flip-flop is set (logic high), non selective voltage appears on segment output terminals regardless of display RAM data. The display on/off flip-flop cans changes status by instruction. The display data at all segments disappear while RSTB is low. The status of the flip-flop is output to DB5 by status read instruction. The display on/off flip-flop synchronized by CL signal.

6-10 X Page Register

X page register designates pages of the internal display data RAM. Count function is not available. An address is set by instruction.

6-11 Y Address Counter

Y address counter designates address of the internal display data RAM. An address is set by instruction and is increased by 1 automatically by read or write operations of display data.

6-12 Display Data RAM

Display data RAM stores a display data for liquid crystal display. To indicate on state dot matrix of liquid crystal display, write data 1. The other way, off state, writes 0.
Display data RAM address and segment output can be controlled by ADC signal.

_ ADC = H → S0 ~ S127
_ ADC = L → S127 ~ S0

ADC terminal connect the VDD or GND.

6-13 Display Start Line Register

The display start line register indicates of display data RAM to display top line of liquid crystal display. Bit data (DB<0:5>) of the display start line set instruction is latched in display start line register. Latched data is transferred to the Z address counter while FRM is high, presetting the Z address counter. It is used for scrolling of the liquid crystal display screen.

7. Display Control Instruction

The display control instructions control the internal state of the RA8808. Instruction is received from MPU to RA8808 for the display control. The following table shows various instructions.

Table 7-1

Instruction	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
Display on/off	L	L	H	H	H	H	H	L/H	Controls the display on or off. Internal status and display RAM data is not affected. L: OFF, H: ON
Set Address (Y address)	L	H	Y address (0 ~ 63)						Sets the Y address in the Y address counter.
Set page (X address)	H	L	H	H	H	Page (0 ~ 7)			Sets the X address at the X address register.
Display start line (Z address)	H	H	Display start line (0 ~ 63)						Indicates the display data RAM displayed at the top of the screen.
Status Read	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**	**Function**
Status read	Busy	L	On/ Off	Reset	L	L	L	L	Read status. BUSY L: Ready H: In operation ON/OFF L: Display ON H: Display OFF RESET L: Normal H: Reset
Data Write	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**	**Function**
Write display data	Write data								Writes data(DB7~0)into display data RAM. After writing instruction, Y address is increased by 1 automatically.
Data Read	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**	**Function**
Read display data	Read data								Reads data(DB7~0) from display data RAM to the data bus. After reading instruction, Y address is increased by 1 automatically.

7-1 Display ON/OFF

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	1	D

The display data appears when D is 1 and disappears when D is 0. Though the data is not on the screen with D = 0, it remains in the display data RAM. Therefore, you can make it appear by changing D = 0 into D = 1.

7-2 Set Address (Y Address)

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	AC5	AC4	AC3	AC2	AC1	AC0

Y address (AC0 ~ AC5) of the display data RAM is set in the Y address counter. An address is set by instruction and increased by 1 automatically by read or write operations of display data.

7-3 Set Page (X Address)

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	1	1	1	AC2	AC1	AC0

X address(AC0 ~ AC2) of the display data RAM is set in the X address register. Writing or reading to or from MPU is executed in this specified page until the next page is set.

7-4 Display Start Line (Z Address)

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	AC5	AC4	AC3	AC2	AC1	AC0

Z address (AC0 ~ AC5) of the display data RAM is set in the display start line register and displayed at the top of the screen. When the display duty cycle is 1/64 or others(1/48 ~ 1/64), the data of total line number of LCD screen, from the line specified by display start line instruction, is displayed.

7-5 Status Read

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
BUSY	0	ON/OFF	RESET	0	0	0	0

◆ ***BUSY***
When BUSY is 1, the Chip is executing internal operation and no instructions are accepted.
When BUSY is 0, the Chip is ready to accept any instructions.

◆ ***ON/OFF***
When ON/OFF is 1, the display is off.
When ON/OFF is 0, the display is on.

◆ ***RESET***
When RESET is 1, the system is being initialized.
In this condition, no instructions except status read can be accepted.
When RESET is 0, initializing has finished and the system is in the usual operation condition.

7-6 Write Display Data

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
D7	D6	D5	D4	D3	D2	D1	D0

Writes data (D0 ~ D7) into the display data RAM. After writing instruction, Y address is increased by 1 automatically.

7-7 Read Display Data

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
D7	D6	D5	D4	D3	D2	D1	D0

Reads data (D0 ~ D7) from the display data RAM. After reading instruction, Y address is increased by 1 automatically.

8. Application Circuit

8-1 Timing Diagram (1/64 DUTY)

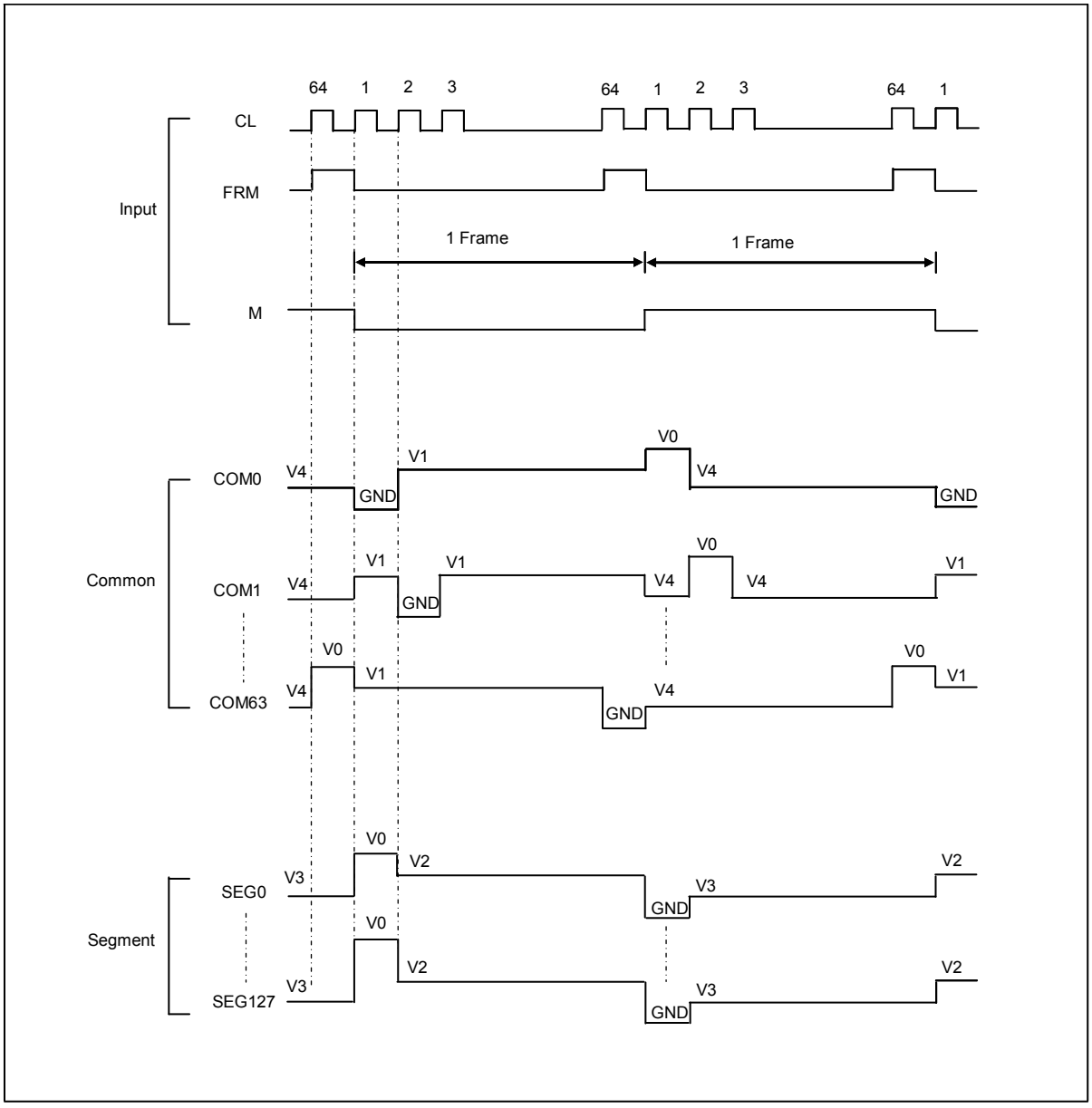


Figure 8-1 : Timing Diagram

8-2 LCD Panel Interface Application Circuit

8-2-1 128X64

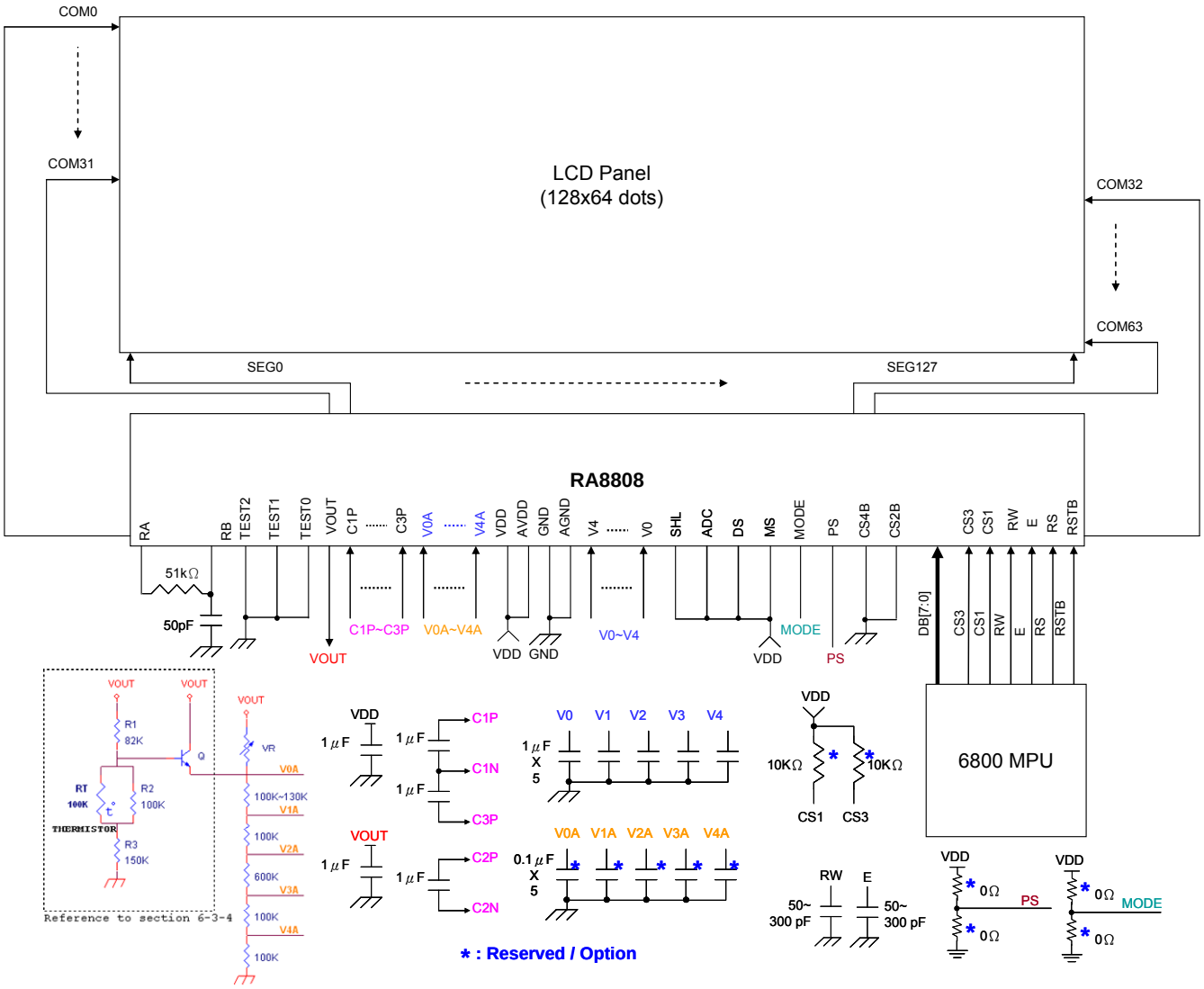


Figure 8-2 : 128X64 Application Circuit

8-2-2 256X64

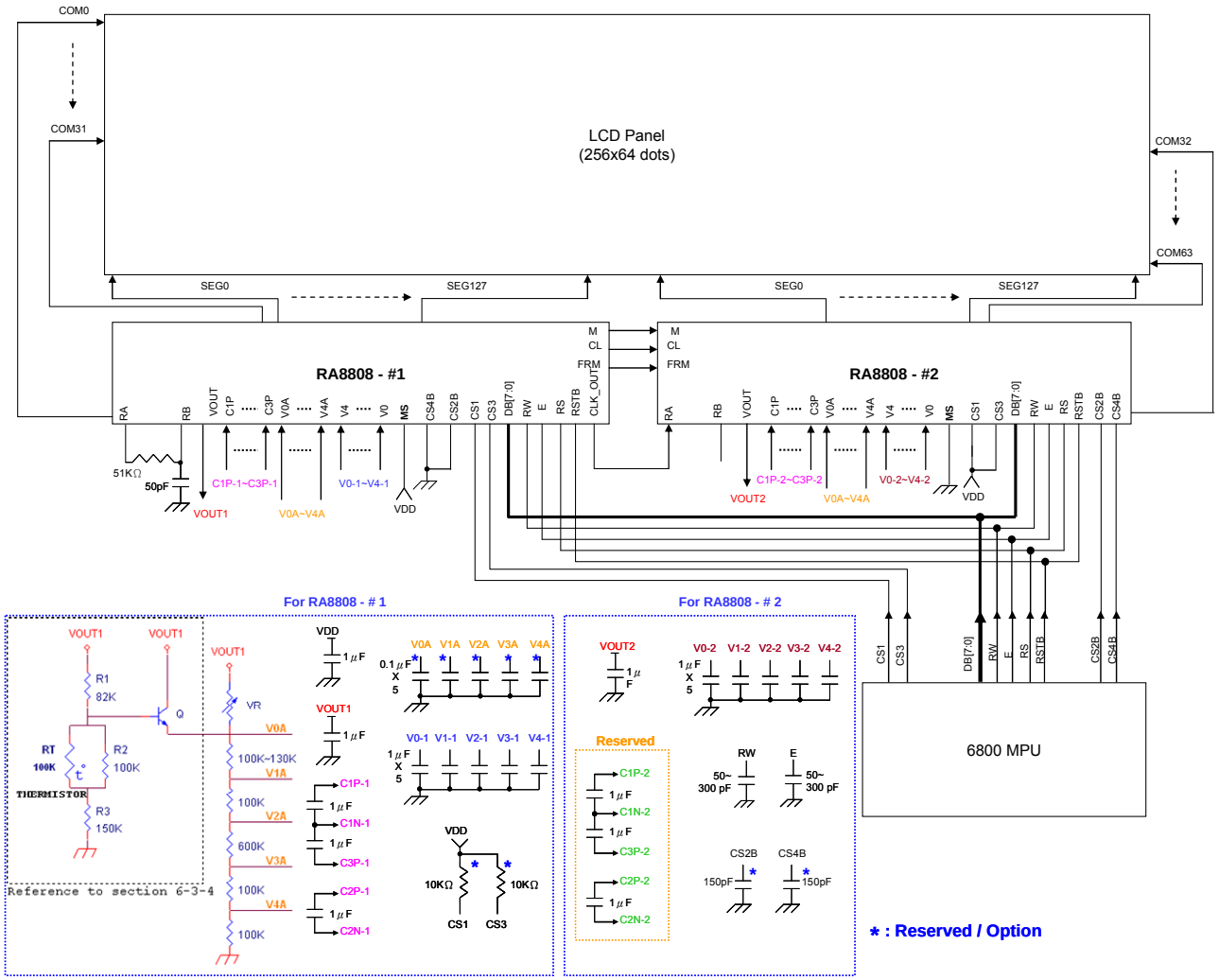


Figure 8-3 : 256X64 Application Circuit

Appendix A. COG/Module Application

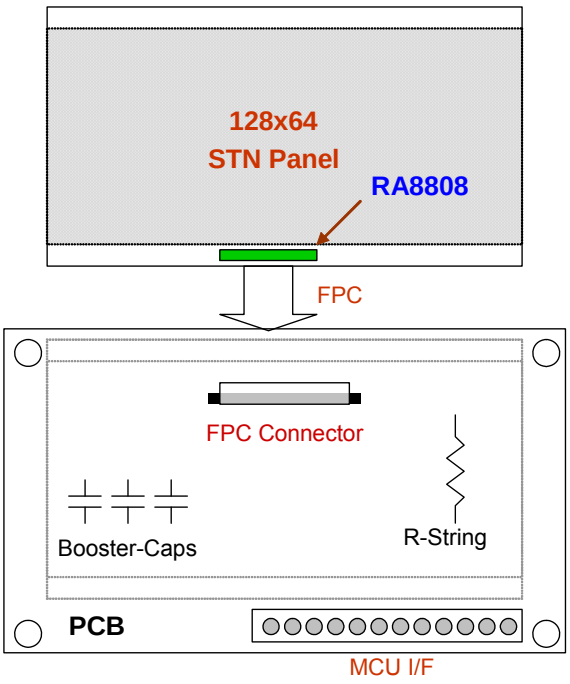


Figure A-1 : 128X64 Module

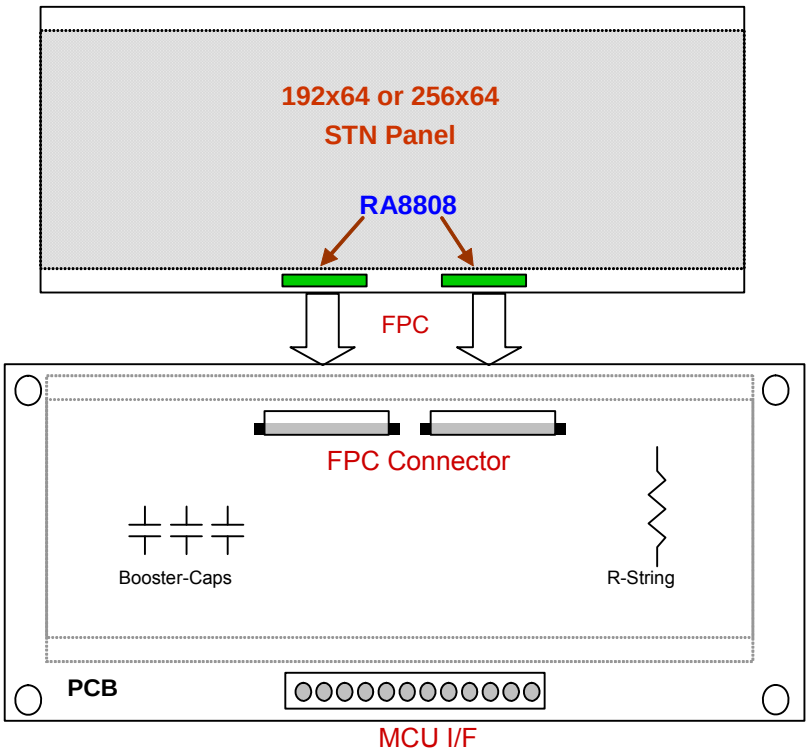


Figure A-2 : 192x64 / 256x64 Module

Appendix B. ITO

Tbale B-1 : Maximum ITO Resistance of COG

PAD Name	ITO(Ohm)	PAD Name	ITO(Ohm)	PAD Name	ITO(Ohm)
VDD , VDDP, AVDD	**100**	DS	200	RA	500
GND , GNDP. AGND	**100**	DB[7..0]	500	RB	500
VOUT	**120**	E	500	CLK_OUT	500
C1N, C1P	**100**	RW	500	MS	500
C2N, C2P	**100**	RS	500	M	500
C3P	**120**	CS1, CS2B	500	CL	500
V0~V4	**120**	CS3, CS4B	500	FRM	500
V0A~V4A	**120**	RSTB	500	TEST[2..0]	500
ADC	200	MODE	500		
SHL	200	PS	500		