



» **DATA SHEET**

(DOC No. HX8288-A02-DS)

» **HX8288-A02**
1026 CH TFT LCD Source Driver
with PBPI Interface
Version 01 October, 2012

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October, 2012

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1. General Description

HX8288-A02 is a 1026 channel outputs source driver with PBPI (Packet Based Point to point Interface) interface. This chip integrates 1026ch single gate source driver for TFT-LCD.

Source driver with 6-bit DAC performs 64 gray scales. The source driver receives 6-bit through PBPI interface, and generates corresponding 64-level gray scale voltage output. Since the output circuit of this source driver incorporates an operational amplifier with low power dissipation, and performs wide voltage supply range and small output deviation. Therefore, a high quality display with less crosstalk can be achieved.

2. Features

- Support PBPI interface with clock pair
- 1026/1020/966/960/768 channel outputs selectable
- 6-bit resolution / 64-gray scale
- V1~V10 for adjusting gamma correction
- 10 or 6 gamma correction reference voltages selectable
- Dynamic output range: 0.1 to VDDA-0.1V
- Applicable dot inversion(normal & Flip-Pixel panel)/
1+2 line inversion/square inversion driving scheme
- Right and left shift capability
- Support terminal resistor tunable
- Support 1 or 2 data pair
- Support 2 repair buffers
- The PBPI interface maximum operation frequency : 150MHz
- Power of digital circuit(VDDD): 2.3V to 3.6V
- Power of analog circuit(VDDA): 6V to 13.5V
- COG package

3. Block Diagram

3.1 Function block diagram

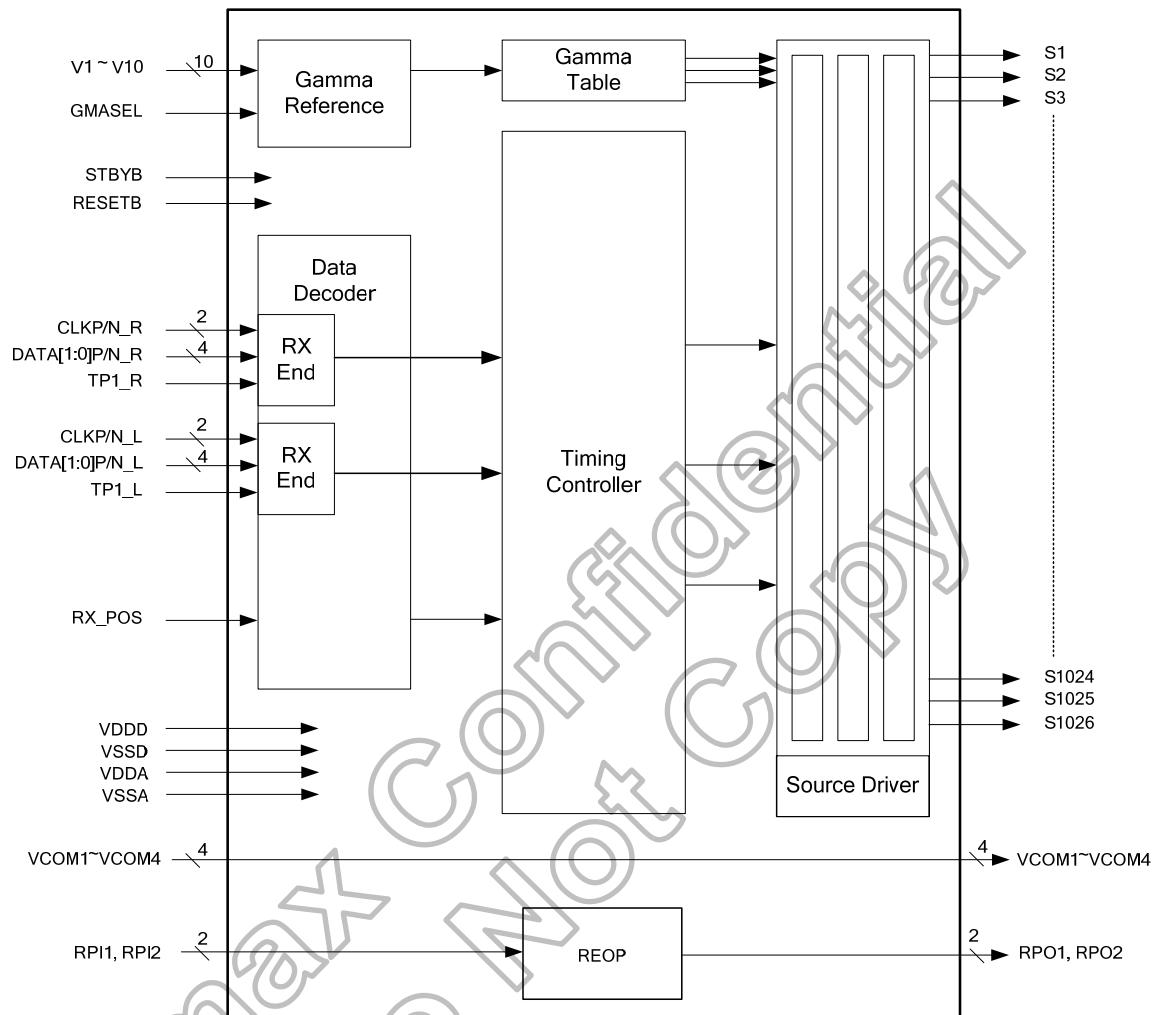


Figure 3.1: HX8288-A02 function block diagram

4. Pin Description

4.1 Pin description

Name	I/O	Description
DATA[1:0]P/N_R	I	PBPI interface data input pin. This is differential data pair at right side of source driver (See pin assignment).
CLKP/N_R	I	PBPI interface clock input pin. This is differential clock pair at right side of source driver (See pin assignment).
TP1_R	I	PBPI interface pocket start pulse at right side source driver. This pin default pull low (See pin assignment).
DATA[1:0]P/N_L	I	PBPI interface data input pin. This is differential data pair at left side of source driver (See pin assignment).
CLKP/N_L	I	PBPI interface clock input pin. This is differential clock pair at left side of source driver (See pin assignment).
TP1_L	I	PBPI interface pocket start pulse at left side of source driver. This pin default pull low (See pin assignment).
RX_POS	I	PBPI interface related signals input position announcement (Default pull high) : 0 : PBPI interface input signal is near side of S1026. 1 : PBPI interface input signal is near side of S1
STBYB	I	Standby mode control. Normally and default pull high . When STBYB=H, Source driver is normal mode. When STBYB=L, Source driver enter standby mode and all output pull ground.
RESETB	I	Global reset. Keep VDDD during operation. Normally pull high. Suggest to connecting with an RC reset circuit for stability.
V1 ~ V10	I	Gamma correction reference voltages. V1 ~ V10 are the external reference gamma control points. The voltage of these pins must be: AGND < V10 < V9 < V8 < V7 < V6, V5 << V4 < V3 < V2 < V1 < VDDA.
GMASEL	I	Gamma correction reference selection. (Default pull high) 1: All gamma correction reference point enables. 0: V2, V4, V7, and V9 disable then keep floating.
RPI 1/2	I	Repair OP input.
RPO 1/2	O	Repair OP output.
VDDD	PI	Digital power.
VSSD	PI	Digital ground.
VDDA	PI	Analog power.
VSSA	PI	Analog ground.
TRIM[15:0]	T	Test pin. Please float it.
TESTD[7:0]	T	Test pin. Please float it.
TESTA[2:0]	T	Test pin. Please float it.
DUMMY	D	Dummy pin.
VCOM1	S	Internal through path. Valid thru range: VSSA ~ VDDA.
VCOM2	S	Internal through path. Valid thru range: VSSA ~ VDDA.
VCOM3	S	Internal through path. Valid thru range: VSSA ~ VDDA.
VCOM4	S	Internal through path. Valid thru range: VSSA ~ VDDA.
S1~S1026	O	Output driver signal. All outputs will be VSSA under stand-by mode.

Note: I: Input, O : Output, I/O : Input/Output, PI : Power input, T : Testing, SH : Shielding, D : Dummy, S: Shorted line

Table 4.1: Pad description

4.2 Value of wiring resistance to each pin

The input wiring resistance values affect power or signal integrity and the display quality. So be sure to design using values that do not exceed those recommendations as below.

Pin name	Wiring resistance value(Ω)
VDDA	<10
VSSA	<10
VDDD	<10
VSSD	<10
V1 ~ V10	<150
CLKP/N_R, CLKP/N_L	<30
DATA[1:0]P/N_R, DATA[1:0]P/N_L	<30
TP1_R, TP1_L	<50

Table 4.2: Wiring resistance values

HX8288-A02 internal link schematic.

Pin name	Internal line resistance (Ω)
VCOM1_Path	<20
VCOM2_Path	<20
VCOM3_Path	<20
VCOM4_Path	<20

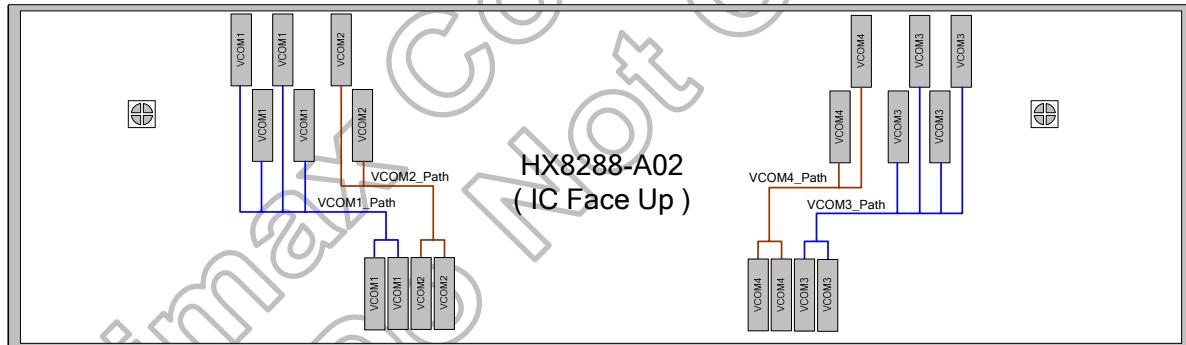
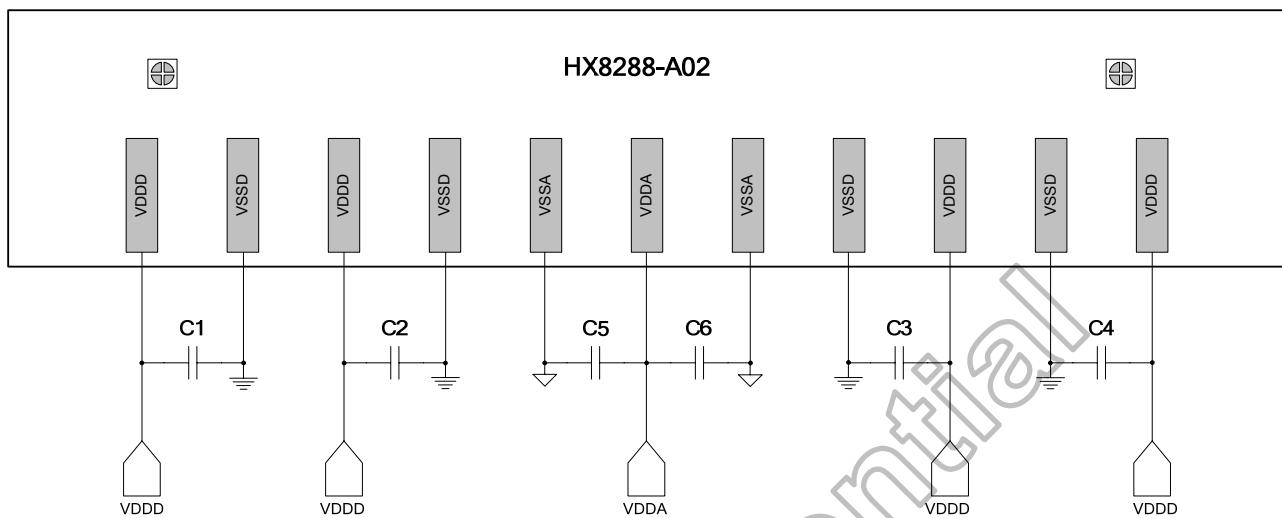


Figure 4.1: Internal link schematic

4.3 Application Power Circuit



Note : (1) $C_1 + C_2 + C_3 + C_4 \geq 10\mu F / 16V$
(2) $C_5 + C_6 \geq 10\mu F / 25V$

Figure 4.2: Power circuit application schematic

5. Register Table

Register group	Class	Name	Description	Default	Settings
Reg1 [5]	SOU	RL	Horizontal scan selection.	0b	1b: S1~S1026 0b: S1026~S1
Reg1 [4:3]	SOU	RES	Input resolution selection.	01b	00b: 1366 RGB 01b: 1280 RGB 10b: 1024 RGB 11b: Reserve
Reg1 [2]	SOU	ZinvP	Z inversion(flip-pixel) panel selection.Only support 1366RGB/1280RGB/1024RGB_3SD.	0b	0b: Normal panel 1b: Z inversion panel (Flip-Pixel M+1 and Flip-pixel M+3)
Reg1 [1:0]	NO	Reserve	These bits are reserve.	-	-
Reg2 [5:4]	NO	Reserve	These bits are reserve.	-	-
Reg2 [3]	SOU	SD_num	For 1024RGB only.	0b	0b: use 4SD architecture 1b: use 3SD architecture
Reg2 [2:0]	NO	Reserve	These bits are reserve.	-	-
Reg3 [5:0]	NO	Reserve	These bits are reserve.	-	-
Reg4 [5:3]	RX	RTERM	Adjst termination resistor for RX.	010b	Approximation resistance: 000b → 50Ω 001b → 75Ω 010b → 100Ω 011b → off (several megaΩ) 100b → 150Ω 101b ~ 111b → reserve
Reg4 [2]	SOU	R_RPOP1EN	Repair OP1 enable. (Notes1)	0b	0b: Repair OP1 diable 1b: Repair OP1 enable
Reg4 [1]	SOU	R_RPOP2EN	Repair OP2 enable. (Notes1)	0b	0b: Repair OP2 diable 1b: Repair OP2 enable
Reg4 [0]	SOU	SQRINV	Square inversion function enable. (This function is for normal panel use only)	0b	0b: Square inversion enable 1b: Square inversion disable

Note: (1).Power on sequence and Standby mode are disable.

5.1 Application block diagram

5.1.1 Output channel selection

Frame update packets include the register of output channel selection. The channel selection is decided by resolution, panel type, and source driver number.

- Normal type panel structure: 1366 RGB with 4 SD.

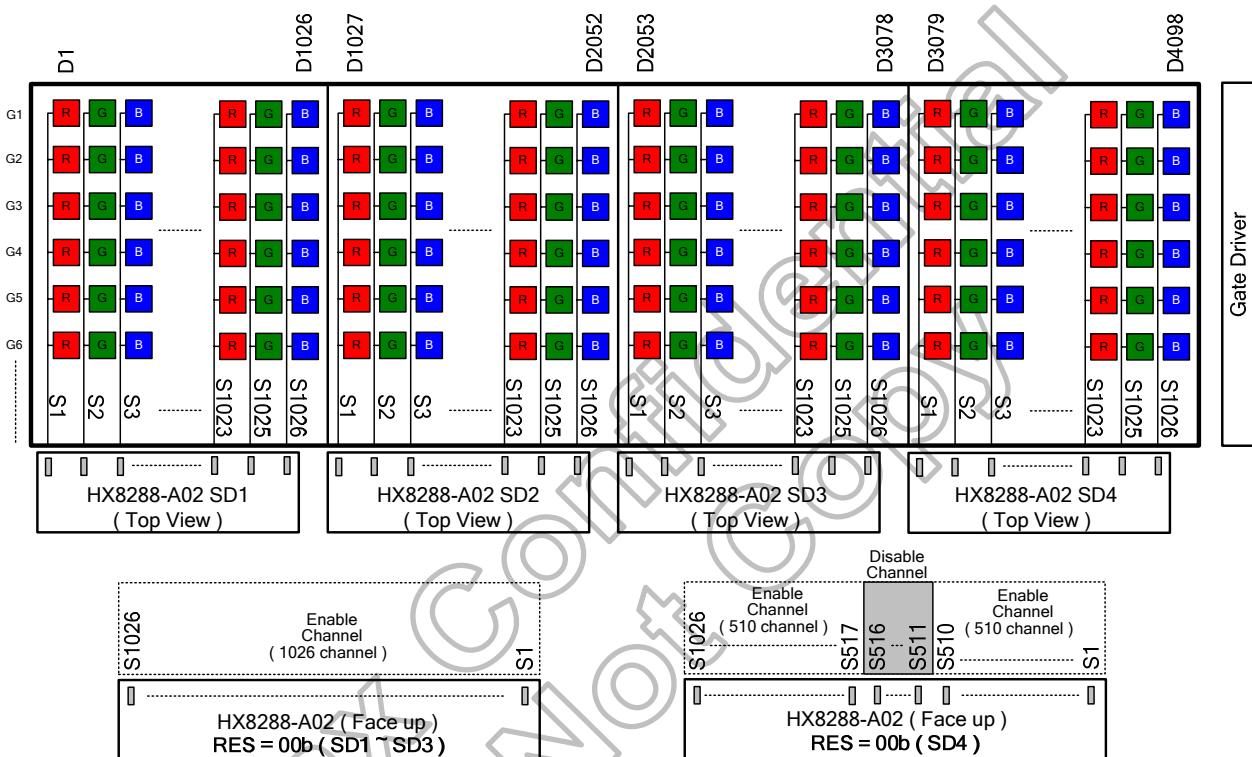


Figure 5.1: Output channel selection for normal type panel structure of 1366 RGB with 4 SD

- **Flip-Pixel M+1 panel structure: 1366 RGB with 4 SD.**

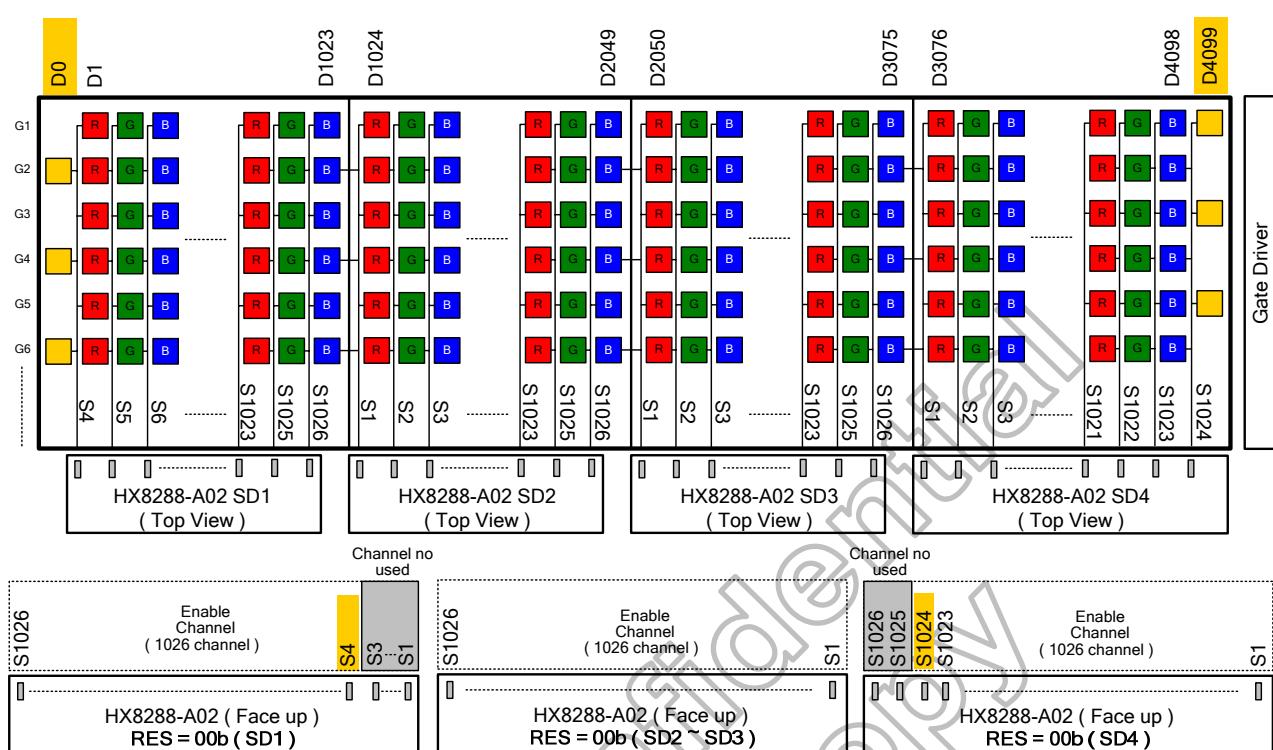


Figure 5.2: Output channel selection for Flip-Pixel M+1 type panel structure of 1366 RGB with 4 SD

- **Flip-Pixel M+3 panel structure: 1366 RGB with 4 SD.**

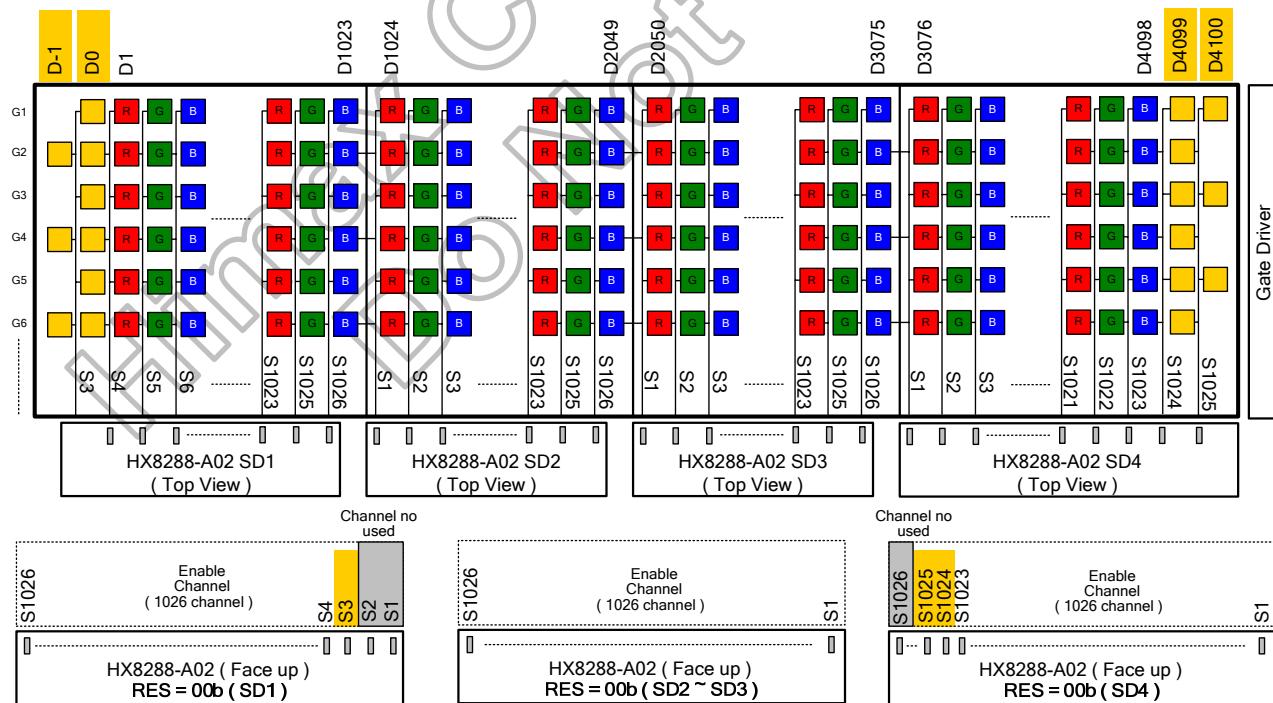


Figure 5.3: Output channel selection for Flip-Pixel M+3 type panel structure of 1366 RGB with 4 SD

- Normal type panel structure: 1280 RGB with 4 SD.

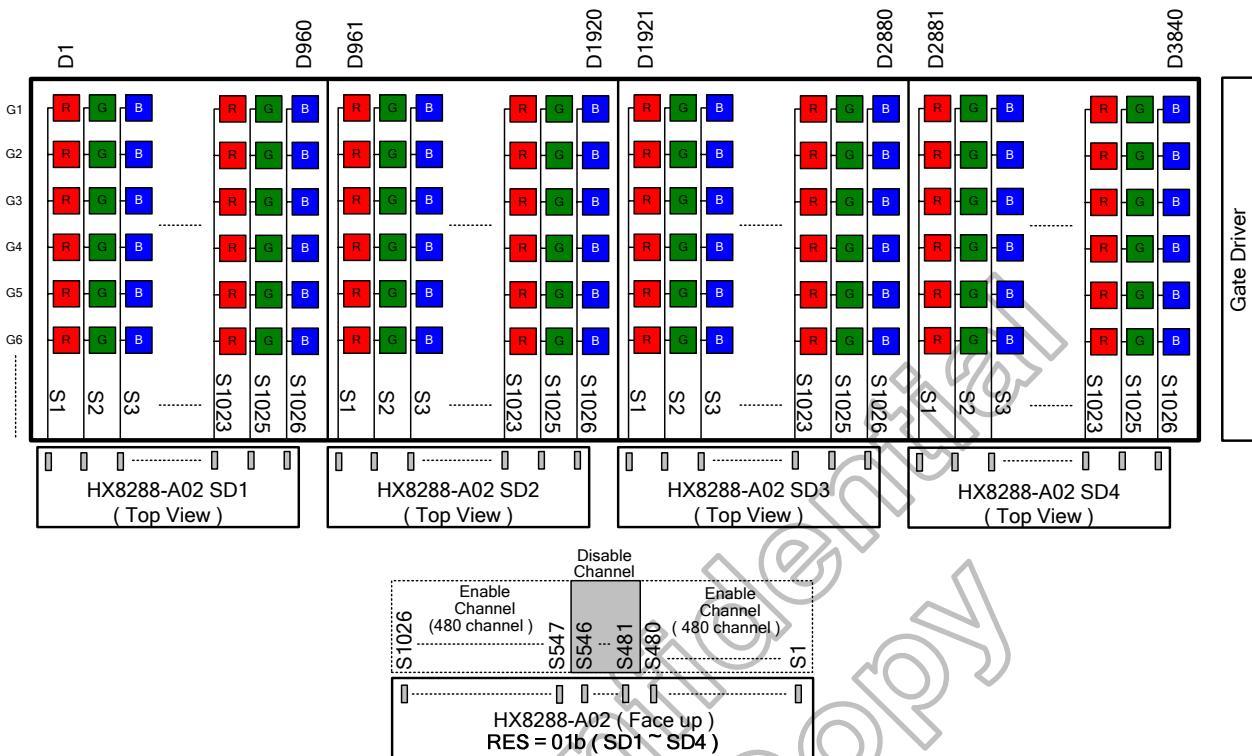


Figure 5.4: Output channel selection for normal type panel structure of 1280 RGB with 4 SD

- Flip-Pixel M+1 panel structure: 1280 RGB with 4 SD.

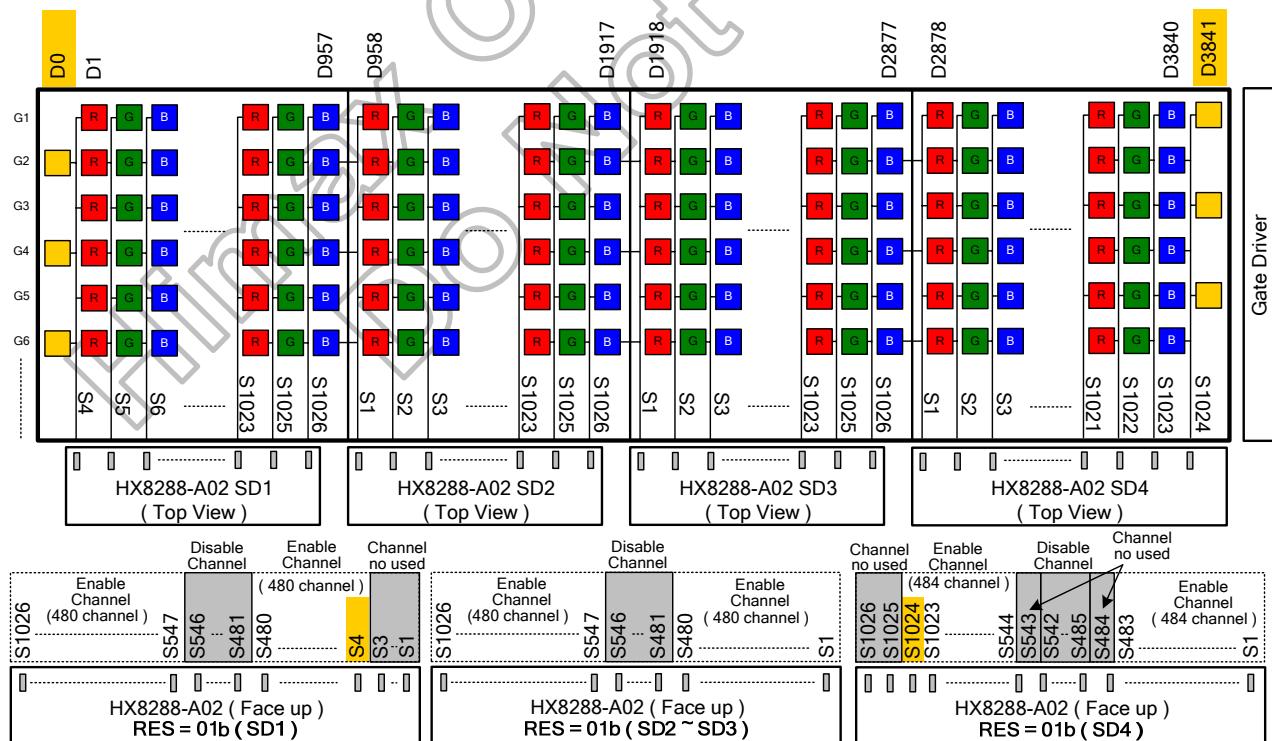


Figure 5.5: Output channel selection for Flip-Pixel M+1 type panel structure of 1280 RGB with 4 SD

- **Flip-Pixel M+3 panel structure: 1280 RGB with 4 SD.**

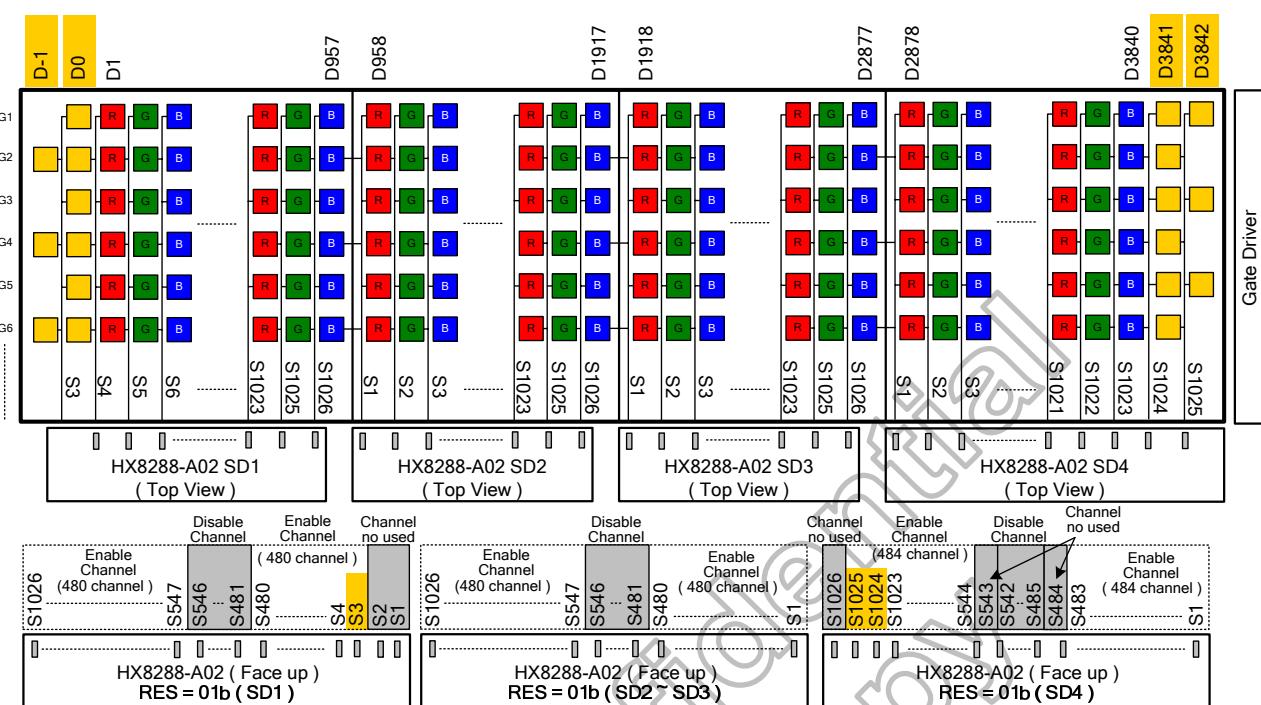


Figure 5.6: Output channel selection for Flip-Pixel M+3 type panel structure of 1280 RGB with 4 SD

- **Normal type panel structure : 1024 RGB with 4 SD.**

(1024 RGB resolution with 4 SD don't support Flip-Pixel M+1 and Flip-Pixel M+3 panel structure)

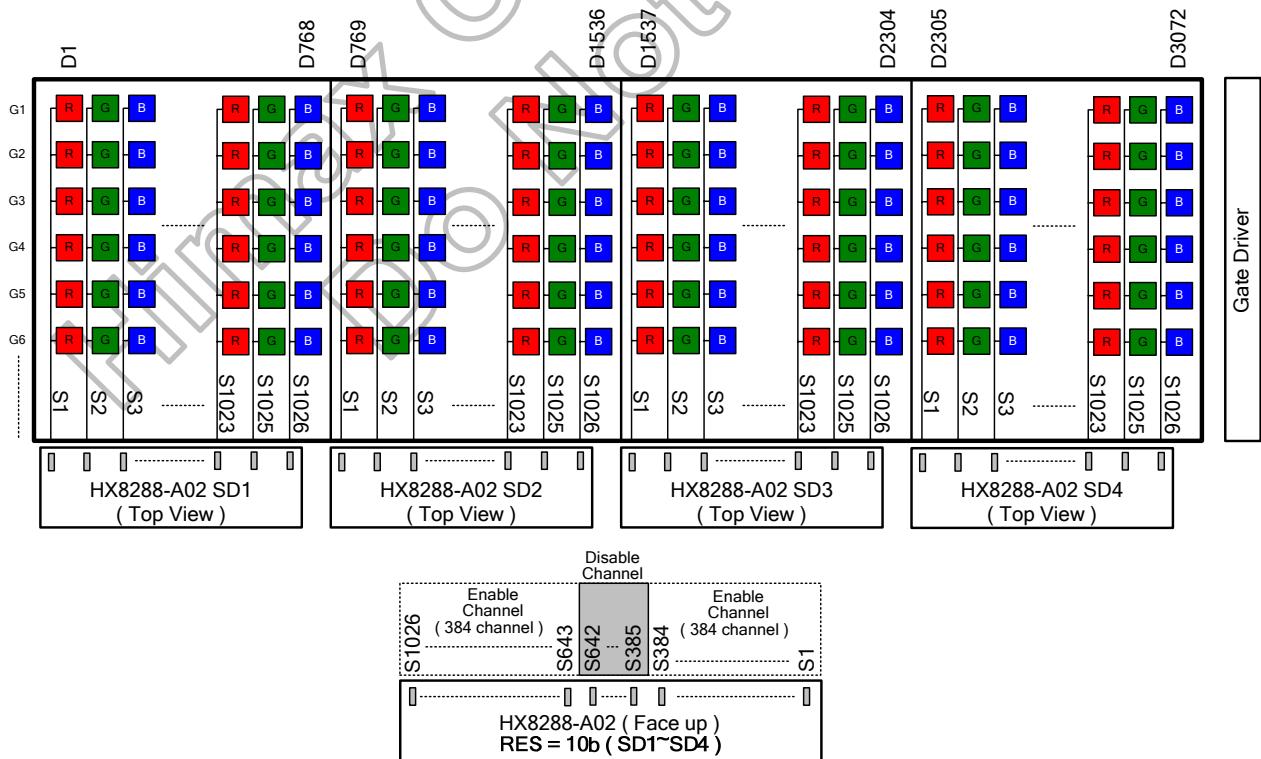


Figure 5.7: Output channel selection for normal type panel structure of 1024 RGB with 4 SD

- Normal type panel structure: 1024 RGB with 3 SD.

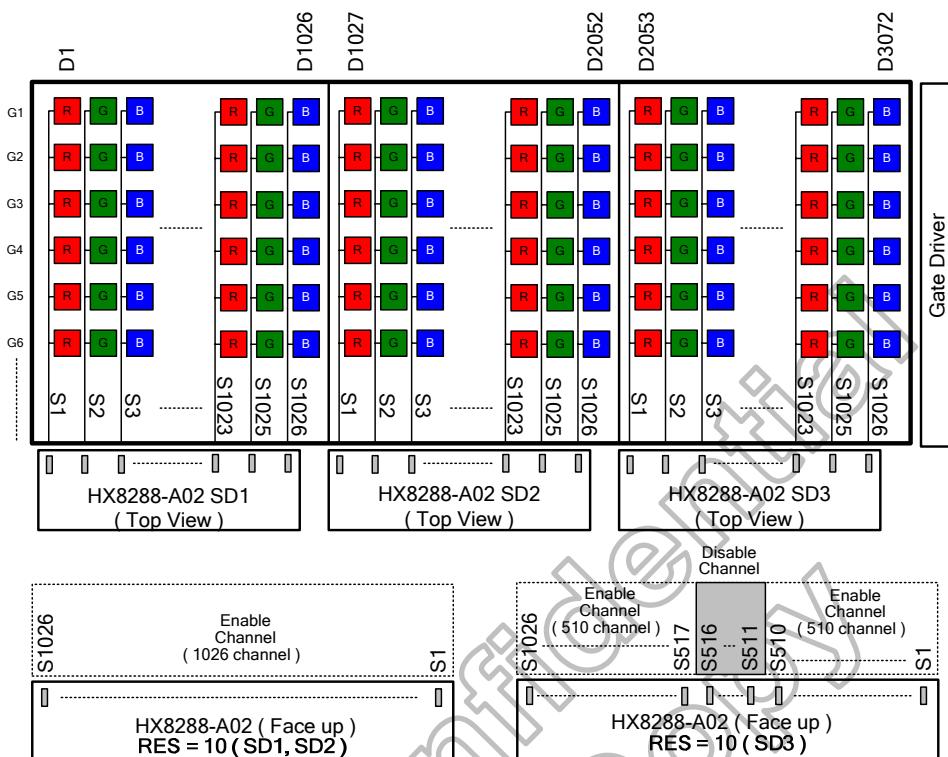


Figure 5.8: Output channel selection for normal type panel structure of 1024 RGB with 3 SD

- Flip-Pixel M+1 panel structure: 1024 RGB with 3 SD.

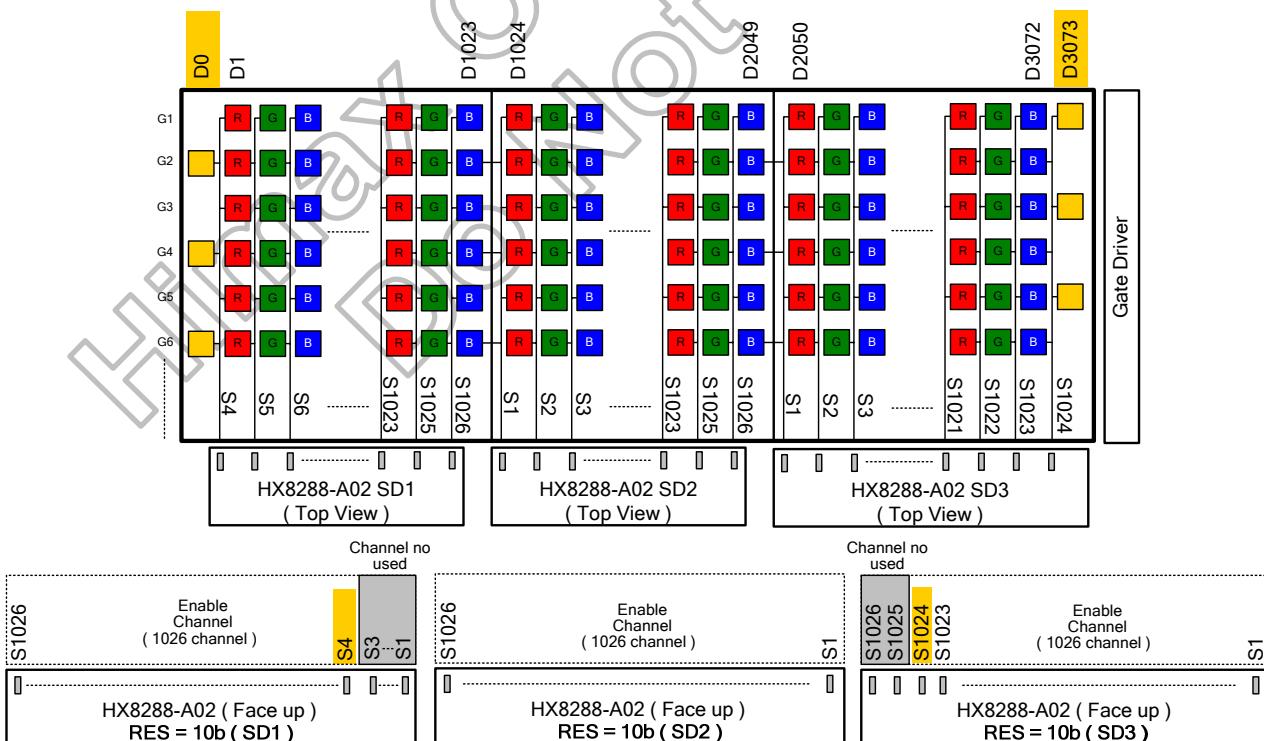


Figure 5.9: Output channel selection for Flip-Pixel M+1 type panel structure of 1024 RGB with 3 SD

- **Flip-Pixel M+3 panel structure: 1024 RGB with 3 SD.**

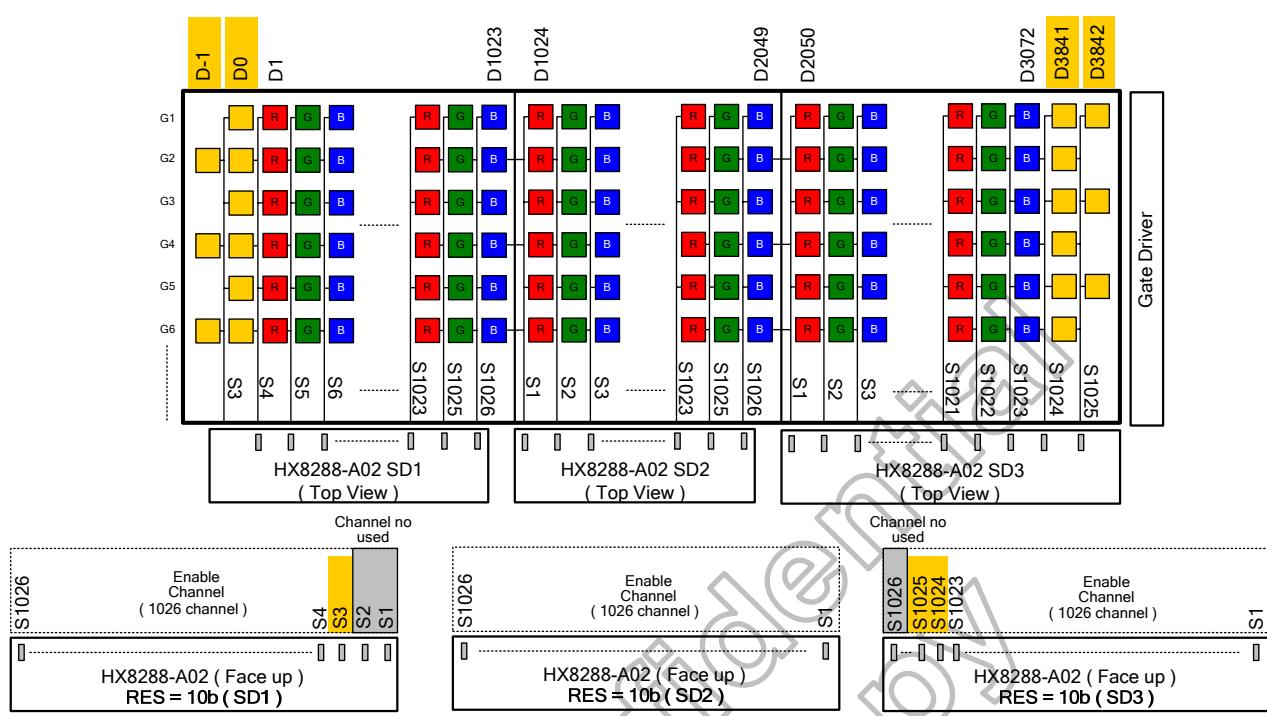


Figure 5.10: Output channel selection for Flip-Pixel M+3 type panel structure of 1024 RGB with 3 SD

5.1.2 Display configuration of resolution 1366 RGB with 4 SD

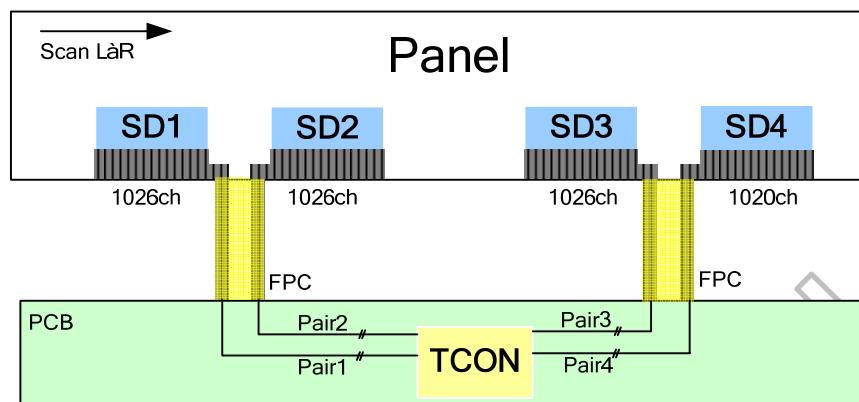
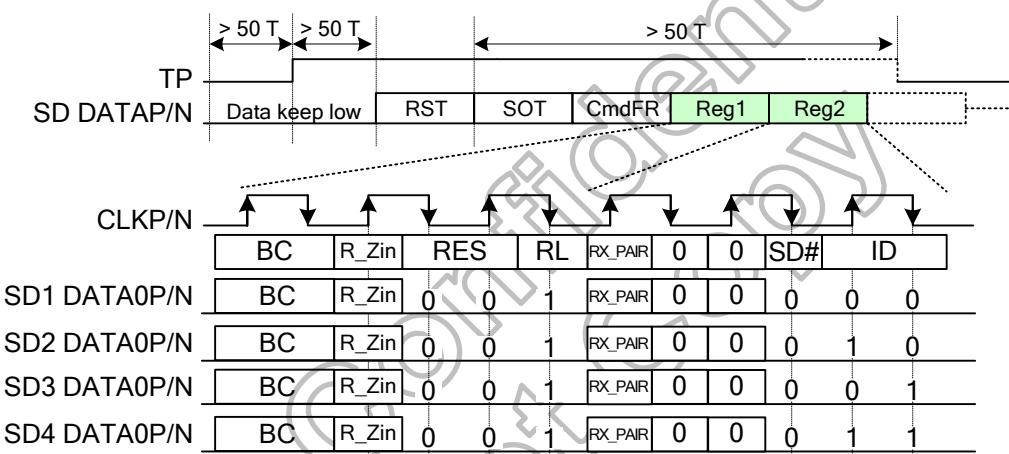


Figure 5.11: Display configuration for resolution 1366 RGB with 4 SD



Note: (1) SD1~SD4 DATA1 P/N is doesn't care.

(2) T is CLK P/N period time.

Figure 5.12: Packet format for resolution 1366 RGB with 4 SD

5.1.3 Display configuration of resolution 1280 RGB with 4 SD

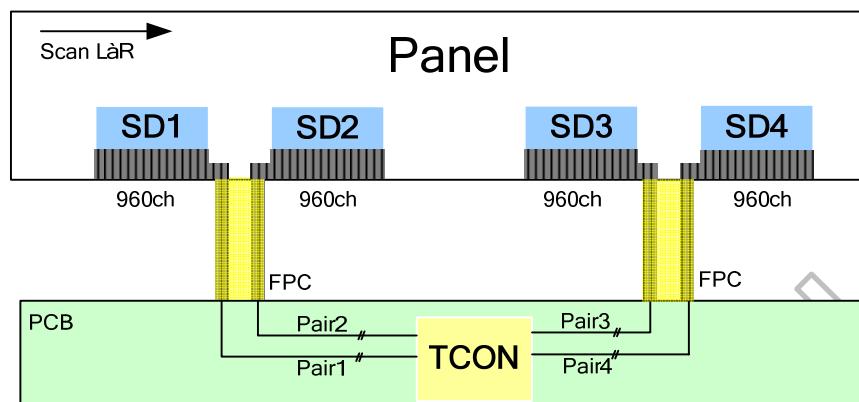
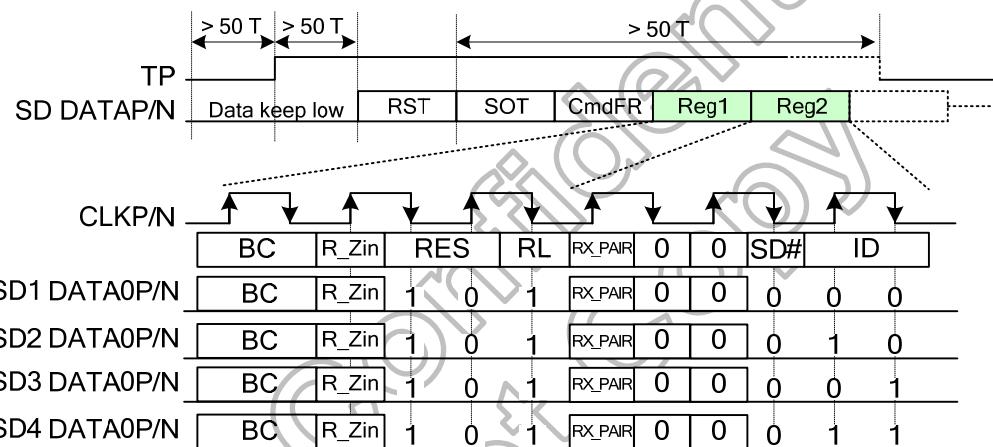


Figure 5.13: Display configuration for resolution 1280 RGB with 4 SD



Note: (1) SD1~SD4 DATA1 P/N is doesn't care.
(2) T is CLK P/N period time.

Figure 5.14: Packet format for resolution 1280 RGB with 4 SD

5.1.4 Display configuration of resolution 1024 RGB with 4 SD

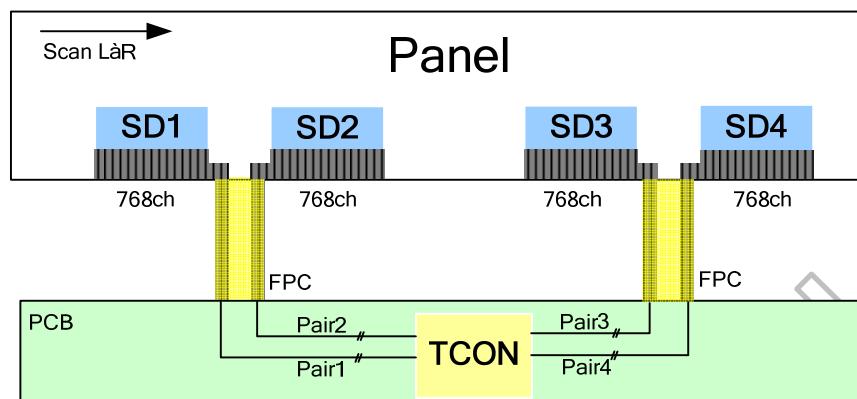
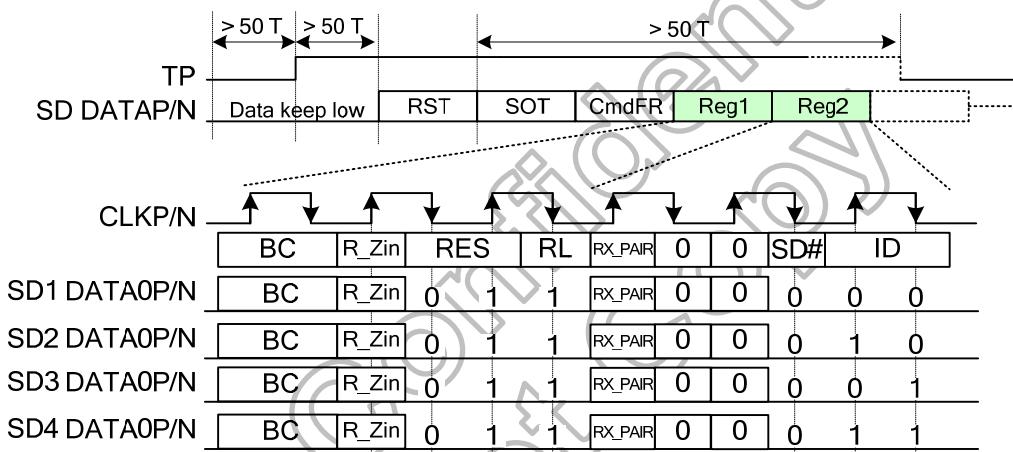


Figure 5.15: Display configuration for resolution 1024 RGB with 4 SD



Note: (1) SD1~SD4 DATA1 P/N is doesn't care.

(2) T is CLKP/N period time.

Figure 5.16: Packet format for resolution 1024 RGB with 4 SD

5.1.5 Display configuration of resolution 1024 RGB with 3 SD

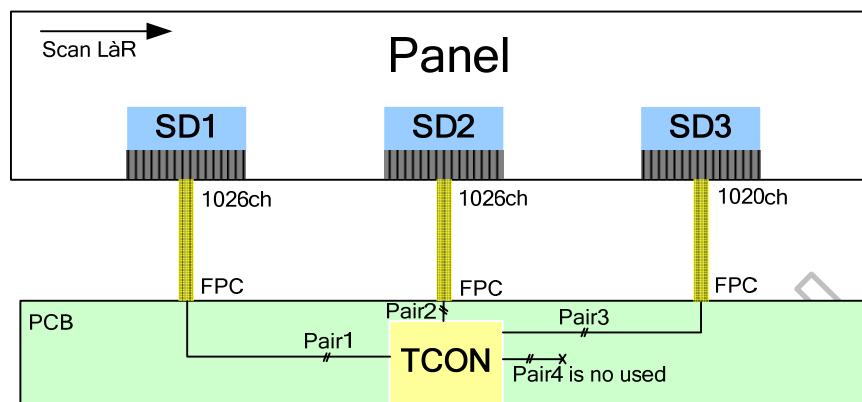
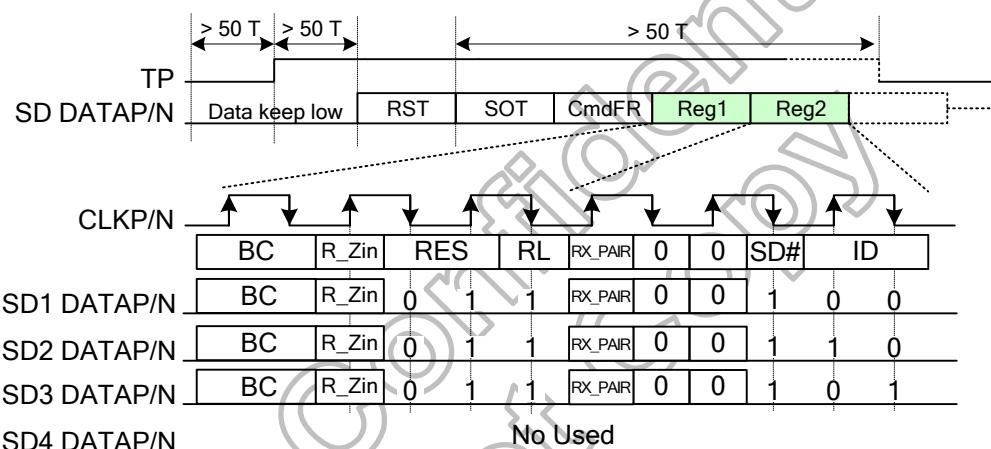


Figure 5.17: Display configuration for resolution 1024 RGB with 3 SD



Note: (1) SD1~SD3 DATA1 P/N is doesn't care.
(2) T is CLKP/N period time.

Figure 5.18: Packet format for resolution 1024 RGB with 3 SD

6. Gamma Adjustment Function

6.1 Gamma table

The figure below shows the relationship between the input data and the output voltage. Refer to the following pages for the relative resistor values and voltage calculation method.

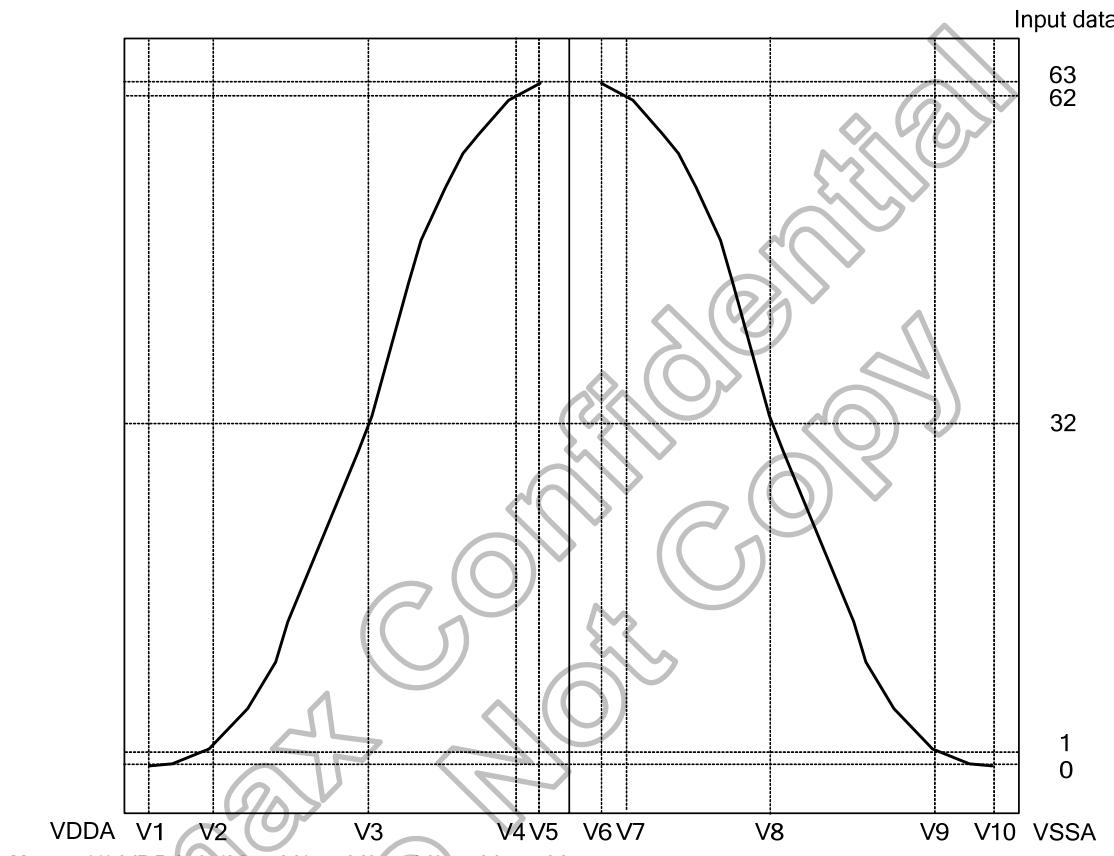


Figure 6.1: Gamma curve

6.2 Gamma correction resistor with GAMSEL=1

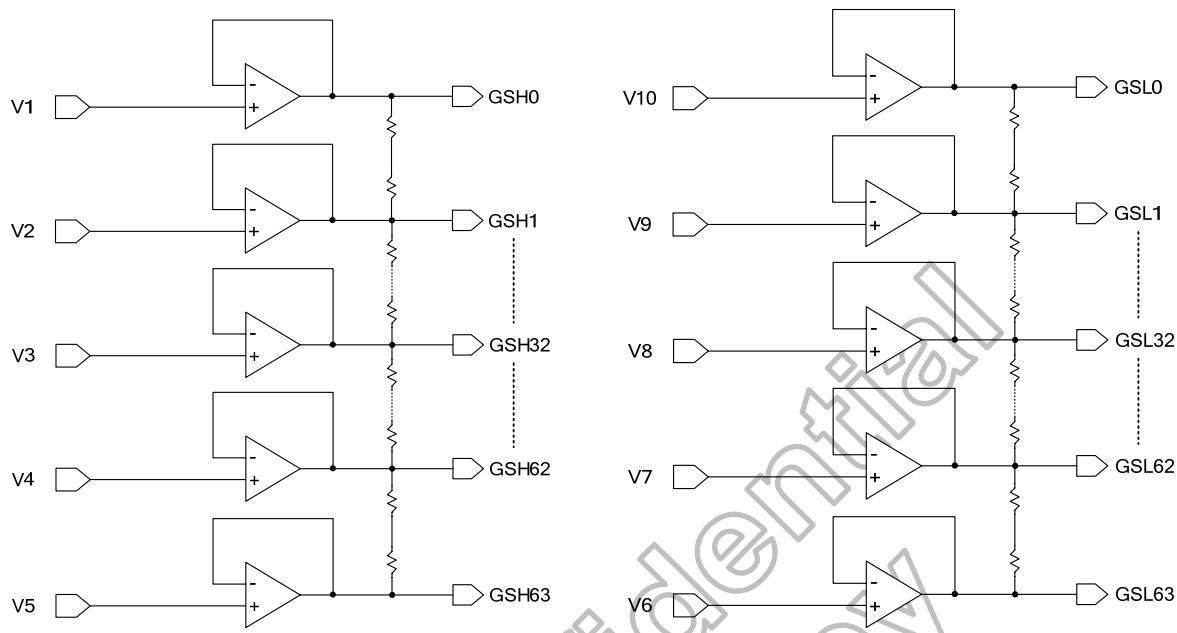


Figure 6.2: Gamma correction resistor with GAMSEL=1

6.3 Gamma correction resistor with GAMSEL=0

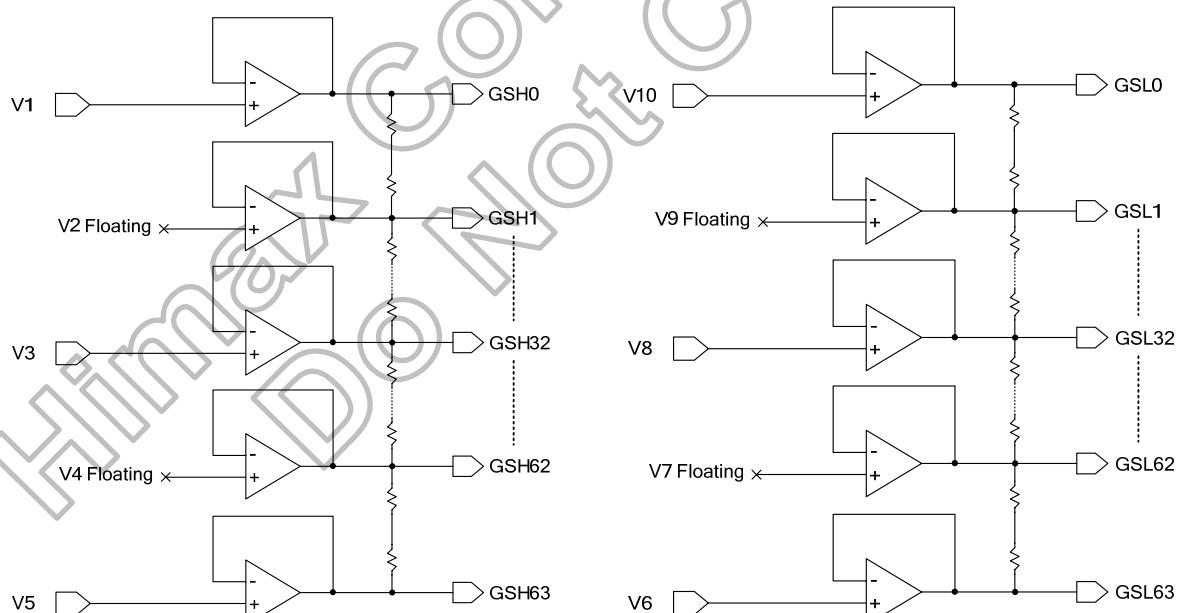


Figure 6.3: Gamma correction resistor with GAMSEL=0

6.4 Resistor table

Positive polarity

Name	Resistor Value (ohm)	
V1 → R0	1233	
V2 → R1	891	
R2	702	
R3	612	
R4	540	
R5	468	
R6	414	
R7	387	
R8	360	
R9	342	
R10	324	
R11	297	
R12	279	
R13	261	
R14	252	
R15	234	
R16	234	
R17	225	
R18	216	
R19	207	
R20	207	
R21	216	
R22	198	
R23	180	
R24	171	
R25	162	
R26	153	
R27	153	
R28	153	
R29	144	
R30	144	
R31	144	
R32	144	V3 ←
R33	144	
R34	153	
R35	153	
R36	153	
R37	162	
R38	162	
R39	162	
R40	171	
R41	180	
R42	198	
R43	180	
R44	180	
R45	180	
R46	189	
R47	198	
R48	198	
R49	216	
R50	243	
R51	270	
R52	288	
R53	324	
R54	360	
R55	387	
R56	414	
R57	468	
R58	558	
R59	666	
R60	900	
R61	1413	V4 ←
R62	1404	V5 ←

Negative polarity

Name	Resistor Value (ohm)	
R0	1233	V10
R1	891	V9
R2	702	
R3	612	
R4	540	
R5	468	
R6	414	
R7	387	
R8	360	
R9	342	
R10	324	
R11	297	
R12	279	
R13	261	
R14	252	
R15	234	
R16	234	
R17	225	
R18	216	
R19	207	
R20	207	
R21	216	
R22	198	
R23	180	
R24	171	
R25	162	
R26	153	
R27	153	
R28	153	
R29	144	
R30	144	
R31	144	
R32	144	V8
R33	144	
R34	153	
R35	153	
R36	153	
R37	162	
R38	162	
R39	162	
R40	171	
R41	180	
R42	198	
R43	180	
R44	180	
R45	180	
R46	189	
R47	198	
R48	198	
R49	216	
R50	243	
R51	270	
R52	288	
R53	324	
R54	360	
R55	387	
R56	414	
R57	468	
R58	558	
R59	666	
R60	900	
R61	1413	V7
R62	1404	V6

7. Power Function and Power On/Off Sequence

To prevent the device damage from latch up, the power on/off sequence shown below must be followed.

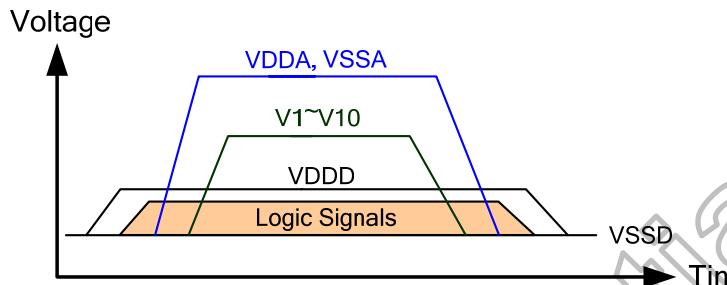
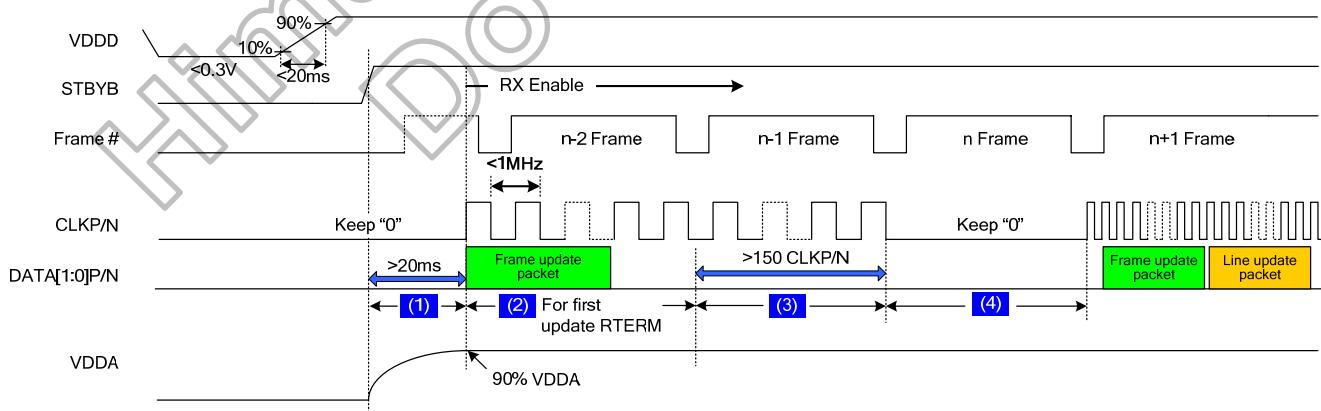


Figure 7.1: Power on/off sequence

7.1 Power on/off control

HX8288-A02 has a power on/off sequence control function. In order to prevent IC from power on reset fail, the rising time of the digital power supply VDDD should be maintained within the given specifications.

- (1). Settling time must be great than 20ms for RX bias settling down consideration. The CLKP/N can't send any clock signal within the duration.
- (2). First frame update packet decides the termination resistor. For make sure RTERM register update, the frequency CLKP/N should be much less than normal operation one (**recommend < 1MHz**).
- (3). This is waiting for load 8bit fuse after load first frame update packet.
- (4). Before valid data update, the CLKP/N will transit from slow-clock to fast-clock, so CLKP/N should keep low within the duration.

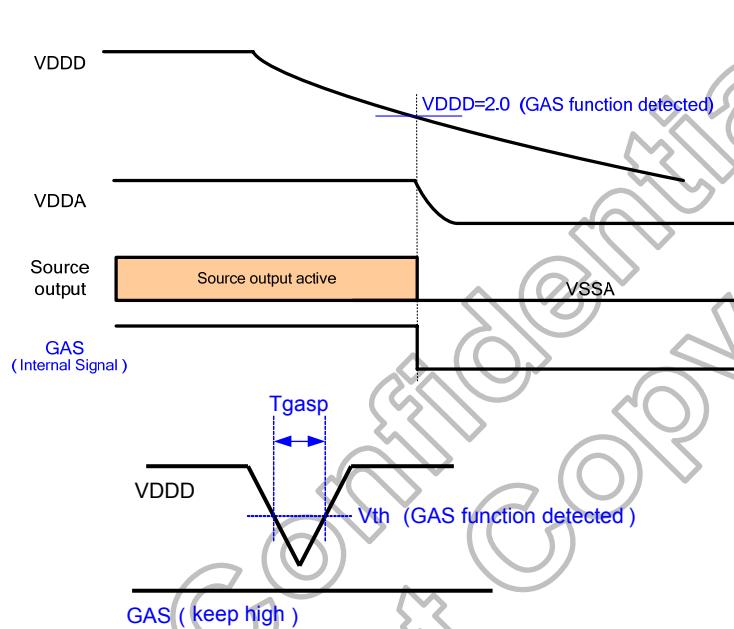


Note: (1) "frame n" is based on power on sequence of TCON.

Figure 7.2: Power on/off timing sequence

7.2 Power supply drop detection (GAS function)

- When user doesn't follow power off sequence and power down directly, HX8288-A02 built in GAS function can be used to improve panel discharge and prevent the image sticking issue.
- When VDDD is lower than 2.0V, HX8288-A02 will activate GAS function.
- If the period (T_{gasp}), which is pulse during $VDDD < 2.0V$, is smaller than 100ns, HX8288-A02 will ignore it and GAS function would not be executed.



Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Note
T_{gasp}	VDDD power drop noise filter period.	-	100	-		ns	-
V_{th}	GAS function detection threshold voltage. If VDDD lower than V_{th} , IC will execute GAS function.	-	1.8	-	2.2	V	-

8. DC Characteristics

8.1 Absolute maximum rating (VSSD=VSSA=0V)

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Power supply voltage 1	VDDD	-0.5	-	+3.96	V
Power supply voltage 2	VDDA	-0.5	-	+14.85	V
Logic Output Voltage	V _{OUT}	-0.5	-	+5.0	V
Input voltage	V _{IN}	-0.5	-	VDDA+0.5	V
Operation temperature	T _{OPR}	-20	-	+85	°C
Storage temperature	T _{STG}	-55	-	+125	°C

Note: (1) All of the voltages listed above are with respective to VSSD=0V.

(2) Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

Table 8.1: Absolute maximum rating

8.2 Recommended operating range

(VSSD=VSSA=0V, TA=-20°C to 85°C)

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Digital supply voltage	VDDD	2.3	-	3.6	V
Analog supply voltage	VDDA	6	-	13.5	V
Digital input voltage	V _{IN}	0	-	VDDD	V

8.3 PBPI DC electrical characteristics

(VDDD=2.3 to 3.6V, VDDA=6 to 13.5V, VSSD=VSSA=0V, TA= -20°C ~+85°C)

Parameter	Symbol	Spec.			Unit	Condition
		Min.	Typ.	Max.		
Power supply voltage	VDDD	2.3	-	3.6	V	-
Power supply voltage	VDDA	6	-	13.5	V	-
Low level input voltage	V _{IL}	0	-	0.3VDDD	V	For digital circuit
High level input voltage	V _{IH}	0.7VDDD	-	VDDD	V	For digital circuit
Output low voltage	V _{OL}	-	-	GND+0.4	V	I _{OL} =400μA
Output high voltage	V _{OH}	VDDD-0.4	-	-	V	I _{OH} =-400μA
Pull low/high resistance	R _i	200	300	500	kΩ	For the digital input pin
Input leakage current	I _i	-	-	±1	uA	For digital circuit
Digital Operation current	I _{dd}	-	6.7		mA	CLKP/N=150MHz, VDDD=3.3V
Digital stand-by current	I _{st1}	-	30		μA	Clock & all functions are stopped
Analog Operating current	I _{dda}	-	5	-	mA	CLKP/N=150MHz, VDDD=3.3V, VDDA=10V, V1=8V, V10=0.4V, No load.
Analog Stand-by current	I _{st2}	-	30	-	μA	clock & all functions are stopped, No load.
Input level of V1 and V5	V _{ref1}	0.4VDDA	-	VDDA-0.1	V	Gamma correction voltage input
Input level of V6 and V10	V _{ref2}	0.1	-	0.6VDDA	V	Gamma correction voltage input
Output Voltage deviation	V _{od1}	-	-	±30	mV	Vo=VSSA+0.1V~VSSA+0.5V & Vo=VDDA-0.5V~VDDA-0.1V
Output Voltage deviation	V _{od2}	-	-	±20	mV	Vo=VSSA+0.5V~VDDA-0.5V
Output Voltage Offset between Chips	V _{oc}	-	-	±35	mV	Vo=VSSA+0.5V~VDDA-0.5V
Dynamic Range of Output	V _{dr}	0.1	-	VDDA-0.1	V	S1~S1026
Sinking Current of Outputs	I _{OLy}	I-80	-	-	μA	S1~S1026; Vo=0.1V vs. 1.0V, VDDA=13.5V
Driving Current of Outputs	I _{OHy}	80	-	-	μA	S1~S1026 ;Vo=12.5V vs. 13.4V, VDDA=13.5V
Resistance of Gamma Table	R _g	0.7*R _n	1.0*R _n	1.3*R _n	Ω	R _n : Internal gamma resistor

Table 8.2: DC electrical characteristics

8.4 PBPI characteristics

(VDDD=2.3 to 3.6V, VDDA=8 to 13.5V, VSSD=VSSA=0V, TA=-20°C ~+85°C)

Parameter	Symbol	Spec.			Unit	Condition
		Min.	Typ.	Max.		
PBPI interface differential voltage (amplitude: peak to peak)	V_{ID}	100	-	400	mV	Clock and data input pair pin.
PBPI interface common mode input voltage range (center)	V_I	0.7V	-	VDDD-1.3	V	Clock and data input pair pins.
Input voltage range (singled-end)	V_{in}	0.3V	-	$VDDD-1.3 + V_{ID} /2$	V	-
Differential input leakage Current	RV_{Xliz}	-10	-	+10	μA	-

Table 8.3: PBPI interface DC electrical characteristics

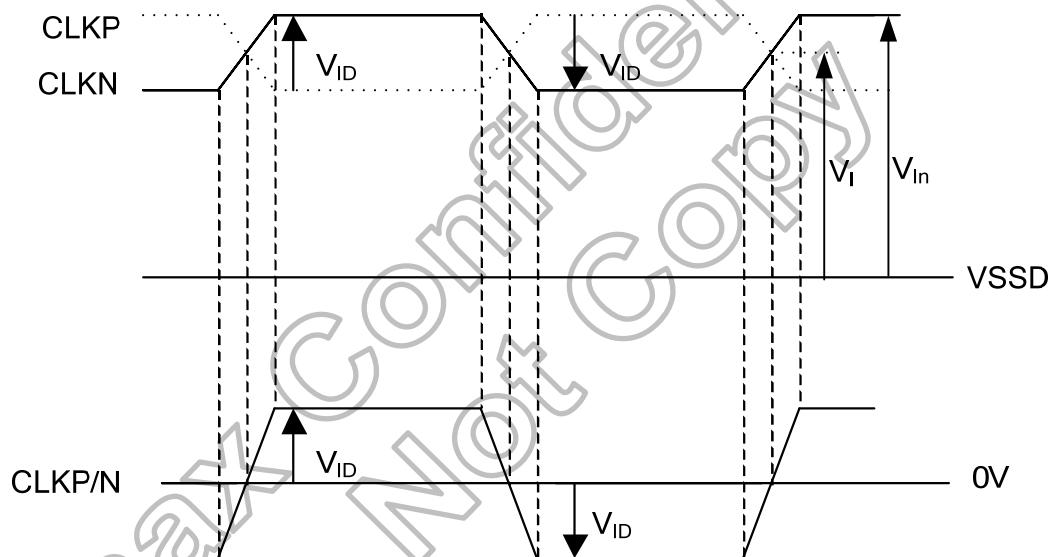


Figure 8.1: PBPI interface differential AC electrical characteristics

9. AC Characteristics

9.1 PBPI AC electrical characteristics

Parameter	Symbol	Spec.			Unit	Condition
		Min.	Typ.	Max.		
VDDD Power On Slew rate	T_{POR}	-	-	5	ms	From 0V to 90% VDDD
RESETB pulse width	T_{Rst}	10	-	-	us	-
CLKP/N cycle time	T_{cph}	6.67	-	-	ns	150MHz
CLKP/N pulse duty	T_{cwh}	42	50	58	%	-
Data set-up time	T_{dsu}	2.65	-	-	ns	DATAP/N to CLK/N
Data hold time	T_{dhd}	-	-	0.85	ns	DATAP/N to CLK/N
Output stable time	T_{sst}	-	-	10	μs	10% to 90% target voltage CL=125pF, R=10K ohm

Table 9.1: PBPI interface AC electrical characteristics

10. Timing Waveform

10.1 Input clock and data timing diagram

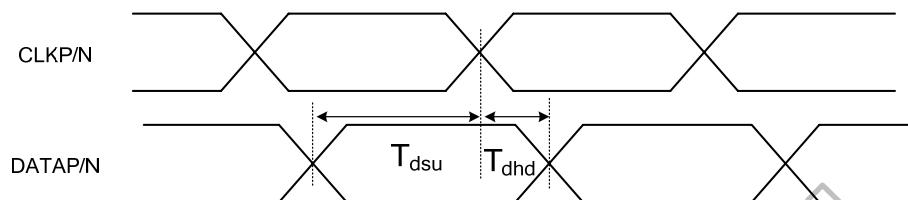


Figure 10.1: Input clock and data timing diagram

10.2 Timing Requirements for RESETB



Figure 10.2: RESETB timing diagram

10.3 Source output timing diagram

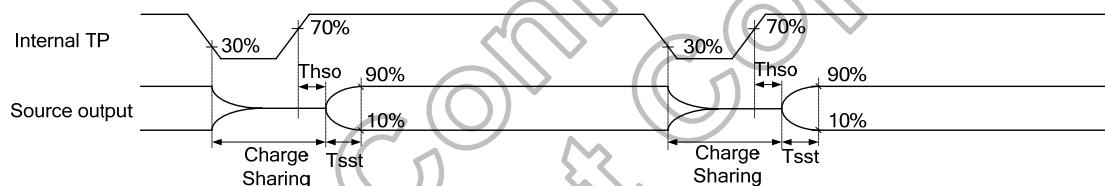


Figure 10.3: Source output timing diagram

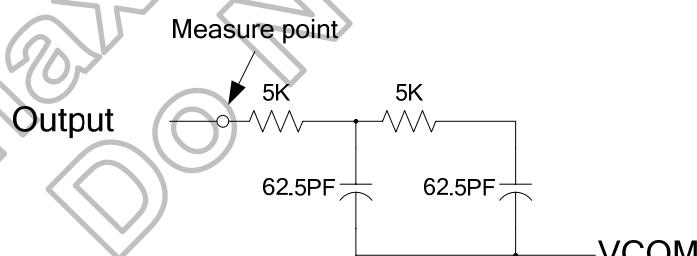


Figure 10.4: Output load condition

11. Pin Assignment (IC Face View)

11.1 PAD sequence

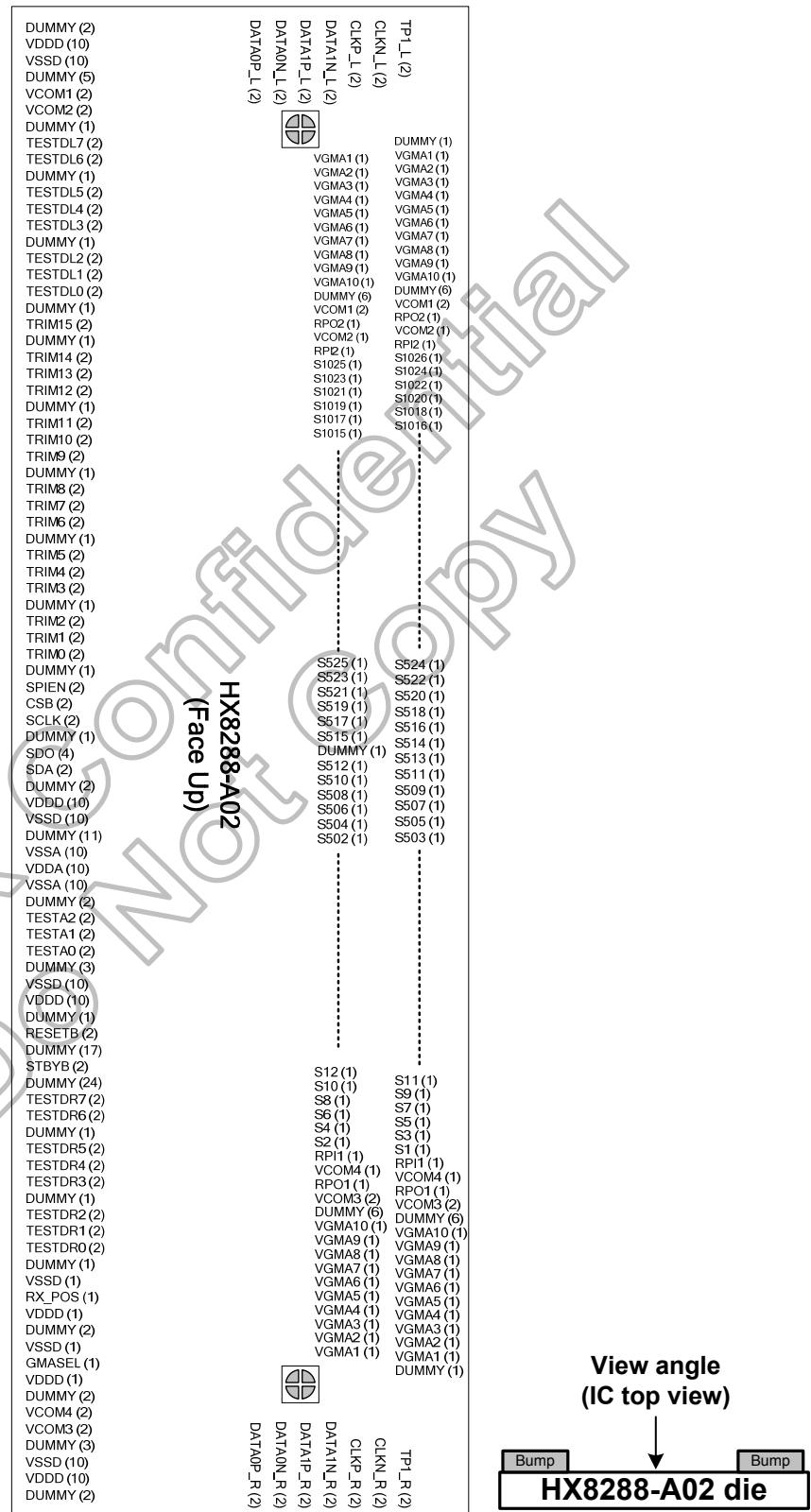


Figure 11.1: Pad sequence

11.2 Bump information

11.2.1 Chip outline dimensions

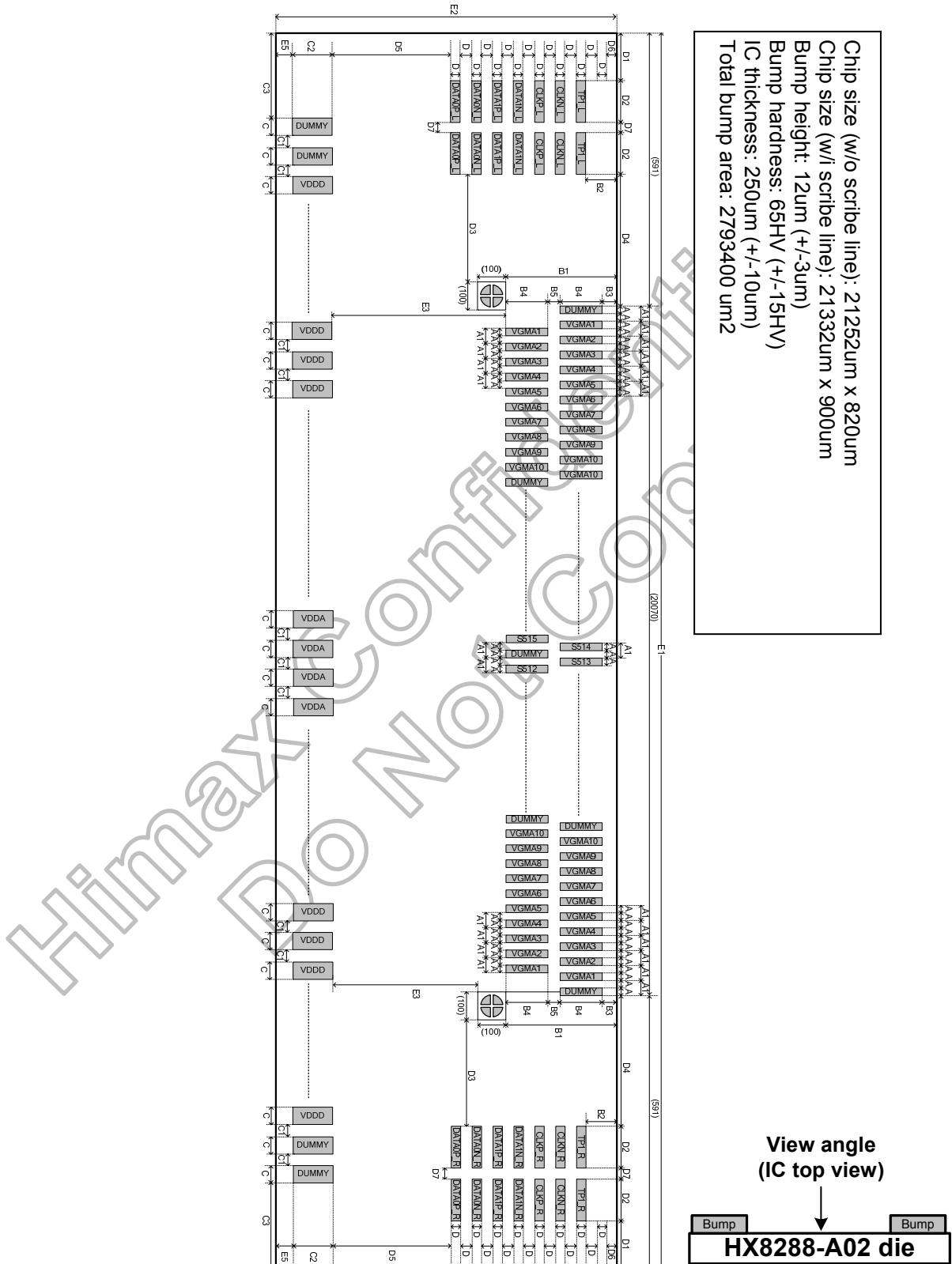


Figure 11.2: Chip outline dimensions

11.2.2 Alignment mark

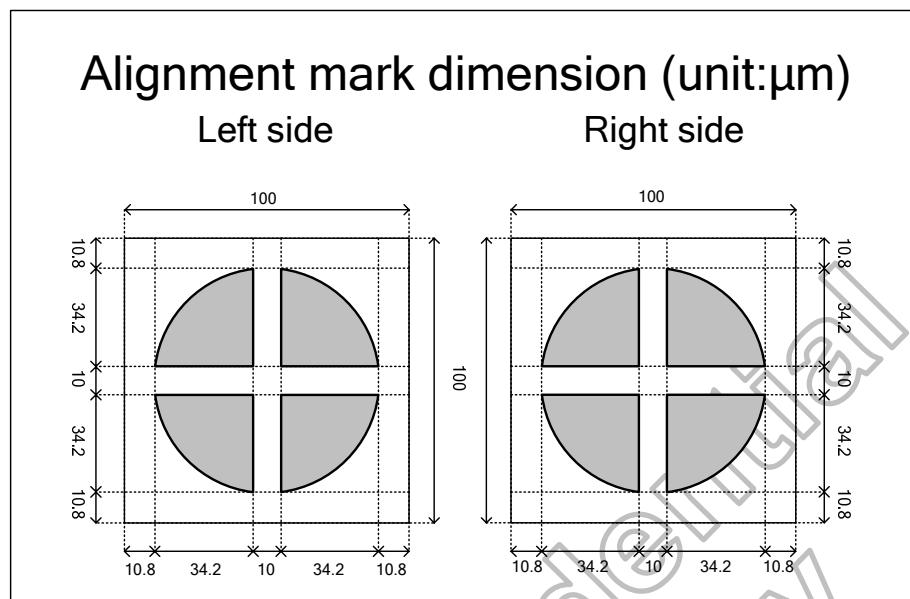


Figure 11.3: Alignment mark

11.2.3 Pad information

Symbol	Dimension (um)
A	18
A1	36
C	40
C1	30
C2	60
C3	141
B1	265
B2	72.5
B3	35
B4	100
B5	30

Symbol	Dimension (um)
D	25
D1	50
D2	100
D3	225
D4	316
D5	317.5
D6	22.5
D7	25
E1	21252
E2	820
E3	450
E5	45

Table 11.1: Pad information

11.3 Pad coordinates

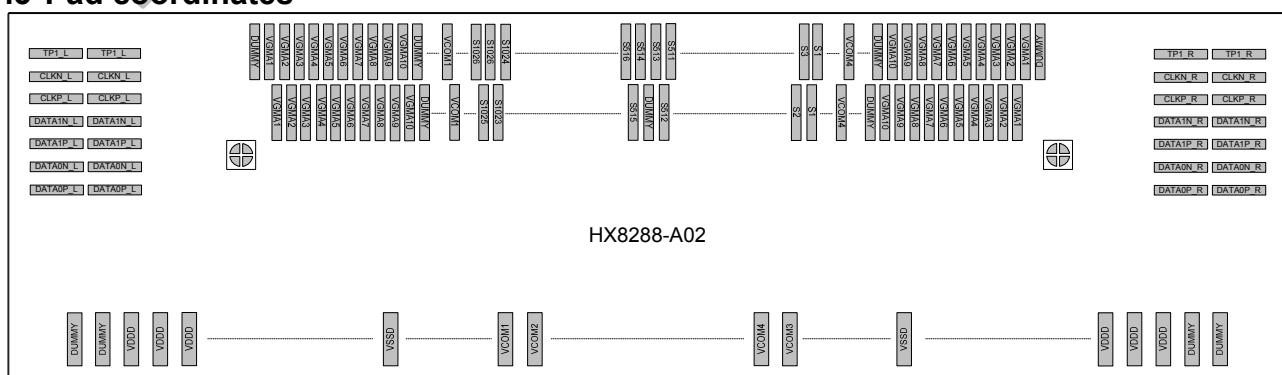


Figure 11.4: Pad coordinate

No.	Name	X	Y	Bump size(μm)
1401	DUMMY	-9540	195	18 x 100
1402	DUMMY	-9558	325	18 x 100
1403	DUMMY	-9576	195	18 x 100
1404	DUMMY	-9594	325	18 x 100
1405	DUMMY	-9612	195	18 x 100
1406	DUMMY	-9630	325	18 x 100
1407	VGMA10	-9648	195	18 x 100
1408	VGMA10	-9666	325	18 x 100
1409	VGMA9	-9684	195	18 x 100
1410	VGMA9	-9702	325	18 x 100
1411	VGMA8	-9720	195	18 x 100
1412	VGMA8	-9738	325	18 x 100
1413	VGMA7	-9756	195	18 x 100
1414	VGMA7	-9774	325	18 x 100
1415	VGMA6	-9792	195	18 x 100
1416	VGMA6	-9810	325	18 x 100
1417	VGMA5	-9828	195	18 x 100
1418	VGMA5	-9846	325	18 x 100
1419	VGMA4	-9864	195	18 x 100
1420	VGMA4	-9882	325	18 x 100
1421	VGMA3	-9900	195	18 x 100
1422	VGMA3	-9918	325	18 x 100
1423	VGMA2	-9936	195	18 x 100
1424	VGMA2	-9954	325	18 x 100
1425	VGMA1	-9972	195	18 x 100
1426	VGMA1	-9990	325	18 x 100
1427	DUMMY	-10026	325	18 x 100
1428	CLKP_L	-10401	225	100 x 25
1429	CLKN_L	-10401	275	100 x 25
1430	TP1_L	-10401	325	100 x 25
1431	TP1_L	-10526	325	100 x 25
1432	CLKN_L	-10526	275	100 x 25
1433	CLKP_L	-10526	225	100 x 25
1434	DATA1N_L	-10526	175	100 x 25
1435	DATA1N_L	-10401	175	100 x 25
1436	DATA1P_L	-10526	125	100 x 25
1437	DATA1P_L	-10401	125	100 x 25
1438	DATA0N_L	-10526	75	100 x 25
1439	DATA0N_L	-10401	75	100 x 25
1440	DATA0P_L	-10526	25	100 x 25
1441	DATA0P_L	-10401	25	100 x 25

Alignment mark			
L_AMK	-10076	95	100 x 100
R_AMK	10076	95	100 x 100

Table 11.2: Pad coordinate

12. Ordering Information

Part No.	Package Type
HX8288-A02 <u>XPD</u> xxx	X : meab fab code PD : mean COG xxx : mean chip thickness (μm)

13. Revision History

Version	Date	Description of changes
01	2012/10/29	New setup

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