S6B0086

80 CH SEGMENT / COMMON DRIVER FOR DOT MATRIX LCD

June. 2000.

Ver. 0.0

INTRODUCTION

The S6B0086 is an LCD driver LSI which is fabricated by low power CMOS high voltage process technology. In segment driver mode, it can be interfaced in 1-bit serial or 4-bit parallel method by the controller. In common driver mode, dual type mode is applicable. And in segment mode application, the power down function reduces power consumption.

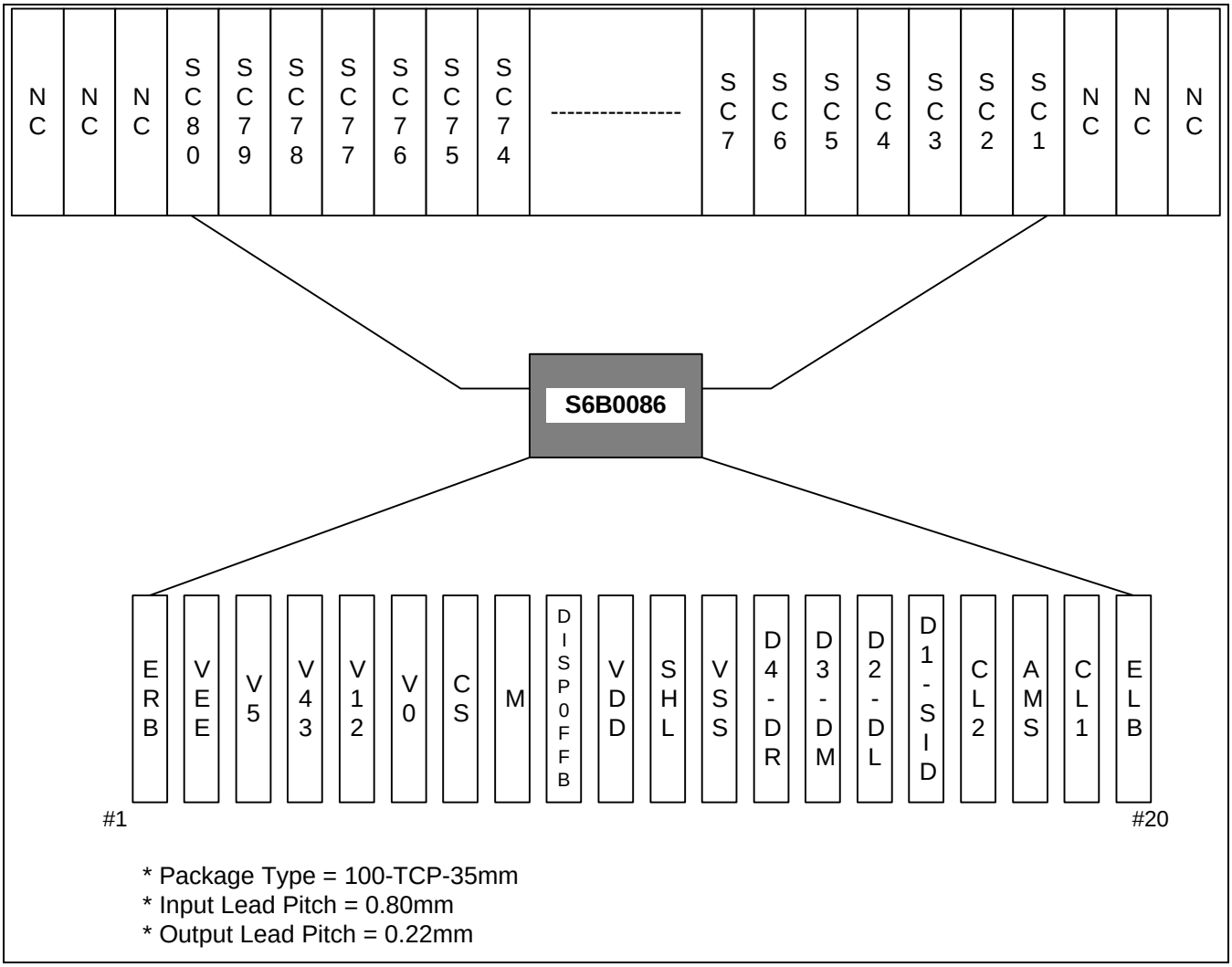
FEATURES

- Power supply voltage: + 5V ± 10 %, + 3V ± 10%
- Supply voltage for display: 6 to 28V (V_{DD}-V_{EE})
- 4-bit parallel / 1-bit serial data processing (in segment mode)
- Single mode operation / dual mode operation (in common mode)
- Power down function (in segment mode)
- Applicable LCD duty: 1/64 – 1/256
- Interface

DRIVERS	
COM (cascade)	SEG (cascade)
S6B0086	S6B0086

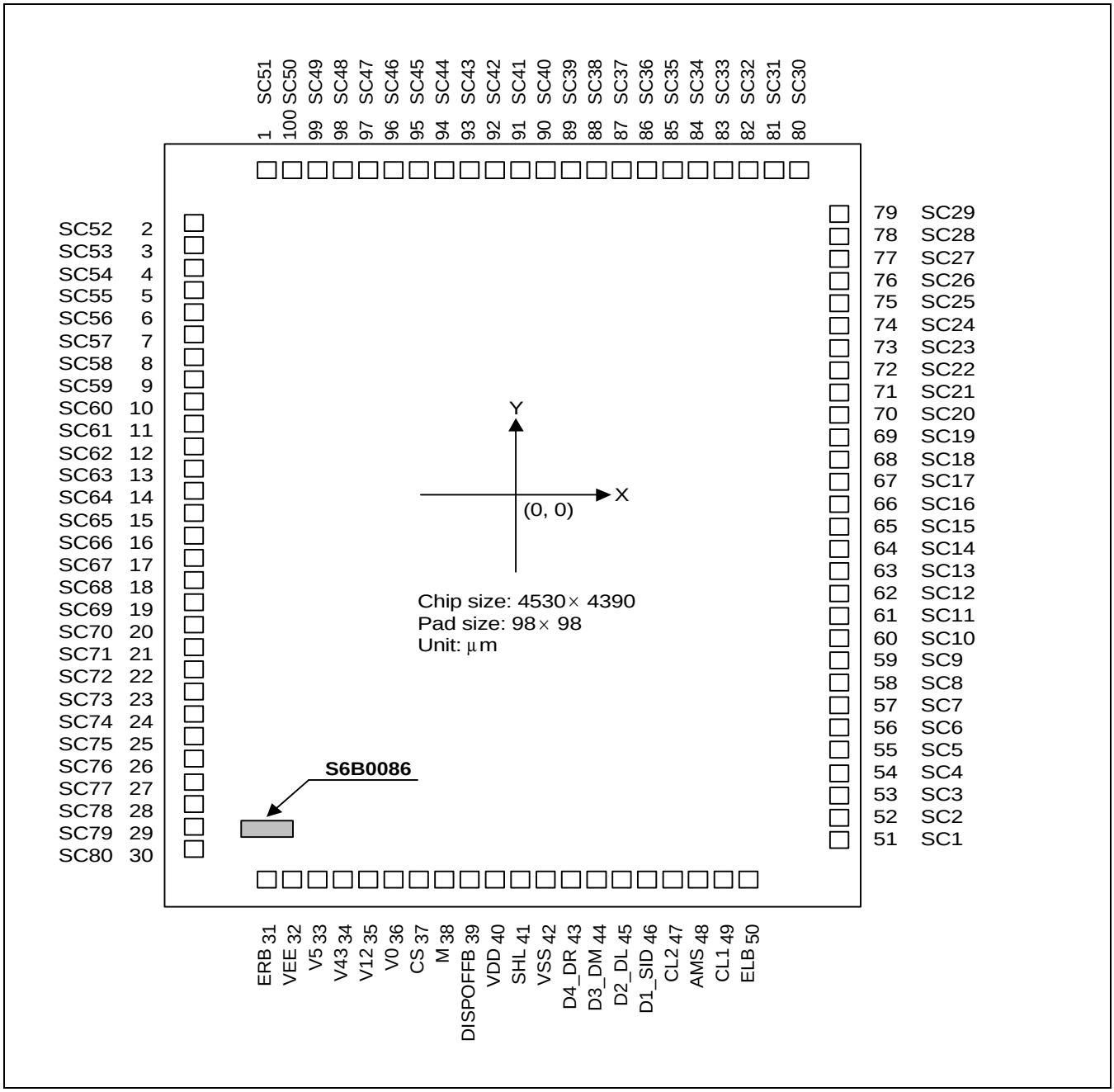
- High voltage CMOS process
- Bare die or TCP available

TCP



* Package Type = 100-TCP-35mm
* Input Lead Pitch = 0.80mm
* Output Lead Pitch = 0.22mm

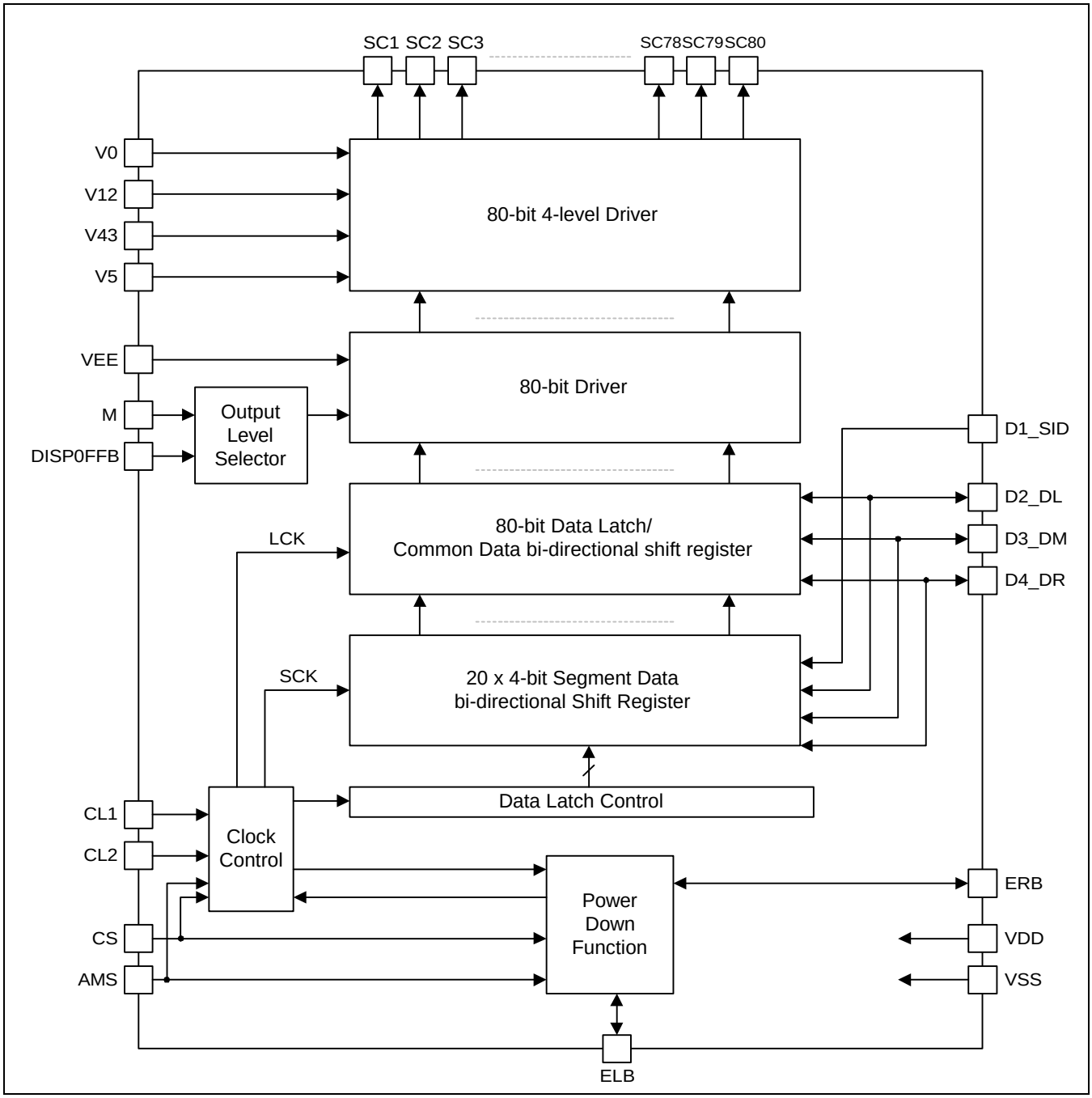
PAD DIAGRAM (S6B0086 / S6B0086 TCP)



PAD CENTER COORDINATES (S6B0086 / S6B0086TCP)

Pad No.	Pad Name	Coordinates X	Coordinates Y	Pad No.	Pad Name	Coordinates X	Coordinates Y	Pad No.	Pad Name	Coordinates X	Coordinates Y
1	SC51	-1690	1959	35	V12	-900	-1959	69	SC19	2029	544
2	SC52	-2029	1884	36	V0	-775	-1959	70	SC20	2029	678
3	SC53	-2029	1750	37	VS	-600	-1959	71	SC21	2029	812
4	SC54	-2029	1616	38	M	-475	-1959	72	SC22	2029	946
5	SC55	-2029	1482	39	DISP0FFB	-350	-1959	73	SC23	2029	1080
6	SC56	-2029	1348	40	VDD	-225	-1959	74	SC24	2029	1214
7	SC57	-2029	1214	41	SHL	-100	-1959	75	SC25	2029	1348
8	SC58	-2029	1080	42	VSS	25	-1959	76	SC26	2029	1482
9	SC59	-2029	946	43	D4_DR	266	-1959	77	SC27	2029	1616
10	SC60	-2029	812	44	D3_DM	470	-1959	78	SC28	2029	1750
11	SC61	-2029	678	45	D2_DL	711	-1959	79	SC29	2029	1884
12	SC62	-2029	544	46	D1_SID	915	-1959	80	SC30	1690	1959
13	SC63	-2029	410	47	CL2	1040	-1959	81	SC31	1529	1959
14	SC64	-2029	276	48	ELB	1165	-1959	82	SC32	1368	1959
15	SC65	-2029	142	49	CL1	1290	-1959	83	SC33	1207	1959
16	SC66	-2029	8	50	ELB	1496	-1959	84	SC34	1046	1959
17	SC67	-2029	-126	51	SC1	2029	-1884	85	SC35	885	1959
18	SC68	-2029	-260	52	SC2	2029	-1735	86	SC36	724	1959
19	SC69	-2029	-394	53	SC3	2029	-1601	87	SC37	563	1959
20	SC70	-2029	-528	54	SC4	2029	-1467	88	SC38	402	1959
21	SC71	-2029	-662	55	SC5	2029	-1333	89	SC39	241	1959
22	SC72	-2029	-797	56	SC6	2029	-1199	90	SC40	80	1959
23	SC73	-2029	-931	57	SC7	2029	-1065	91	SC41	-80	1959
24	SC74	-2029	-1065	58	SC8	2029	-931	92	SC42	-241	1959
25	SC75	-2029	-1199	59	SC9	2029	-797	93	SC43	-402	1959
26	SC76	-2029	-1333	60	SC10	2029	-662	94	SC44	-563	1959
27	SC77	-2029	-1467	61	SC11	2029	-528	95	SC45	-724	1959
28	SC78	-2029	-1601	62	SC12	2029	-394	96	SC46	-885	1959
29	SC79	-2029	-1735	63	SC13	2029	-260	97	SC47	-1046	1959
30	SC80	-2029	-1884	64	SC14	2029	-126	98	SC48	-1207	1959
31	ERB	-1479	-1959	65	SC15	2029	8	99	SC49	-1368	1959
32	VEE	-1275	-1959	66	SC16	2029	142	100	SC50	-1529	1959
33	V5	-1150	-1959	67	SC17	2029	276				
34	V43	-1025	-1959	68	SC18	2029	410				

BLOCK DIAGRAM



BLOCK DESCRIPTION

Name	Function	COM / SEG
Clock control	Generates latch clock (LCK), shift clock (SCK) and control clock timing according to the input of CL1, CL2 and control inputs (CS, AMS). In common driver application mode, this block generates the shift clock (LCK) for the common data Bi-directional shift register.	COM / SEG
Data latch control	Determines the direction of segment data shift, and input data of each Bi-directional shift register. In 4-bit segment data parallel transfer mode, data is shifted by a 4-bit unit. In common driver application mode, data is transferred to the common data shift register directly, which disables this block.	SEG
Power down function	Controls the clock enable state of the current driver according to the input value of enable pin (ELB or ERB). If enable input value is “Low”, every clock of the current driver is enabled and the clock control block works. But if enable input is “High”, current driver is disabled and the input data value has no effect on the output level. So power consumption can be lowered.	SEG
Output level selector	Controls the output voltage level according to the input control pin (M and DISPOFFB) (refer to PIN DESCRIPTION).	COM / SEG
20x4-bit segment data I-directional shift register	Stores output data value by shifting the input values. In 1-bit serial interface mode application, all 80 shift clocks (SCK) are needed to store all the display data. But in 4-bit parallel transfer mode application, only 20 clocks are needed. In common driver application mode, this block does not work.	SEG
80-bit data latch / common data I-directional shift register	In segment driver application mode, the data from the 20x4-bit segment data shift register are latched for segment driver output. In single-type common driver application,1-bit input data (from DL or DR pin) is shifted and latched by the direction according to the SHL signal input. In dual-type common application mode, 80-bit registers are divided by two blocks and controlled independently (refer to NOTE 3).	COM / SEG
80-bit level shifter	Voltage level shifter block for high voltage part. The inputs of this block are of logical voltage level and the outputs of this block are at high voltage level value. These values are input in to the driver.	SEG
80-bit 4-level driver	Selects the output voltage level according to M and latched data value. If the data value is "High" the driver output is at selected voltage level (V0 or V5), and in the reverse case the driver output value is at the non-selected level (V12 or V43). In segment driver application mode, non-selected output value is V2 or V3. and when in common driver application, this value becomes V1 or V4.	SEG

PIN DESCRIPTION

Pin	I / O	Name	Function	Interface
VDD		Power supply	Logical "High" input port (+5V ± 10%, +3V ± 10%)	Power
VSS			0V (GND)	
VEE			Logical "Low" for high voltage part	
V0, V12, V43, V5	I	LCD driver output voltage level	Bias supply voltage input to drive the LCD. Bias voltage divided by the resistance is usually used as a supply voltage source (refer to NOTE 2).	Power
SC1 - SC80	O	LCD driver output	Display data output pin which corresponds to the respective latch contents. One of V0, V12, V34 and V5 is selected as a display driving voltage source according to the combination of the latched data level and M signal (refer to NOTE 1).	LCD
CL2	I	Data shift clock	Clock pulse input for the bi-directional shift register. – In segment driver application mode, the data is shifted to 20 x 4-bit segment data shift The clock pulse, which was input when the enable bit (ELB/ERB) is in not active condition, is invalid. – In common driver application mode, the data is shifted to 80-bit common data bi-directional shift register by the CL1 clock. Hence, this clock pin is not used (Open or connect this pin to VDD).	Controller
M	I	AC signal for LCD driver output	Alternate signal input pin for LCD driving. Normal frame inversion signal is input in to this pin.	Controller
CL1	I	Data latch clock	– In segment driver application mode, this signal is used for latching the shift register contents at the falling edge of this clock pulse. CL1 pulse "High" level initializes power-down function block. – In common driver application mode, CL1 is used as a shifting clock of common output data.	Controller
DISPOFFB	I	Display OFF control	Control input pin to fix the driver output (SC1~SC80) to V0 level, during "Low" value input. LCD becomes non-selected by V0 level output from every output of segment drivers and every output of common drivers.	Controller
CS	I	COM / SEG mode control	When CS = "Low", S6B0086 is used as an 80-bit segment driver. When CS = "High", S6B0086 is set to an 80-bit common driver	VDD / VSS

<table>
<tr>
<td>AMS</td>
<td>I</td>
<td>Application mode select</td>
<td>According to the input value of the AMS and the CS pin, application mode of S6B0086 is differs as shown below.
<table>
<tr><th>CS</th><th>AMS</th><th>Application mode</th><th>COM/SEG</th></tr>
<tr><td>0</td><td>0</td><td>4-bit parallel interface mode</td><td rowspan="2"></td></tr>
<tr><td>0</td><td>1</td><td>1-bit serial interface mode</td></tr>
<tr><td>1</td><td>0</td><td>Single type application mode</td><td rowspan="2">COM</td></tr>
<tr><td>1</td><td>1</td><td>Dual type application mode</td></tr>
</table>
</td>
<td>VDD / VSS</td>
</tr>
</table>

PIN DESCRIPTION (CONTINUED)

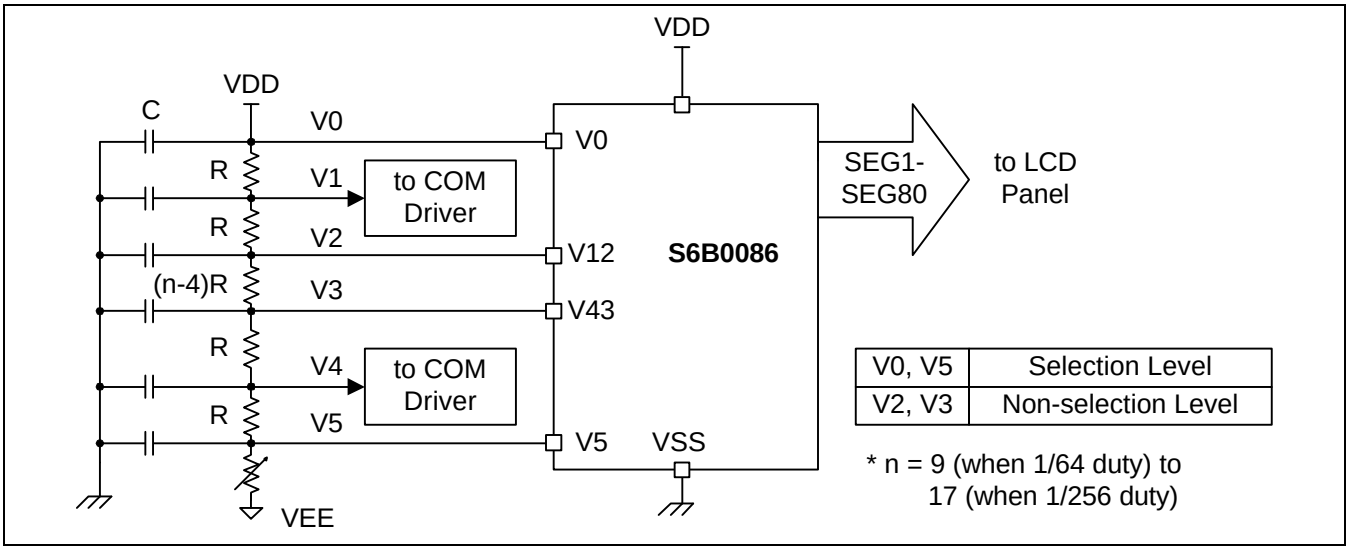
<table>
<tr><th>Pin</th><th>I / O</th><th>Name</th><th>Function</th><th>Interface</th></tr>
<tr>
<td>D1_SID, D2_DL, D3_DM, D4_DR</td>
<td>I / O</td>
<td>Display data input / serial input data / left, right data input output</td>
<td>In segment driver application mode, these pins are used as 4-bit data input pin (when 4-bit parallel interface mode : AMS = "Low"), or D1_SID is used as serial data input pin and other pins are not used (connect these to VDD) (when 1-bit serial interface mode : AMS = "High").
– In common driver application mode, the data is shifted from D2_DL(D4_DR) to D4_DR(D2_DL), when in single type interface mode (AMS = "Low"). In dual-type application case, the data are shifted from D2_DL and D3_DM (D4_DR and D3_DM) to D4_DR(D2_DL). In each case the direction of the data shift and the connection of data pins are determined by SHL input (refer to NOTE 3, NOTE 4).</td>
<td>Controller</td>
</tr>
<tr>
<td>SHL</td>
<td>Input</td>
<td>Shift direction control</td>
<td>When SHL = "Low", data is shifted from left to right.
When SHL = "High", the direction is reversed. (refer to NOTE3)</td>
<td>VDD/VSS</td>
</tr>
<tr>
<td>ELB, ERB</td>
<td>I / O</td>
<td>Enable data input/output</td>
<td>– In segment driver application mode, the internal operation is enabled only when enable input (ELB or ERB) is “Low” (power down function). When several drivers are serially connected, the enable state of each driver is shifted according to the SHL input. Connect these pins as below.
<table>
<tr><td></td><td colspan="2">Segment Driver</td></tr>
<tr><td></td><td>ELB</td><td>ERB</td></tr>
<tr><td>L</td><td>Output (open)</td><td>Input (VSS)</td></tr>
<tr><td>H</td><td>Input (VSS)</td><td>Output (open)</td></tr>
</table>
- In common driver application mode, power down function is not used.
Open these pins.</td>
<td></td>
</tr>
</table>

NOTE 1. Output Level Control

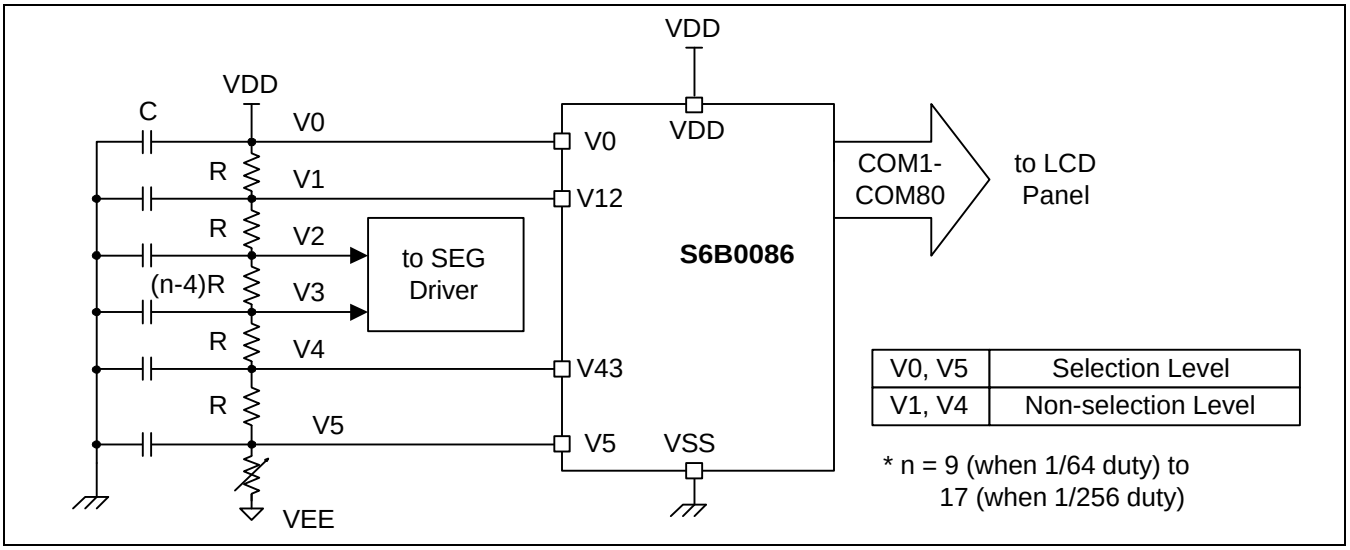
M	Latched data	DISPOFFB	Output level (SC1 – SC80)	
			SEG Mode	COM Mode
L	L	H	V12 (V2)	V12 (V1)
L	H	H	V0	V5
H	L	H	V43 (V3)	V43 (V4)
H	H	H	V5	V0
X	X	L	V0	V0

NOTE 2. LCD Driving Voltage Application Circuit

(1) Segment driver application (CS = “Low”)

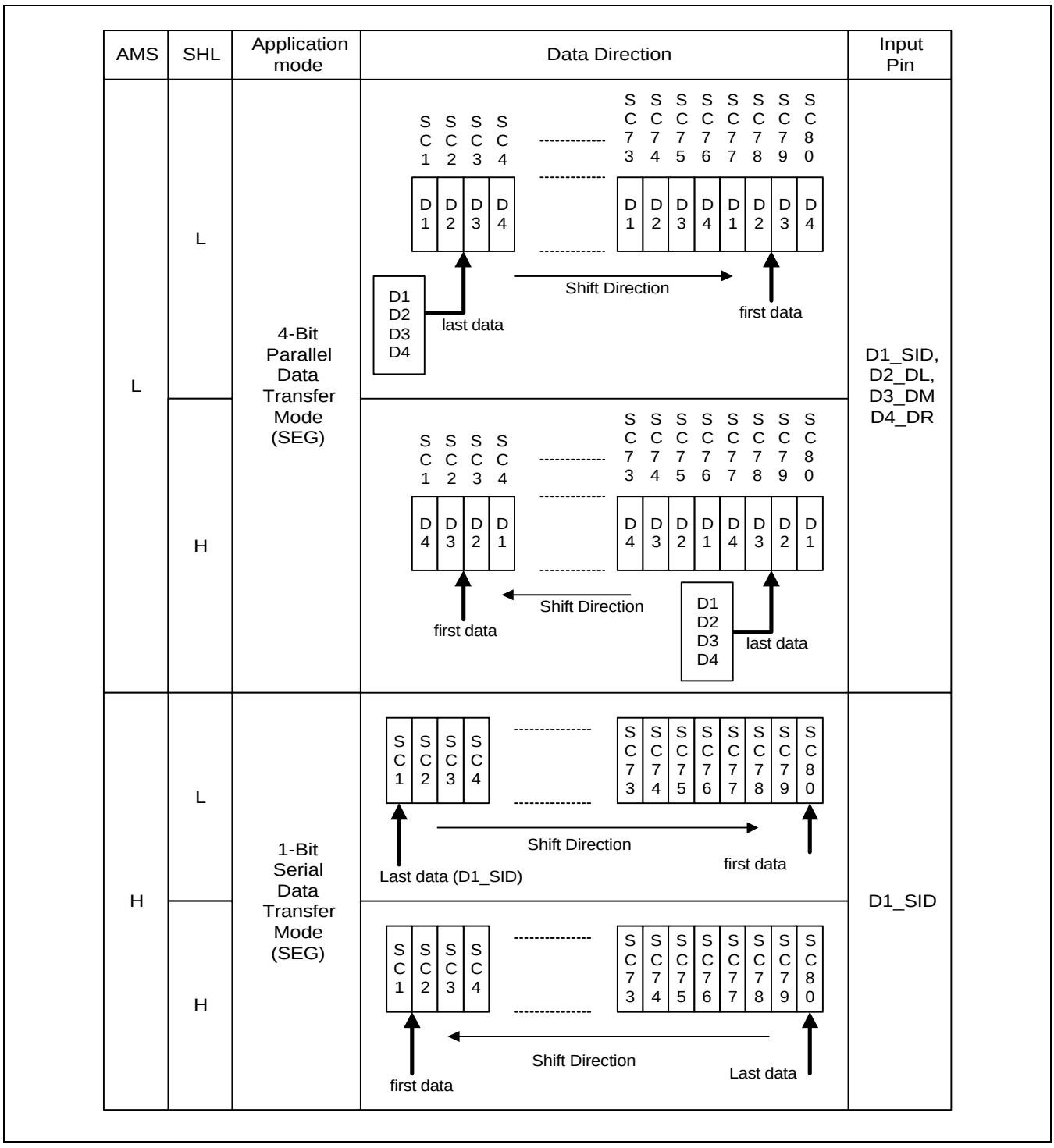


(2) Common driver application (CS = “High”)

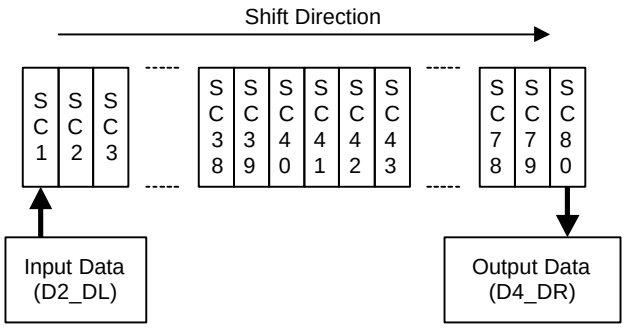
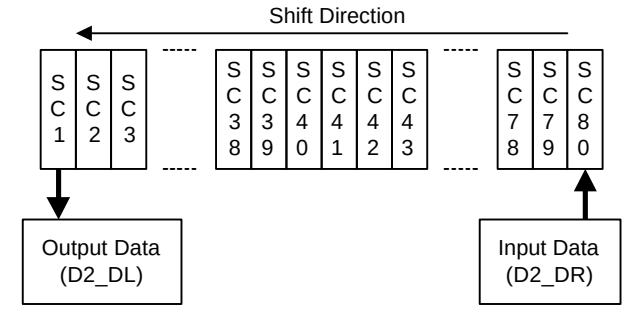
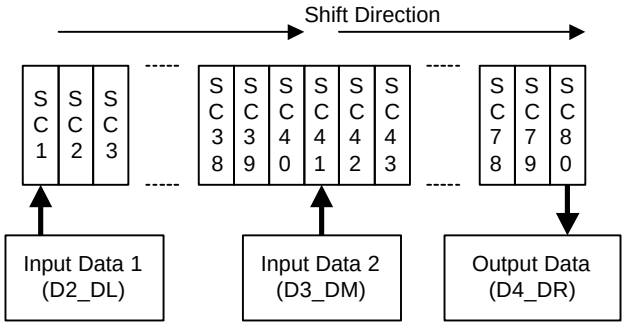
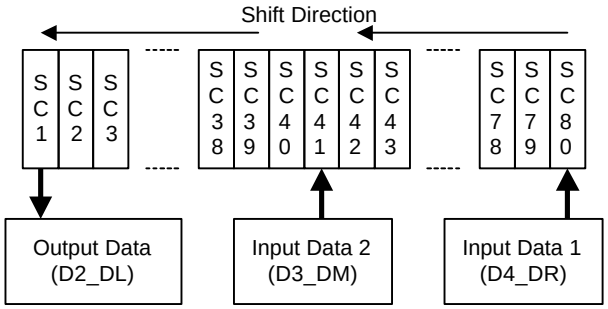


NOTE 3. Data Shift Direction according to Control Signals

(1) When CS = “Low” (segment driver application)



(2) When CS = “High” (common driver application)

AMS	SHL	Application mode	Data Direction	Input Pin
L	L	Single-type Application Mode (COM)		D2_DL
	H			D4_DR
H	L	Dual-type Application Mode (COM)		D2_DL, D3_DM
	H			D4_DR, D3_DM

NOTE 4. Usage of Data Pins

COM / SEG (CS pin)	Application mode (AMS pin)	SHL	Data interface pin			
			D1_SID	D2_DL	D3_DM	D4_DR
SEG (CS ="Low")	4-bit parallel interface mode (AMS = "Low")	X	D1 (input)	D2 (input2)	D3 (input3)	D4 (input4)
	1-bit serial interface mode (AMS = "High")	X	SID (input)	Connect to VDD		
COM (CS = "High")	single-type application mode (AMS = "Low")	L	open	DL (input)	Open	DR (output)
		H		DL (output)		DR (input)
	dual-type application mode (AMS = "High")	L	open	DL (input1)	DM (input2)	DR (output2)
		H		DL (output2)	DM (input2)	DR (input1)

MAXIMUM ABSOLUTE LIMIT

Characteristic	Symbol	Value	Unit
Power supply voltage	V_{DD}	-0.3 – +7.0	V
Driver supply voltage	V_{LCD}	0 – +30	
Input voltage	V_{IN}	-0.3 – V_{DD} + 0.3	
Operating temperature	Topr	-30 – +85	°C
Storage temperature	Tstg	-55 – +150	

*** NOTE:** Voltage greater than above may do damage to the circuit.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

(1) Segment Driver Application

(V_{SS} = 0V, Ta = - 30 – +85°C)

Characteristic	Symbol	Test Condition		Min.	Typ.	Max.	Unit
Operating Voltage1	V_{DD}	-		2.7	-	5.5	V
	V_{LCD}	$V_{IN} = V_{DD} - V_{EE}$		6	-	28	
Input voltage (1)	V_{IH}	-		$0.8V_{DD}$	-	V_{DD}	
	V_{IL}	-		0	-	$0.2V_{DD}$	
Output voltage (2)	V_{OH}	I_{OH} = -0.4mA		V_{DD}-0.4	-	-	V
	V_{OL}	I_{OL} = 0.4mA		-	-	0.4	
Input leakage current 1 (1)	I_{IL1}	$V_{IN} = V_{DD}$ to V_{SS}		-10	-	10	µA
Input leakage current 2 (3)	I_{IL2}	$V_{IN} = V_{DD}$ to V_{EE}		-25	-	25	
On resistance (4)	R_{ON}	I_{ON} = 100µA		-	2	4	kΩ
Supply current (5)	I_{STBY}	f_{CL1} = 32kHz M = V_{SS}	V_{SS} pin	-	-	100	µA
	I_{DD}	f_{CL1} = 32kHz f_M = 80Hz	V_{DD} = 5V	-	-	5	mA
			V_{DD} = 3V	-	-	2	
	I_{EE}		V_{DD} = 5V	-	-	500	µA

NOTES:

1. Applied to CL1, CL2, ELB, ERB, D1_SID - D4_DR, SHL, DISPOFFB, M, CS, AMS pin
2. ELB, ERB pin
3. V0, V12, V43, V5 pin
4. V_{LCD} = V_{DD} - V_{EE}, V0 = V_{DD} = 5V, V5= V_{EE} = -23 V
   V12 = V_{DD}-2/n(V_{LCD}), V43 = V_{EE}+2/n(V_{LCD}), n = 17 (1/256 duty, 1/17 bias)
5. V0 = V_{DD}, V12 = 1.71V(V_{DD} = 5V) or -0.06V (V_{DD} = 3V),
   V43 = -19.71 V(V_{DD} = 5V) or -19.94V (V_{DD} = 3V), V5 = V_{EE} = -23V, no-load condition (1/256 duty, 1/17 bias)
   4-bit parallel interface mode
   I_{STBY} : V_{DD} = 5V, f_{CL2} = 5.12MHz, SHL = V_{SS}, DISPOFFB = V_{DD}, M = V_{SS}, display data pattern = 0000
   I_{DD} : V_{DD} = 3V, f_{CL2} = 4MHz, display data pattern = 0101
   V_{DD} = 5 V, f_{CL2} = 5.12MHz, display data pattern = 0101
   I_{EE} : V_{DD} = 5V, f_{CL2} = 5.12MHz, display data pattern = 0101, V_{EE} pin

DC CHARACTERISTICS (CONTINUED)

(2) Common Driver Application

(V_{SS} = 0V, Ta = - 30 – +85°C)

Characteristic	Symbol	Test Condition		Min.	Typ.	Max.	Unit
Operating voltage	V_{DD}	-		2.7	-	5.5	V
	V_{LCD}	$V_{IN} = V_{DD} - V_{EE}$		6	-	28	
Input voltage (1)	V_{IH}	-		$0.8V_{DD}$	-	V_{DD}	
	V_{IL}	-		0	-	$0.2V_{DD}$	
Output voltage (3)	V_{OH}	I_{OH} = -0.4mA		V_{DD}-0.4	-	-	V
	V_{OL}	I_{OL} = 0.4mA		-	-	0.4	
Input leakage current 1 (1)	I_{IL1}	$V_{IN} = V_{DD}$ to V_{SS}		-10	-	10	µA
Input leakage current 2 (2)	I_{IL2}	V_{IN} = 0V, V_{DD} = 5V (PULL UP)		-50	-125	-250	
Input leakage current 3 (4)	I_{IL3}	$V_{IN} = V_{DD}$ to V_{EE}		-25	-	25	
On resistance(5)	R_{ON}	I_{ON} = 100µA		-	2	4	kΩ
Supply current (6)	I_{STBY}	f_{CL1} = 32kHz	V_{SS} pin	-	-	100	µA
	I_{DD}	f_{CL1} = 32kHz, f_M = 80Hz	V_{DD} = 5V	-	-	200	
			V_{DD} = 3V	-	-	120	
	I_{EE}		V_{DD} = 5V	-	-	150	

NOTES:

1. Applied to CL1, D2_DL (SHL = LOW), D4_DR (SHL = HIGH), SHL, DISPOFFB, M, CS, AMS pin
2. Pull-up input pins : CL2, D1_SID, D3_DM (AMS = HIGH), ELB (SHL = LOW), ERB (SHL = HIGH)
3. D2_DL (SHL = HIGH) , D4_DR (SHL = LOW) pin
4. V0, V12, V43, V5 pin
5. $V_{LCD} = V_{DD}$-V_{EE}, V0 = V_{DD} = 5V, V5 = V_{EE} = -23V
   V12 = V_{DD}-1/n(V_{LCD}), V43 = V_{EE}+1/n(V_{LCD}), n = 17(1/256 duty, 1/17 bias)
6. V0 = V_{DD}, V12 = 3.35V (V_{DD} = 5V) or 1.47V (V_{DD} = 3V),
   V43 = -21.35V (V_{DD} = 5 V) or -21.47V (V_{DD} = 3 V), V5 = V_{EE} = -23 V, no-load condition (1/256 duty, 1/17 bias)
   single-type mode operation : AMS = V_{SS}, SHL = V_{SS}, DISPOFFB = V_{DD}
   D1_SID = D3_DM = V_{DD}, D4_DR = OPEN, ELB = ERB = OPEN,
   I_{STBY} : V_{DD} = 5V, M = V_{SS}, D2_DL = V_{SS}
   I_{DD} : f_M = 80Hz, D2_DL = V_{DD}
   V_{DD} = 3 V, display data pattern = 10000000..., 01000000..., 00100000..., 00010000..., ..
   V_{DD} = 5 V, display data pattern = 10000000..., 01000000..., 00100000..., 00010000..., ..
   I_{EE} : f_M = 80Hz, D2_DL = V_{DD}
   V_{DD} = 5V, current through V_{EE} Pin, display data pattern = 10000000..., 01000000..., 00100000..., 00010000...

AC CHARACTERISTICS

(1) Segment Driver Application

(V_{SS} = 0V, Ta = - 30 – +85°C)

Characteristic	Symbol	Test Condition	(1) V_{DD} = 5V ±10%			(2) V_{DD} = 3V ±10%			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock cycle time	t_{CY}	Duty = 50%	125	-	-	250	-	-	ns
Clock pulse width	t_{WCK}	-	45	-	-	95	-	-	
Clock rise / fall time	t_R/t_F	-	-	-	-	-	-	30	
Data set-up time	t_{DS}	-	30	-	-	65	-	-	
Data hold time	t_{DH}	-	30	-	-	65	-	-	
Clock set-up time	t_{CS}	-	80	-	-	120	-	-	
Clock hold time	t_{CH}	-	80	-	-	120	-	-	
Propagation delay time	t_{PHL}	ELB Output	-	-	60	-	-	125	
		ERB Output			60			125	
ELB,ERB set-up time	t_{PSU}	ELB Input	30	-	-	65	-	-	
		ERB Input	30			65			
DISPOFFB low pulse width	t_{WDL}	-	1.2	-	-	1.2	-	-	µs
DISPOFFB clear time	t_{CD}	-	100	-	-	100	-		ns
M - OUT propagation delay time	t_{PD1}	C_L = 15pF	-	-	1.0	-	-	1.2	µs
CL1 - OUT propagation delay time	t_{PD2}		-	-	1.0	-	-	1.2	
DISPOFFB - OUT propagation delay time	t_{PD3}		-	-	1.0	-	-	-	

AC CHARACTERISTICS (CONTINUED)

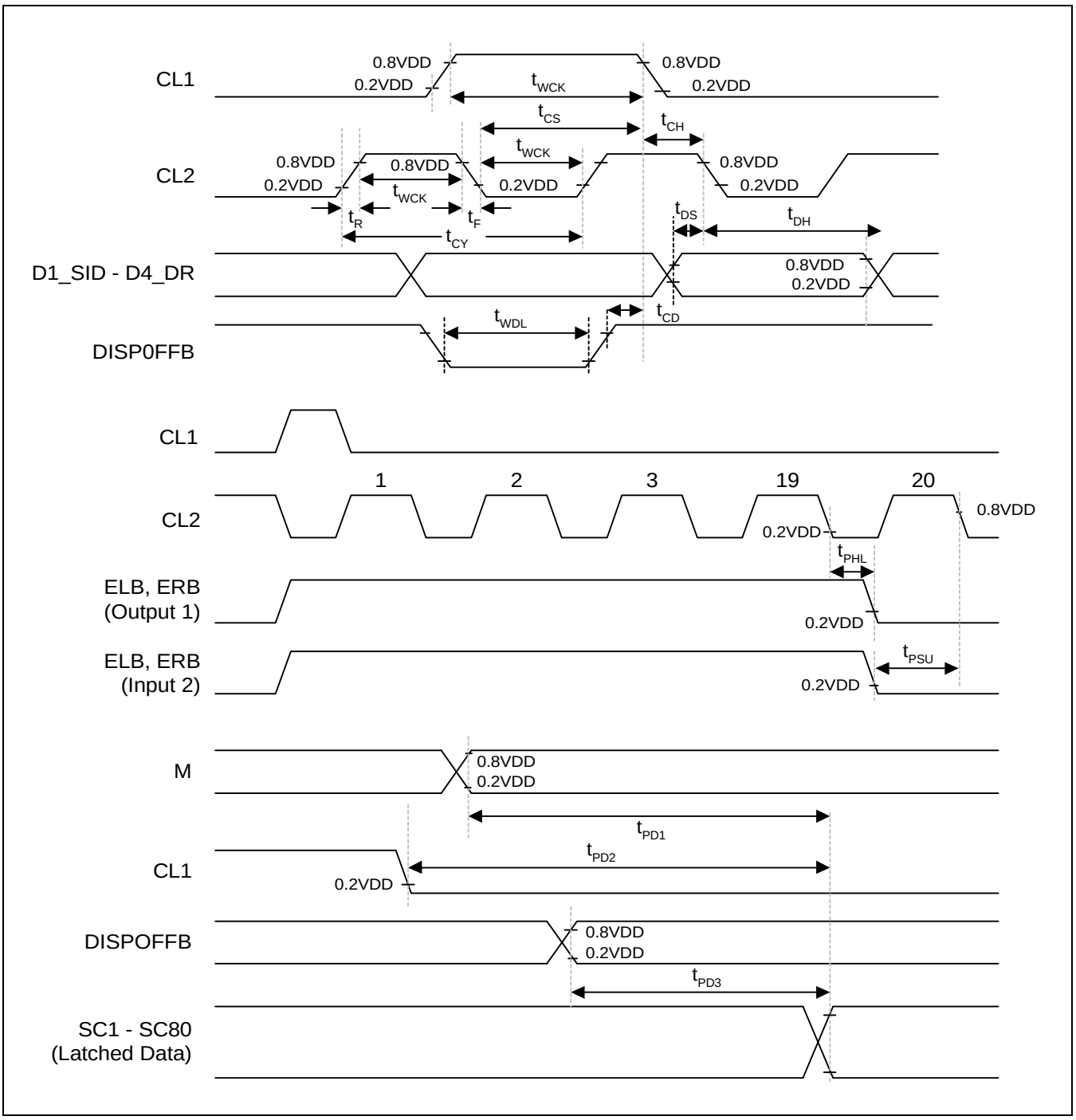
(2) Common Driver Application

(V_{SS} = 0V, Ta = - 30 – +85°C)

Characteristic	Symbol	Test Condition	(1) V_{DD} = 5 V ± 10%			(2) V_{DD} = 3V ±10%			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock cycle time	t_{CY}	Duty = 50%	250	-	-	500	-	-	ns
Clock pulse width	t_{WCK}	-	45	-	-	95	-	-	
Clock rise / fall time	t_R/t_F	-	-	-	50	-	-	50	
Data set-up time	t_{DS}	-	30	-	-	65	-	-	
Data hold time	t_{DH}	-	30	-	-	65	-	-	
DISPOFFB low pulse width	t_{WDL}	-	1.2	-	-	1.2	-	-	µs
DISPOFFB clear time	t_{CD}	-	100	-	-	100	-	-	ns
Output delay time	t_{DL}	C_L = 15pF	-	-	200	-	-	250	
M – OUT propagation delay time	t_{PD1}		-	-	1.0	-	-	1.2	µs
CL1 - OUT propagation delay time	t_{PD2}		-	-	1.0	-	-	1.2	
DISPOFFB - OUT propagation delay time	t_{PD3}		-	-	1.0	-	-	1.2	

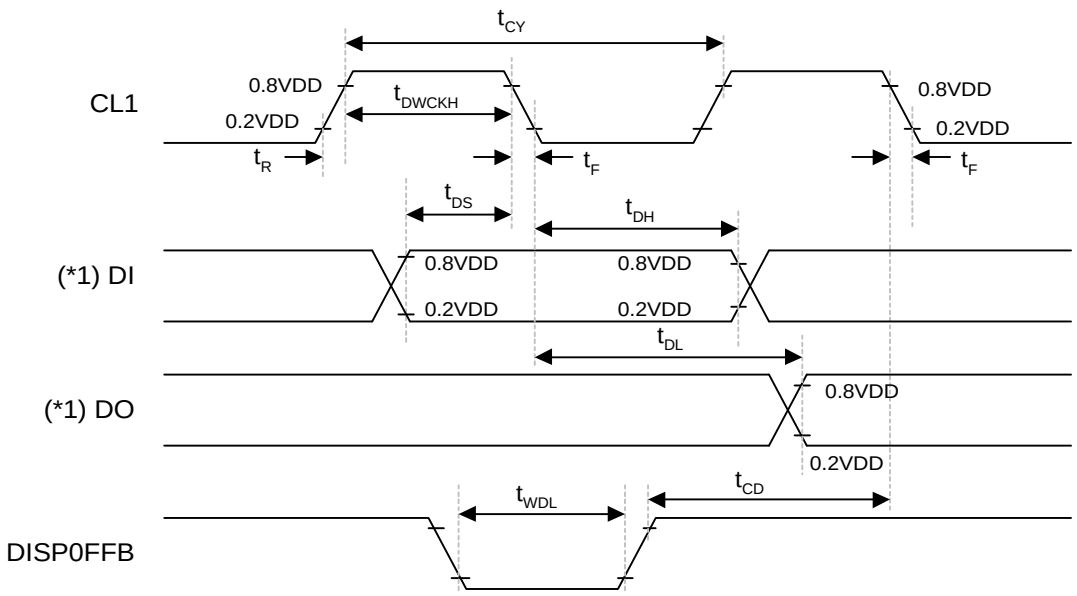
AC CHARACTERISTICS (CONTINUED)

(3) Segment Driver Application Timing

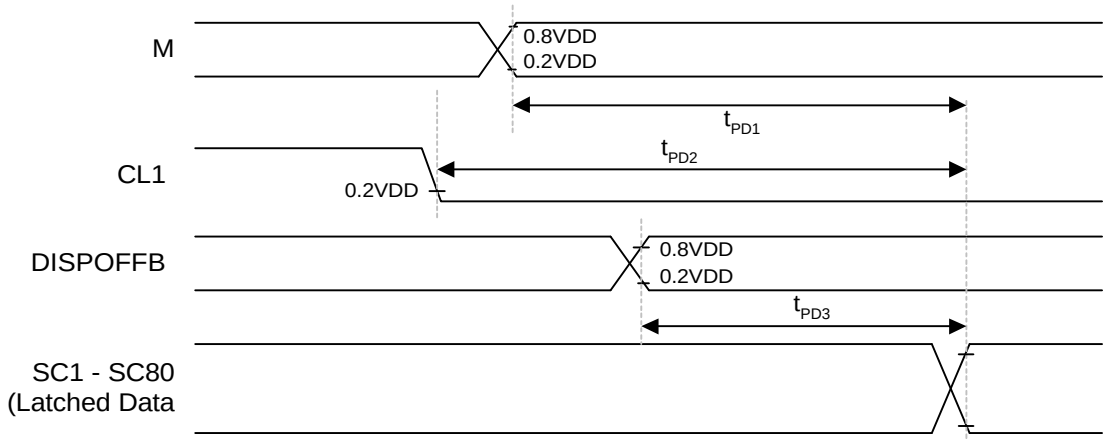


AC CHARACTERISTICS (CONTINUED)

(4) Common Driver Application Timing



(*1) When in single-type interface mode
DI => D2_DL (SHL = L), D4_DR (SHL = H)
DO => D4_DR (SHL = L), D2_DL (SHL = H)
When in dual-type interface mode
DI => D2_DL and D3_DM (SHL = L), D4_DR and D3_DM (SHL = H)
DO => D4_DR (SHL = L), D2_DL (SHL = H)

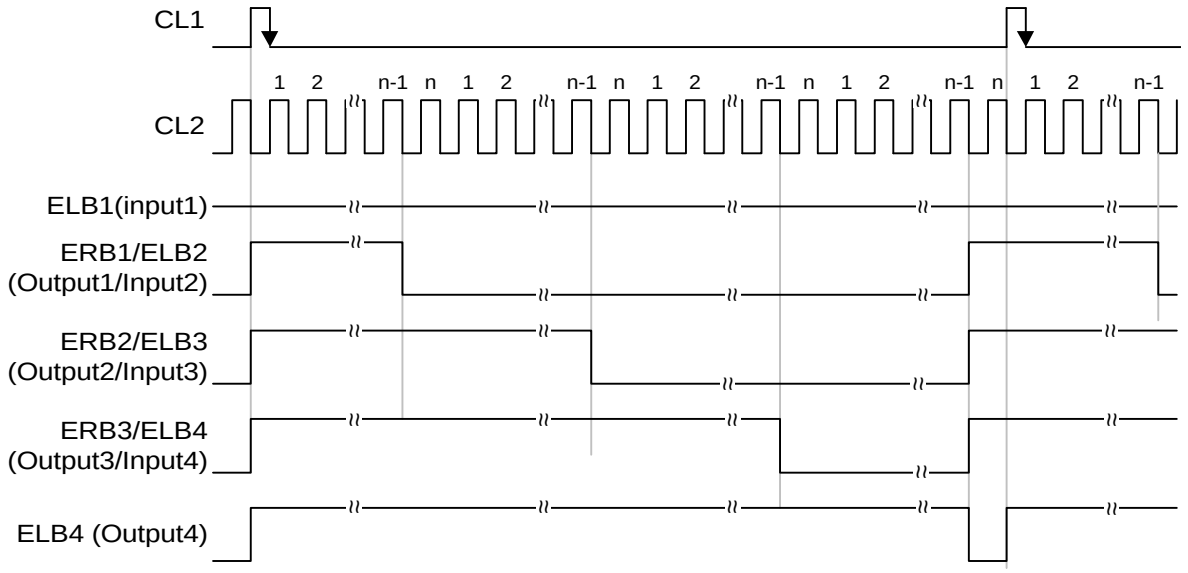


POWER DOWN FUNCTION

In the case of cascade connection of segment mode drivers, S6B0086 has a "power down function" In order to reduce the power consumption.

SHL	Enable input	Enable output	Current driver status	The other drivers status
L	ERB	ELB	While ERB ="Low", current driver is enabled.	Disabled
H	ELB	ERB	While ELB ="Low", current driver is enabled.	Disabled

* In the case of common driver application, power down function does not work.



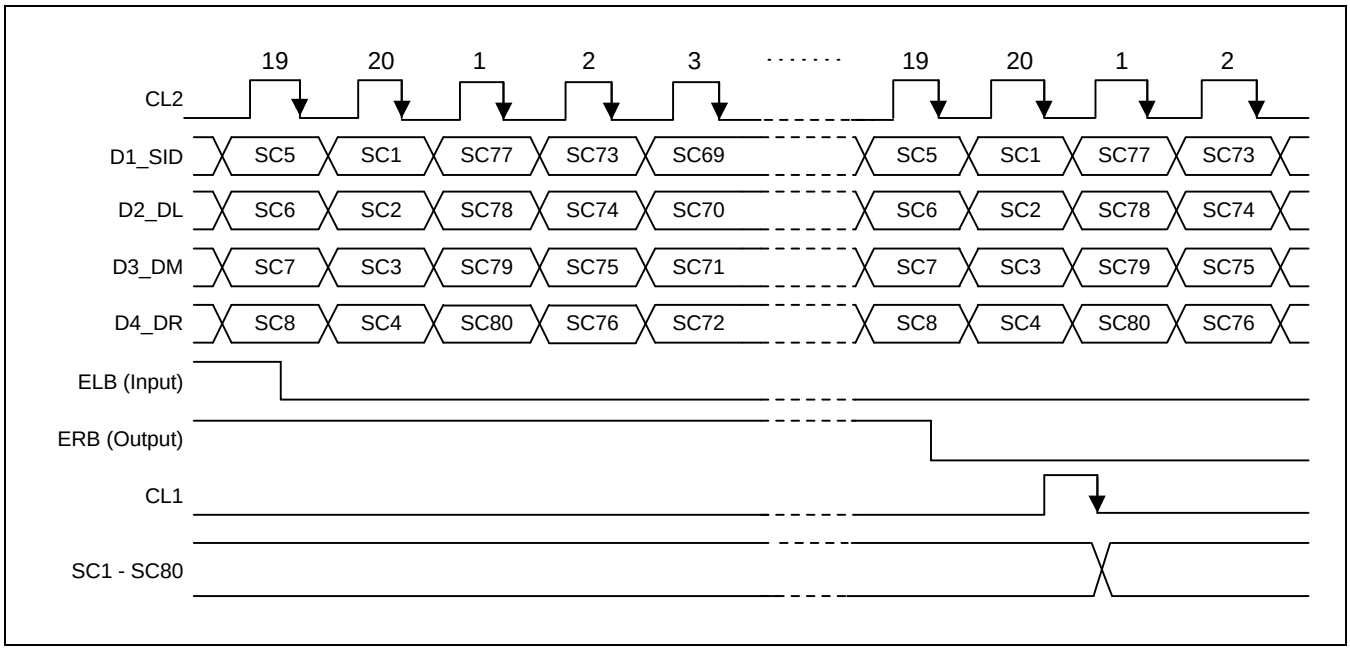
NOTES:

1. SHL = High (EBL = Input, ERB = Output)
   Current S6A0086's ERB must be connected to the next S6A0086's ELB.
2. When in 4-bit parallel interface mode: n = 20
   When in 1-bit serial interface mode: n = 80

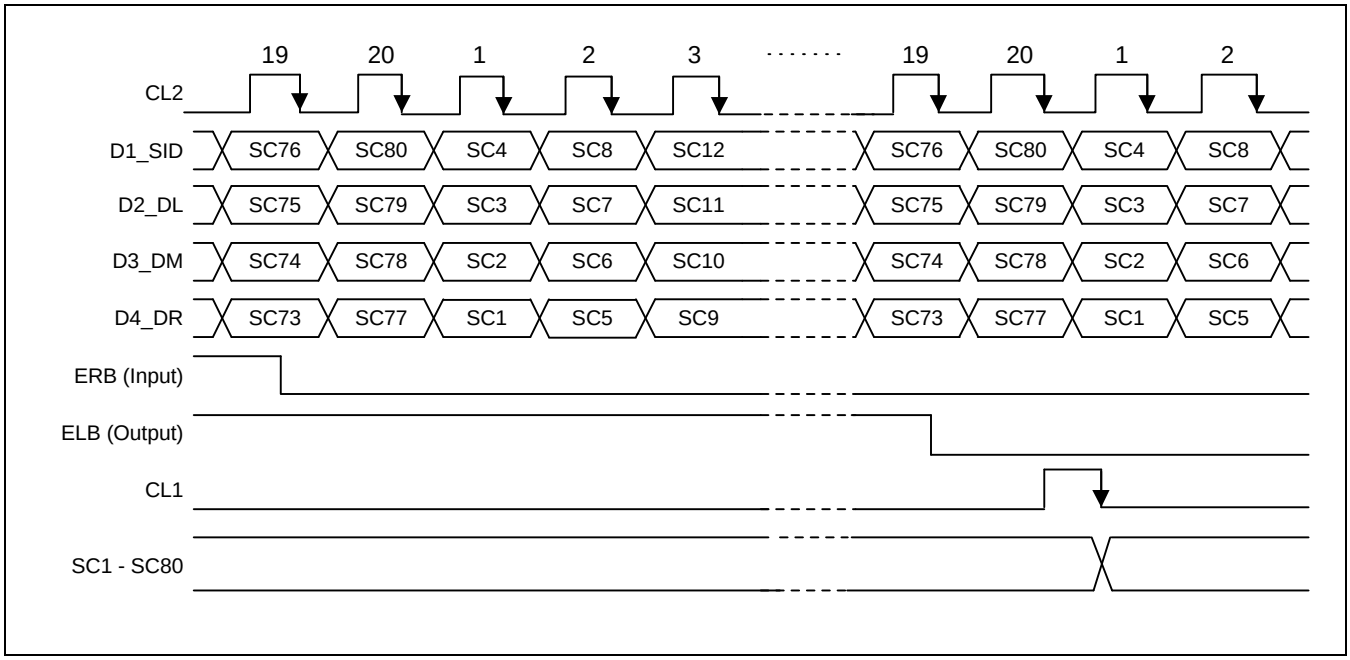
OPERATION TIMING DIAGRAM

(1) 4-bit Parallel Mode Interface Segment Driver

- When SHL = "Low"

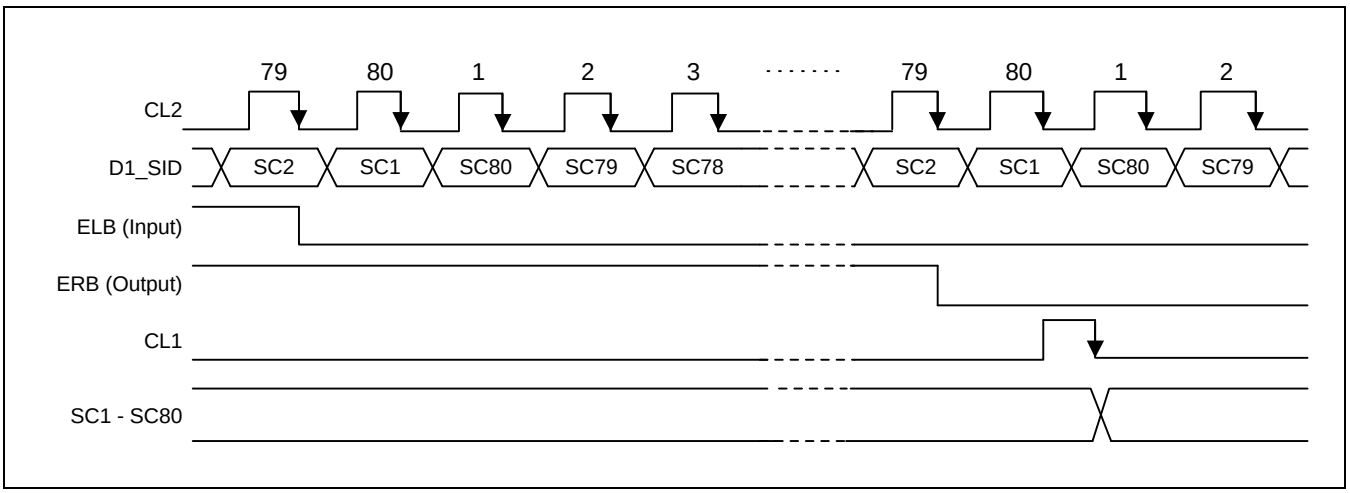


- When SHL = “High”

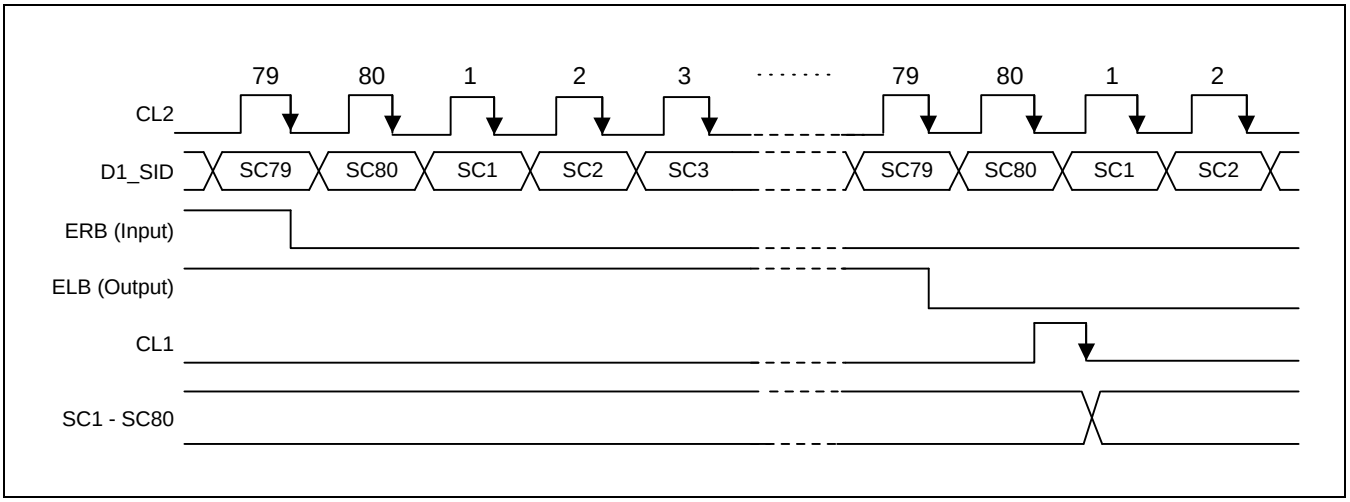


(2) 1-bit Serial Mode Interface Segment Driver

- When SHL = “Low”

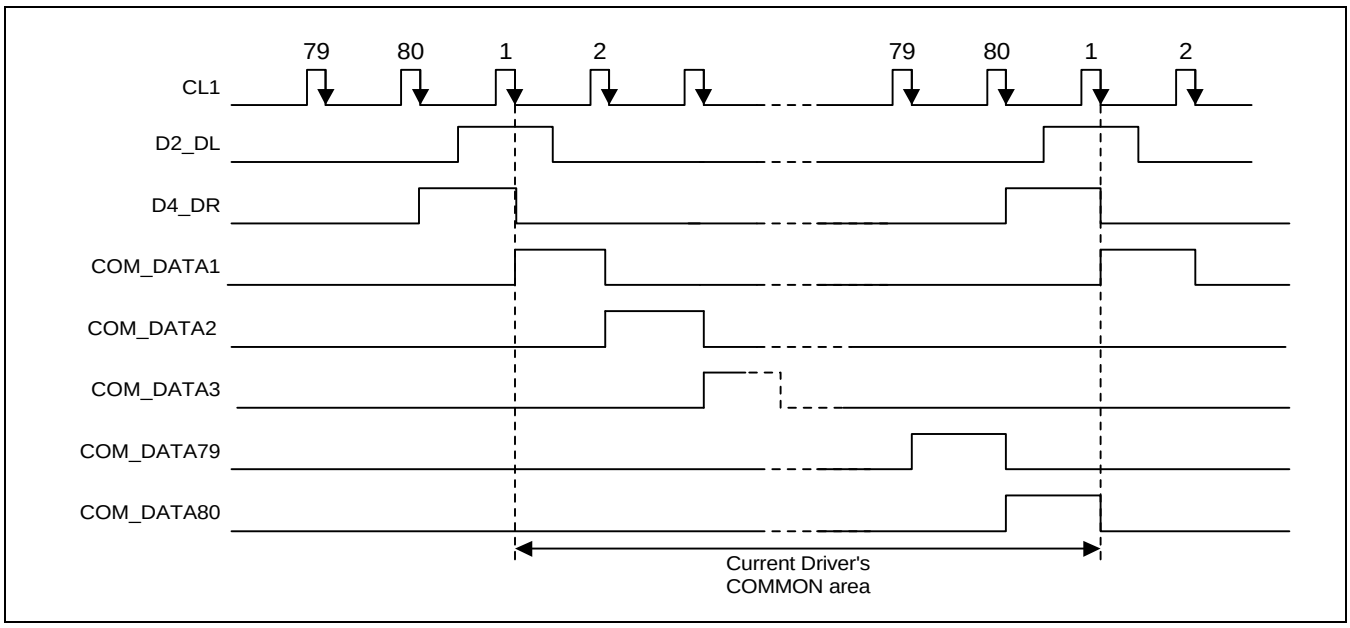


- When SHL = “High”

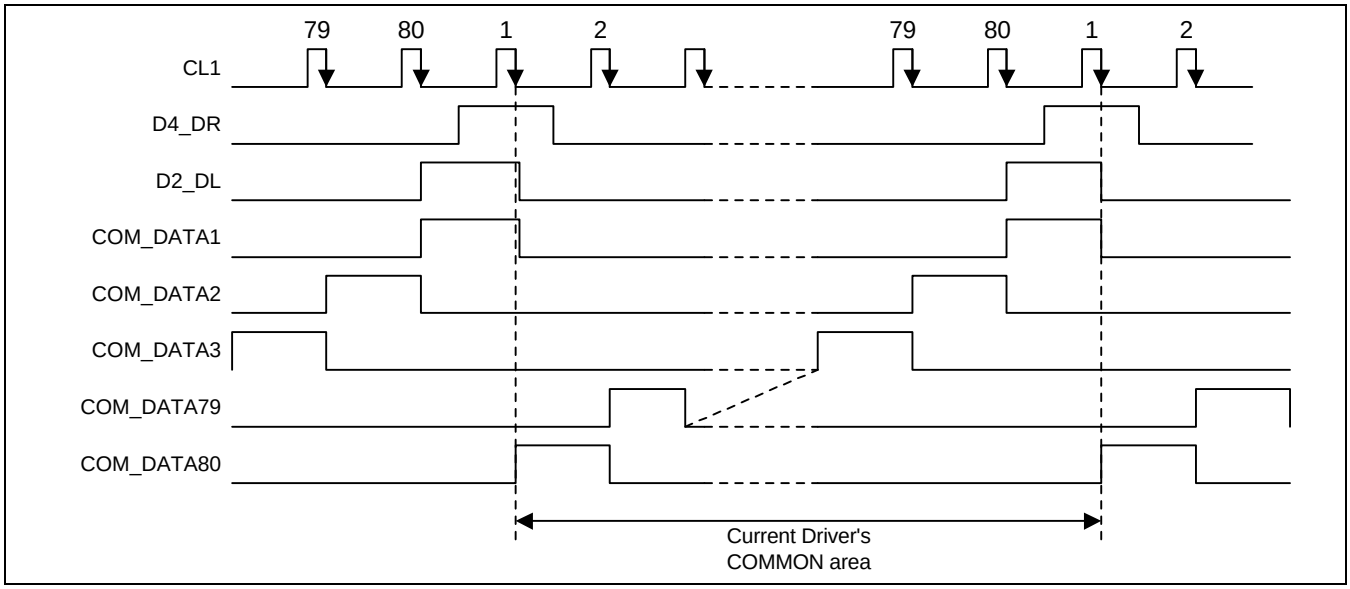


(3) Single-type Interface Mode Common Driver

- When SHL = “Low”

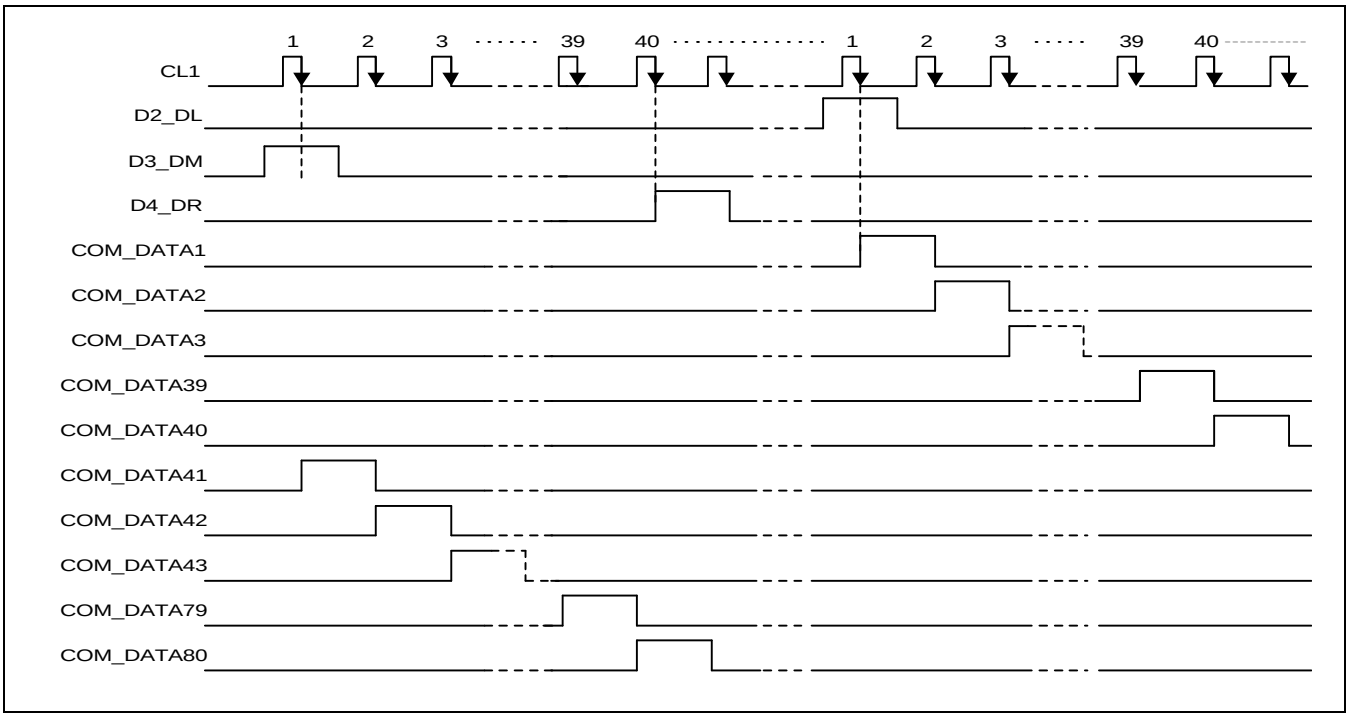


- When SHL = “High”

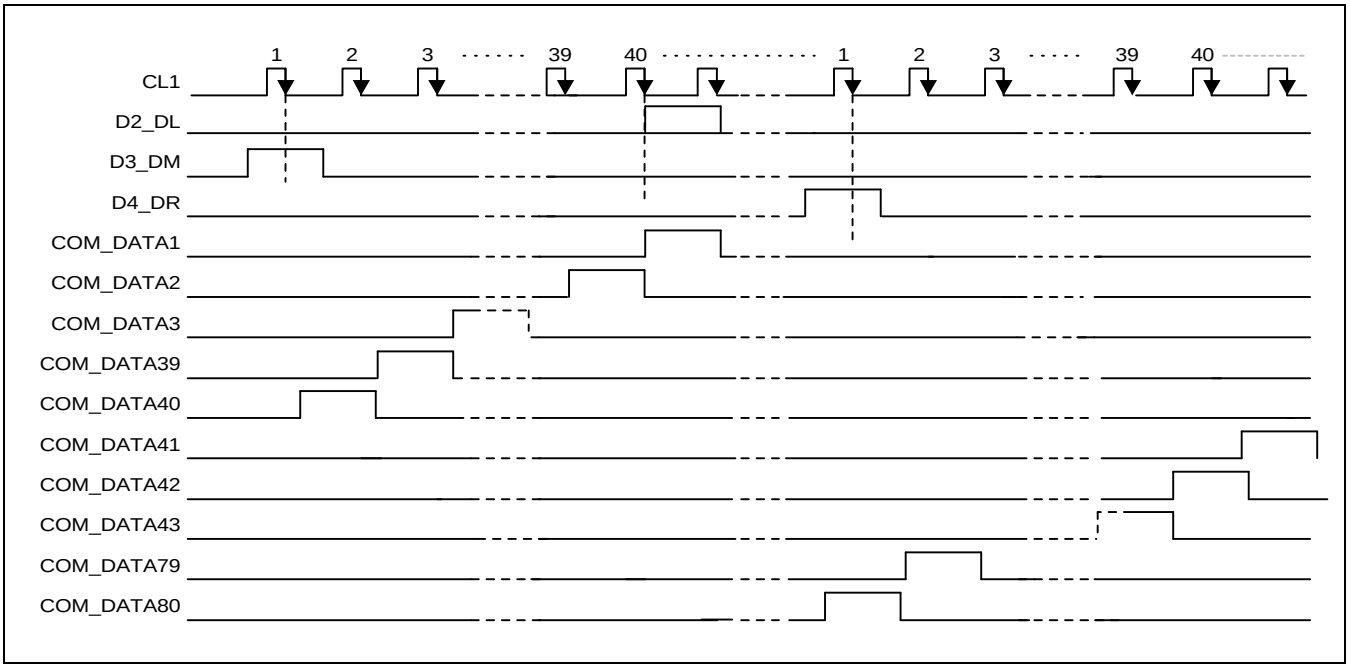


(4) DUAL-type Interface Mode Common Driver

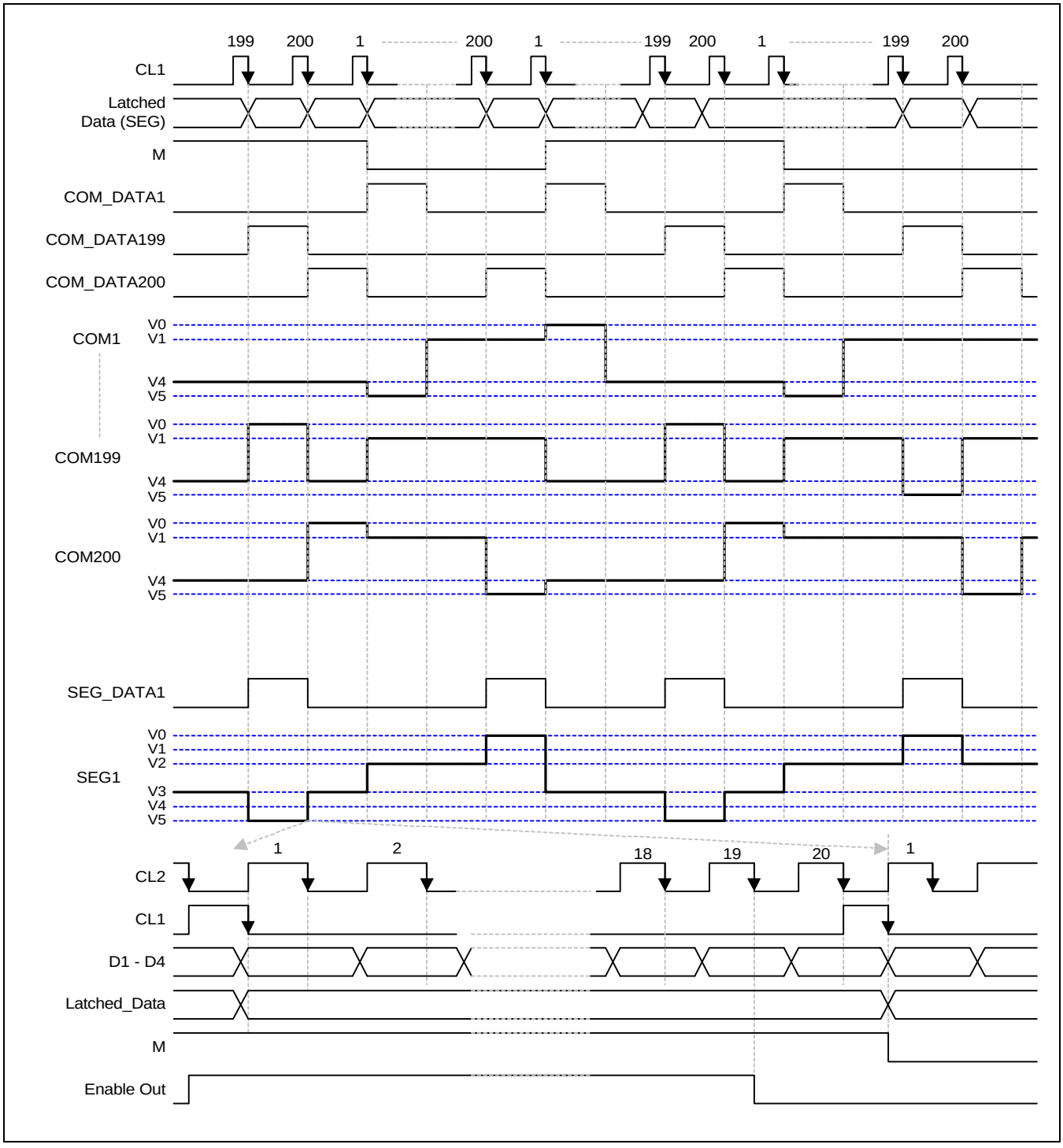
- When SHL = “Low”



- When SHL = “High”



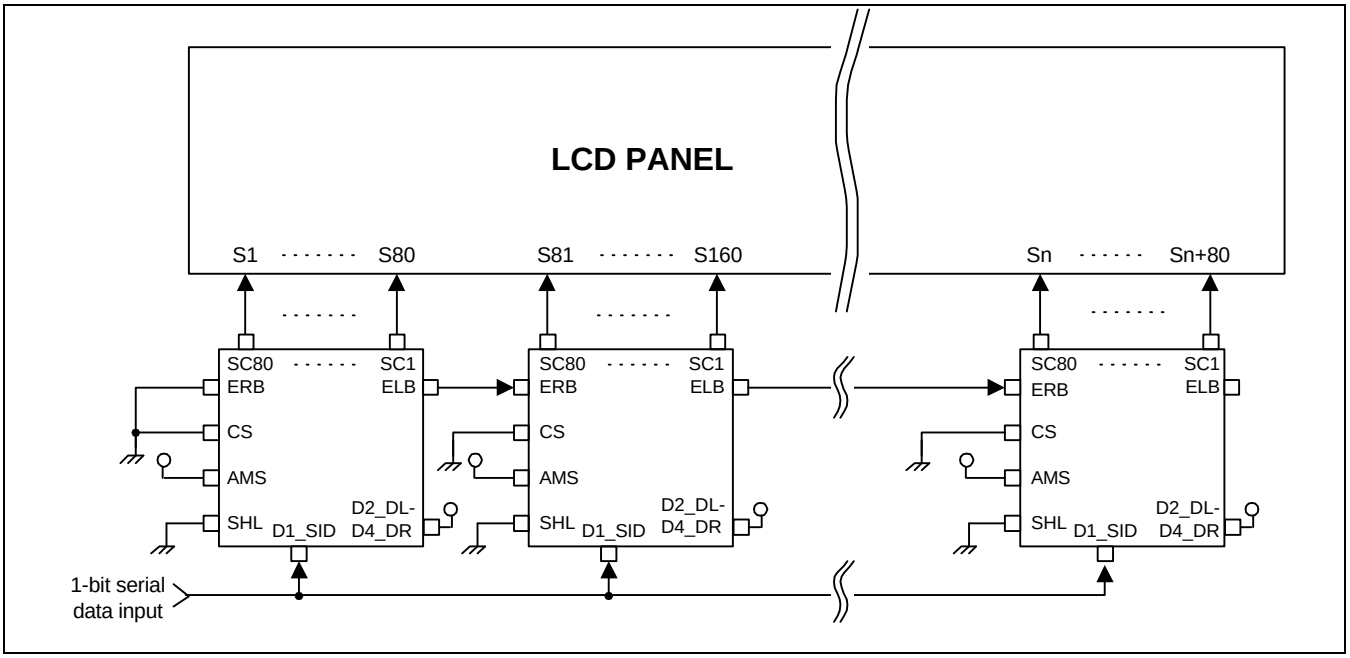
(5) Common / Segment Driver Timing (1/200 DUTY)



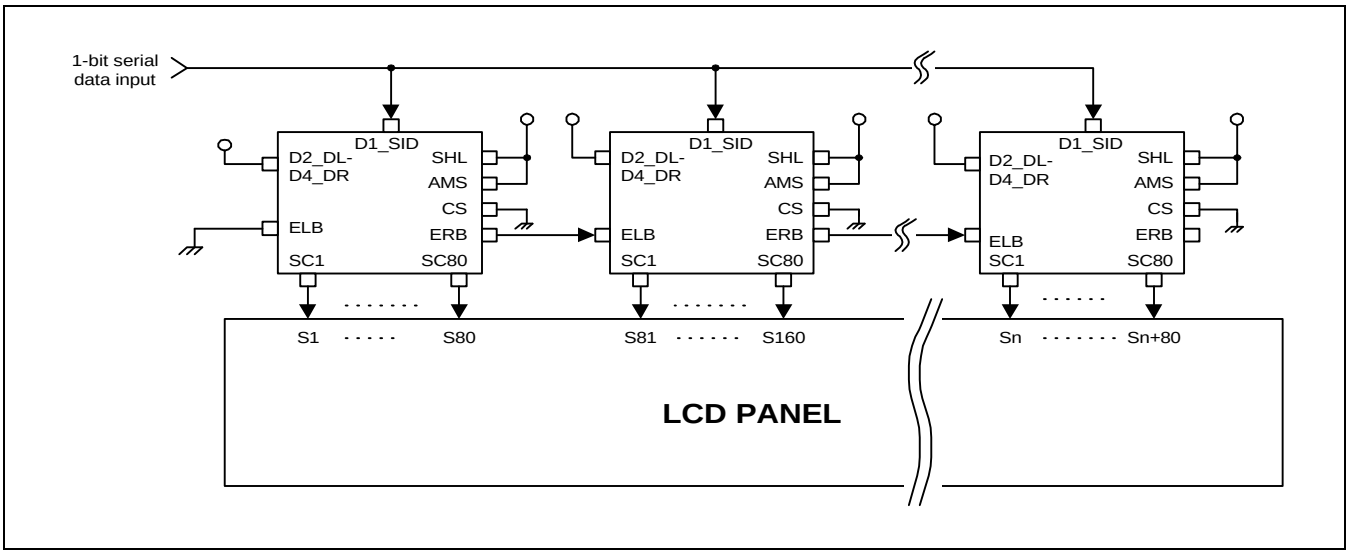
APPLICATION INFORMATION

1-bit Serial Interface Mode (80-Ch. Segment Driver)

a) Lower View (SHL = L, AMS = H)

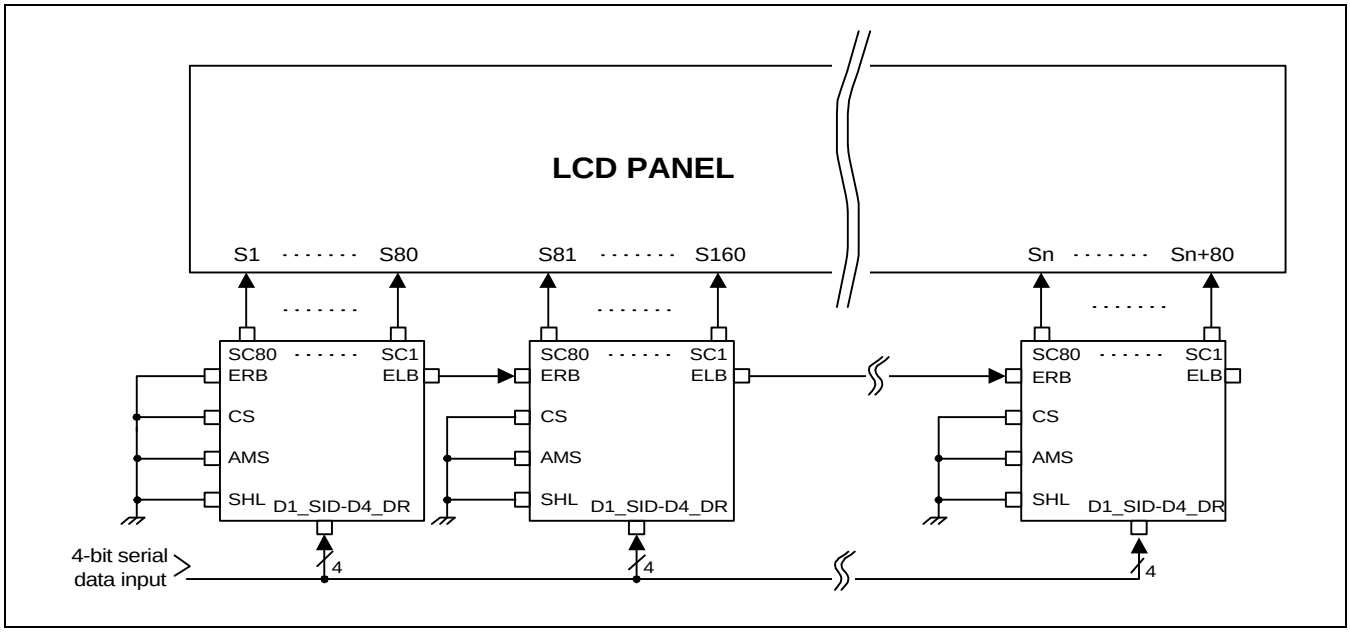


b) Upper View (SHL = H, AMS = H)

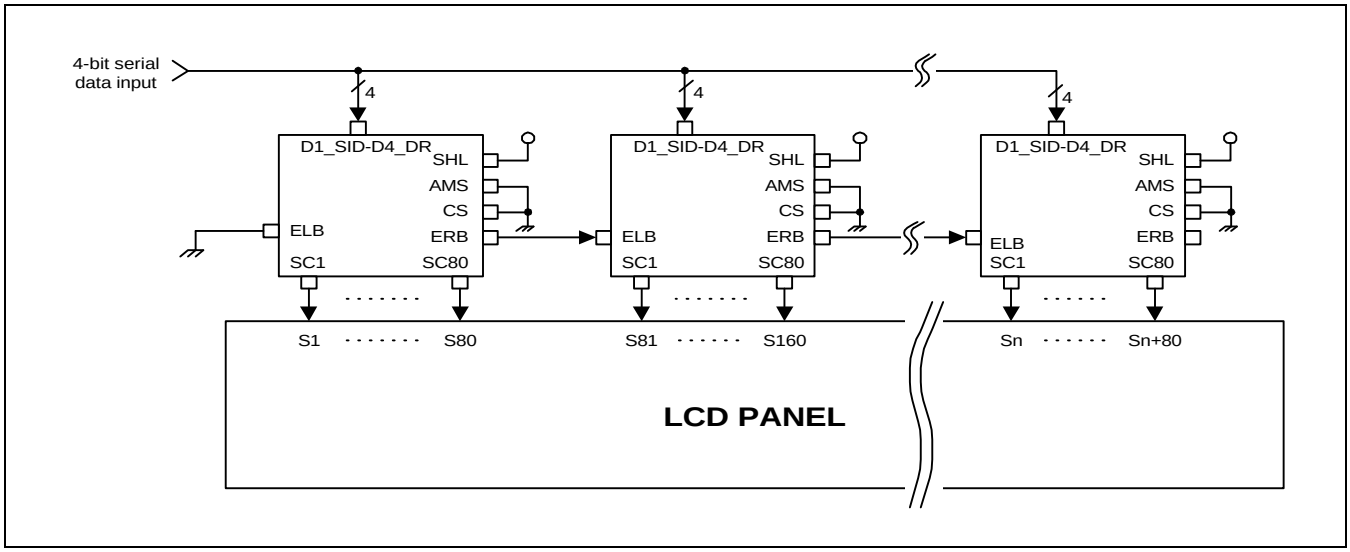


4-Bit Parallel Interface Mode (80 Ch. Segment Driver)

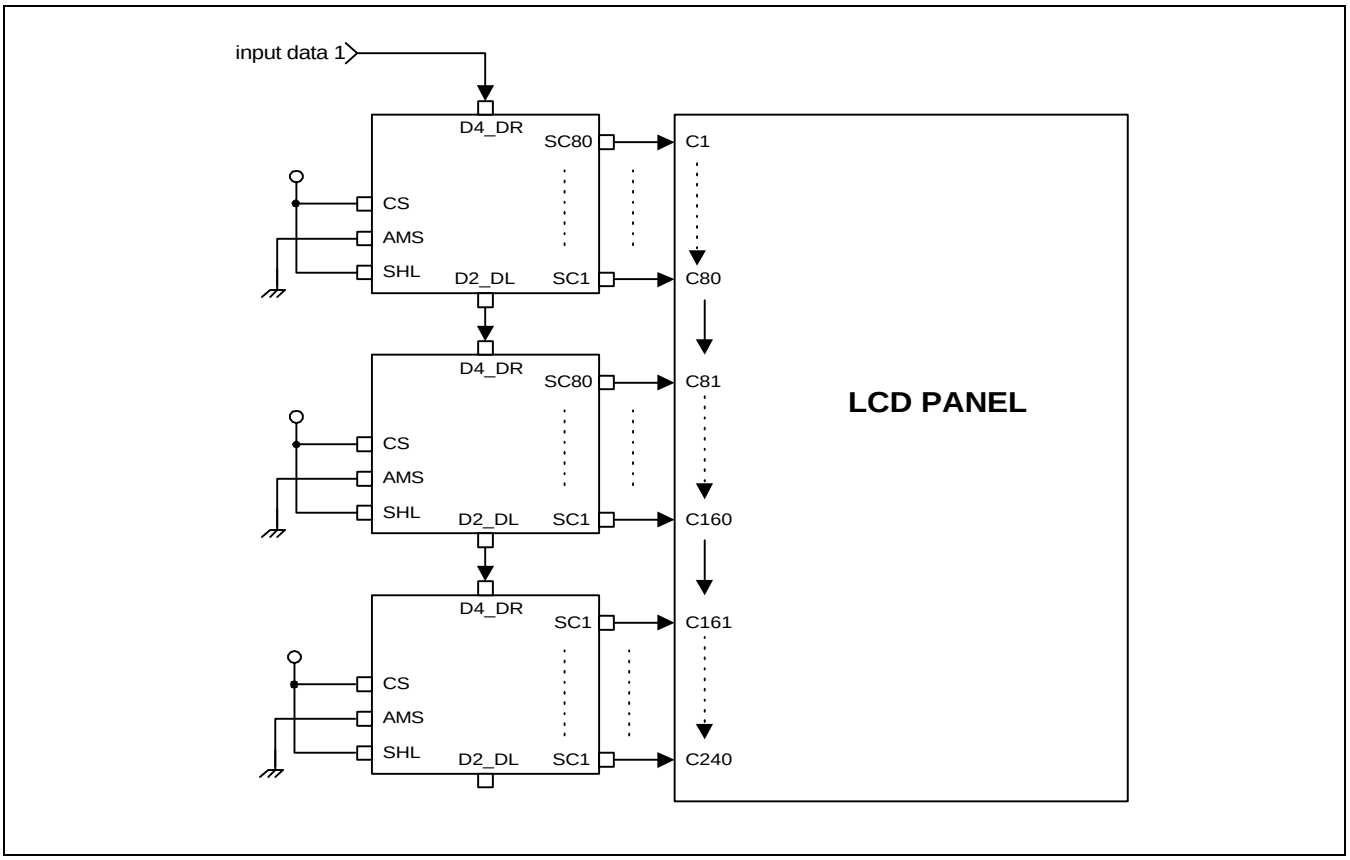
a) Lower View (SHL = L, AMS = L)



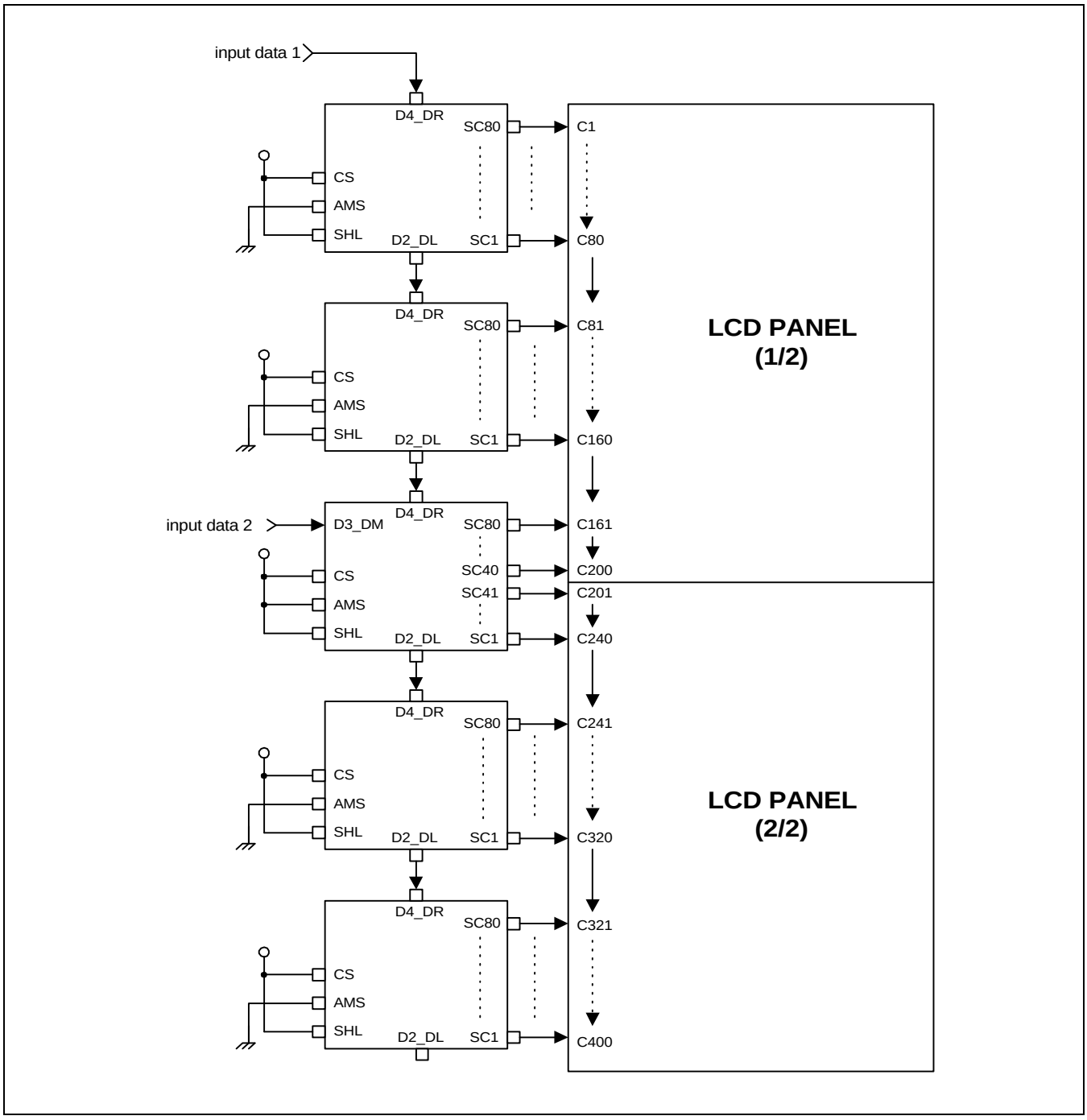
b) Upper View (SHL = H, AMS = L)



Single-type Interface Mode (80 Ch. Common Driver)



Dual-type Interface Mode (40 Ch. + 40 Ch. Common Driver)



NOTE: Using this application mode (dual-type common mode), the duty ratio can be reduced to half. In case, 1/200 duty can be used to drive the 400 common LCD panel.

APPLICATION CIRCUIT EXAMPLE