

## 1200-Output Channel TFT LCD Source Driver with TCON

### Specification *Preliminary*

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## 1. Introduction

ILI6126 is a 1200-channel output source driver with TTL interface timing controller (TCON). ILI6126 supports Dual-Gate mode to extend source channel to achieve more various resolution applications.

The interface follows digital 24-bit parallel RGB input format. The TCON generates the 800x480, 800x600, 640x480, 400x240 resolutions and provides horizontal and vertical control timing to source driver and gate driver. It also supports dithering feature, apply source driver with 6-bit DAC to perform 8-bit resolution 256 gray scales. Operating parameters can be set via pin control for all control features. Since the output circuit of this source driver incorporates an operational amplifier with low power dissipation, and performs wide voltage supply range and small output deviation.

ILI6126 can be configured as dual-gate operation mode for reducing FPC amount and saving the cost. With wide range of supply voltages and many pin control features make this chip mode suitable for various applications.

## 2. Features

### ◆ TCON

- Supports display resolution 800x480, 800x600, 640x480, 400x240
- Supports digital 24-bit parallel RGB input mode
- Supports to configure CABC block via 3-line SPI mode
- Source output with 8-bit resolution for 256 gray scales (2-bit dithering)
- Supports Dual-gate & Normal operation mode
- Support Dual Gate Z/ inverse Z/ 𠄎/ Z+𠄎 scan inversion
- Maximum Operation frequency: 50 MHz
- Support different color filter cell layout type at Dual-gat mode.
- Built-in internal gamma and support external gamma buffer
- Supports stand-by mode for saving power consumption
- Logic operation Voltage Level 2.7V to 3.6V
- Support LED Backlight Enable Control Signal With CABC Function( CABC\_PWM )
- Normally white/black selection ( Control By NBWB Pin )
- Display Mode: Single Gate 1Dot/1+2Dot inversion; Dual gate 2Dot inversion
- Support BIST & Mute Function

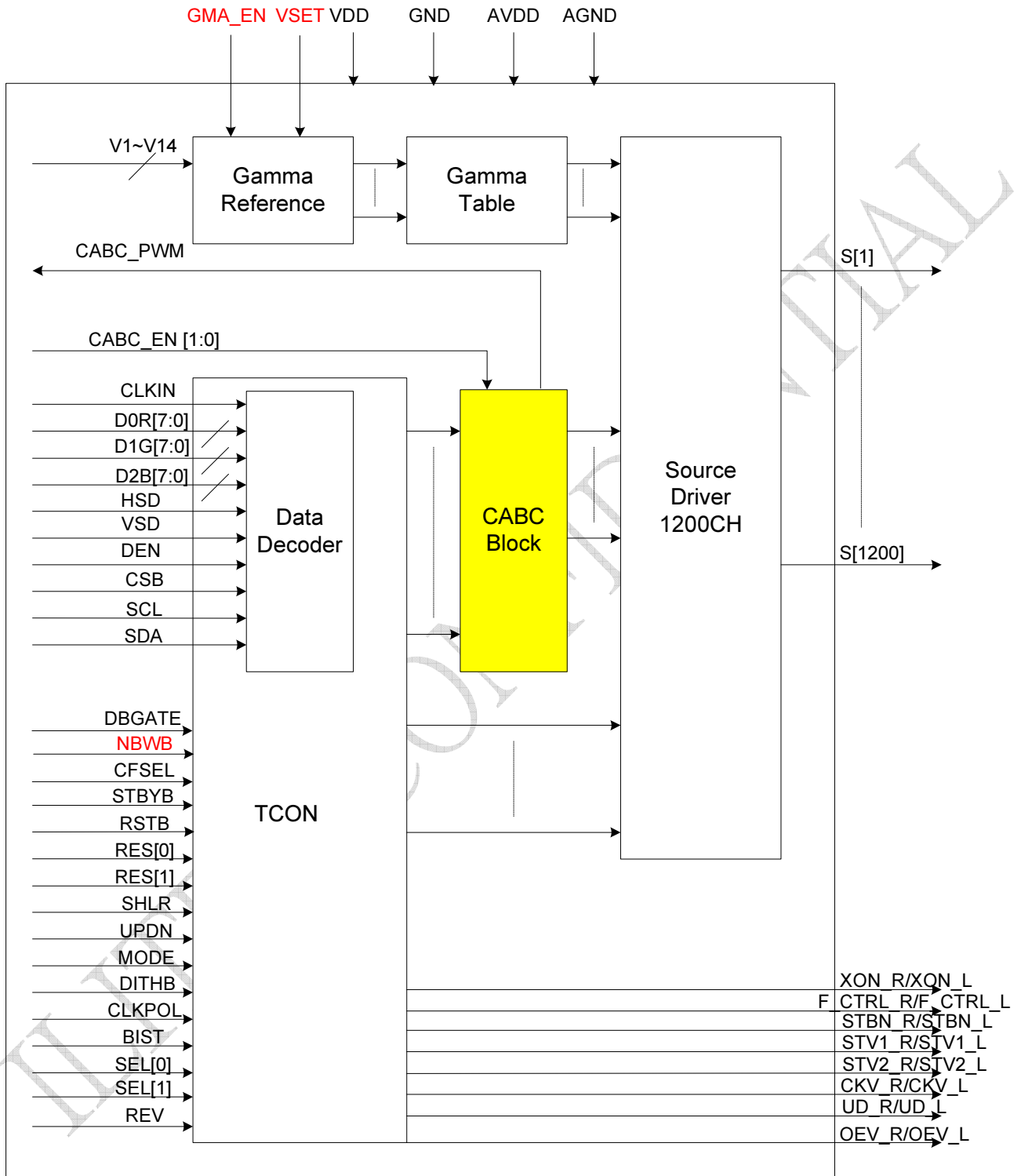
### ◆ Source Driver

- 1200/960 channels output source driver for TFT LCD panel
- Output dynamic range : 0.1V ~ AVDD-0.1V
- Voltage deviation of outputs:  $\pm 20\text{mV}$
- Power for source driver voltage (AVDD) : 6.5V ~ 13.5V

### ◆ Others

- COG package
- Supports CABC (Content Adaptive Brightness Control) function

### 3. Block Diagram

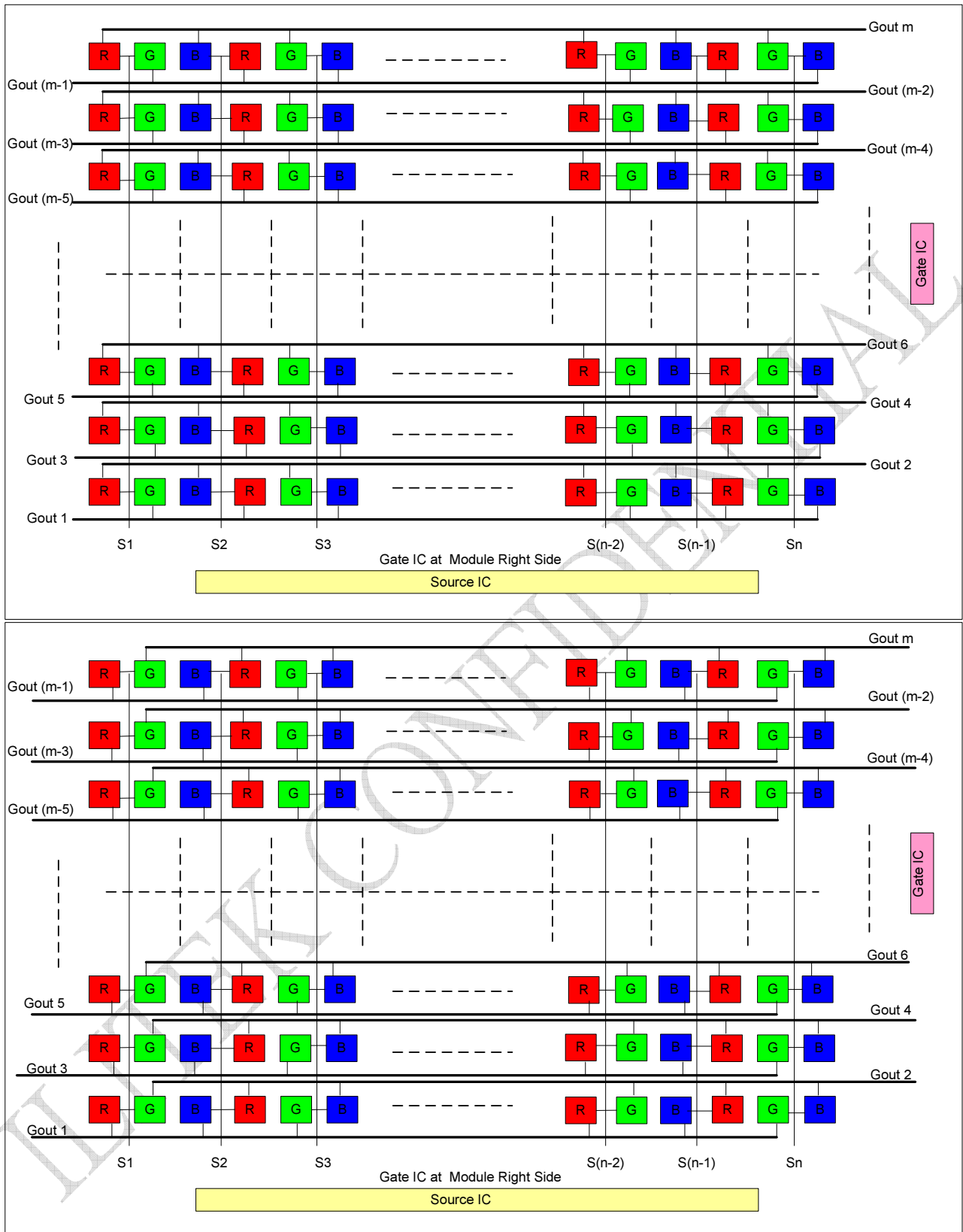




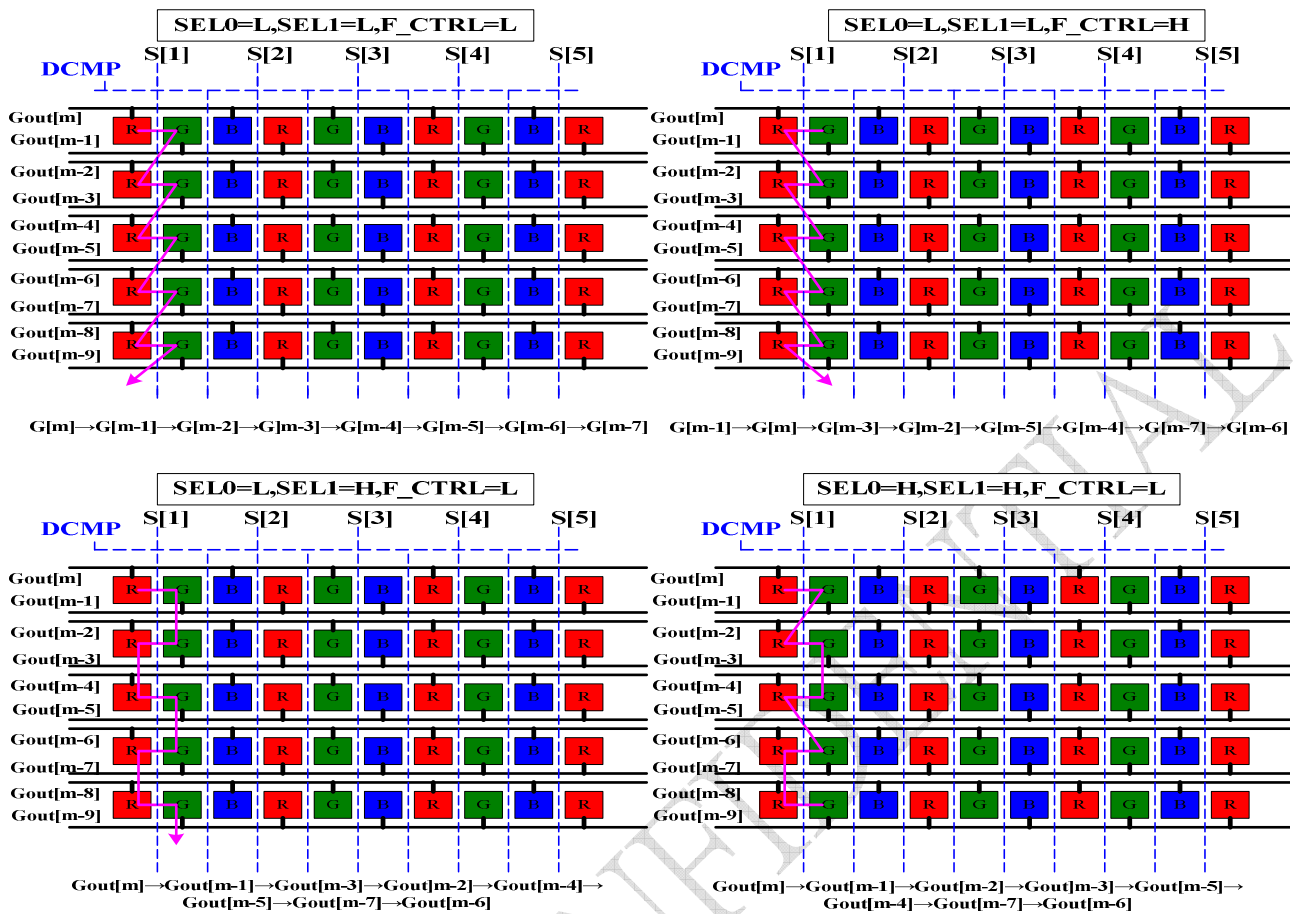








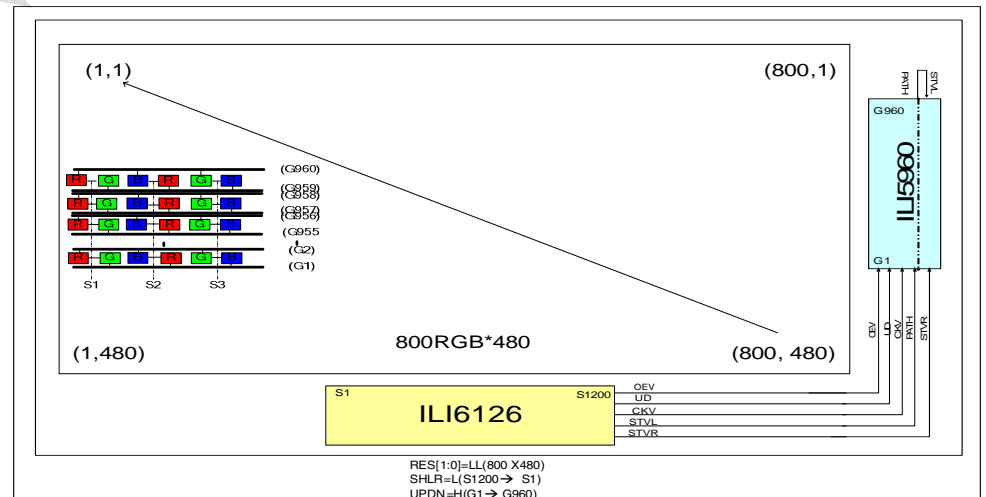
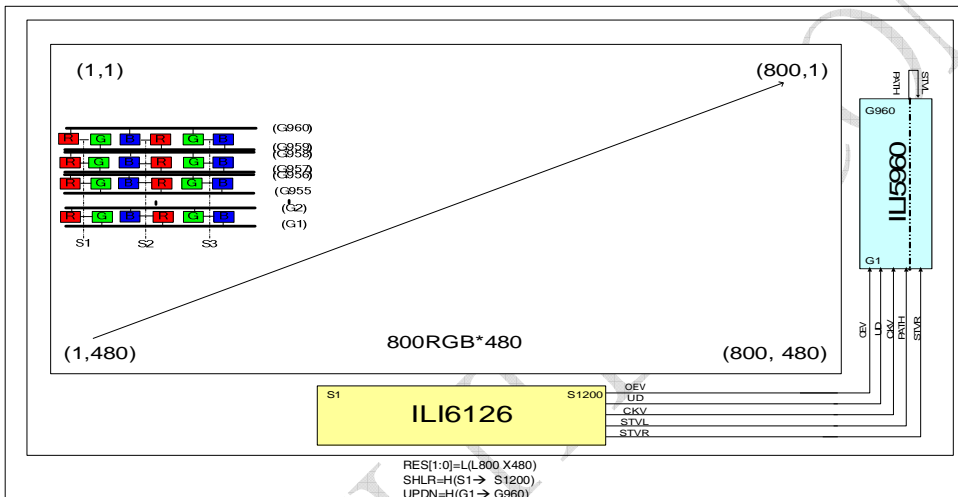
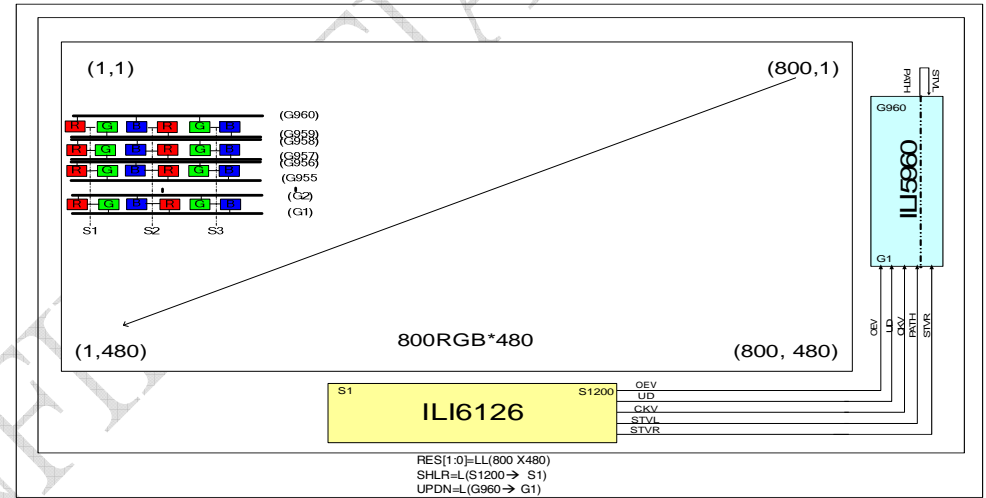
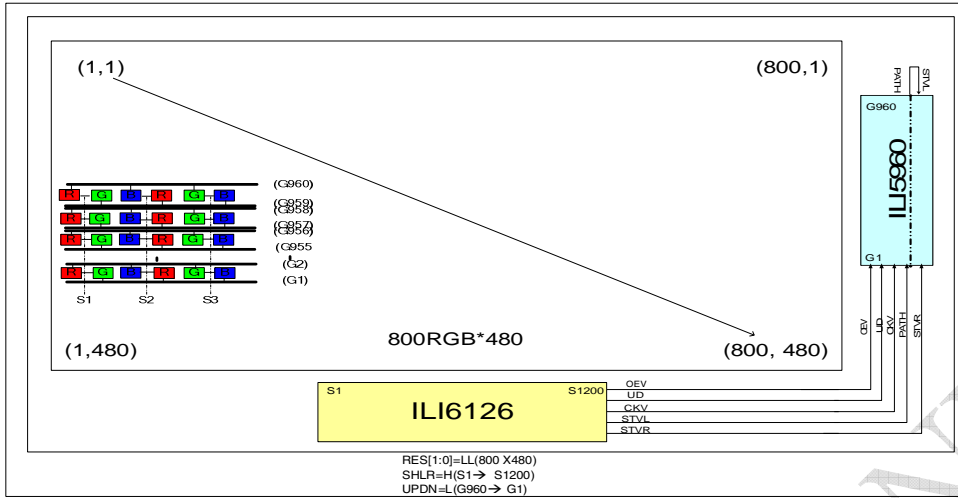
Note: Gout1~Gout m → Gate IC out channel.  
S1~Sn → Source IC out channel.



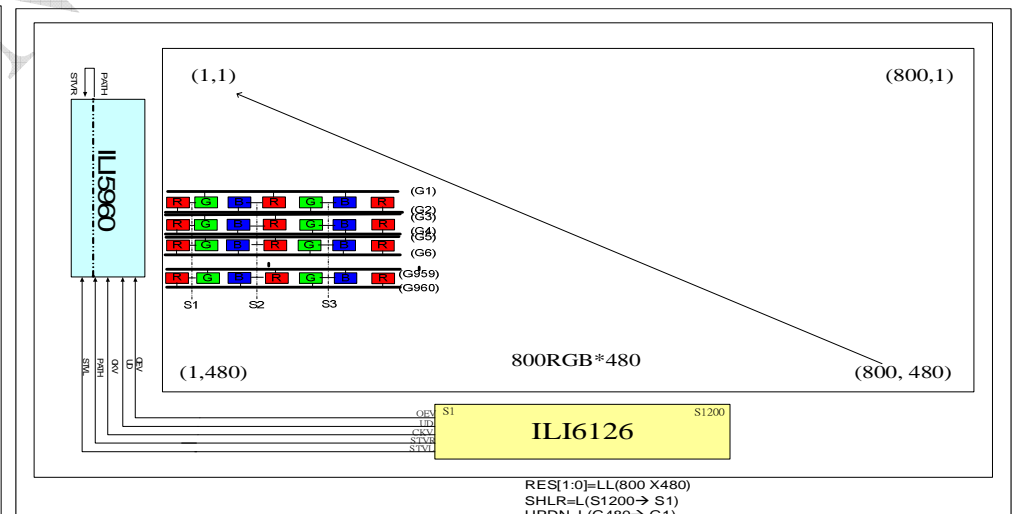
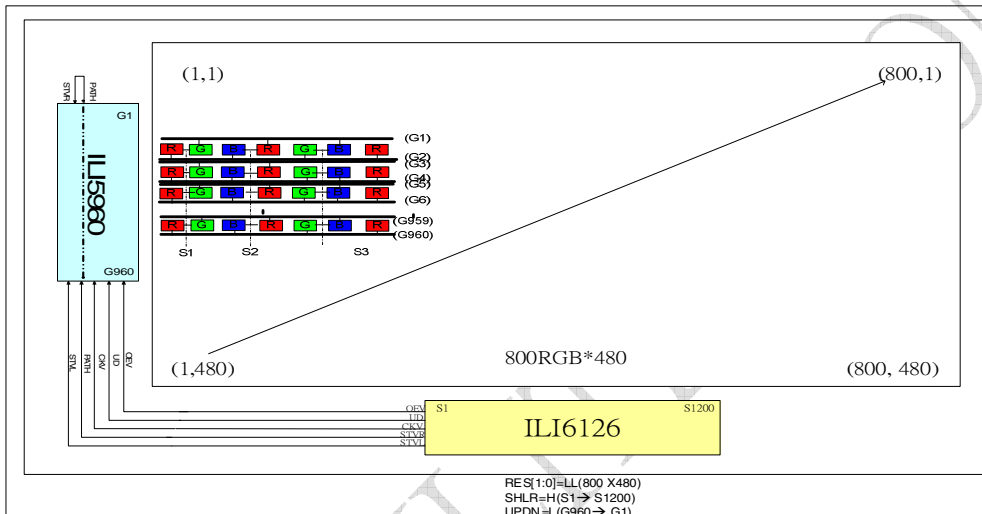
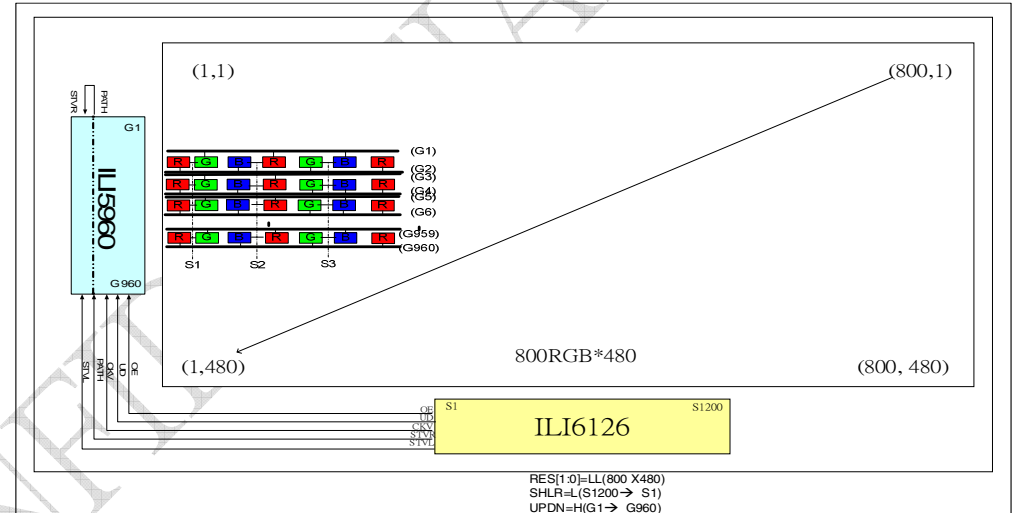
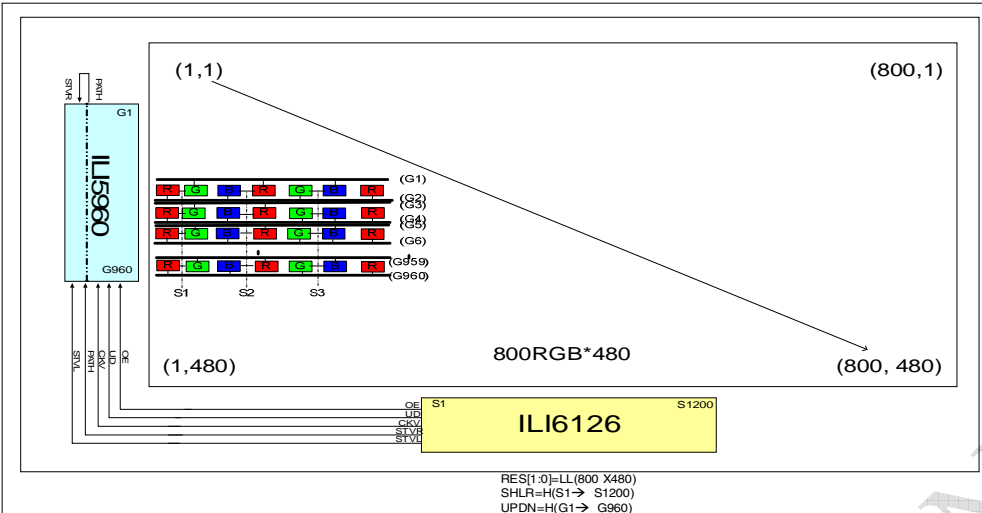
Note: Gate driver scan and output sequence (ILI5602)

800(RGB) x 480 (Gate driver on right side)

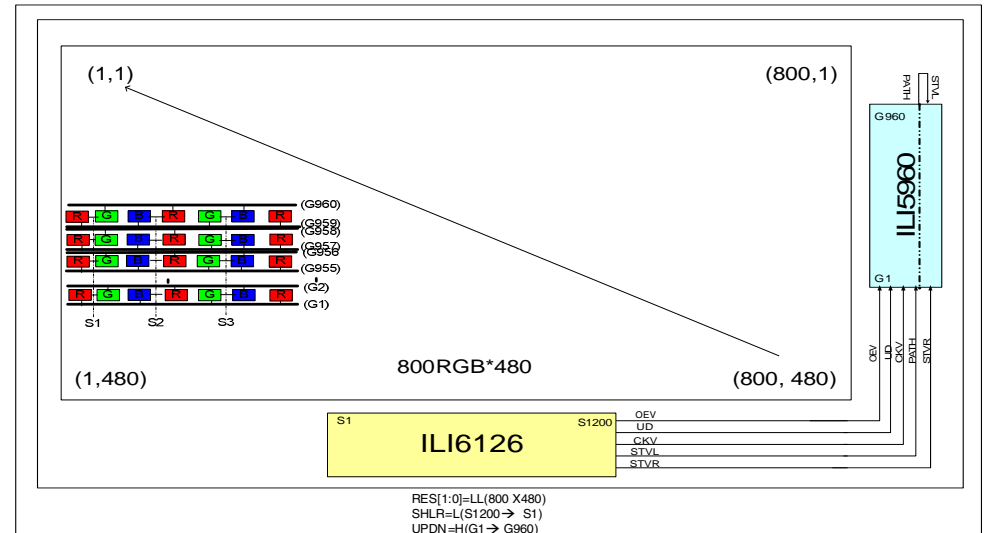
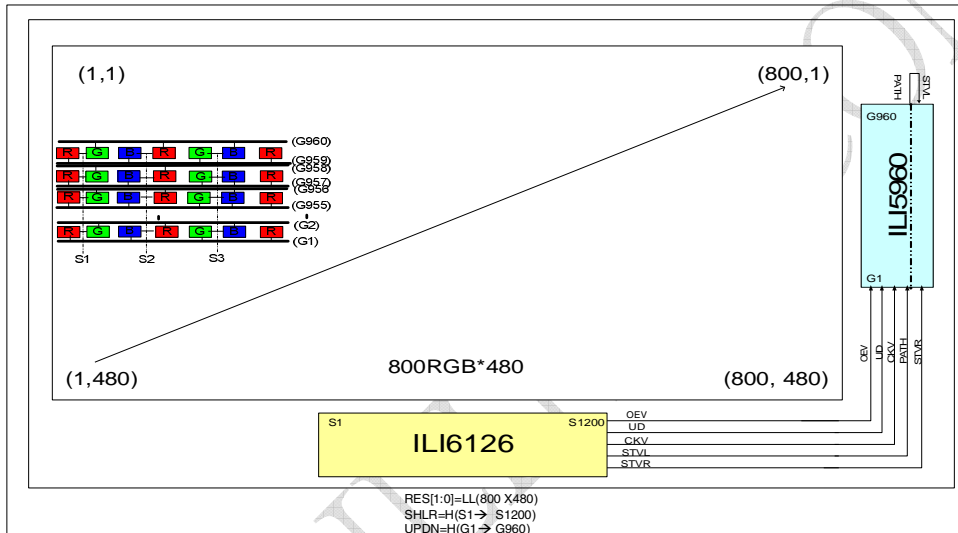
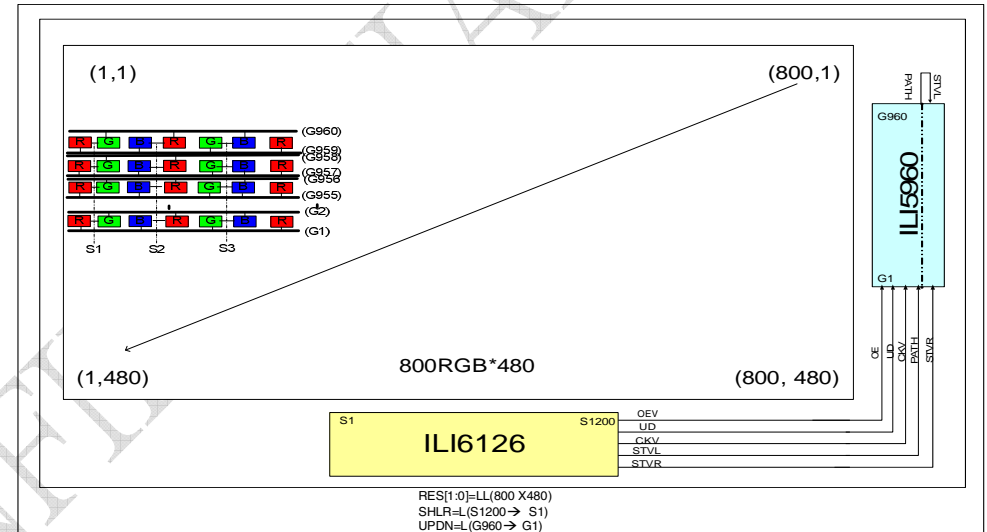
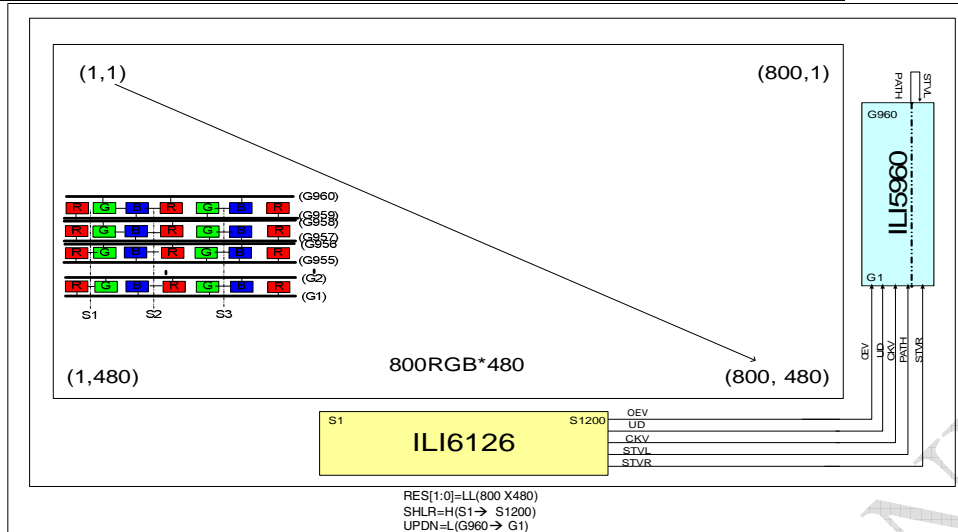
CFSEL	UPDN	Scan Direction	Color Filter Mapping
L	L	G960→G001	G960→ <b>R</b>
L	H	G001→G960	G001→ <b>G</b>



CFSEL	UPDN	Scan Direction	Color Filter Mapping
L	H	G001→G960	G001→G
L	L	G960→G001	G960→R

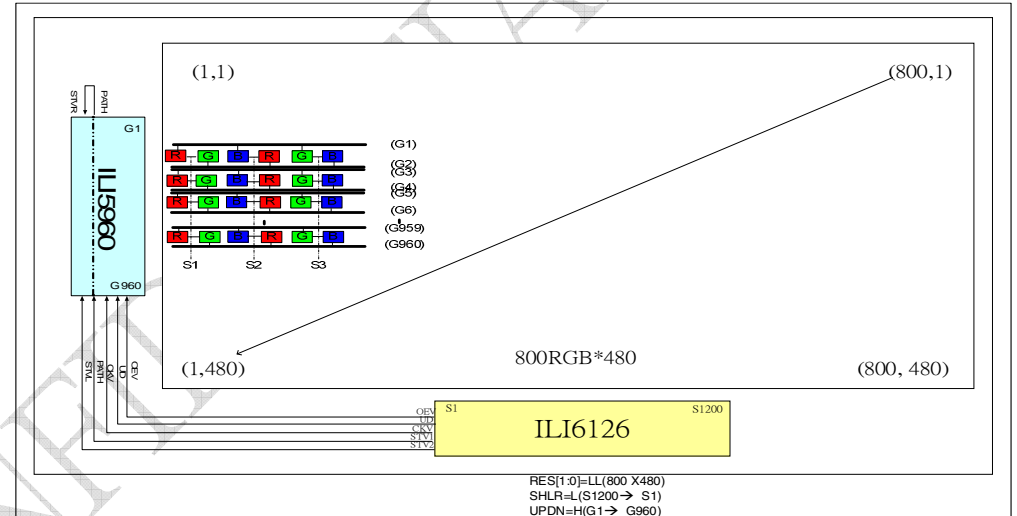
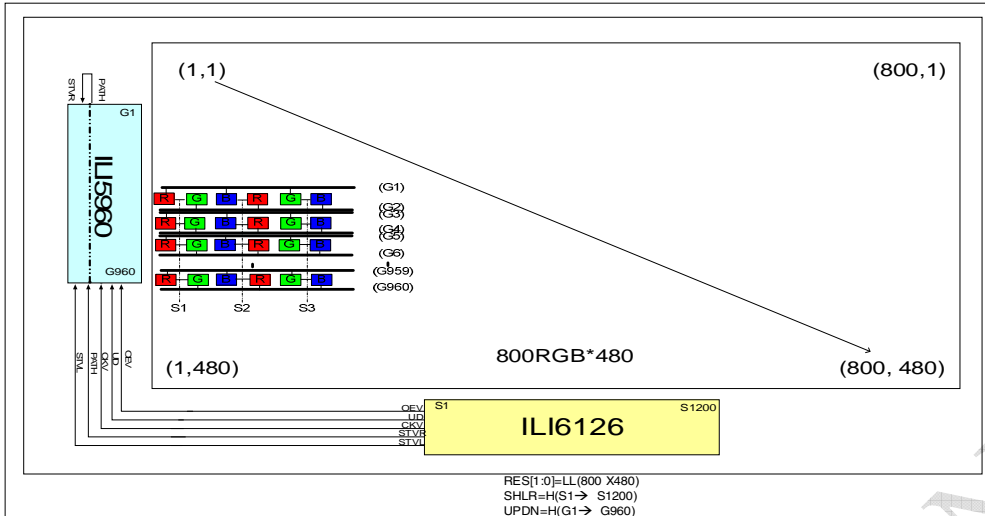


CFSEL	UPDN	Scan Direction	Color Filter Mapping
H	L	G960→G001	G960→G
H	H	G001→G960	G001→R

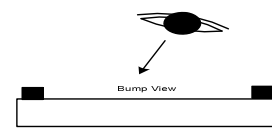
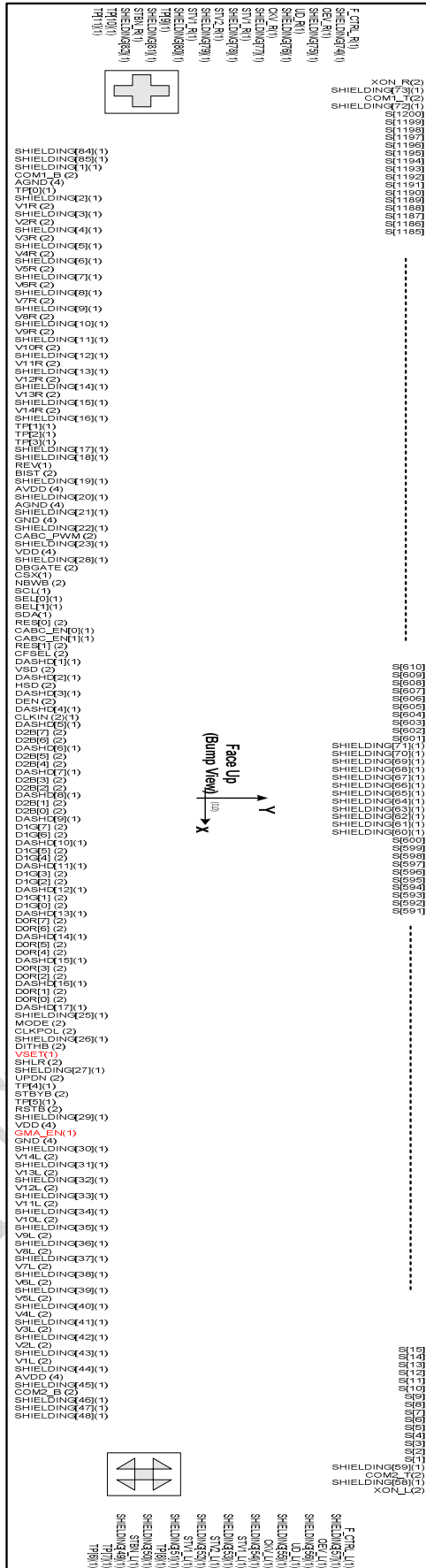


800(RGB) x 480 (Gate driver on left side)

CFSEL	UPDN	Scan Direction	Color Filter Mapping
H	H	G001→G960	G001→R
H	L	G960→G001	G960→G



### 5. Pad Sequence (Bump Side)



## 6. Pin Descriptions

Pin Name	I/O	Descriptions
CLKIN	I	Clock for input data. Data latched at rising/falling edge of this signal. Default is falling edge.
D0R[7:0] D1G[7:0] D2B[7:0]	I	Digital data input. Dx0 is LSB and Dx7 is MSB. D0[7:0] = R[7:0] data; D1[7:0] = G[7:0] data; D2[7:0]=B[7:0] data When 18-bit RGB interface (disable dithering function), please use Dx[7:2] as 6-bit input and connect Dx[1:0] to DGND.
HSD	I	Horizontal sync input in digital parallel RGB. Negative polarity.
VSD	I	Vertical sync input in digital parallel RGB. Negative polarity.
DEN	I	Input data enable control. When DE mode, active High to enable data input. <b>Note: Normal pull low</b>
MODE	I	DE / SYNC mode select. MODE="L", for entering SYNC mode. MODE="H", for entering DE mode. <b>Note: Normal pull high</b>
NBWB	I	Normally black / white panel selection NBWB="H", normally white NBWB="L", normally black <b>Note: Normal pull high</b>
CFSEL	I	Color Filter type selection. ( Only For Dual-Gate Type Control ) CFSEL=L: 1 <sup>st</sup> Gate output start at "R" pixel CFSEL=H: 1 <sup>st</sup> Gate output start at "G" pixel <b>Note: Normal pull low</b>
GMA_EN	I	internal Gamma enable GMA_EN="H":disable GMA_EN="L": enable <b>Note: Normal pull low</b>
VSET	I	Gamma Voltage input selection L: 10 gamma voltage input H: 14 gamma voltage input <b>Note: Normal pull low</b>
CSB	I	SPI chip select <b>Note: Normal pull high</b>
SCL	I	SPI clock <b>Note: Normal pull high</b>
SDA	I/O	SPI data <b>Note: Normal pull high</b>
RSTB	I	Hardware global reset. Low active. <b>Note: Normal pull high</b>
RES[1:0]	I	Display resolution selection. RES[1:0]="00", for 800(RGB)x480 display resolution. RES[1:0]="01", for 800(RGB)x600 display resolution. RES[1:0]="10", for 640(RGB)x480 display resolution. RES[1:0]="11", for 400(RGB)x240 display resolution. <b>Note: Normal pull "LL"</b>
DITHB	I	Dithering function enable control. DITHB="L", to enable internal dithering function. DITHB="H", to disable internal dithering function. <b>Note: Normal pull high</b>
CLKPOL	I	Input clock edge selection. CLKPOL="L", latch data at CLKIN falling edge. CLKPOL="H", latch data at CLKIN rising edge.



Pin Name	I/O	Descriptions																					
		<b>Note: Normal pull low</b>																					
VR[14:1] VL[14:1]	P	Gamma correction reference voltage. These input voltages must be offered by user. The relationship between V1~V14 must be : When VSET=H AGND+0.1V<V14<V13<V12<V11<V10<V9<V8<V7<V6<V5<V4<V3<V2<V1<AVDD-0.1V When VSET=L AGND+0.1V<V14 <V12<V11<V10 <V8<V7<V5<V4<V3 <V1<AVDD-0.1V																					
DBGATE	I	Dual gate function enables control. Normally pull low. DBGATE="L", disable dual gate function. <b>(Default)</b> DBGATE="H", enable dual gate function <b>Note: Normal pull low</b>																					
SEL[1:0]	I	DBGATE="H" Gate driver scan scheme selection <b>Note: Normal pull low</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>SELO</th> <th>SEL1</th> <th>Scan type</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>Z(default)</td> </tr> <tr> <td>L</td> <td>H</td> <td>Inverse Z</td> </tr> <tr> <td>H</td> <td>L</td> <td>弓</td> </tr> <tr> <td>H</td> <td>H</td> <td>Z+弓</td> </tr> </tbody> </table> DBGATE="L" <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>SELO</th> <th>Dot Polarity Inversion</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>1+2 dot</td> </tr> <tr> <td>L</td> <td>1 dot</td> </tr> </tbody> </table>	SELO	SEL1	Scan type	L	L	Z(default)	L	H	Inverse Z	H	L	弓	H	H	Z+弓	SELO	Dot Polarity Inversion	H	1+2 dot	L	1 dot
SELO	SEL1	Scan type																					
L	L	Z(default)																					
L	H	Inverse Z																					
H	L	弓																					
H	H	Z+弓																					
SELO	Dot Polarity Inversion																						
H	1+2 dot																						
L	1 dot																						
STBYB	I	Standby mode control. STBYB="L", enter standby mode for power saving. Timing controller and source driver will turn off, all outputs are Hi-Z. STBYB="H", normal operation. <b>Note: Normal pull high</b>																					
SHLR	I	Source shift direction control. SHLR="L", shift direction is "S[1200] → S[1199] → S[1198] → ... → S[3] → S[2] → S[1]" SHLR="H", shift direction is "S[1] → S[2] → S[3] → ... → S[1198] → S[1199] → S[1200]". <b>Note: Normal pull high</b>																					
UPDN	I	Gate scan direction control UPDN="L", STV2 outputs the vertical start pulse and UD pin outputs "L" to Gate driver. UPDN="H", STV1 outputs the vertical start pulse and UD pin outputs "H" to Gate driver. <b>Note: Normal pull low</b>																					
BIST	I	Normal operation / BIST pattern select. BIST="L", Normal operation BIST="H", BIST (DCLK input is not needed) <b>Note: Normal pull low</b>																					
CABC_EN[1:0]	I	CABC mode selection CABC_EN_IN[1:0]=[00], CABC OFF( <b>default pull low</b> ), CABC_PWM =High (default) CABC_EN_IN[1:0]=[01], UI CABC_EN_IN[1:0]=[10], Still picture CABC_EN_IN[1:0]=[11], moving image																					
CABC_PWM	O	Dimming brightness output for external controller CABC_PWM="L" : turn off external backlight controller CABC_PWM="H" : turn on external backlight controller																					
REV	I	Data invert or not control REV="L", keep data REV="H", invert data <b>Note: Normal pull low</b>																					
AVDD	P	Power supply for analog block.																					
AGND	P	Ground level for analog block.																					
VDD	P	Power supply for digital block.																					
GND	P	Ground level for digital block.																					
S[1] ~ S[1200]	O	Source driver output signals.																					
COM1_B COM2_B	S	Internal link together between input side and out side																					
COM1_T COM2_T	S	Internal link together between input side and out side																					

Pin Name	I/O	Descriptions						
CKV_L/ CKV_R	O	Gate Driver output control						
STV1_L/ STV1_R	O	Gate Driver output control						
STV2_L/ STV2_R	O	Gate Driver output control						
OEV_L/ OEV_R	O	Gate Driver output control						
UD_L/ UD_R	O	Gate Driver output control						
XON_L/ XON_R	O	Gate Driver output control						
F_CTRL_L/ F_CTRL_R	O	Gate Driver output control This pin decides to inverse output sequence or not in odd or even frame. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Frame</th> <th>F_CTRL</th> </tr> </thead> <tbody> <tr> <td>Odd</td> <td>L</td> </tr> <tr> <td>Even</td> <td>H</td> </tr> </tbody> </table>	Frame	F_CTRL	Odd	L	Even	H
Frame	F_CTRL							
Odd	L							
Even	H							
STBN_L/ STBN_R	O	Gate Driver output control						
TP[0] ~ TP[11]	T	Test pin for ILITEK only Float those pins for normal operation.						
SHIELDING[1]~[85]	--	IC shielding pads. Those pins are internally connected to AGND level.						
DASHD	--	Data bus shielding pad. Those pins are internally connected to DGND level.						

**Note:**

I: Input, O: Output, P: Power, D: Dummy, S: Shorted line, M: Mark, PI: Power input, PO: Power output, T: Testing, SH: Shielding, I / O: Input / Output, PS: Power Setting, COM1 Pass line description:

Pass Line No:	Pad Name	
1	COM1_B	COM1_T
2	COM2_B	COM2_T

T: Testing, SH: Shielding, I / O: Input / Output, PS: Power Setting, C: Capacitor pin.

**Value of wiring resistance to each pin**

The recommended wiring resistance values are shown below. The wiring resistance values affect the

current capacity of the power supply, so be sure to design using values that do not exceed those recommended

Pin Name	Wiring resistance value(Ω)	Pin Name	Wiring resistance value(Ω)
VDD	<25	RSTB	<1K
AVDD	<5	BIST	<1K
GND	<25	REV	<1K
AGND	<5	CSB	<1K
VR[14:1]/VL[14:1]	<20	SCL	<1K
D0R[7:0]	<200	SDA	<1K
D1G[7:0]	<200	STBYB	<1K
D2B[7:0]	<200	CKV_L / CKV_R	< 200 & 20 pf
DEN	<200	STV1_L / STV1_R	< 200 & 20 pf
CLKIN	<50	STV2_L / STV2_R	< 200 & 20 pf
HSD	<200	OEV_L / OEV_R	< 200 & 20 pf
VSD	<200	UD_L / UD_R	< 200 & 20 pf
MODE	<1K	XON_L / XON_R	< 200 & 20 pf
RES[1:0]	<1K	F_CTRL_L / F_CTRL_R	< 200 & 20 pf
DITHB	<1K	STBN_L / STBN_R	< 200 & 20 pf
CLKPOL	<1K	CABC_EN[1:0]	<1K
CABC_PWM	<1K	SEL[1:0]	<1K
CFSEL	<1K	UPDN	<1K
VSET	<1K	DBGATE	<1K
SHLR	<1K	<b>GMA_EN</b>	<1K

Source Output Status With RES[1:0] Pin Selection:

RES[1:0]	Resolution	Enable Channel	Disable Channel
L L	800X480	S[1]~S[1200]	--
L H	800X600	S[1]~S[1200]	--
H L	640X480	S[1]~S[480] ; S[721]~S[1200]	S[481]~S[720] ( Hi-Z )
H H	400X240	S[1]~S[1200]	--

## 7. Relationship between input data and output channels

1. DBGATE="0": Dual Gate Disable and Color Filter with Stripe Type.

(1) SHLR="1", right shift ( Default ) Note: Gout1~Gout m → Gate IC out channel. S[1]~S[n] → Source IC out channel

Output	S[1]	S[2]	S[3]	---	S[1198]	S[1199]	S[1200]	
Order	First data				→	Last data		
Odd Line	D0R[7]~D0R[0]	D1G[7]~D1G[0]	D2B[7]~D2B[0]	---	D0R[7]~D0R[0]	D1G[7]~D1G[0]	D2B[7]~D2B[0]	
Even Line	D0R[7]~D0R[0]	D1G[7]~D1G[0]	D2B[7]~D2B[0]	---	D0R[7]~D0R[0]	D1G[7]~D1G[0]	D2B[7]~D2B[0]	

(2) SHLR="0", left shift

Output	S[1]	S[2]	S[3]	---	S[1198]	S[1199]	S[1200]	
Order	Last data				←	First data		
Odd Line	D0R[7]~D0R[0]	D1G[7]~D1G[0]	D2B[7]~D2B[0]	---	D0R[7]~D0R[0]	D1G[7]~D1G[0]	D2B[7]~D2B[0]	
Even Line	D0R[7]~D0R[0]	D1G[7]~D1G[0]	D2B[7]~D2B[0]	---	D0R[7]~D0R[0]	D1G[7]~D1G[0]	D2B[7]~D2B[0]	

2. DBGATE="1", CFSEL="L": Dual Gate Enable and Color Filter with Stripe Type. ( Gate driver on right side)

(1) SHLR="1", right shift

Output	S[1]	S[2]	S[3]	---	S[1198]	S[1199]	S[1200]	
Order	First data				→	Last data		
Gout m	D0R[7]~D0R[0]	D2B[7]~D2B[0]	D1G[7]~D1G[0]	---	D0R[7]~D0R[0]	D2B[7]~D2B[0]	D1G[7]~D1G[0]	
Gout(m-1)	D1G[7]~D1G[0]	D0R[7]~D0R[0]	D2B[7]~D2B[0]	---	D1G[7]~D1G[0]	D0R[7]~D0R[0]	D2B[7]~D2B[0]	
Gout(m-2)	D0R[7]~D0R[0]	D2B[7]~D2B[0]	D1G[7]~D1G[0]	---	D0R[7]~D0R[0]	D2B[7]~D2B[0]	D1G[7]~D1G[0]	
Gout(m-3)	D1G[7]~D1G[0]	D0R[7]~D0R[0]	D2B[7]~D2B[0]	---	D1G[7]~D1G[0]	D0R[7]~D0R[0]	D2B[7]~D2B[0]	

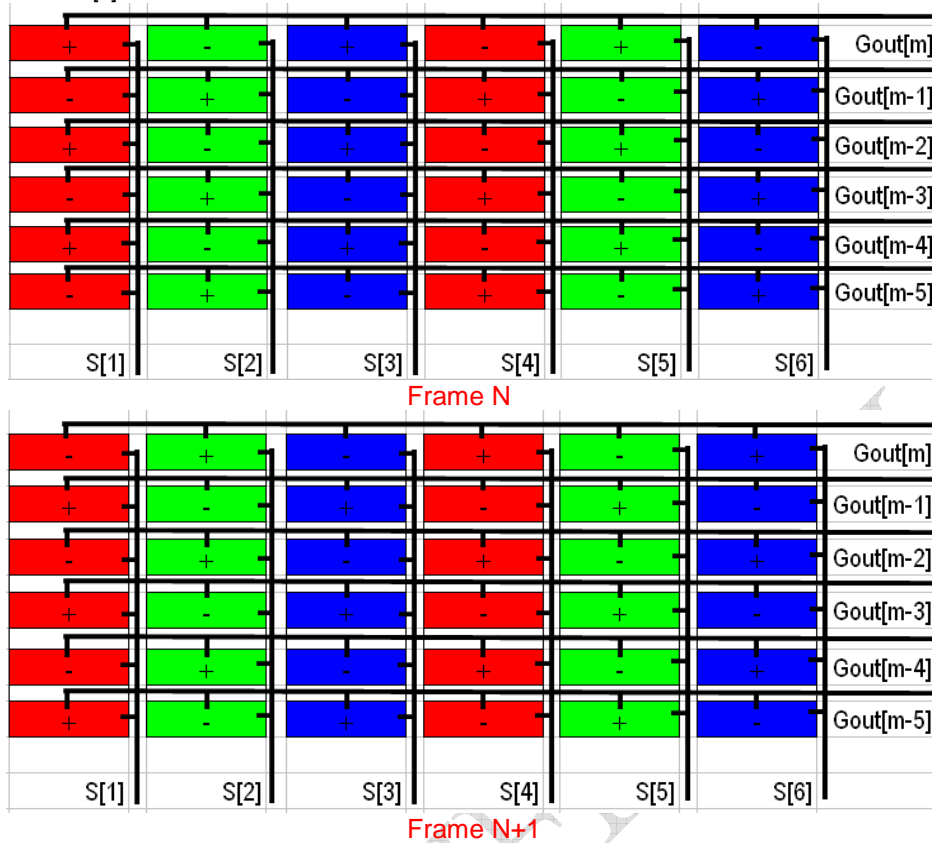
(2) SHLR="0", Left shift

Output	S[1]	S[2]	S[3]	---	S[1198]	S[1199]	S[1200]	
Order	Last data				←	First data		
Gout m	D0R[7]~D0R[0]	D2B[7]~D2B[0]	D1G[7]~D1G[0]	---	D0R[7]~D0R[0]	D2B[7]~D2B[0]	D1G[7]~D1G[0]	
Gout(m-1)	D1G[7]~D1G[0]	D0R[7]~D0R[0]	D2B[7]~D2B[0]	---	D1G[7]~D1G[0]	D0R[7]~D0R[0]	D2B[7]~D2B[0]	
G(m-2)	D0R[7]~D0R[0]	D2B[7]~D2B[0]	D1G[7]~D1G[0]	---	D0R[7]~D0R[0]	D2B[7]~D2B[0]	D1G[7]~D1G[0]	
G(m-3)	D1G[7]~D1G[0]	D0R[7]~D0R[0]	D2B[7]~D2B[0]	---	D1G[7]~D1G[0]	D0R[7]~D0R[0]	D2B[7]~D2B[0]	

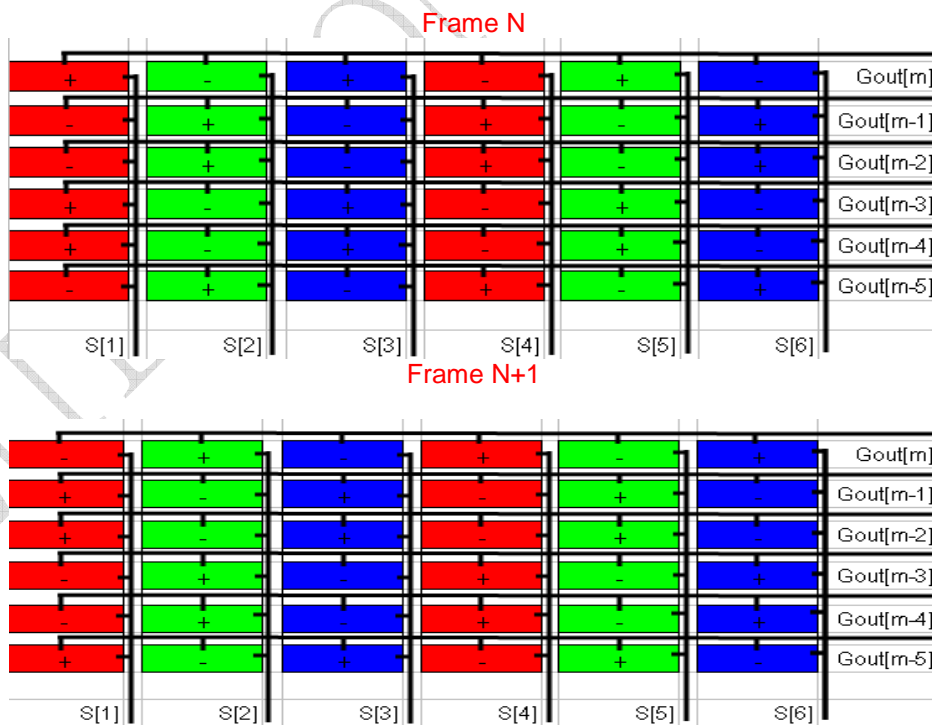
### Dot Polarity Inversion

ILI6126 supplies both of 2-dot and 1+2-dot inversion, the pixel polarity inversion was illustrated as below:

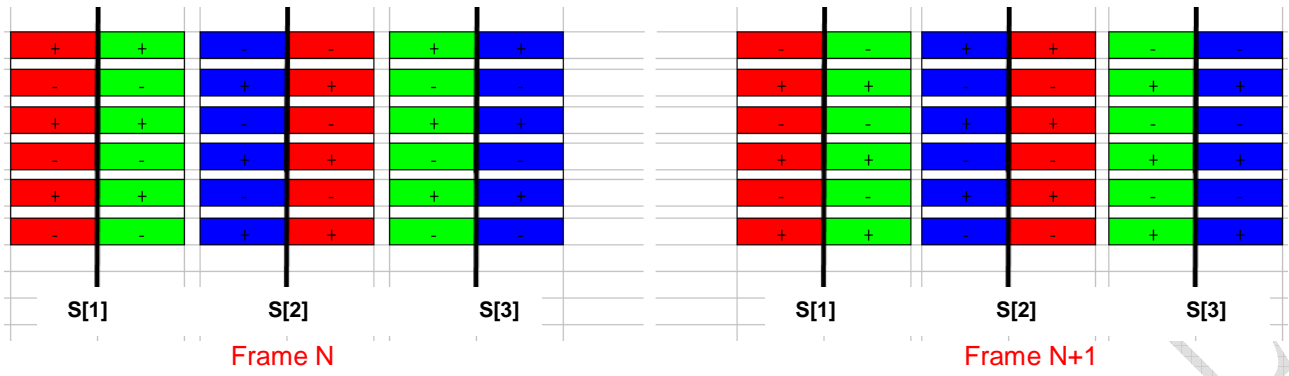
Case1: DBGATE =L & SEL[0]=L With Normal mode at 1 Dot



Case2: DBGATE =L & SEL[0]=H With Normal Mode at 1+2 Dot



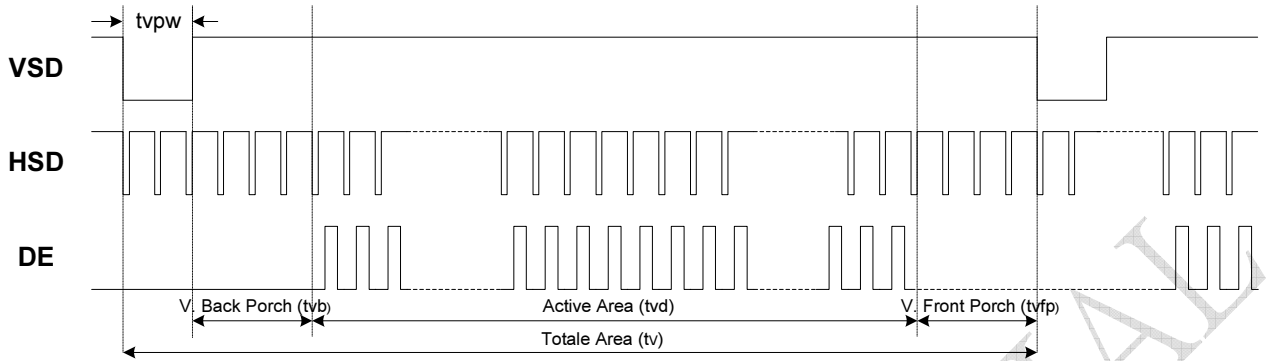
Case3: DBGATE =H at Gual-Gate Mode with 2-Dot Inversion



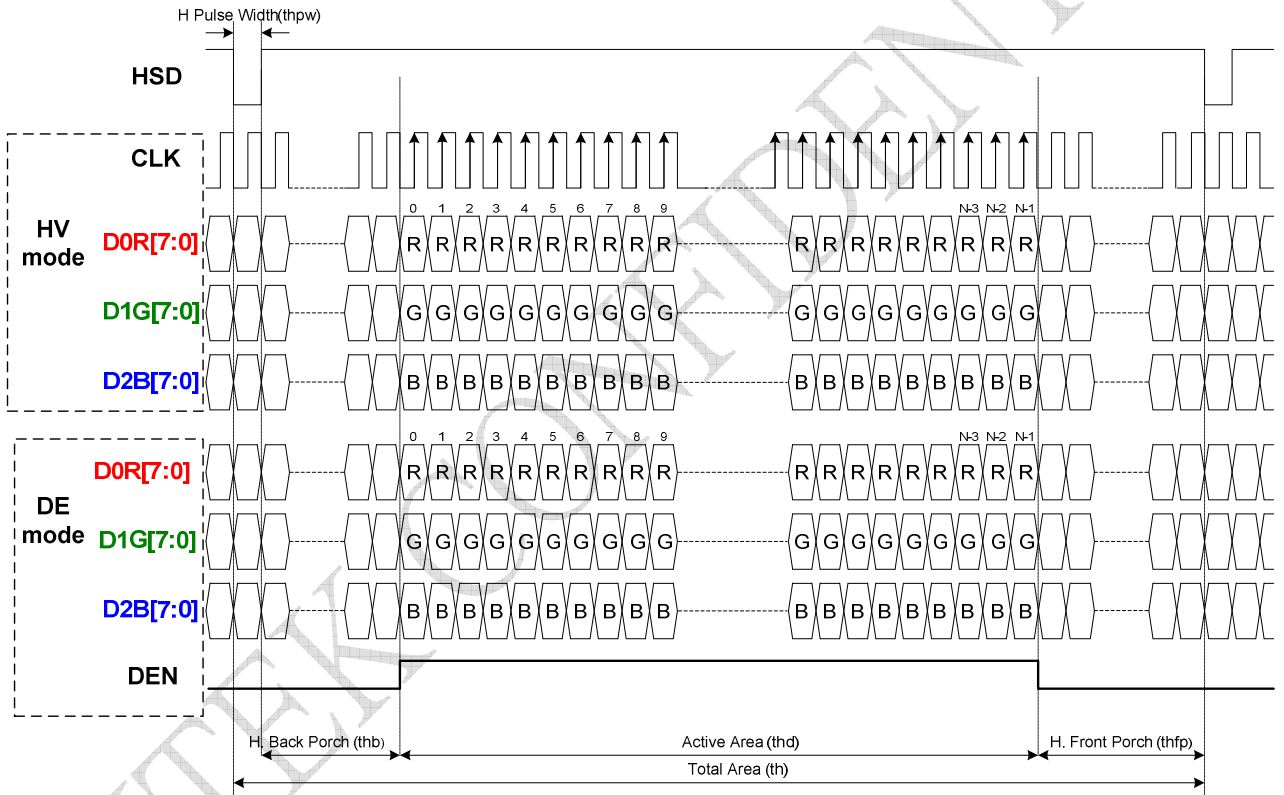
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## 8. Display Data Input Timing

### 8.1. Vertical Input Timing



### 8.2. Horizontal Input Timing



### 8.3. Timing Characteristic

A. Resolution 800\*480

A.1: HV Mode

Horizontal input timing

Parameter	Symbol	Value			Unit	Note
Horizontal display area	thd	800			DCLK	
DCLK frequency	fclk	Min.	Typ.	Max.	--	
		-	33.3	50	MHz	
1 Horizontal Line	th	908	928	1010	DCLK	thb+thpw=88 DCLK is fixed.
HSD pulse width	thpw	4	48	64		
HSD Back Porch (Blanking)	thb	20	40	84		
HSD Front Porch	thfp	20	40	122		

Vertical input timing

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Vertical display area	tvd	480			H	
VSD period time	tv	515	525	-	H	
VSD pulse width	tpw	1	3	31	H	tpw+tvb=32H Is fixed
VSD Back Porch (Blanking)	tvb	1	29	31	H	
VSD Front Porch	tvfp	3	13	-	H	

A.2: DE Mode

Parameter	Symbol	Spec			Unit
		Min.	Typ.	Max.	
CLK frequency	fclk	-	33.3	50	MHz
DE H period	thpw+thb+thd+thfp = th	920	1000	1010	DCLK
DE H-Display Area	thd	800			DCLK
DE H-Blanking	th-thd	120	200	210	DCLK
DE V period	tpw+tvb+tvd+tvfp	500	512	-	DCLK
DE V-Display Area	tvd	480			th
DE V-Blanking	tv-tvd	20	32	-	th

B. Resolution 800\*600

B.1: HV Mode

Horizontal input timing

Parameter	Symbol	Value			Unit	Note
Horizontal display area	thd	800			DCLK	
DCLK frequency	fclk	Min.	Typ.	Max.	--	
		-	40	50	MHz	
1 Horizontal Line	th	908	1000	1010	DCLK	thb+thpw=88 DCLK is fixed.
HSD pulse width	thpw	4	48	64		
HSD Back Porch (Blanking)	thb	20	40	84		
HSD Front Porch	thfp	20	112	122		

Vertical input timing

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Vertical display area	tvd	600			H	
VSD period time	tv	642	660	-	H	
VSD pulse width	tpw	1	3	38	H	tpw+tvb=39H Is fixed
VSD Back Porch (Blanking)	tvb	1	36	38	H	
VSD Front Porch	tvfp	3	21	-	H	



B.2: DE Mode

Parameter	Symbol	Spec			Unit
		Min.	Typ.	Max.	
CLK frequency	fclk	-	40	50	MHz
DE H period	thpw+thb+thd+thfp = th	920	1000	1010	DCLK
DE H-Display Area	thd	800			DCLK
DE H-Blanking	th-thd	120	200	210	DCLK
DE V period	tpw+tvb+tvd+tvfp	620	632	-	DCLK
DE V-Display Area	tvd	600			th
DE V-Blanking	tv-tvd	20	39	-	th

C. Resolution 640\*480

C.1: HV Mode

Horizontal input timing

Parameter	Symbol	Value			Unit	Note
Horizontal display area	thd	640			DCLK	
DCLK frequency	fclk	Min.	Typ.	Max.	--	
		-	24	50		
1 Horizontal Line	th	748	760	1010	DCLK	thb+thpw=88 DCLK is fixed.
HSD pulse width	thpw	4	48	64		
HSD Back Porch (Blanking)	thb	20	40	84		
HSD Front Porch	thfp	20	32	282		

Vertical input timing

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Vertical display area	tvd	480			H	
VSD period time	tv	515	525	--	H	
VSD pulse width	tpw	1	3	31	H	tpw+tvb=32H Is fixed
VSD Back Porch (Blanking)	tvb	1	29	31	H	
VSD Front Porch	tvfp	3	13	--	H	

C.2: DE Mode

Parameter	Symbol	Spec			Unit
		Min.	Typ.	Max.	
CLK frequency	fclk	-	24	50	MHz
DE H period	thpw+thb+thd+thfp = th	960	840	1010	DCLK
DE H-Display Area	thd	640			DCLK
DE H-Blanking	th-thd	120	200	370	DCLK
DE V period	tpw+tvb+tvd+tvfp	500	512	-	DCLK
DE V-Display Area	tvd	480			th
DE V-Blanking	tv-tvd	20	32	-	th

D. Resolution 400\*240

D.1: HV Mode

Horizontal input timing

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Horizontal display area	thd	400			DCLK	
DCLK frequency	fclk	--	7.1	50	--	
					MHz	
1 Horizontal Line	th	508	520	1010	DCLK	thb+thpw=88 DCLK is fixed.
HSD pulse width	thpw	4	40	64		
HSD Back Porch (Blanking)	thb	20	48	84		
HSD Front Porch	thfp	20	32	570		

Vertical input timing

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Vertical display area	tvd	240			H	
VSD period time	tv	260	270	--	H	
VSD pulse width	tvpw	1	3	16	H	tvpw+tvb=17H Is fixed
VSD Back Porch (Blanking)	tvb	1	14	16	H	
VSD Front Porch	tvfp	3	13	--	H	

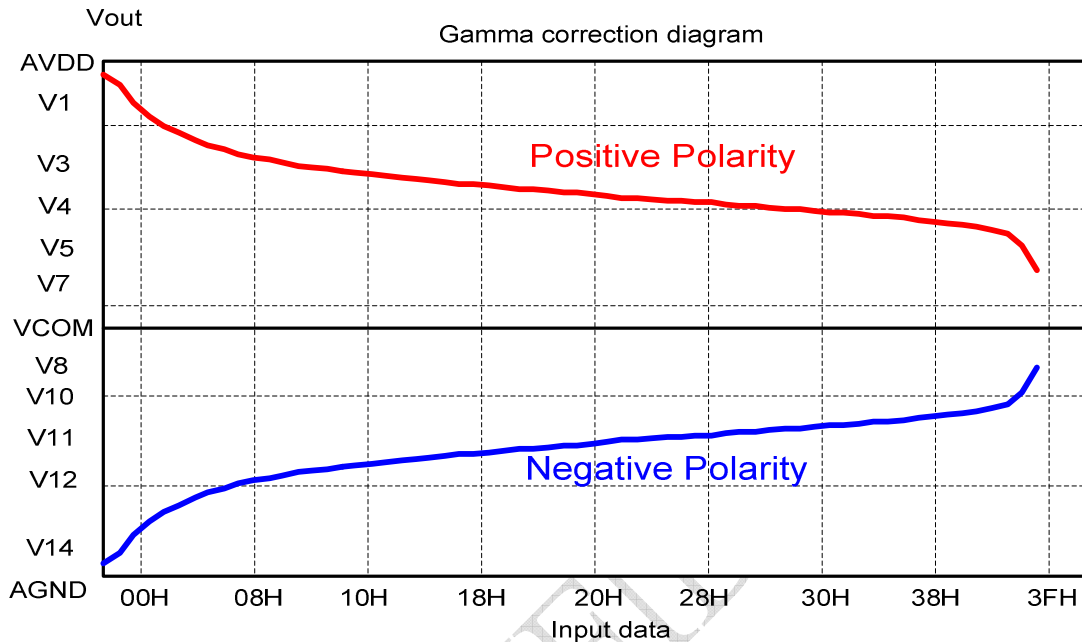
D.2: DE Mode

Parameter	Symbol	Spec			Unit
		Min.	Typ.	Max.	
CLK frequency	fclk	--	7.1	50	MHz
DE H period	thpw+thb+thd+thfp = th	520	600	1010	DCLK
DE H-Display Area	thd	400			DCLK
DE H-Blanking	th-thd	120	200	490	DCLK
DE V period	tvpw+tvb+tvd+tvfp	260	272	--	DCLK
DE V-Display Area	tvd	240			th
DE V-Blanking	tv-tvd	20	32	--	th

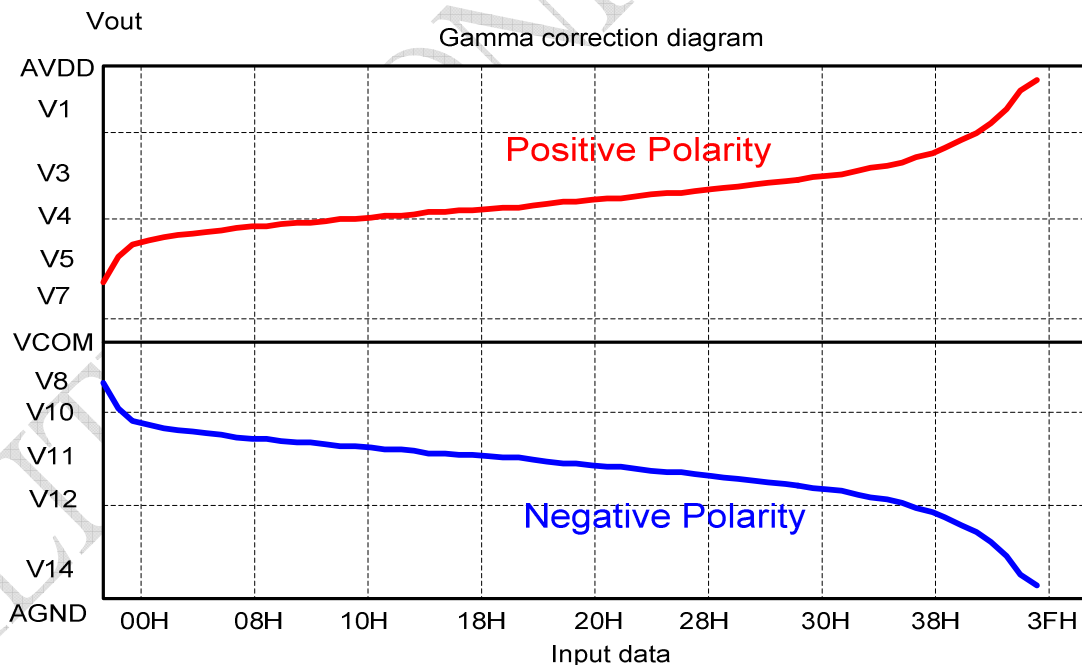
## 9. Relationship between gamma correction and output voltage

The output voltage is determined by the 6-bit digital input data, and the V1 ~ V14 gamma correction reference voltage inputs. The figure in the following shows the relationship between the input data and the output voltage. Refer the next page for the relative values and voltage calculation method.

Gamma correction characteristic curve:

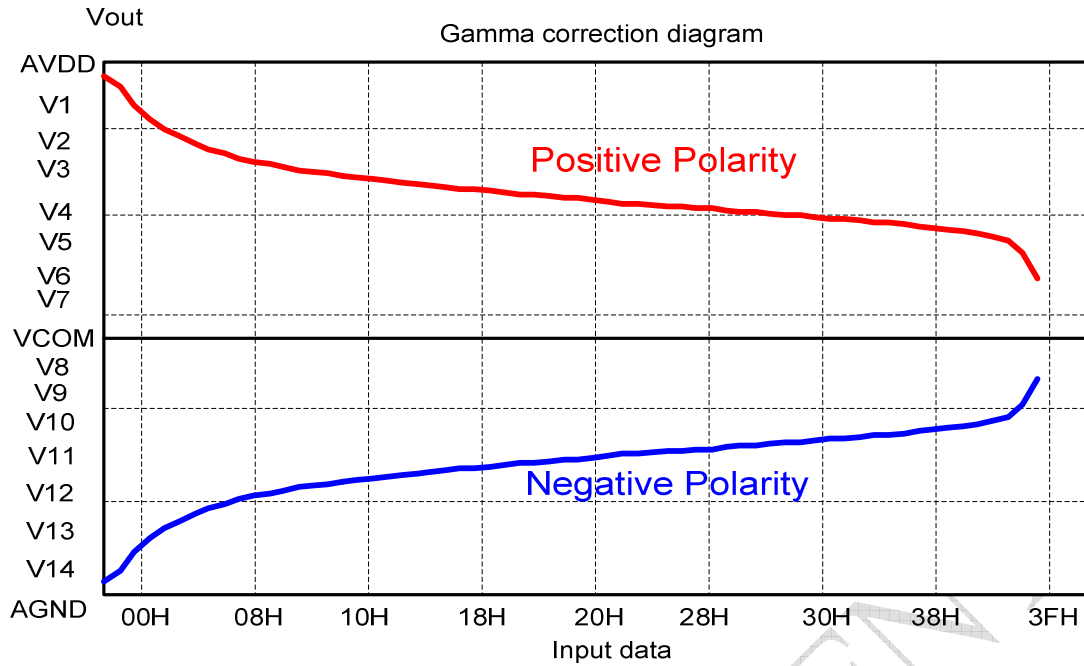


REV=L & NBWB = H ( Default ) ; VSET=L

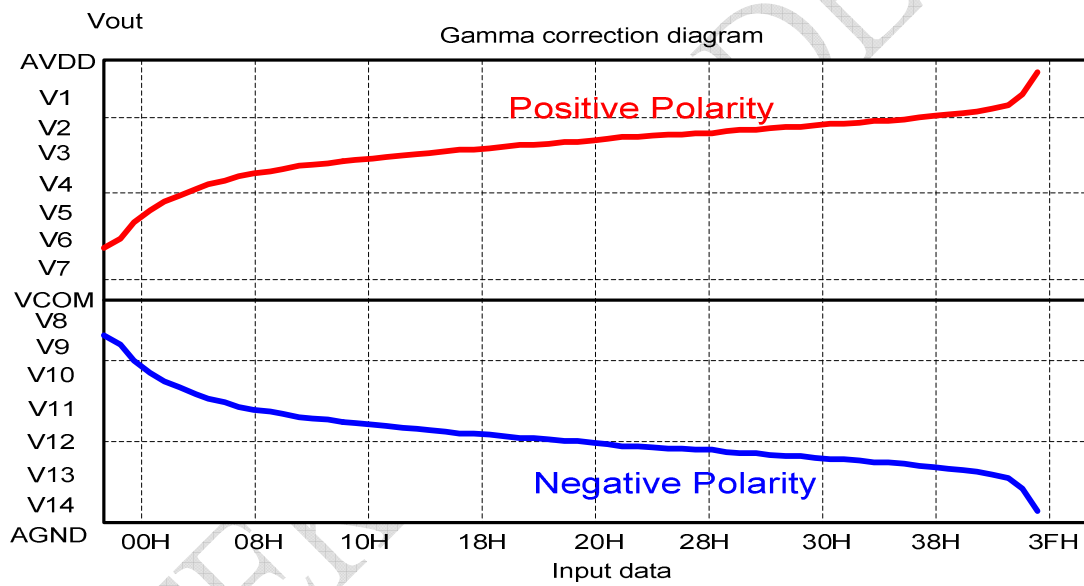


REV=L & NBWB = L ; VSET=L

Note: AVDD-0.1V > V1 > V3 > V4 > V5 > V7; V8 > V10 > V11 > V12 > V14 > AGND+0.1V



REV=L & NBWB = H ( Default ) ; VSET=H



REV=L & NBWB = L ; VSET=H

Note: AVDD-0.1V > V1 > V2 > V3 > V4 > V5 > V6 > V7; V8 > V9 > V10 > V11 > V12 > V13 > V14 > AGND+0.1V

### Input Data and Output Voltage Reference Table

AVDD= 8.8V VSET=H

GAMMA	V1	V2	V3	V4	V5	V6	V7	V8	V9	V10	V11	V12	V13	V14
AVDD Ratio	0.8085	0.7905	0.6896	0.6445	0.6096	0.5867	0.5496	0.38126	0.29906	0.24794	0.21378	0.16875	0.06778	0.0495
	*AVDD	*AVDD	*AVDD	*AVDD	*AVDD	*AVDD	*AVDD	*AVDD	*AVDD	*AVDD	*AVDD	*AVDD	*AVDD	*AVDD
Voltage(V)	7.1148	6.9564	6.06848	5.6716	5.36448	5.16296	4.83648	3.355088	2.631728	2.181872	1.881264	1.485	0.596464	0.4356

### 9.1. Gamma correction resistor ratio

**NBWB=H REV=L ( default ) VSET=L (V2,V6,V9,V13 disable)**

	Name	Ratio		Name	Ratio	
V1/V14 →	R0	12.9		R32	1	← V4/V11
	R1	11.5		R33	1	
	R2	10		R34	1	
	R3	8.6		R35	1	
	R4	7.2		R36	1	
	R5	5.7		R37	1	
	R6	4.8		R38	1	
	R7	4		R39	1	
	R8	3.5		R40	1	
	R9	3		R41	1	
	R10	2.7		R42	1	
	R11	2.5		R43	1	
	R12	2.2		R44	1	
	R13	2.1		R45	1	
	R14	2		R46	1.1	
V3/V12 →	R15	1.8		R47	1.1	← V5/V10
	R16	1.7		R48	1.1	
	R17	1.6		R49	1.1	
	R18	1.5		R50	1.1	
	R19	1.5		R51	1.2	
	R20	1.4		R52	1.3	
	R21	1.4		R53	1.3	
	R22	1.3		R54	1.4	
	R23	1.3		R55	1.6	
	R24	1.2		R56	1.7	
	R25	1.2		R57	1.9	
	R26	1.2		R58	2.2	
	R27	1.1		R59	2.6	
	R28	1.1		R60	3.2	
	R29	1.1		R61	5.6	
	R30	1.1		R62	44	← V7/V8
V4/V11 →	R31	1		R63		

Ratio → 1: 125ohm

Total Ratio = 192.7

**NBWB=H REV=L ( default ) VSET=H**

	Name	Ratio		Name	Ratio	
V1/V14	R0	12.9		R32	1	V4/V11
V2/V13	R1	11.5		R33	1	
	R2	10		R34	1	
	R3	8.6		R35	1	
	R4	7.2		R36	1	
	R5	5.7		R37	1	
	R6	4.8		R38	1	
	R7	4		R39	1	
	R8	3.5		R40	1	
	R9	3		R41	1	
	R10	2.7		R42	1	
	R11	2.5		R43	1	
	R12	2.2		R44	1	
	R13	2.1		R45	1	
	R14	2		R46	1.1	
V3/V12	R15	1.8		R47	1.1	V5/V10
	R16	1.7		R48	1.1	
	R17	1.6		R49	1.1	
	R18	1.5		R50	1.1	
	R19	1.5		R51	1.2	
	R20	1.4		R52	1.3	
	R21	1.4		R53	1.3	
	R22	1.3		R54	1.4	
	R23	1.3		R55	1.6	
	R24	1.2		R56	1.7	
	R25	1.2		R57	1.9	
	R26	1.2		R58	2.2	
	R27	1.1		R59	2.6	
	R28	1.1		R60	3.2	
	R29	1.1		R61	5.6	V6/V9
	R30	1.1		R62	44	V7/V8
V4/V11	R31	1		R63		

Ratio→ 1: 125ohm

Total  
Ratio= 192.7

## 9.2. Output Voltage VS Input Data

REV = L & **NBWB=H** ; **VSET=L**

Data	Positive polarity Output Voltage	Negative polarity Output Voltage	Data	Positive polarity Output Voltage	Negative polarity Output Voltage
<b>00H</b>	V1	V14	<b>20H</b>	V4	V11
<b>01H</b>	$V3 + (V1 - V3) \times 71.6/84.5$	$V14 + (V12 - V14) \times 12.9/84.5$	<b>21H</b>	$V5 + (V4 - V5) \times 15.2/16.2$	$V11 + (V10 - V11) \times 1/16.2$
<b>02H</b>	$V3 + (V1 - V3) \times 60.1/84.5$	$V14 + (V12 - V14) \times 24.4/84.5$	<b>22H</b>	$V5 + (V4 - V5) \times 14.2/16.2$	$V11 + (V10 - V11) \times 2/16.2$
<b>03H</b>	$V3 + (V1 - V3) \times 50.1/84.5$	$V14 + (V12 - V14) \times 34.4/84.5$	<b>23H</b>	$V5 + (V4 - V5) \times 13.2/16.2$	$V11 + (V10 - V11) \times 3/16.2$
<b>04H</b>	$V3 + (V1 - V3) \times 41.5/84.5$	$V14 + (V12 - V14) \times 43/84.5$	<b>24H</b>	$V5 + (V4 - V5) \times 12.2/16.2$	$V11 + (V10 - V11) \times 4/16.2$
<b>05H</b>	$V3 + (V1 - V3) \times 34.3/84.5$	$V14 + (V12 - V14) \times 50.2/84.5$	<b>25H</b>	$V5 + (V4 - V5) \times 11.2/16.2$	$V11 + (V10 - V11) \times 5/16.2$
<b>06H</b>	$V3 + (V1 - V3) \times 28.6/84.5$	$V14 + (V12 - V14) \times 55.9/84.5$	<b>26H</b>	$V5 + (V4 - V5) \times 10.2/16.2$	$V11 + (V10 - V11) \times 6/16.2$
<b>07H</b>	$V3 + (V1 - V3) \times 23.8/84.5$	$V14 + (V12 - V14) \times 60.7/84.5$	<b>27H</b>	$V5 + (V4 - V5) \times 9.2/16.2$	$V11 + (V10 - V11) \times 7/16.2$
<b>08H</b>	$V3 + (V1 - V3) \times 19.8/84.5$	$V14 + (V12 - V14) \times 64.7/84.5$	<b>28H</b>	$V5 + (V4 - V5) \times 8.2/16.2$	$V11 + (V10 - V11) \times 8/16.2$
<b>09H</b>	$V3 + (V1 - V3) \times 16.3/84.5$	$V14 + (V12 - V14) \times 68.2/84.5$	<b>29H</b>	$V5 + (V4 - V5) \times 7.2/16.2$	$V11 + (V10 - V11) \times 9/16.2$
<b>0AH</b>	$V3 + (V1 - V3) \times 13.3/84.5$	$V14 + (V12 - V14) \times 71.2/84.5$	<b>2AH</b>	$V5 + (V4 - V5) \times 6.2/16.2$	$V11 + (V10 - V11) \times 10/16.2$
<b>0BH</b>	$V3 + (V1 - V3) \times 10.6/84.5$	$V14 + (V12 - V14) \times 73.9/84.5$	<b>2BH</b>	$V5 + (V4 - V5) \times 5.2/16.2$	$V11 + (V10 - V11) \times 11/16.2$
<b>0CH</b>	$V3 + (V1 - V3) \times 8.1/84.5$	$V14 + (V12 - V14) \times 76.4/84.5$	<b>2CH</b>	$V5 + (V4 - V5) \times 4.2/16.2$	$V11 + (V10 - V11) \times 12/16.2$
<b>0DH</b>	$V3 + (V1 - V3) \times 5.9/84.5$	$V14 + (V12 - V14) \times 78.6/84.5$	<b>2DH</b>	$V5 + (V4 - V5) \times 3.2/16.2$	$V11 + (V10 - V11) \times 13/16.2$
<b>0EH</b>	$V3 + (V1 - V3) \times 3.8/84.5$	$V14 + (V12 - V14) \times 80.7/84.5$	<b>2EH</b>	$V5 + (V4 - V5) \times 2.2/16.2$	$V11 + (V10 - V11) \times 14/16.2$
<b>0FH</b>	$V3 + (V1 - V3) \times 1.8/84.5$	$V14 + (V12 - V14) \times 82.7/84.5$	<b>2FH</b>	$V5 + (V4 - V5) \times 1.1/16.2$	$V11 + (V10 - V11) \times 15.1/16.2$
<b>10H</b>	V3	V12	<b>30H</b>	V5	V10
<b>11H</b>	$V4 + (V3 - V4) \times 19/20.7$	$V12 + (V11 - V12) \times 1.7/20.7$	<b>31H</b>	$V7 + (V5 - V7) \times 70.2/71.3$	$V10 + (V8 - V10) \times 1.1/71.3$
<b>12H</b>	$V4 + (V3 - V4) \times 17.4/20.7$	$V12 + (V11 - V12) \times 3.3/20.7$	<b>32H</b>	$V7 + (V5 - V7) \times 69.1/71.3$	$V10 + (V8 - V10) \times 2.2/71.3$
<b>13H</b>	$V4 + (V3 - V4) \times 15.9/20.7$	$V12 + (V11 - V12) \times 4.8/20.7$	<b>33H</b>	$V7 + (V5 - V7) \times 68/71.3$	$V10 + (V8 - V10) \times 3.3/71.3$
<b>14H</b>	$V4 + (V3 - V4) \times 14.4/20.7$	$V12 + (V11 - V12) \times 6.3/20.7$	<b>34H</b>	$V7 + (V5 - V7) \times 66.8/71.3$	$V10 + (V8 - V10) \times 4.5/71.3$
<b>15H</b>	$V4 + (V3 - V4) \times 13/20.7$	$V12 + (V11 - V12) \times 7.7/20.7$	<b>35H</b>	$V7 + (V5 - V7) \times 65.5/71.3$	$V10 + (V8 - V10) \times 5.8/71.3$
<b>16H</b>	$V4 + (V3 - V4) \times 11.6/20.7$	$V12 + (V11 - V12) \times 9.1/20.7$	<b>36H</b>	$V7 + (V5 - V7) \times 64.2/71.3$	$V10 + (V8 - V10) \times 7.1/71.3$
<b>17H</b>	$V4 + (V3 - V4) \times 10.3/20.7$	$V12 + (V11 - V12) \times 10.4/20.7$	<b>37H</b>	$V7 + (V5 - V7) \times 62.8/71.3$	$V10 + (V8 - V10) \times 8.5/71.3$
<b>18H</b>	$V4 + (V3 - V4) \times 9/20.7$	$V12 + (V11 - V12) \times 11.7/20.7$	<b>38H</b>	$V7 + (V5 - V7) \times 61.2/71.3$	$V10 + (V8 - V10) \times 10.1/71.3$
<b>19H</b>	$V4 + (V3 - V4) \times 7.8/20.7$	$V12 + (V11 - V12) \times 12.9/20.7$	<b>39H</b>	$V7 + (V5 - V7) \times 59.5/71.3$	$V10 + (V8 - V10) \times 11.8/71.3$
<b>1AH</b>	$V4 + (V3 - V4) \times 6.6/20.7$	$V12 + (V11 - V12) \times 14.1/20.7$	<b>3AH</b>	$V7 + (V5 - V7) \times 57.6/71.3$	$V10 + (V8 - V10) \times 13.7/71.3$
<b>1BH</b>	$V4 + (V3 - V4) \times 5.4/20.7$	$V12 + (V11 - V12) \times 15.3/20.7$	<b>3BH</b>	$V7 + (V5 - V7) \times 55.4/71.3$	$V10 + (V8 - V10) \times 15.9/71.3$
<b>1CH</b>	$V4 + (V3 - V4) \times 4.3/20.7$	$V12 + (V11 - V12) \times 16.4/20.7$	<b>3CH</b>	$V7 + (V5 - V7) \times 52.8/71.3$	$V10 + (V8 - V10) \times 18.5/71.3$
<b>1DH</b>	$V4 + (V3 - V4) \times 3.2/20.7$	$V12 + (V11 - V12) \times 17.5/20.7$	<b>3DH</b>	$V7 + (V5 - V7) \times 49.6/71.3$	$V10 + (V8 - V10) \times 21.7/71.3$
<b>1EH</b>	$V4 + (V3 - V4) \times 2.1/20.7$	$V12 + (V11 - V12) \times 18.6/20.7$	<b>3EH</b>	$V7 + (V5 - V7) \times 44/71.3$	$V10 + (V8 - V10) \times 27.3/71.3$
<b>1FH</b>	$V4 + (V3 - V4) \times 1/20.7$	$V12 + (V11 - V12) \times 19.7/20.7$	<b>3FH</b>	V7	V8

REV = L & NBWB=L ; VSET=L

Data	Positive polarity Output Voltage	Negative polarity Output Voltage	Data	Positive polarity Output Voltage	Negative polarity Output Voltage
<b>3FH</b>	V1	V14	<b>1FH</b>	V4	V11
<b>3EH</b>	$V3 + (V1 - V3) \times 71.6/84.5$	$V14 + (V12 - V14) \times 12.9/84.5$	<b>1EH</b>	$V5 + (V4 - V5) \times 15.2/16.2$	$V11 + (V10 - V11) \times 1/16.2$
<b>3DH</b>	$V3 + (V1 - V3) \times 60.1/84.5$	$V14 + (V12 - V14) \times 24.4/84.5$	<b>1DH</b>	$V5 + (V4 - V5) \times 14.2/16.2$	$V11 + (V10 - V11) \times 2/16.2$
<b>3CH</b>	$V3 + (V1 - V3) \times 50.1/84.5$	$V14 + (V12 - V14) \times 34.4/84.5$	<b>1CH</b>	$V5 + (V4 - V5) \times 13.2/16.2$	$V11 + (V10 - V11) \times 3/16.2$
<b>3BH</b>	$V3 + (V1 - V3) \times 41.5/84.5$	$V14 + (V12 - V14) \times 43/84.5$	<b>1BH</b>	$V5 + (V4 - V5) \times 12.2/16.2$	$V11 + (V10 - V11) \times 4/16.2$
<b>3AH</b>	$V3 + (V1 - V3) \times 34.3/84.5$	$V14 + (V12 - V14) \times 50.2/84.5$	<b>1AH</b>	$V5 + (V4 - V5) \times 11.2/16.2$	$V11 + (V10 - V11) \times 5/16.2$
<b>39H</b>	$V3 + (V1 - V3) \times 28.6/84.5$	$V14 + (V12 - V14) \times 55.9/84.5$	<b>19H</b>	$V5 + (V4 - V5) \times 10.2/16.2$	$V11 + (V10 - V11) \times 6/16.2$
<b>38H</b>	$V3 + (V1 - V3) \times 23.8/84.5$	$V14 + (V12 - V14) \times 60.7/84.5$	<b>18H</b>	$V5 + (V4 - V5) \times 9.2/16.2$	$V11 + (V10 - V11) \times 7/16.2$
<b>37H</b>	$V3 + (V1 - V3) \times 19.8/84.5$	$V14 + (V12 - V14) \times 64.7/84.5$	<b>17H</b>	$V5 + (V4 - V5) \times 8.2/16.2$	$V11 + (V10 - V11) \times 8/16.2$
<b>36H</b>	$V3 + (V1 - V3) \times 16.3/84.5$	$V14 + (V12 - V14) \times 68.2/84.5$	<b>16H</b>	$V5 + (V4 - V5) \times 7.2/16.2$	$V11 + (V10 - V11) \times 9/16.2$
<b>35H</b>	$V3 + (V1 - V3) \times 13.3/84.5$	$V14 + (V12 - V14) \times 71.2/84.5$	<b>15H</b>	$V5 + (V4 - V5) \times 6.2/16.2$	$V11 + (V10 - V11) \times 10/16.2$
<b>34H</b>	$V3 + (V1 - V3) \times 10.6/84.5$	$V14 + (V12 - V14) \times 73.9/84.5$	<b>14H</b>	$V5 + (V4 - V5) \times 5.2/16.2$	$V11 + (V10 - V11) \times 11/16.2$
<b>33H</b>	$V3 + (V1 - V3) \times 8.1/84.5$	$V14 + (V12 - V14) \times 76.4/84.5$	<b>13H</b>	$V5 + (V4 - V5) \times 4.2/16.2$	$V11 + (V10 - V11) \times 12/16.2$
<b>32H</b>	$V3 + (V1 - V3) \times 5.9/84.5$	$V14 + (V12 - V14) \times 78.6/84.5$	<b>12H</b>	$V5 + (V4 - V5) \times 3.2/16.2$	$V11 + (V10 - V11) \times 13/16.2$
<b>31H</b>	$V3 + (V1 - V3) \times 3.8/84.5$	$V14 + (V12 - V14) \times 80.7/84.5$	<b>11H</b>	$V5 + (V4 - V5) \times 2.2/16.2$	$V11 + (V10 - V11) \times 14/16.2$
<b>30H</b>	$V3 + (V1 - V3) \times 1.8/84.5$	$V14 + (V12 - V14) \times 82.7/84.5$	<b>10H</b>	$V5 + (V4 - V5) \times 1.1/16.2$	$V11 + (V10 - V11) \times 15.1/16.2$
<b>2FH</b>	V3	V12	<b>0FH</b>	V5	V10
<b>2EH</b>	$V4 + (V3 - V4) \times 19 / 20.7$	$V12 + (V11 - V12) \times 1.7/20.7$	<b>0EH</b>	$V7 + (V5 - V7) \times 70.2/71.3$	$V10 + (V8 - V10) \times 1.1/71.3$
<b>2DH</b>	$V4 + (V3 - V4) \times 17.4/20.7$	$V12 + (V11 - V12) \times 3.3/20.7$	<b>0DH</b>	$V7 + (V5 - V7) \times 69.1/71.3$	$V10 + (V8 - V10) \times 2.2/71.3$
<b>2CH</b>	$V4 + (V3 - V4) \times 15.9/20.7$	$V12 + (V11 - V12) \times 4.8/20.7$	<b>0CH</b>	$V7 + (V5 - V7) \times 68/71.3$	$V10 + (V8 - V10) \times 3.3/71.3$
<b>2BH</b>	$V4 + (V3 - V4) \times 14.4/20.7$	$V12 + (V11 - V12) \times 6.3/20.7$	<b>0BH</b>	$V7 + (V5 - V7) \times 66.8/71.3$	$V10 + (V8 - V10) \times 4.5/71.3$
<b>2AH</b>	$V4 + (V3 - V4) \times 13/20.7$	$V12 + (V11 - V12) \times 7.7/20.7$	<b>0AH</b>	$V7 + (V5 - V7) \times 65.5/71.3$	$V10 + (V8 - V10) \times 5.8/71.3$
<b>29H</b>	$V4 + (V3 - V4) \times 11.6/20.7$	$V12 + (V11 - V12) \times 9.1/20.7$	<b>09H</b>	$V7 + (V5 - V7) \times 64.2/71.3$	$V10 + (V8 - V10) \times 7.1/71.3$
<b>28H</b>	$V4 + (V3 - V4) \times 10.3/20.7$	$V12 + (V11 - V12) \times 10.4/20.7$	<b>08H</b>	$V7 + (V5 - V7) \times 62.8/71.3$	$V10 + (V8 - V10) \times 8.5/71.3$
<b>27H</b>	$V4 + (V3 - V4) \times 9/20.7$	$V12 + (V11 - V12) \times 11.7/20.7$	<b>07H</b>	$V7 + (V5 - V7) \times 61.2/71.3$	$V10 + (V8 - V10) \times 10.1/71.3$
<b>26H</b>	$V4 + (V3 - V4) \times 7.8/20.7$	$V12 + (V11 - V12) \times 12.9/20.7$	<b>06H</b>	$V7 + (V5 - V7) \times 59.5/71.3$	$V10 + (V8 - V10) \times 11.8/71.3$
<b>25H</b>	$V4 + (V3 - V4) \times 6.6/20.7$	$V12 + (V11 - V12) \times 14.1/20.7$	<b>05H</b>	$V7 + (V5 - V7) \times 57.6/71.3$	$V10 + (V8 - V10) \times 13.7/71.3$
<b>24H</b>	$V4 + (V3 - V4) \times 5.4/20.7$	$V12 + (V11 - V12) \times 15.3/20.7$	<b>04H</b>	$V7 + (V5 - V7) \times 55.4/71.3$	$V10 + (V8 - V10) \times 15.9/71.3$
<b>23H</b>	$V4 + (V3 - V4) \times 4.3/20.7$	$V12 + (V11 - V12) \times 16.4/20.7$	<b>03H</b>	$V7 + (V5 - V7) \times 52.8/71.3$	$V10 + (V8 - V10) \times 18.5/71.3$
<b>22H</b>	$V4 + (V3 - V4) \times 3.2/20.7$	$V12 + (V11 - V12) \times 17.5/20.7$	<b>02H</b>	$V7 + (V5 - V7) \times 49.6/71.3$	$V10 + (V8 - V10) \times 21.7/71.3$
<b>21H</b>	$V4 + (V3 - V4) \times 2.1/20.7$	$V12 + (V11 - V12) \times 18.6/20.7$	<b>01H</b>	$V7 + (V5 - V7) \times 44/71.3$	$V10 + (V8 - V10) \times 27.3/71.3$
<b>20H</b>	$V4 + (V3 - V4) \times 1/20.7$	$V12 + (V11 - V12) \times 19.7/20.7$	<b>00H</b>	V7	V8



REV = L & **NBWB=H** ; **VSET=H**

Data	Positive polarity Output Voltage	Negative polarity Output Voltage	Data	Positive polarity Output Voltage	Negative polarity Output Voltage
00H	V1	V14	20H	V4	V11
01H	V2	V13	21H	$V5 + (V4 - V5) \times 15.2/16.2$	$V11 + (V10 - V11) \times 1/16.2$
02H	$V3 + (V2 - V3) \times 60.1/71.6$	$V13 + (V12 - V13) \times 11.5/71.6$	22H	$V5 + (V4 - V5) \times 14.2/16.2$	$V11 + (V10 - V11) \times 2/16.2$
03H	$V3 + (V2 - V3) \times 50.1/71.6$	$V13 + (V12 - V13) \times 21.5/71.6$	23H	$V5 + (V4 - V5) \times 13.2/16.2$	$V11 + (V10 - V11) \times 3/16.2$
04H	$V3 + (V2 - V3) \times 41.5/71.6$	$V13 + (V12 - V13) \times 30.1/71.6$	24H	$V5 + (V4 - V5) \times 12.2/16.2$	$V11 + (V10 - V11) \times 4/16.2$
05H	$V3 + (V2 - V3) \times 34.3/71.6$	$V13 + (V12 - V13) \times 37.3/71.6$	25H	$V5 + (V4 - V5) \times 11.2/16.2$	$V11 + (V10 - V11) \times 5/16.2$
06H	$V3 + (V2 - V3) \times 28.6/71.6$	$V13 + (V12 - V13) \times 43/71.6$	26H	$V5 + (V4 - V5) \times 10.2/16.2$	$V11 + (V10 - V11) \times 6/16.2$
07H	$V3 + (V2 - V3) \times 23.8/71.6$	$V13 + (V12 - V13) \times 47.8/71.6$	27H	$V5 + (V4 - V5) \times 9.2/16.2$	$V11 + (V10 - V11) \times 7/16.2$
08H	$V3 + (V2 - V3) \times 19.8/71.6$	$V13 + (V12 - V13) \times 51.8/71.6$	28H	$V5 + (V4 - V5) \times 8.2/16.2$	$V11 + (V10 - V11) \times 8/16.2$
09H	$V3 + (V2 - V3) \times 16.3/71.6$	$V13 + (V12 - V13) \times 55.3/71.6$	29H	$V5 + (V4 - V5) \times 7.2/16.2$	$V11 + (V10 - V11) \times 9/16.2$
0AH	$V3 + (V2 - V3) \times 13.3/71.6$	$V13 + (V12 - V13) \times 58.3/71.6$	2AH	$V5 + (V4 - V5) \times 6.2/16.2$	$V11 + (V10 - V11) \times 10/16.2$
0BH	$V3 + (V2 - V3) \times 10.6/71.6$	$V13 + (V12 - V13) \times 61/71.6$	2BH	$V5 + (V4 - V5) \times 5.2/16.2$	$V11 + (V10 - V11) \times 11/16.2$
0CH	$V3 + (V2 - V3) \times 8.1/71.6$	$V13 + (V12 - V13) \times 63.5/71.6$	2CH	$V5 + (V4 - V5) \times 4.2/16.2$	$V11 + (V10 - V11) \times 12/16.2$
0DH	$V3 + (V2 - V3) \times 5.9/71.6$	$V13 + (V12 - V13) \times 65.7/71.6$	2DH	$V5 + (V4 - V5) \times 3.2/16.2$	$V11 + (V10 - V11) \times 13/16.2$
0EH	$V3 + (V2 - V3) \times 3.8/71.6$	$V13 + (V12 - V13) \times 67.8/71.6$	2EH	$V5 + (V4 - V5) \times 2.2/16.2$	$V11 + (V10 - V11) \times 14/16.2$
0FH	$V3 + (V2 - V3) \times 1.8/71.6$	$V13 + (V12 - V13) \times 69.8/71.6$	2FH	$V5 + (V4 - V5) \times 1.1/16.2$	$V11 + (V10 - V11) \times 15.1/16.2$
10H	V3	V12	30H	V5	V10
11H	$V4 + (V3 - V4) \times 19/20.7$	$V12 + (V11 - V12) \times 1.7/20.7$	31H	$V6 + (V5 - V6) \times 26.2/27.3$	$V10 + (V8 - V10) \times 1.1/27.3$
12H	$V4 + (V3 - V4) \times 17.4/20.7$	$V12 + (V11 - V12) \times 3.3/20.7$	32H	$V6 + (V5 - V6) \times 25.1/27.3$	$V10 + (V8 - V10) \times 2.2/27.3$
13H	$V4 + (V3 - V4) \times 15.9/20.7$	$V12 + (V11 - V12) \times 4.8/20.7$	33H	$V6 + (V5 - V6) \times 24/27.3$	$V10 + (V8 - V10) \times 3.3/27.3$
14H	$V4 + (V3 - V4) \times 14.4/20.7$	$V12 + (V11 - V12) \times 6.3/20.7$	34H	$V6 + (V5 - V6) \times 22.8/27.3$	$V10 + (V8 - V10) \times 4.5/27.3$
15H	$V4 + (V3 - V4) \times 13/20.7$	$V12 + (V11 - V12) \times 7.7/20.7$	35H	$V6 + (V5 - V6) \times 21.5/27.3$	$V10 + (V8 - V10) \times 5.8/27.3$
16H	$V4 + (V3 - V4) \times 11.6/20.7$	$V12 + (V11 - V12) \times 9.1/20.7$	36H	$V6 + (V5 - V6) \times 20.2/27.3$	$V10 + (V8 - V10) \times 7.1/27.3$
17H	$V4 + (V3 - V4) \times 10.3/20.7$	$V12 + (V11 - V12) \times 10.4/20.7$	37H	$V6 + (V5 - V6) \times 18.8/27.3$	$V10 + (V8 - V10) \times 8.5/27.3$
18H	$V4 + (V3 - V4) \times 9/20.7$	$V12 + (V11 - V12) \times 11.7/20.7$	38H	$V6 + (V5 - V6) \times 17.2/27.3$	$V10 + (V8 - V10) \times 10.1/27.3$
19H	$V4 + (V3 - V4) \times 7.8/20.7$	$V12 + (V11 - V12) \times 12.9/20.7$	39H	$V6 + (V5 - V6) \times 15.5/27.3$	$V10 + (V8 - V10) \times 11.8/27.3$
1AH	$V4 + (V3 - V4) \times 6.6/20.7$	$V12 + (V11 - V12) \times 14.1/20.7$	3AH	$V6 + (V5 - V6) \times 13.6/27.3$	$V10 + (V8 - V10) \times 13.7/27.3$
+ 1BH	$V4 + (V3 - V4) \times 5.4/20.7$	$V12 + (V11 - V12) \times 15.3/20.7$	3BH	$V6 + (V5 - V6) \times 11.4/27.3$	$V10 + (V8 - V10) \times 15.9/27.3$
1CH	$V4 + (V3 - V4) \times 4.3/20.7$	$V12 + (V11 - V12) \times 16.4/20.7$	3CH	$V6 + (V5 - V6) \times 8.8/27.3$	$V10 + (V8 - V10) \times 18.5/27.3$
1DH	$V4 + (V3 - V4) \times 3.2/20.7$	$V12 + (V11 - V12) \times 17.5/20.7$	3DH	$V6 + (V5 - V6) \times 5.6/27.3$	$V10 + (V8 - V10) \times 21.7/27.3$
1EH	$V4 + (V3 - V4) \times 2.1/20.7$	$V12 + (V11 - V12) \times 18.6/20.7$	3EH	V6	V7
1FH	$V4 + (V3 - V4) \times 1/20.7$	$V12 + (V11 - V12) \times 19.7/20.7$	3FH	V7	V8

REV = L & **NBWB=L** **VSET=H**

Data	Positive polarity Output Voltage	Negative polarity Output Voltage	Data	Positive polarity Output Voltage	Negative polarity Output Voltage
<b>3FH</b>	V1	V14	<b>1FH</b>	V4	V11
<b>3EH</b>	V2	V13	<b>1EH</b>	$V5 + (V4 - V5) \times 15.2/16.2$	$V11 + (V10 - V11) \times 1/16.2$
<b>3DH</b>	$V3 + (V2 - V3) \times 60.1/71.6$	$V13 + (V12 - V13) \times 11.5/71.6$	<b>1DH</b>	$V5 + (V4 - V5) \times 14.2/16.2$	$V11 + (V10 - V11) \times 2/16.2$
<b>3CH</b>	$V3 + (V2 - V3) \times 50.1/71.6$	$V13 + (V12 - V13) \times 21.5/71.6$	<b>1CH</b>	$V5 + (V4 - V5) \times 13.2/16.2$	$V11 + (V10 - V11) \times 3/16.2$
<b>3BH</b>	$V3 + (V2 - V3) \times 41.5/71.6$	$V13 + (V12 - V13) \times 30.1/71.6$	<b>1BH</b>	$V5 + (V4 - V5) \times 12.2/16.2$	$V11 + (V10 - V11) \times 4/16.2$
<b>3AH</b>	$V3 + (V2 - V3) \times 34.3/71.6$	$V13 + (V12 - V13) \times 37.3/71.6$	<b>1AH</b>	$V5 + (V4 - V5) \times 11.2/16.2$	$V11 + (V10 - V11) \times 5/16.2$
<b>39H</b>	$V3 + (V2 - V3) \times 28.6/71.6$	$V13 + (V12 - V13) \times 43/71.6$	<b>19H</b>	$V5 + (V4 - V5) \times 10.2/16.2$	$V11 + (V10 - V11) \times 6/16.2$
<b>38H</b>	$V3 + (V2 - V3) \times 23.8/71.6$	$V13 + (V12 - V13) \times 47.8/71.6$	<b>18H</b>	$V5 + (V4 - V5) \times 9.2/16.2$	$V11 + (V10 - V11) \times 7/16.2$
<b>37H</b>	$V3 + (V2 - V3) \times 19.8/71.6$	$V13 + (V12 - V13) \times 51.8/71.6$	<b>17H</b>	$V5 + (V4 - V5) \times 8.2/16.2$	$V11 + (V10 - V11) \times 8/16.2$
<b>36H</b>	$V3 + (V2 - V3) \times 16.3/71.6$	$V13 + (V12 - V13) \times 55.3/71.6$	<b>16H</b>	$V5 + (V4 - V5) \times 7.2/16.2$	$V11 + (V10 - V11) \times 9/16.2$
<b>35H</b>	$V3 + (V2 - V3) \times 13.3/71.6$	$V13 + (V12 - V13) \times 58.3/71.6$	<b>15H</b>	$V5 + (V4 - V5) \times 6.2/16.2$	$V11 + (V10 - V11) \times 10/16.2$
<b>34H</b>	$V3 + (V2 - V3) \times 10.6/71.6$	$V13 + (V12 - V13) \times 61/71.6$	<b>14H</b>	$V5 + (V4 - V5) \times 5.2/16.2$	$V11 + (V10 - V11) \times 11/16.2$
<b>33H</b>	$V3 + (V2 - V3) \times 8.1/71.6$	$V13 + (V12 - V13) \times 63.5/71.6$	<b>13H</b>	$V5 + (V4 - V5) \times 4.2/16.2$	$V11 + (V10 - V11) \times 12/16.2$
<b>32H</b>	$V3 + (V2 - V3) \times 5.9/71.6$	$V13 + (V12 - V13) \times 65.7/71.6$	<b>12H</b>	$V5 + (V4 - V5) \times 3.2/16.2$	$V11 + (V10 - V11) \times 13/16.2$
<b>31H</b>	$V3 + (V2 - V3) \times 3.8/71.6$	$V13 + (V12 - V13) \times 67.8/71.6$	<b>11H</b>	$V5 + (V4 - V5) \times 2.2/16.2$	$V11 + (V10 - V11) \times 14/16.2$
<b>30H</b>	$V3 + (V2 - V3) \times 1.8/71.6$	$V13 + (V12 - V13) \times 69.8/71.6$	<b>10H</b>	$V5 + (V4 - V5) \times 1.1/16.2$	$V11 + (V10 - V11) \times 15.1/16.2$
<b>2FH</b>	V3	V12	<b>0FH</b>	V5	V10
<b>2EH</b>	$V4 + (V3 - V4) \times 19 / 20.7$	$V12 + (V11 - V12) \times 1.7/20.7$	<b>0EH</b>	$V6 + (V5 - V6) \times 26.2/27.3$	$V10 + (V8 - V10) \times 1.1/27.3$
<b>2DH</b>	$V4 + (V3 - V4) \times 17.4/20.7$	$V12 + (V11 - V12) \times 3.3/20.7$	<b>0DH</b>	$V6 + (V5 - V6) \times 25.1/27.3$	$V10 + (V8 - V10) \times 2.2/27.3$
<b>2CH</b>	$V4 + (V3 - V4) \times 15.9/20.7$	$V12 + (V11 - V12) \times 4.8/20.7$	<b>0CH</b>	$V6 + (V5 - V6) \times 24/27.3$	$V10 + (V8 - V10) \times 3.3/27.3$
<b>2BH</b>	$V4 + (V3 - V4) \times 14.4/20.7$	$V12 + (V11 - V12) \times 6.3/20.7$	<b>0BH</b>	$V6 + (V5 - V6) \times 22.8/27.3$	$V10 + (V8 - V10) \times 4.5/27.3$
<b>2AH</b>	$V4 + (V3 - V4) \times 13/20.7$	$V12 + (V11 - V12) \times 7.7/20.7$	<b>0AH</b>	$V6 + (V5 - V6) \times 21.5/27.3$	$V10 + (V8 - V10) \times 5.8/27.3$
<b>29H</b>	$V4 + (V3 - V4) \times 11.6/20.7$	$V12 + (V11 - V12) \times 9.1/20.7$	<b>09H</b>	$V6 + (V5 - V6) \times 20.2/27.3$	$V10 + (V8 - V10) \times 7.1/27.3$
<b>28H</b>	$V4 + (V3 - V4) \times 10.3/20.7$	$V12 + (V11 - V12) \times 10.4/20.7$	<b>08H</b>	$V6 + (V5 - V6) \times 18.8/27.3$	$V10 + (V8 - V10) \times 8.5/27.3$
<b>27H</b>	$V4 + (V3 - V4) \times 9/20.7$	$V12 + (V11 - V12) \times 11.7/20.7$	<b>07H</b>	$V6 + (V5 - V6) \times 17.2/27.3$	$V10 + (V8 - V10) \times 10.1/27.3$
<b>26H</b>	$V4 + (V3 - V4) \times 7.8/20.7$	$V12 + (V11 - V12) \times 12.9/20.7$	<b>06H</b>	$V6 + (V5 - V6) \times 15.5/27.3$	$V10 + (V8 - V10) \times 11.8/27.3$
<b>25H</b>	$V4 + (V3 - V4) \times 6.6/20.7$	$V12 + (V11 - V12) \times 14.1/20.7$	<b>05H</b>	$V6 + (V5 - V6) \times 13.6/27.3$	$V10 + (V8 - V10) \times 13.7/27.3$
<b>24H</b>	$V4 + (V3 - V4) \times 5.4/20.7$	$V12 + (V11 - V12) \times 15.3/20.7$	<b>04H</b>	$V6 + (V5 - V6) \times 11.4/27.3$	$V10 + (V8 - V10) \times 15.9/27.3$
<b>23H</b>	$V4 + (V3 - V4) \times 4.3/20.7$	$V12 + (V11 - V12) \times 16.4/20.7$	<b>03H</b>	$V6 + (V5 - V6) \times 8.8/27.3$	$V10 + (V8 - V10) \times 18.5/27.3$
<b>22H</b>	$V4 + (V3 - V4) \times 3.2/20.7$	$V12 + (V11 - V12) \times 17.5/20.7$	<b>02H</b>	$V6 + (V5 - V6) \times 5.6/27.3$	$V10 + (V8 - V10) \times 21.7/27.3$
<b>21H</b>	$V4 + (V3 - V4) \times 2.1/20.7$	$V12 + (V11 - V12) \times 18.6/20.7$	<b>01H</b>	V6	V7
<b>20H</b>	$V4 + (V3 - V4) \times 1/20.7$	$V12 + (V11 - V12) \times 19.7/20.7$	<b>00H</b>	V7	V8

## 10. Power ON/OFF Sequence

### 10.1. Normal mode power on/ off

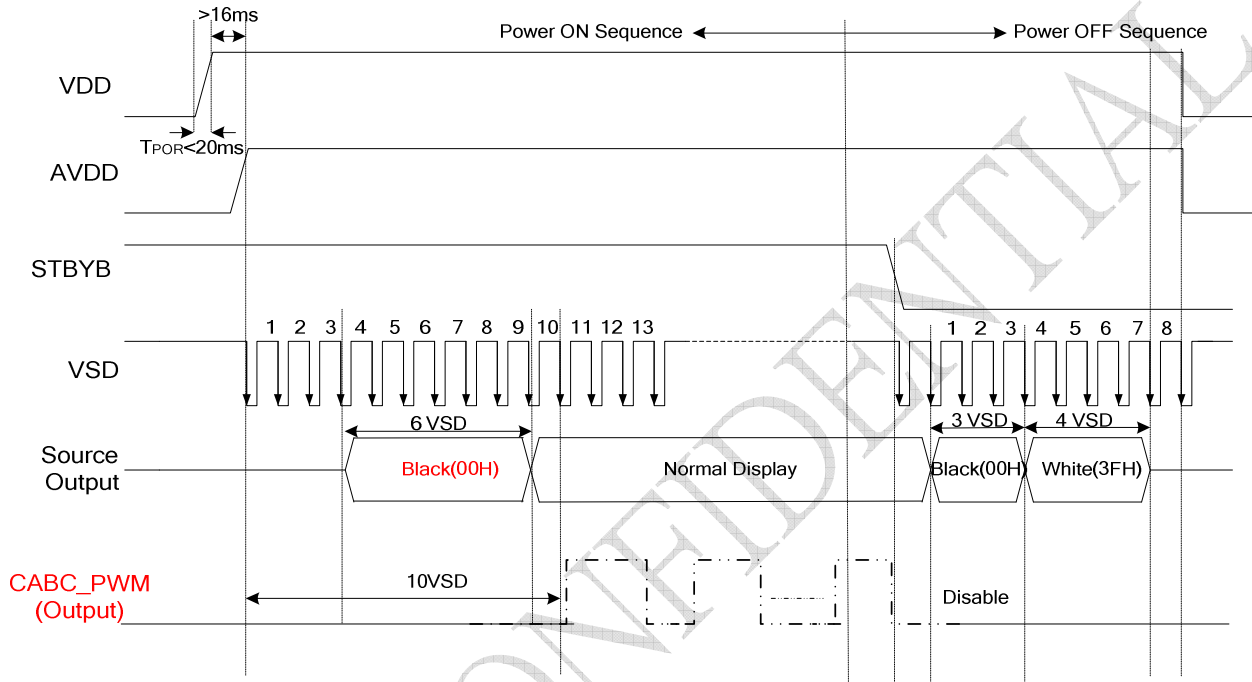
To prevent the device damage from latch up, the power ON/OFF sequence shown below must be followed.

Power ON: VDD, DGND → AVDD, AGND → V1 to V14

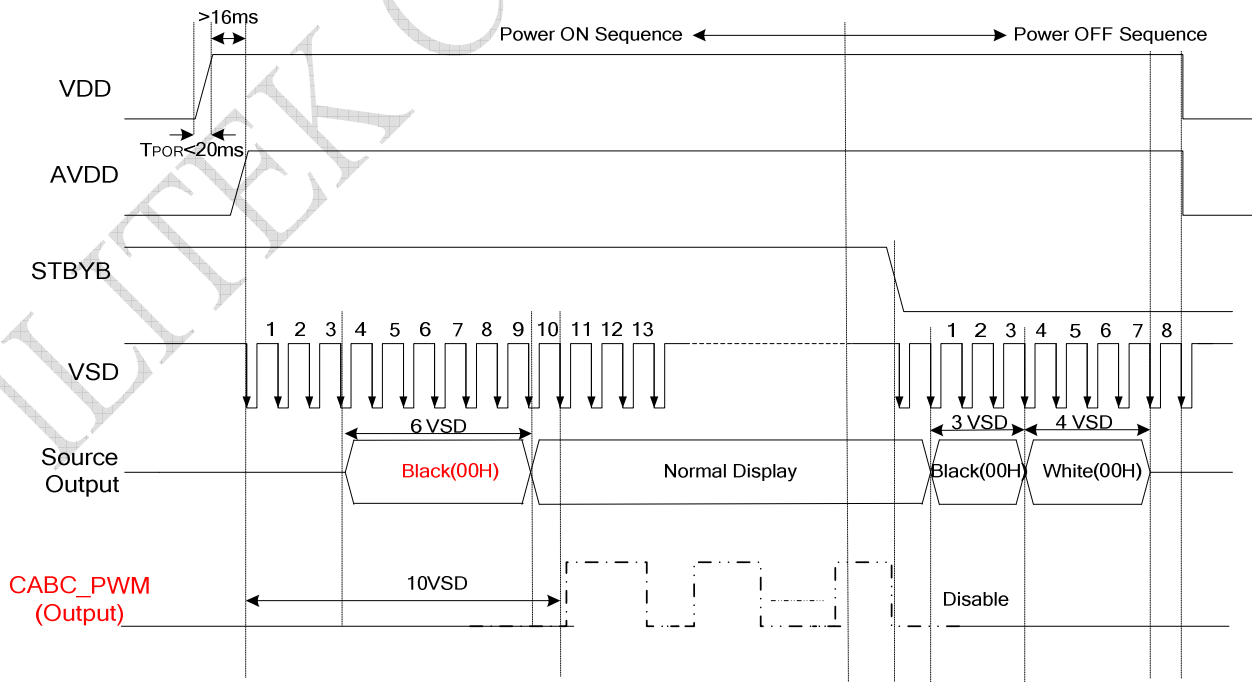
Power OFF: V1 to V14 → AVDD, AGND → VDD, DGND

In order to prevent ILI6126 from power ON reset fail, the rising time ( $t_{POR}$ ) of the digital power supply VDD should be maintained within given specifications. The power ON/OFF timing sequence is illustrated as below:

**REV=L & NBWB=H**



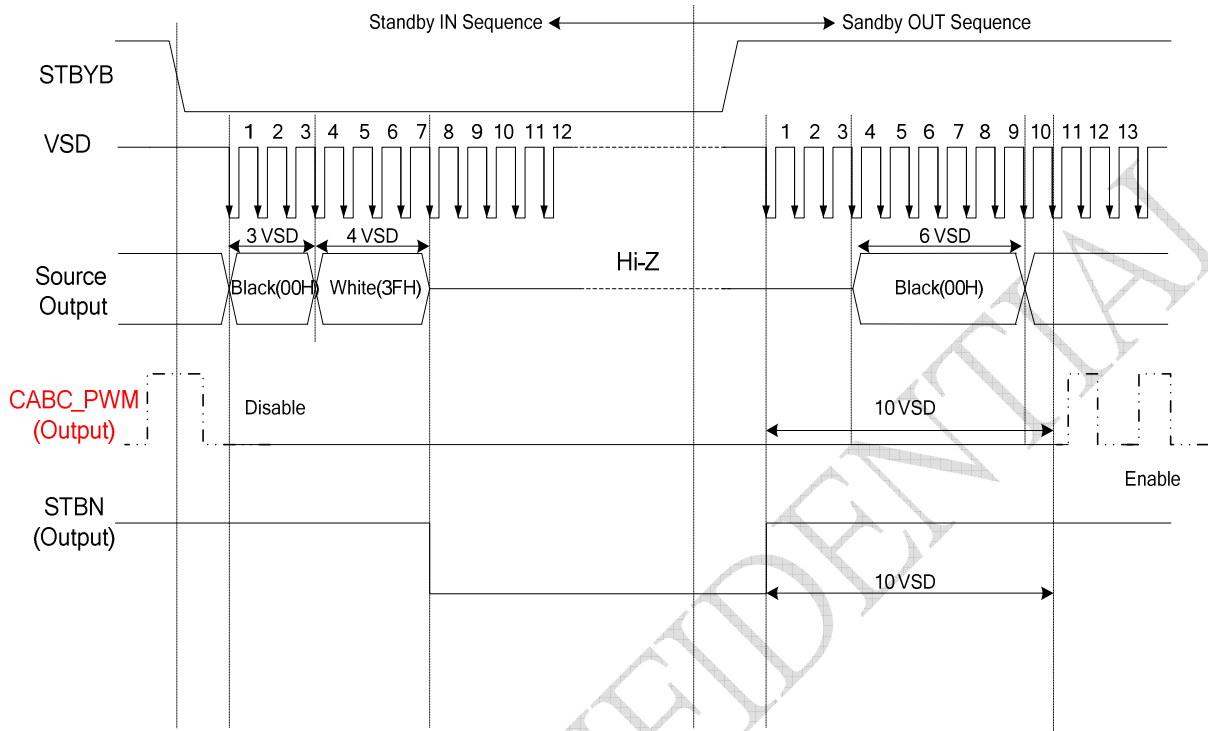
**REV=L & NBWB=L**



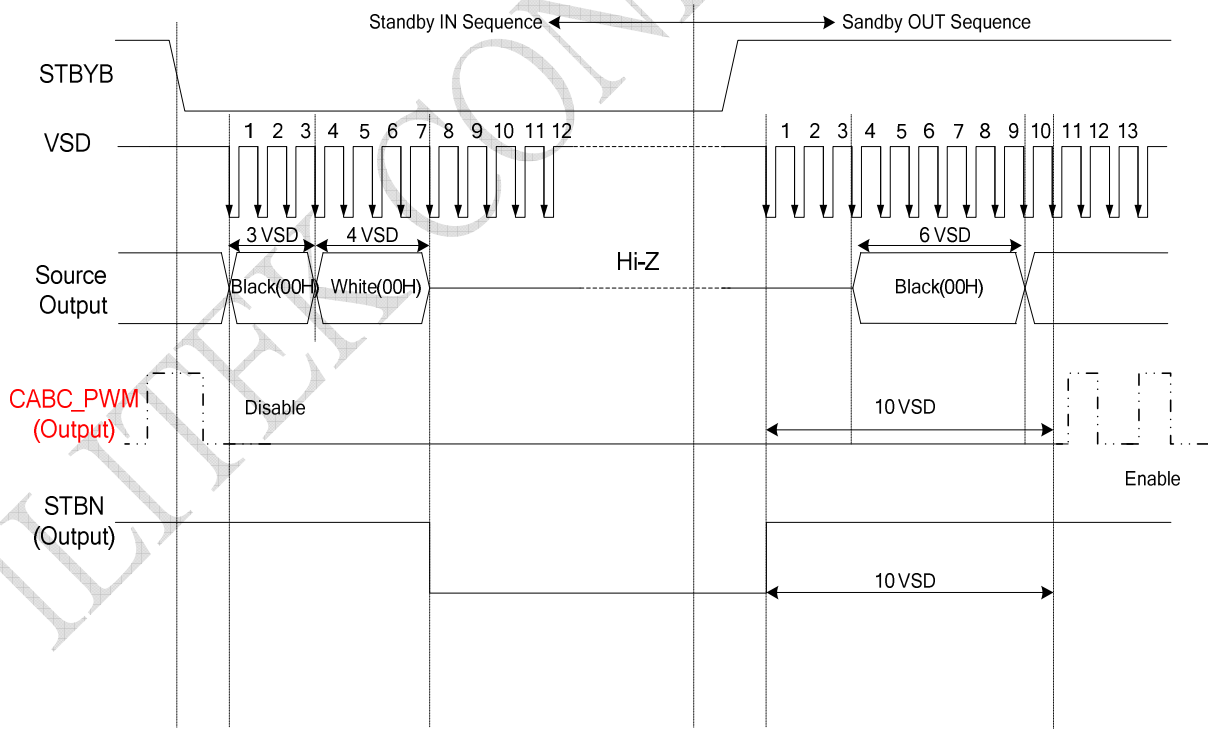
## 10.2. Standby ON/OFF Control

ILI6126 supports Standby mode for saving power consumption, the source driver will turn off and all source output channel will be Hi-Z state when chip in Standby mode. The Standby mode can be controlled via STBYB pin and the Standby ON/OFF timing sequence is illustrated as below:

**REV=L & NBWB=H**




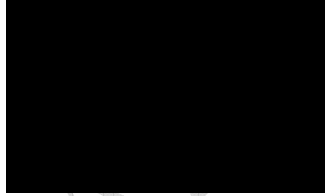

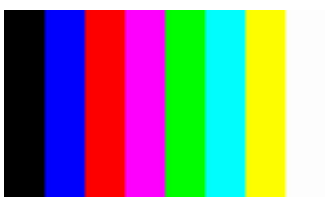








**REV=L & NBWB=L**



## 11. The BIST Patterns for Aging Mode Test

ILI6126 supports the function to generate BIST patterns for Aging mode test automatically. When external BIST pin goes "H" level, then ILI6126 will leave Normal operation mode and starts to generate the BIST patterns to LCD panel without external clock signal, The BIST patterns is illustrated as below:

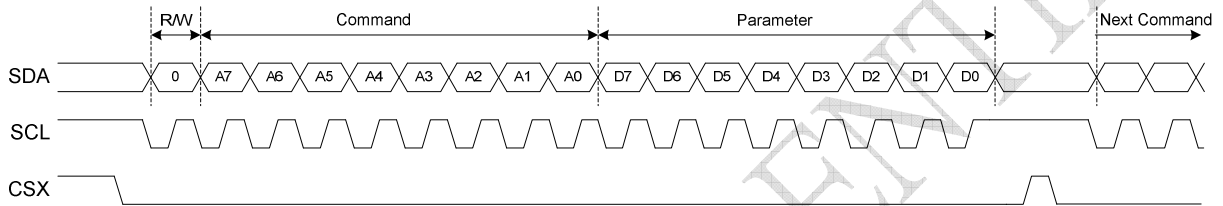
1	2	3	4
Red	Green	Blue	Black
			
5	6	7	8
White	Vertical 8-color stripe	Horizontal 64-gray scale	Vertical 64-gray scale
			
9	10	11	12
Gray with black block	Gray with black dot	Gray with black line	Black with white frame
			

## 12. The Command Format for 3-line Serial Interface

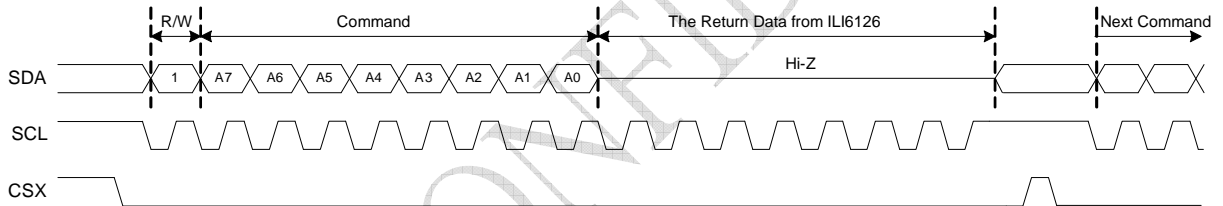
ILI6126 using the 3-line serial port as communication interface for all the commands and parameters of CABC function. This 3-line serial communication can be bi-directional controlled by the “R/W” bit in address field. Under read mode, the 3-line engine in ILI6126 will return the data during “Data phase”. The returned data should be latched at the rising edge of SCL by external controller. Data in the “Hi-Z phase” will be ignored by 3-line engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SDA pin under “Hi-Z phase” and “Data phase”. Each Read/Write operation should be exactly 17 bit. To prevent from incorrect setting of the internal register, any write operation with more or less than 17 bit data during a CSB Low period will be ignored by 3-line engine.

The timing diagram of read/write operation is illustrated as below:

### Write Operation



### Read Operation



## 12.1. BIST & Mute Function

DE Mode:

Mode	BIST	Clock	DE	Function
H (DE)	H	Enable	Enable	BIST Function
	H	OFF	XXX	BIST Function
	H	XXX	OFF	BIST Function
	L	Enable	Enable	Normal Operation
	L	OFF	XXX	Mute Function
	L	XXX	OFF	N.A

SYNC Mode:

Mode	BIST	Clock	VS	HS	Function
L (SYNC)	H	Enable	Enable	Enable	BIST Function
	H	OFF	XXX	XXX	BIST Function
	H	XXX	OFF	XXX	BIST Function
	H	XXX	XXX	OFF	BIST Function
	L	Enable	Enable	Enable	Normal Operation
	L	OFF	XXX	XXX	Mute Function
	L	XXX	OFF	XXX	N.A
	L	XXX	XXX	OFF	N.A

Note:

- A. XXX: Don't Care Input Signal Setting of Enable or Disable status
- B. OFF: Signal Open

## 12.2. Absolute Maximum Rating

Parameter	Symbol	Spec			Unit
		Min.	Typ.	Max.	
Power supply voltage 1	VDD	-0.5	--	+5.0	V
Power supply voltage 2	AVDD	-0.5	--	+15	V
Operation temperature	TOPR	-20	--	+85	°C
Storage temperature	TSTG	-55	--	+125	°C

### \*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposed to absolute maximum rating conditions for extended periods may affect device reliability.

## 12.3. DC Electrical Characteristics

Note: VDD=2.7 ~ 3.6V, AVDD=6.5~13.5V, GND=AGND=0V, Ta=-20~+85°C

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Low level input voltage	Vil	0	-	0.3XVDD	V	For the digital circuit
High level input voltage	Vih	0.7xVDD	-	VDD	V	For the digital circuit
Input leakage current	Ii	-	-	±1	uA	For the digital circuit
High level output voltage	Voh	VDD-0.4	-	-	V	Ioh= -400mA
Low level output voltage	Vol	-	-	GND+0.4	V	Iol= +400mA
Pull low/high resistor	Ri	50K	100K	200K	ohm	For the digital input pin @ VDD=3.3V
Digital Operation current	Idd	-	4	-	mA	Fclk=30 MHz, , FLD=32.65KHz , VDD=2.7V
Digital Stand-by current	Ist1	-	70	-	ua	Clock & all functions are stopped
Analog Operating Current	Idda	-	6	-	mA	No load, Fclk=30MHz, FLD=32.65KHz @ AVDD=13.5V, V1=12.5V, V14=0.1V
Analog Stand-by current	Ist2	-	150	-	ua	No load, clock and all functions are stopped
Input level of V1 ~ V7	Vref1	0.4* AVDD	-	AVDD-1	V	Gamma correction voltage input
Input level of V8 ~ V14	Vref2	0.1	-	0.6* AVDD	V	Gamma correction voltage input
Output Voltage deviation	Vod1	-	± 20	± 35	mV	Vo = AGND+0.1V ~ AGND+0.5V & Vo = AVDD-0.5V ~ AVDD-0.1V
Output Voltage deviation	Vod2	-	± 15	± 20	mV	Vo = AGND+0.5V ~ AVDD-0.5V
Output Voltage offset between Chips	Voc	-	-	± 20	mV	Vo = AGND+0.5V ~ AVDD-0.5V
Dynamic Range of Output	Vdr	0.1	-	AVDD-0.1	V	S1 ~ S1200
Sinking Current of Outputs	IOLy	80	-	-	uA	S1 ~ S1200; Vo=0.1V v.s 1.0V , AVDD=13.5V
Driving Current of Outputs	IOHy	80	-	-	uA	S1 ~ S1200; Vo=13.4V v.s 12.5V , AVDD=13.5V
Resistance of Gamma Table	Rg	0.7*Rn	1.0*Rn	1.3*Rn	ohm	Rn: Internal gamma resistor



## 12.4. AC Electrical Characteristics

Note: VDD=2.7V ~ 3.6V, AVDD=6.5V~13.5V, GND=AGND=0V, Ta=-20~+85℃

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
VDD Power On Slew rate	TPOR	-	-	20	ms	From 0V to 90% VDD
RSTB pulse width	Trst	10	-	-	us	CLKIN = 45MHz
CLKIN cycle time	Tcph	20			ns	
CLKIN pulse duty	Tcwh	40	50	60	%	
VSD setup time	Tvst	8	-	-	ns	
VSD hold time	Tvhd	8	-	-	ns	
HSD setup time	Thst	8	-	-	ns	
HSD hold time	Thhd	8	-	-	ns	
Data set-up time	Tdsu	8	-	-	ns	D0R[7:0], D1G[7:0], D2B[7:0] to CLKIN
Data hold time	Tdhd	8	-	-	ns	D0R[7:0], D1G[7:0], D2B[7:0] to CLKIN
DE setup time	Tesu	8	-	-	ns	
DE hold time	Tehd	8	-	-	ns	
Output stable time	Tsst	-	-	6	us	10% to 90% target voltage. CL=120pF, R=10K ohm

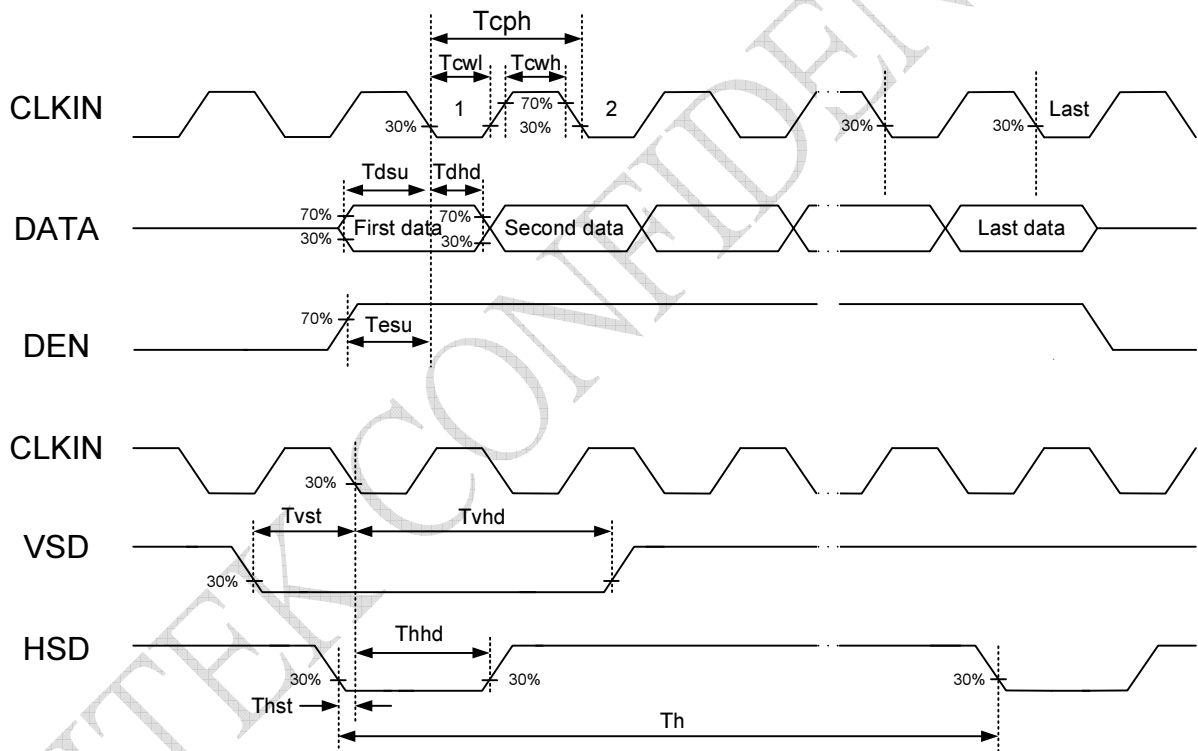
## 13. Timing

### 13.1. Parallel 24-bit RGB Mode

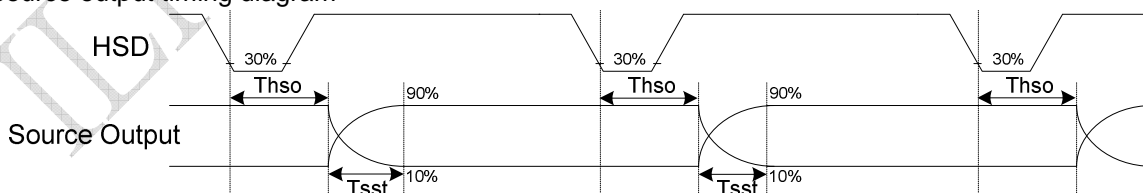
( Note:  $VDD=2.7V \sim 3.6V$ ,  $AVDD=6.5V \sim 13.5V$ ,  $GND=AGND=0V$ ,  $Ta=-20 \sim +85^{\circ}C$  )

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLKIN Frequency	Fclk	-	33	50	MHz	VDD = 2.7V ~3.6V
CLKIN Cycle Time	Tclk	20	30	-	ns	
CLKIN Pulse Duty	Tcwh	40	50	60	%	Tclk
Time from HSD to Source Output	Thso	-	64	-	CLKIN	
Time from HSD to LD	Thld	-	64	-	CLKIN	
Time from HSD to STV	Thstv	-	2	-	CLKIN	
Time from HSD to CKV	Thckv	-	20	-	CLKIN	
Time from HSD to OEV	Thoev	-	4	-	CLKIN	
LD Pulse Width	Twld	-	10	-	CLKIN	
CKV Pulse Width	Twckv	-	66	-	CLKIN	
OEV Pulse Width	Twoev	-	92	-	CLKIN	

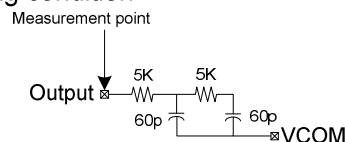
### 13.2. Input Clock and Data Timing Diagram



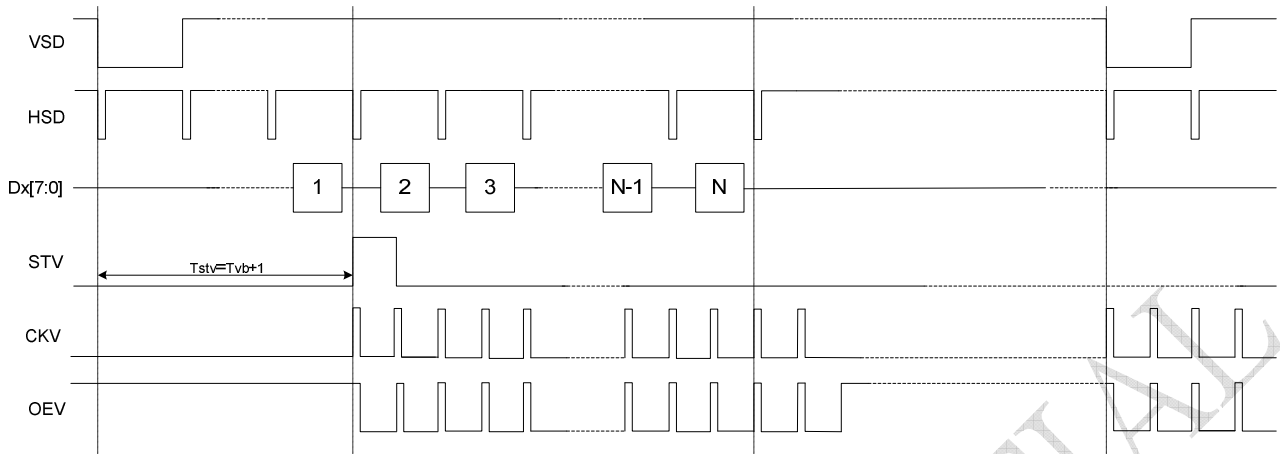
Source output timing diagram



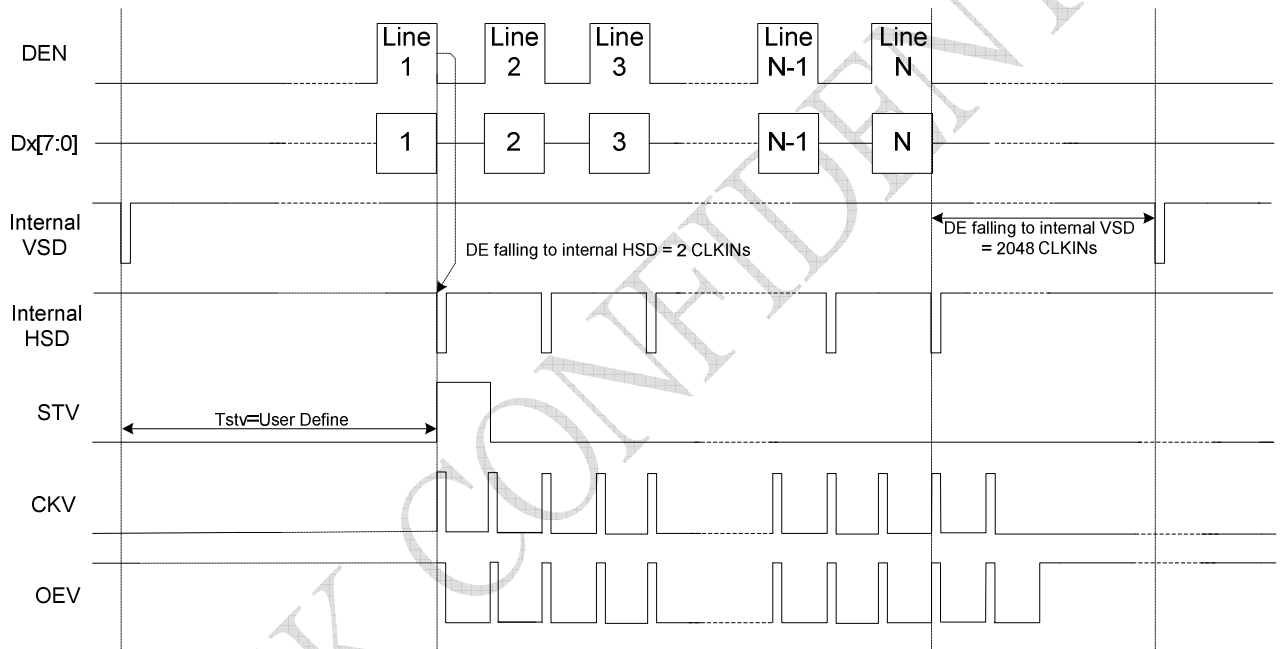
Output Loading condition



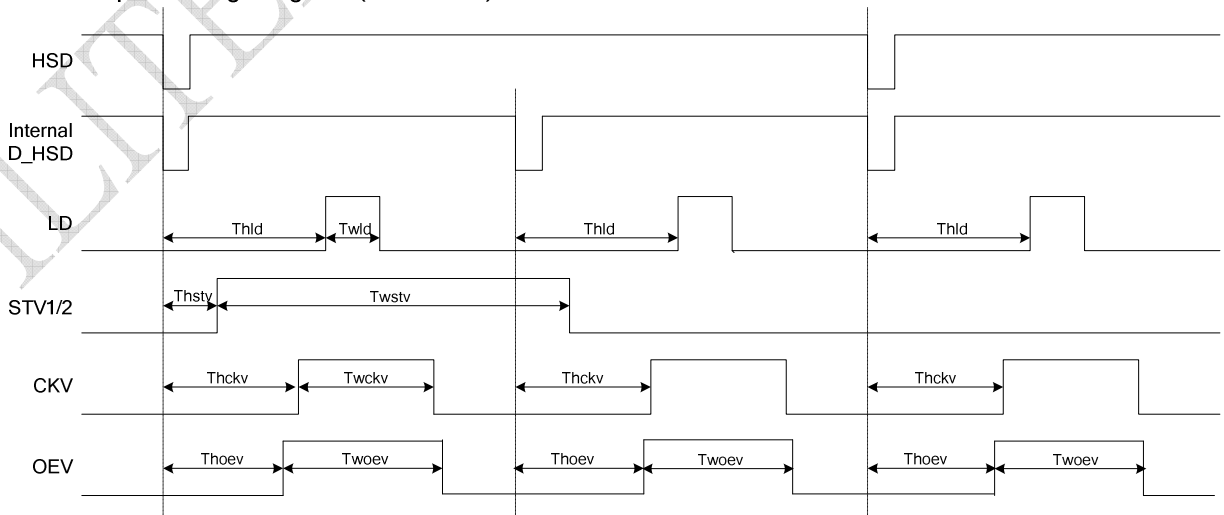
Vertical Timing Diagram of HV Mode (Dual Gate)



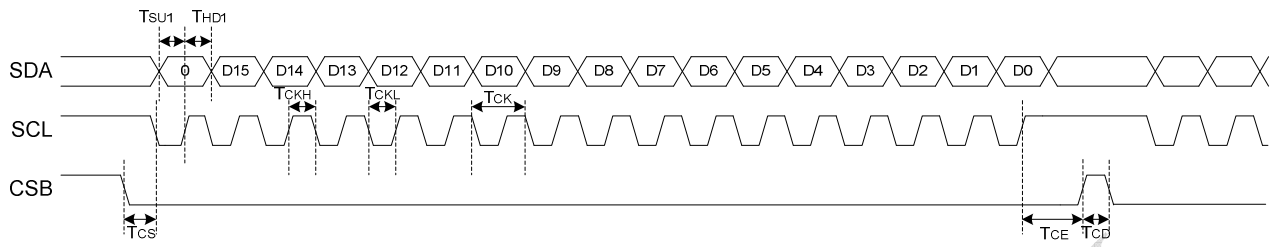
Vertical Timing Diagram of DE Mode (Dual Gate)



Gate Output Timing Diagram (Dual Gate)

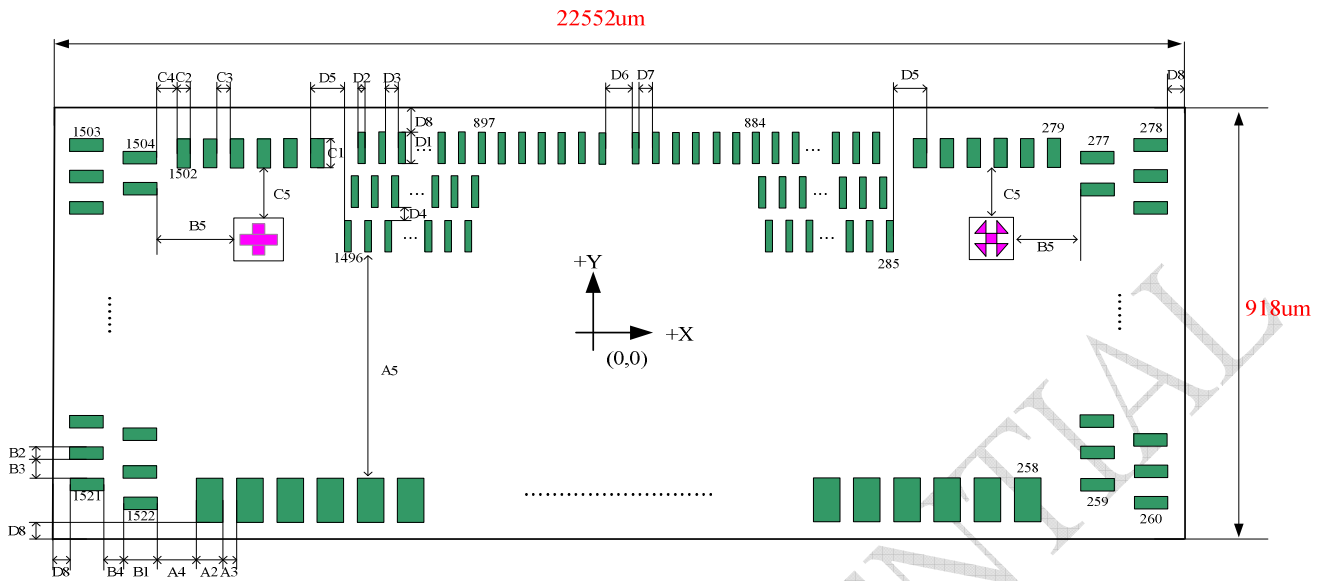


**SPI Timing**



Parameter	Symbol	Spec			Unit	Conditions
		Min.	Typ.	Max.		
SCL period	$T_{CK}$	60	--	--	ns	
SCL high width	$T_{CKH}$	30	--	--	ns	
SCL low width	$T_{CKL}$	30	--	--	ns	
Data setup time	$T_{SU1}$	12	--	--	ns	
Data hold time	$T_{HD1}$	12	--	--	ns	
CSB to SCL setup time	$T_{CS}$	20	--	--	ns	
CSB to SDA hold time	$T_{CE}$	20	--	--	ns	
CSB high pulse width	$T_{CD}$	50	--	--	ns	

### 14. Pad Arrangement and Coordination



Symbol	Size	Symbol	Size	Symbol	Size	Symbol	Size	Symbol	Size
A1	110	B1	100	C1	70	D1	110	D6	450
A2	65	B2	30	C2	30	D2	17	D7	17
A3	20	B3	50	C3	20	D3	34	D8	47
A4	44	B4	30	C4	70	D4	30	Unit:um	
A5	324	B5	168.5	C5	191.5	D5	50		

number	pad name	x	y	number	pad name	x	y	number	pad name	x	y
1	SHIELDING[84]	-10922.5	-357	61	BIST	-5822.5	-357	121	D2B[5]	-722.5	-357
2	SHIELDING[85]	-10837.5	-357	62	SHIELDING[19]	-5737.5	-357	122	D2B[5]	-637.5	-357
3	SHIELDING[1]	-10752.5	-357	63	AVDD	-5652.5	-357	123	D2B[4]	-552.5	-357
4	COM1_B	-10667.5	-357	64	AVDD	-5567.5	-357	124	D2B[4]	-467.5	-357
5	COM1_B	-10582.5	-357	65	AVDD	-5482.5	-357	125	DASHD[7]	-382.5	-357
6	AGND	-10497.5	-357	66	AVDD	-5397.5	-357	126	D2B[3]	-297.5	-357
7	AGND	-10412.5	-357	67	SHIELDING[20]	-5312.5	-357	127	D2B[3]	-212.5	-357
8	AGND	-10327.5	-357	68	AGND	-5227.5	-357	128	D2B[2]	-127.5	-357
9	AGND	-10242.5	-357	69	AGND	-5142.5	-357	129	D2B[2]	-42.5	-357
10	TP[0]	-10157.5	-357	70	AGND	-5057.5	-357	130	DASHD[8]	42.5	-357
11	SHIELDING[2]	-10072.5	-357	71	AGND	-4972.5	-357	131	D2B[1]	127.5	-357
12	V1R	-9987.5	-357	72	SHIELDING[21]	-4887.5	-357	132	D2B[1]	212.5	-357
13	V1R	-9902.5	-357	73	GND	-4802.5	-357	133	D2B[0]	297.5	-357
14	SHIELDING[3]	-9817.5	-357	74	GND	-4717.5	-357	134	D2B[0]	382.5	-357
15	V2R	-9732.5	-357	75	GND	-4632.5	-357	135	DASHD[9]	467.5	-357
16	V2R	-9647.5	-357	76	GND	-4547.5	-357	136	D1G[7]	552.5	-357
17	SHIELDING[4]	-9562.5	-357	77	SHIELDING[22]	-4462.5	-357	137	D1G[7]	637.5	-357
18	V3R	-9477.5	-357	78	CABC_PWM	-4377.5	-357	138	D1G[6]	722.5	-357
19	V3R	-9392.5	-357	79	CABC_PWM	-4292.5	-357	139	D1G[6]	807.5	-357
20	SHIELDING[5]	-9307.5	-357	80	SHIELDING[23]	-4207.5	-357	140	DASHD[10]	892.5	-357
21	V4R	-9222.5	-357	81	VDD	-4122.5	-357	141	D1G[5]	977.5	-357
22	V4R	-9137.5	-357	82	VDD	-4037.5	-357	142	D1G[5]	1062.5	-357
23	SHIELDING[6]	-9052.5	-357	83	VDD	-3952.5	-357	143	D1G[4]	1147.5	-357
24	V5R	-8967.5	-357	84	VDD	-3867.5	-357	144	D1G[4]	1232.5	-357
25	V5R	-8882.5	-357	85	SHIELDING[28]	-3782.5	-357	145	DASHD[11]	1317.5	-357
26	SHIELDING[7]	-8797.5	-357	86	DBGATE	-3697.5	-357	146	D1G[3]	1402.5	-357
27	V6R	-8712.5	-357	87	DBGATE	-3612.5	-357	147	D1G[3]	1487.5	-357
28	V6R	-8627.5	-357	88	CSX	-3527.5	-357	148	D1G[2]	1572.5	-357
29	SHIELDING[8]	-8542.5	-357	89	NBWB	-3442.5	-357	149	D1G[2]	1657.5	-357
30	V7R	-8457.5	-357	90	NBWB	-3357.5	-357	150	DASHD[12]	1742.5	-357
31	V7R	-8372.5	-357	91	SCL	-3272.5	-357	151	D1G[1]	1827.5	-357
32	SHIELDING[9]	-8287.5	-357	92	SEL[0]	-3187.5	-357	152	D1G[1]	1912.5	-357
33	V8R	-8202.5	-357	93	SEL[1]	-3102.5	-357	153	D1G[0]	1997.5	-357
34	V8R	-8117.5	-357	94	SDA	-3017.5	-357	154	D1G[0]	2082.5	-357
35	SHIELDING[10]	-8032.5	-357	95	RES[0]	-2932.5	-357	155	DASHD[13]	2167.5	-357
36	V9R	-7947.5	-357	96	RES[0]	-2847.5	-357	156	D0R[7]	2252.5	-357
37	V9R	-7862.5	-357	97	CABC_EN[0]	-2762.5	-357	157	D0R[7]	2337.5	-357
38	SHIELDING[11]	-7777.5	-357	98	CABC_EN[1]	-2677.5	-357	158	D0R[6]	2422.5	-357
39	V10R	-7692.5	-357	99	RES[1]	-2592.5	-357	159	D0R[6]	2507.5	-357
40	V10R	-7607.5	-357	100	RES[1]	-2507.5	-357	160	DASHD[14]	2592.5	-357
41	SHIELDING[12]	-7522.5	-357	101	CFSEL	-2422.5	-357	161	D0R[5]	2677.5	-357
42	V11R	-7437.5	-357	102	CFSEL	-2337.5	-357	162	D0R[5]	2762.5	-357
43	V11R	-7352.5	-357	103	DASHD[1]	-2252.5	-357	163	D0R[4]	2847.5	-357
44	SHIELDING[13]	-7267.5	-357	104	VSD	-2167.5	-357	164	D0R[4]	2932.5	-357
45	V12R	-7182.5	-357	105	VSD	-2082.5	-357	165	DASHD[15]	3017.5	-357
46	V12R	-7097.5	-357	106	DASHD[2]	-1997.5	-357	166	D0R[3]	3102.5	-357
47	SHIELDING[14]	-7012.5	-357	107	HSD	-1912.5	-357	167	D0R[3]	3187.5	-357
48	V13R	-6927.5	-357	108	HSD	-1827.5	-357	168	D0R[2]	3272.5	-357
49	V13R	-6842.5	-357	109	DASHD[3]	-1742.5	-357	169	D0R[2]	3357.5	-357
50	SHIELDING[15]	-6757.5	-357	110	DEN	-1657.5	-357	170	DASHD[16]	3442.5	-357
51	V14R	-6672.5	-357	111	DEN	-1572.5	-357	171	D0R[1]	3527.5	-357
52	V14R	-6587.5	-357	112	DASHD[4]	-1487.5	-357	172	D0R[1]	3612.5	-357
53	SHIELDING[16]	-6502.5	-357	113	CLKIN	-1402.5	-357	173	D0R[0]	3697.5	-357
54	TP[1]	-6417.5	-357	114	CLKIN	-1317.5	-357	174	D0R[0]	3782.5	-357
55	TP[2]	-6332.5	-357	115	DASHD[5]	-1232.5	-357	175	DASHD[17]	3867.5	-357
56	TP[3]	-6247.5	-357	116	D2B[7]	-1147.5	-357	176	SHIELDING[25]	3952.5	-357
57	SHIELDING[17]	-6162.5	-357	117	D2B[7]	-1062.5	-357	177	MODE	4037.5	-357
58	SHIELDING[18]	-6077.5	-357	118	D2B[6]	-977.5	-357	178	MODE	4122.5	-357
59	REV	-5992.5	-357	119	D2B[6]	-892.5	-357	179	CLKPOL	4207.5	-357
60	BIST	-5907.5	-357	120	DASHD[6]	-807.5	-357	180	CLKPOL	4292.5	-357

number	pad name	x	y	number	Pad name	X	y	number	Pad name	x	y
181	SHIELDING[26]	4377.5	-357	241	V3L	9477.5	-357	301	S[17]	10348.5	217
182	DITHB	4462.5	-357	242	SHIELDING[42]	9562.5	-357	302	S[18]	10331.5	357
183	DITHB	4547.5	-357	243	V2L	9647.5	-357	303	S[19]	10314.5	77
184	VSET	4632.5	-357	244	V2L	9732.5	-357	304	S[20]	10297.5	217
185	SHLR	4717.5	-357	245	SHIELDING[43]	9817.5	-357	305	S[21]	10280.5	357
186	SHLR	4802.5	-357	246	V1L	9902.5	-357	306	S[22]	10263.5	77
187	SHIELDING[27]	4887.5	-357	247	V1L	9987.5	-357	307	S[23]	10246.5	217
188	UPDN	4972.5	-357	248	SHIELDING[44]	10072.5	-357	308	S[24]	10229.5	357
189	UPDN	5057.5	-357	249	AVDD	10157.5	-357	309	S[25]	10212.5	77
190	TP[4]	5142.5	-357	250	AVDD	10242.5	-357	310	S[26]	10195.5	217
191	STBYB	5227.5	-357	251	AVDD	10327.5	-357	311	S[27]	10178.5	357
192	STBYB	5312.5	-357	252	AVDD	10412.5	-357	312	S[28]	10161.5	77
193	TP[5]	5397.5	-357	253	SHIELDING[45]	10497.5	-357	313	S[29]	10144.5	217
194	RSTB	5482.5	-357	254	COM2_B	10582.5	-357	314	S[30]	10127.5	357
195	RSTB	5567.5	-357	255	COM2_B	10667.5	-357	315	S[31]	10110.5	77
196	SHIELDING[29]	5652.5	-357	256	SHIELDING[46]	10752.5	-357	316	S[32]	10093.5	217
197	VDD	5737.5	-357	257	SHIELDING[47]	10837.5	-357	317	S[33]	10076.5	357
198	VDD	5822.5	-357	258	SHIELDING[48]	10922.5	-357	318	S[34]	10059.5	77
199	VDD	5907.5	-357	259	TP[6]	11049	-363	319	S[35]	10042.5	217
200	VDD	5992.5	-357	260	TP[7]	11179	-323	320	S[36]	10025.5	357
201	GMA_EN	6077.5	-357	261	SHIELDING[49]	11049	-283	321	S[37]	10008.5	77
202	GND	6162.5	-357	262	STBN_L	11179	-243	322	S[38]	9991.5	217
203	GND	6247.5	-357	263	SHIELDING[50]	11049	-203	323	S[39]	9974.5	357
204	GND	6332.5	-357	264	TP[8]	11179	-163	324	S[40]	9957.5	77
205	GND	6417.5	-357	265	SHIELDING[51]	11049	-123	325	S[41]	9940.5	217
206	SHIELDING[30]	6502.5	-357	266	STV1_L	11179	-83	326	S[42]	9923.5	357
207	V14L	6587.5	-357	267	SHIELDING[52]	11049	-43	327	S[43]	9906.5	77
208	V14L	6672.5	-357	268	STV2_L	11179	-3	328	S[44]	9889.5	217
209	SHIELDING[31]	6757.5	-357	269	SHIELDING[53]	11049	37	329	S[45]	9872.5	357
210	V13L	6842.5	-357	270	STV1_L	11179	77	330	S[46]	9855.5	77
211	V13L	6927.5	-357	271	SHIELDING[54]	11049	117	331	S[47]	9838.5	217
212	SHIELDING[32]	7012.5	-357	272	CKV_L	11179	157	332	S[48]	9821.5	357
213	V12L	7097.5	-357	273	SHIELDING[55]	11049	197	333	S[49]	9804.5	77
214	V12L	7182.5	-357	274	UD_L	11179	237	334	S[50]	9787.5	217
215	SHIELDING[33]	7267.5	-357	275	SHIELDING[56]	11049	277	335	S[51]	9770.5	357
216	V11L	7352.5	-357	276	OEV_L	11179	317	336	S[52]	9753.5	77
217	V11L	7437.5	-357	277	SHIELDING[57]	11049	357	337	S[53]	9736.5	217
218	SHIELDING[34]	7522.5	-357	278	F_CTRL_L	11179	397	338	S[54]	9719.5	357
219	V10L	7607.5	-357	279	XON_L	10914	377	339	S[55]	9702.5	77
220	V10L	7692.5	-357	280	XON_L	10864	377	340	S[56]	9685.5	217
221	SHIELDING[35]	7777.5	-357	281	SHIELDING[58]	10814	377	341	S[57]	9668.5	357
222	V9L	7862.5	-357	282	COM2_T	10764	377	342	S[58]	9651.5	77
223	V9L	7947.5	-357	283	COM2_T	10714	377	343	S[59]	9634.5	217
224	SHIELDING[36]	8032.5	-357	284	SHIELDING[59]	10664	377	344	S[60]	9617.5	357
225	V8L	8117.5	-357	285	S[1]	10620.5	77	345	S[61]	9600.5	77
226	V8L	8202.5	-357	286	S[2]	10603.5	217	346	S[62]	9583.5	217
227	SHIELDING[37]	8287.5	-357	287	S[3]	10586.5	357	347	S[63]	9566.5	357
228	V7L	8372.5	-357	288	S[4]	10569.5	77	348	S[64]	9549.5	77
229	V7L	8457.5	-357	289	S[5]	10552.5	217	349	S[65]	9532.5	217
230	SHIELDING[38]	8542.5	-357	290	S[6]	10535.5	357	350	S[66]	9515.5	357
231	V6L	8627.5	-357	291	S[7]	10518.5	77	351	S[67]	9498.5	77
232	V6L	8712.5	-357	292	S[8]	10501.5	217	352	S[68]	9481.5	217
233	SHIELDING[39]	8797.5	-357	293	S[9]	10484.5	357	353	S[69]	9464.5	357
234	V5L	8882.5	-357	294	S[10]	10467.5	77	354	S[70]	9447.5	77
235	V5L	8967.5	-357	295	S[11]	10450.5	217	355	S[71]	9430.5	217
236	SHIELDING[40]	9052.5	-357	296	S[12]	10433.5	357	356	S[72]	9413.5	357
237	V4L	9137.5	-357	297	S[13]	10416.5	77	357	S[73]	9396.5	77
238	V4L	9222.5	-357	298	S[14]	10399.5	217	358	S[74]	9379.5	217
239	SHIELDING[41]	9307.5	-357	299	S[15]	10382.5	357	359	S[75]	9362.5	357
240	V3L	9392.5	-357	300	S[16]	10365.5	77	360	S[76]	9345.5	77



number	pad name	x	y	number	pad name	x	y	number	pad name	x	y
361	S[77]	9328.5	217	421	S[137]	8308.5	217	481	S[197]	7288.5	217
362	S[78]	9311.5	357	422	S[138]	8291.5	357	482	S[198]	7271.5	357
363	S[79]	9294.5	77	423	S[139]	8274.5	77	483	S[199]	7254.5	77
364	S[80]	9277.5	217	424	S[140]	8257.5	217	484	S[200]	7237.5	217
365	S[81]	9260.5	357	425	S[141]	8240.5	357	485	S[201]	7220.5	357
366	S[82]	9243.5	77	426	S[142]	8223.5	77	486	S[202]	7203.5	77
367	S[83]	9226.5	217	427	S[143]	8206.5	217	487	S[203]	7186.5	217
368	S[84]	9209.5	357	428	S[144]	8189.5	357	488	S[204]	7169.5	357
369	S[85]	9192.5	77	429	S[145]	8172.5	77	489	S[205]	7152.5	77
370	S[86]	9175.5	217	430	S[146]	8155.5	217	490	S[206]	7135.5	217
371	S[87]	9158.5	357	431	S[147]	8138.5	357	491	S[207]	7118.5	357
372	S[88]	9141.5	77	432	S[148]	8121.5	77	492	S[208]	7101.5	77
373	S[89]	9124.5	217	433	S[149]	8104.5	217	493	S[209]	7084.5	217
374	S[90]	9107.5	357	434	S[150]	8087.5	357	494	S[210]	7067.5	357
375	S[91]	9090.5	77	435	S[151]	8070.5	77	495	S[211]	7050.5	77
376	S[92]	9073.5	217	436	S[152]	8053.5	217	496	S[212]	7033.5	217
377	S[93]	9056.5	357	437	S[153]	8036.5	357	497	S[213]	7016.5	357
378	S[94]	9039.5	77	438	S[154]	8019.5	77	498	S[214]	6999.5	77
379	S[95]	9022.5	217	439	S[155]	8002.5	217	499	S[215]	6982.5	217
380	S[96]	9005.5	357	440	S[156]	7985.5	357	500	S[216]	6965.5	357
381	S[97]	8988.5	77	441	S[157]	7968.5	77	501	S[217]	6948.5	77
382	S[98]	8971.5	217	442	S[158]	7951.5	217	502	S[218]	6931.5	217
383	S[99]	8954.5	357	443	S[159]	7934.5	357	503	S[219]	6914.5	357
384	S[100]	8937.5	77	444	S[160]	7917.5	77	504	S[220]	6897.5	77
385	S[101]	8920.5	217	445	S[161]	7900.5	217	505	S[221]	6880.5	217
386	S[102]	8903.5	357	446	S[162]	7883.5	357	506	S[222]	6863.5	357
387	S[103]	8886.5	77	447	S[163]	7866.5	77	507	S[223]	6846.5	77
388	S[104]	8869.5	217	448	S[164]	7849.5	217	508	S[224]	6829.5	217
389	S[105]	8852.5	357	449	S[165]	7832.5	357	509	S[225]	6812.5	357
390	S[106]	8835.5	77	450	S[166]	7815.5	77	510	S[226]	6795.5	77
391	S[107]	8818.5	217	451	S[167]	7798.5	217	511	S[227]	6778.5	217
392	S[108]	8801.5	357	452	S[168]	7781.5	357	512	S[228]	6761.5	357
393	S[109]	8784.5	77	453	S[169]	7764.5	77	513	S[229]	6744.5	77
394	S[110]	8767.5	217	454	S[170]	7747.5	217	514	S[230]	6727.5	217
395	S[111]	8750.5	357	455	S[171]	7730.5	357	515	S[231]	6710.5	357
396	S[112]	8733.5	77	456	S[172]	7713.5	77	516	S[232]	6693.5	77
397	S[113]	8716.5	217	457	S[173]	7696.5	217	517	S[233]	6676.5	217
398	S[114]	8699.5	357	458	S[174]	7679.5	357	518	S[234]	6659.5	357
399	S[115]	8682.5	77	459	S[175]	7662.5	77	519	S[235]	6642.5	77
400	S[116]	8665.5	217	460	S[176]	7645.5	217	520	S[236]	6625.5	217
401	S[117]	8648.5	357	461	S[177]	7628.5	357	521	S[237]	6608.5	357
402	S[118]	8631.5	77	462	S[178]	7611.5	77	522	S[238]	6591.5	77
403	S[119]	8614.5	217	463	S[179]	7594.5	217	523	S[239]	6574.5	217
404	S[120]	8597.5	357	464	S[180]	7577.5	357	524	S[240]	6557.5	357
405	S[121]	8580.5	77	465	S[181]	7560.5	77	525	S[241]	6540.5	77
406	S[122]	8563.5	217	466	S[182]	7543.5	217	526	S[242]	6523.5	217
407	S[123]	8546.5	357	467	S[183]	7526.5	357	527	S[243]	6506.5	357
408	S[124]	8529.5	77	468	S[184]	7509.5	77	528	S[244]	6489.5	77
409	S[125]	8512.5	217	469	S[185]	7492.5	217	529	S[245]	6472.5	217
410	S[126]	8495.5	357	470	S[186]	7475.5	357	530	S[246]	6455.5	357
411	S[127]	8478.5	77	471	S[187]	7458.5	77	531	S[247]	6438.5	77
412	S[128]	8461.5	217	472	S[188]	7441.5	217	532	S[248]	6421.5	217
413	S[129]	8444.5	357	473	S[189]	7424.5	357	533	S[249]	6404.5	357
414	S[130]	8427.5	77	474	S[190]	7407.5	77	534	S[250]	6387.5	77
415	S[131]	8410.5	217	475	S[191]	7390.5	217	535	S[251]	6370.5	217
416	S[132]	8393.5	357	476	S[192]	7373.5	357	536	S[252]	6353.5	357
417	S[133]	8376.5	77	477	S[193]	7356.5	77	537	S[253]	6336.5	77
418	S[134]	8359.5	217	478	S[194]	7339.5	217	538	S[254]	6319.5	217
419	S[135]	8342.5	357	479	S[195]	7322.5	357	539	S[255]	6302.5	357
420	S[136]	8325.5	77	480	S[196]	7305.5	77	540	S[256]	6285.5	77



number	pad name	x	y	number	pad name	x	y	number	pad name	x	y
541	S[257]	6268.5	217	601	S[317]	5248.5	217	661	S[377]	4228.5	217
542	S[258]	6251.5	357	602	S[318]	5231.5	357	662	S[378]	4211.5	357
543	S[259]	6234.5	77	603	S[319]	5214.5	77	663	S[379]	4194.5	77
544	S[260]	6217.5	217	604	S[320]	5197.5	217	664	S[380]	4177.5	217
545	S[261]	6200.5	357	605	S[321]	5180.5	357	665	S[381]	4160.5	357
546	S[262]	6183.5	77	606	S[322]	5163.5	77	666	S[382]	4143.5	77
547	S[263]	6166.5	217	607	S[323]	5146.5	217	667	S[383]	4126.5	217
548	S[264]	6149.5	357	608	S[324]	5129.5	357	668	S[384]	4109.5	357
549	S[265]	6132.5	77	609	S[325]	5112.5	77	669	S[385]	4092.5	77
550	S[266]	6115.5	217	610	S[326]	5095.5	217	670	S[386]	4075.5	217
551	S[267]	6098.5	357	611	S[327]	5078.5	357	671	S[387]	4058.5	357
552	S[268]	6081.5	77	612	S[328]	5061.5	77	672	S[388]	4041.5	77
553	S[269]	6064.5	217	613	S[329]	5044.5	217	673	S[389]	4024.5	217
554	S[270]	6047.5	357	614	S[330]	5027.5	357	674	S[390]	4007.5	357
555	S[271]	6030.5	77	615	S[331]	5010.5	77	675	S[391]	3990.5	77
556	S[272]	6013.5	217	616	S[332]	4993.5	217	676	S[392]	3973.5	217
557	S[273]	5996.5	357	617	S[333]	4976.5	357	677	S[393]	3956.5	357
558	S[274]	5979.5	77	618	S[334]	4959.5	77	678	S[394]	3939.5	77
559	S[275]	5962.5	217	619	S[335]	4942.5	217	679	S[395]	3922.5	217
560	S[276]	5945.5	357	620	S[336]	4925.5	357	680	S[396]	3905.5	357
561	S[277]	5928.5	77	621	S[337]	4908.5	77	681	S[397]	3888.5	77
562	S[278]	5911.5	217	622	S[338]	4891.5	217	682	S[398]	3871.5	217
563	S[279]	5894.5	357	623	S[339]	4874.5	357	683	S[399]	3854.5	357
564	S[280]	5877.5	77	624	S[340]	4857.5	77	684	S[400]	3837.5	77
565	S[281]	5860.5	217	625	S[341]	4840.5	217	685	S[401]	3820.5	217
566	S[282]	5843.5	357	626	S[342]	4823.5	357	686	S[402]	3803.5	357
567	S[283]	5826.5	77	627	S[343]	4806.5	77	687	S[403]	3786.5	77
568	S[284]	5809.5	217	628	S[344]	4789.5	217	688	S[404]	3769.5	217
569	S[285]	5792.5	357	629	S[345]	4772.5	357	689	S[405]	3752.5	357
570	S[286]	5775.5	77	630	S[346]	4755.5	77	690	S[406]	3735.5	77
571	S[287]	5758.5	217	631	S[347]	4738.5	217	691	S[407]	3718.5	217
572	S[288]	5741.5	357	632	S[348]	4721.5	357	692	S[408]	3701.5	357
573	S[289]	5724.5	77	633	S[349]	4704.5	77	693	S[409]	3684.5	77
574	S[290]	5707.5	217	634	S[350]	4687.5	217	694	S[410]	3667.5	217
575	S[291]	5690.5	357	635	S[351]	4670.5	357	695	S[411]	3650.5	357
576	S[292]	5673.5	77	636	S[352]	4653.5	77	696	S[412]	3633.5	77
577	S[293]	5656.5	217	637	S[353]	4636.5	217	697	S[413]	3616.5	217
578	S[294]	5639.5	357	638	S[354]	4619.5	357	698	S[414]	3599.5	357
579	S[295]	5622.5	77	639	S[355]	4602.5	77	699	S[415]	3582.5	77
580	S[296]	5605.5	217	640	S[356]	4585.5	217	700	S[416]	3565.5	217
581	S[297]	5588.5	357	641	S[357]	4568.5	357	701	S[417]	3548.5	357
582	S[298]	5571.5	77	642	S[358]	4551.5	77	702	S[418]	3531.5	77
583	S[299]	5554.5	217	643	S[359]	4534.5	217	703	S[419]	3514.5	217
584	S[300]	5537.5	357	644	S[360]	4517.5	357	704	S[420]	3497.5	357
585	S[301]	5520.5	77	645	S[361]	4500.5	77	705	S[421]	3480.5	77
586	S[302]	5503.5	217	646	S[362]	4483.5	217	706	S[422]	3463.5	217
587	S[303]	5486.5	357	647	S[363]	4466.5	357	707	S[423]	3446.5	357
588	S[304]	5469.5	77	648	S[364]	4449.5	77	708	S[424]	3429.5	77
589	S[305]	5452.5	217	649	S[365]	4432.5	217	709	S[425]	3412.5	217
590	S[306]	5435.5	357	650	S[366]	4415.5	357	710	S[426]	3395.5	357
591	S[307]	5418.5	77	651	S[367]	4398.5	77	711	S[427]	3378.5	77
592	S[308]	5401.5	217	652	S[368]	4381.5	217	712	S[428]	3361.5	217
593	S[309]	5384.5	357	653	S[369]	4364.5	357	713	S[429]	3344.5	357
594	S[310]	5367.5	77	654	S[370]	4347.5	77	714	S[430]	3327.5	77
595	S[311]	5350.5	217	655	S[371]	4330.5	217	715	S[431]	3310.5	217
596	S[312]	5333.5	357	656	S[372]	4313.5	357	716	S[432]	3293.5	357
597	S[313]	5316.5	77	657	S[373]	4296.5	77	717	S[433]	3276.5	77
598	S[314]	5299.5	217	658	S[374]	4279.5	217	718	S[434]	3259.5	217
599	S[315]	5282.5	357	659	S[375]	4262.5	357	719	S[435]	3242.5	357
600	S[316]	5265.5	77	660	S[376]	4245.5	77	720	S[436]	3225.5	77

number	pad name	x	y	number	pad name	x	y	number	pad name	x	y
721	S[437]	3208.5	217	781	S[497]	2188.5	217	841	S[557]	1168.5	217
722	S[438]	3191.5	357	782	S[498]	2171.5	357	842	S[558]	1151.5	357
723	S[439]	3174.5	77	783	S[499]	2154.5	77	843	S[559]	1134.5	77
724	S[440]	3157.5	217	784	S[500]	2137.5	217	844	S[560]	1117.5	217
725	S[441]	3140.5	357	785	S[501]	2120.5	357	845	S[561]	1100.5	357
726	S[442]	3123.5	77	786	S[502]	2103.5	77	846	S[562]	1083.5	77
727	S[443]	3106.5	217	787	S[503]	2086.5	217	847	S[563]	1066.5	217
728	S[444]	3089.5	357	788	S[504]	2069.5	357	848	S[564]	1049.5	357
729	S[445]	3072.5	77	789	S[505]	2052.5	77	849	S[565]	1032.5	77
730	S[446]	3055.5	217	790	S[506]	2035.5	217	850	S[566]	1015.5	217
731	S[447]	3038.5	357	791	S[507]	2018.5	357	851	S[567]	998.5	357
732	S[448]	3021.5	77	792	S[508]	2001.5	77	852	S[568]	981.5	77
733	S[449]	3004.5	217	793	S[509]	1984.5	217	853	S[569]	964.5	217
734	S[450]	2987.5	357	794	S[510]	1967.5	357	854	S[570]	947.5	357
735	S[451]	2970.5	77	795	S[511]	1950.5	77	855	S[571]	930.5	77
736	S[452]	2953.5	217	796	S[512]	1933.5	217	856	S[572]	913.5	217
737	S[453]	2936.5	357	797	S[513]	1916.5	357	857	S[573]	896.5	357
738	S[454]	2919.5	77	798	S[514]	1899.5	77	858	S[574]	879.5	77
739	S[455]	2902.5	217	799	S[515]	1882.5	217	859	S[575]	862.5	217
740	S[456]	2885.5	357	800	S[516]	1865.5	357	860	S[576]	845.5	357
741	S[457]	2868.5	77	801	S[517]	1848.5	77	861	S[577]	828.5	77
742	S[458]	2851.5	217	802	S[518]	1831.5	217	862	S[578]	811.5	217
743	S[459]	2834.5	357	803	S[519]	1814.5	357	863	S[579]	794.5	357
744	S[460]	2817.5	77	804	S[520]	1797.5	77	864	S[580]	777.5	77
745	S[461]	2800.5	217	805	S[521]	1780.5	217	865	S[581]	760.5	217
746	S[462]	2783.5	357	806	S[522]	1763.5	357	866	S[582]	743.5	357
747	S[463]	2766.5	77	807	S[523]	1746.5	77	867	S[583]	726.5	77
748	S[464]	2749.5	217	808	S[524]	1729.5	217	868	S[584]	709.5	217
749	S[465]	2732.5	357	809	S[525]	1712.5	357	869	S[585]	692.5	357
750	S[466]	2715.5	77	810	S[526]	1695.5	77	870	S[586]	675.5	77
751	S[467]	2698.5	217	811	S[527]	1678.5	217	871	S[587]	658.5	217
752	S[468]	2681.5	357	812	S[528]	1661.5	357	872	S[588]	641.5	357
753	S[469]	2664.5	77	813	S[529]	1644.5	77	873	S[589]	624.5	77
754	S[470]	2647.5	217	814	S[530]	1627.5	217	874	S[590]	607.5	217
755	S[471]	2630.5	357	815	S[531]	1610.5	357	875	S[591]	590.5	357
756	S[472]	2613.5	77	816	S[532]	1593.5	77	876	S[592]	573.5	77
757	S[473]	2596.5	217	817	S[533]	1576.5	217	877	S[593]	556.5	217
758	S[474]	2579.5	357	818	S[534]	1559.5	357	878	S[594]	539.5	357
759	S[475]	2562.5	77	819	S[535]	1542.5	77	879	S[595]	522.5	77
760	S[476]	2545.5	217	820	S[536]	1525.5	217	880	S[596]	505.5	217
761	S[477]	2528.5	357	821	S[537]	1508.5	357	881	S[597]	488.5	357
762	S[478]	2511.5	77	822	S[538]	1491.5	77	882	S[598]	471.5	77
763	S[479]	2494.5	217	823	S[539]	1474.5	217	883	S[599]	454.5	217
764	S[480]	2477.5	357	824	S[540]	1457.5	357	884	S[600]	437.5	357
765	S[481]	2460.5	77	825	S[541]	1440.5	77	885	SHIELDING[60]	403.5	357
766	S[482]	2443.5	217	826	S[542]	1423.5	217	886	SHIELDING[61]	369.5	357
767	S[483]	2426.5	357	827	S[543]	1406.5	357	887	SHIELDING[62]	335.5	357
768	S[484]	2409.5	77	828	S[544]	1389.5	77	888	SHIELDING[63]	301.5	357
769	S[485]	2392.5	217	829	S[545]	1372.5	217	889	SHIELDING[64]	267.5	357
770	S[486]	2375.5	357	830	S[546]	1355.5	357	890	SHIELDING[65]	233.5	357
771	S[487]	2358.5	77	831	S[547]	1338.5	77	891	SHIELDING[66]	-233.5	357
772	S[488]	2341.5	217	832	S[548]	1321.5	217	892	SHIELDING[67]	-267.5	357
773	S[489]	2324.5	357	833	S[549]	1304.5	357	893	SHIELDING[68]	-301.5	357
774	S[490]	2307.5	77	834	S[550]	1287.5	77	894	SHIELDING[69]	-335.5	357
775	S[491]	2290.5	217	835	S[551]	1270.5	217	895	SHIELDING[70]	-369.5	357
776	S[492]	2273.5	357	836	S[552]	1253.5	357	896	SHIELDING[71]	-403.5	357
777	S[493]	2256.5	77	837	S[553]	1236.5	77	897	S[601]	-437.5	357
778	S[494]	2239.5	217	838	S[554]	1219.5	217	898	S[602]	-471.5	217
779	S[495]	2222.5	357	839	S[555]	1202.5	357	899	S[603]	-471.5	77
780	S[496]	2205.5	77	840	S[556]	1185.5	77	900	S[604]	-488.5	357

number	pad name	x	y	number	pad name	x	y	number	pad name	x	y
901	S[605]	-505.5	217	961	S[665]	-1525.5	217	1021	S[725]	-2545.5	217
902	S[606]	-522.5	77	962	S[666]	-1542.5	77	1022	S[726]	-2562.5	77
903	S[607]	-539.5	357	963	S[667]	-1559.5	357	1023	S[727]	-2579.5	357
904	S[608]	-556.5	217	964	S[668]	-1576.5	217	1024	S[728]	-2596.5	217
905	S[609]	-573.5	77	965	S[669]	-1593.5	77	1025	S[729]	-2613.5	77
906	S[610]	-590.5	357	966	S[670]	-1610.5	357	1026	S[730]	-2630.5	357
907	S[611]	-607.5	217	967	S[671]	-1627.5	217	1027	S[731]	-2647.5	217
908	S[612]	-624.5	77	968	S[672]	-1644.5	77	1028	S[732]	-2664.5	77
909	S[613]	-641.5	357	969	S[673]	-1661.5	357	1029	S[733]	-2681.5	357
910	S[614]	-658.5	217	970	S[674]	-1678.5	217	1030	S[734]	-2698.5	217
911	S[615]	-675.5	77	971	S[675]	-1695.5	77	1031	S[735]	-2715.5	77
912	S[616]	-692.5	357	972	S[676]	-1712.5	357	1032	S[736]	-2732.5	357
913	S[617]	-709.5	217	973	S[677]	-1729.5	217	1033	S[737]	-2749.5	217
914	S[618]	-726.5	77	974	S[678]	-1746.5	77	1034	S[738]	-2766.5	77
915	S[619]	-743.5	357	975	S[679]	-1763.5	357	1035	S[739]	-2783.5	357
916	S[620]	-760.5	217	976	S[680]	-1780.5	217	1036	S[740]	-2800.5	217
917	S[621]	-777.5	77	977	S[681]	-1797.5	77	1037	S[741]	-2817.5	77
918	S[622]	-794.5	357	978	S[682]	-1814.5	357	1038	S[742]	-2834.5	357
919	S[623]	-811.5	217	979	S[683]	-1831.5	217	1039	S[743]	-2851.5	217
920	S[624]	-828.5	77	980	S[684]	-1848.5	77	1040	S[744]	-2868.5	77
921	S[625]	-845.5	357	981	S[685]	-1865.5	357	1041	S[745]	-2885.5	357
922	S[626]	-862.5	217	982	S[686]	-1882.5	217	1042	S[746]	-2902.5	217
923	S[627]	-879.5	77	983	S[687]	-1899.5	77	1043	S[747]	-2919.5	77
924	S[628]	-896.5	357	984	S[688]	-1916.5	357	1044	S[748]	-2936.5	357
925	S[629]	-913.5	217	985	S[689]	-1933.5	217	1045	S[749]	-2953.5	217
926	S[630]	-930.5	77	986	S[690]	-1950.5	77	1046	S[750]	-2970.5	77
927	S[631]	-947.5	357	987	S[691]	-1967.5	357	1047	S[751]	-2987.5	357
928	S[632]	-964.5	217	988	S[692]	-1984.5	217	1048	S[752]	-3004.5	217
929	S[633]	-981.5	77	989	S[693]	-2001.5	77	1049	S[753]	-3021.5	77
930	S[634]	-998.5	357	990	S[694]	-2018.5	357	1050	S[754]	-3038.5	357
931	S[635]	-1015.5	217	991	S[695]	-2035.5	217	1051	S[755]	-3055.5	217
932	S[636]	-1032.5	77	992	S[696]	-2052.5	77	1052	S[756]	-3072.5	77
933	S[637]	-1049.5	357	993	S[697]	-2069.5	357	1053	S[757]	-3089.5	357
934	S[638]	-1066.5	217	994	S[698]	-2086.5	217	1054	S[758]	-3106.5	217
935	S[639]	-1083.5	77	995	S[699]	-2103.5	77	1055	S[759]	-3123.5	77
936	S[640]	-1100.5	357	996	S[700]	-2120.5	357	1056	S[760]	-3140.5	357
937	S[641]	-1117.5	217	997	S[701]	-2137.5	217	1057	S[761]	-3157.5	217
938	S[642]	-1134.5	77	998	S[702]	-2154.5	77	1058	S[762]	-3174.5	77
939	S[643]	-1151.5	357	999	S[703]	-2171.5	357	1059	S[763]	-3191.5	357
940	S[644]	-1168.5	217	1000	S[704]	-2188.5	217	1060	S[764]	-3208.5	217
941	S[645]	-1185.5	77	1001	S[705]	-2205.5	77	1061	S[765]	-3225.5	77
942	S[646]	-1202.5	357	1002	S[706]	-2222.5	357	1062	S[766]	-3242.5	357
943	S[647]	-1219.5	217	1003	S[707]	-2239.5	217	1063	S[767]	-3259.5	217
944	S[648]	-1236.5	77	1004	S[708]	-2256.5	77	1064	S[768]	-3276.5	77
945	S[649]	-1253.5	357	1005	S[709]	-2273.5	357	1065	S[769]	-3293.5	357
946	S[650]	-1270.5	217	1006	S[710]	-2290.5	217	1066	S[770]	-3310.5	217
947	S[651]	-1287.5	77	1007	S[711]	-2307.5	77	1067	S[771]	-3327.5	77
948	S[652]	-1304.5	357	1008	S[712]	-2324.5	357	1068	S[772]	-3344.5	357
949	S[653]	-1321.5	217	1009	S[713]	-2341.5	217	1069	S[773]	-3361.5	217
950	S[654]	-1338.5	77	1010	S[714]	-2358.5	77	1070	S[774]	-3378.5	77
951	S[655]	-1355.5	357	1011	S[715]	-2375.5	357	1071	S[775]	-3395.5	357
952	S[656]	-1372.5	217	1012	S[716]	-2392.5	217	1072	S[776]	-3412.5	217
953	S[657]	-1389.5	77	1013	S[717]	-2409.5	77	1073	S[777]	-3429.5	77
954	S[658]	-1406.5	357	1014	S[718]	-2426.5	357	1074	S[778]	-3446.5	357
955	S[659]	-1423.5	217	1015	S[719]	-2443.5	217	1075	S[779]	-3463.5	217
956	S[660]	-1440.5	77	1016	S[720]	-2460.5	77	1076	S[780]	-3480.5	77
957	S[661]	-1457.5	357	1017	S[721]	-2477.5	357	1077	S[781]	-3497.5	357
958	S[662]	-1474.5	217	1018	S[722]	-2494.5	217	1078	S[782]	-3514.5	217
959	S[663]	-1491.5	77	1019	S[723]	-2511.5	77	1079	S[783]	-3531.5	77
960	S[664]	-1508.5	357	1020	S[724]	-2528.5	357	1080	S[784]	-3548.5	357

number	pad name	x	y	number	pad name	x	y	number	pad name	x	y
1081	S[785]	-3565.5	217	1141	S[845]	-4585.5	217	1201	S[905]	-5605.5	217
1082	S[786]	-3582.5	77	1142	S[846]	-4602.5	77	1202	S[906]	-5622.5	77
1083	S[787]	-3599.5	357	1143	S[847]	-4619.5	357	1203	S[907]	-5639.5	357
1084	S[788]	-3616.5	217	1144	S[848]	-4636.5	217	1204	S[908]	-5656.5	217
1085	S[789]	-3633.5	77	1145	S[849]	-4653.5	77	1205	S[909]	-5673.5	77
1086	S[790]	-3650.5	357	1146	S[850]	-4670.5	357	1206	S[910]	-5690.5	357
1087	S[791]	-3667.5	217	1147	S[851]	-4687.5	217	1207	S[911]	-5707.5	217
1088	S[792]	-3684.5	77	1148	S[852]	-4704.5	77	1208	S[912]	-5724.5	77
1089	S[793]	-3701.5	357	1149	S[853]	-4721.5	357	1209	S[913]	-5741.5	357
1090	S[794]	-3718.5	217	1150	S[854]	-4738.5	217	1210	S[914]	-5758.5	217
1091	S[795]	-3735.5	77	1151	S[855]	-4755.5	77	1211	S[915]	-5775.5	77
1092	S[796]	-3752.5	357	1152	S[856]	-4772.5	357	1212	S[916]	-5792.5	357
1093	S[797]	-3769.5	217	1153	S[857]	-4789.5	217	1213	S[917]	-5809.5	217
1094	S[798]	-3786.5	77	1154	S[858]	-4806.5	77	1214	S[918]	-5826.5	77
1095	S[799]	-3803.5	357	1155	S[859]	-4823.5	357	1215	S[919]	-5843.5	357
1096	S[800]	-3820.5	217	1156	S[860]	-4840.5	217	1216	S[920]	-5860.5	217
1097	S[801]	-3837.5	77	1157	S[861]	-4857.5	77	1217	S[921]	-5877.5	77
1098	S[802]	-3854.5	357	1158	S[862]	-4874.5	357	1218	S[922]	-5894.5	357
1099	S[803]	-3871.5	217	1159	S[863]	-4891.5	217	1219	S[923]	-5911.5	217
1100	S[804]	-3888.5	77	1160	S[864]	-4908.5	77	1220	S[924]	-5928.5	77
1101	S[805]	-3905.5	357	1161	S[865]	-4925.5	357	1221	S[925]	-5945.5	357
1102	S[806]	-3922.5	217	1162	S[866]	-4942.5	217	1222	S[926]	-5962.5	217
1103	S[807]	-3939.5	77	1163	S[867]	-4959.5	77	1223	S[927]	-5979.5	77
1104	S[808]	-3956.5	357	1164	S[868]	-4976.5	357	1224	S[928]	-5996.5	357
1105	S[809]	-3973.5	217	1165	S[869]	-4993.5	217	1225	S[929]	-6013.5	217
1106	S[810]	-3990.5	77	1166	S[870]	-5010.5	77	1226	S[930]	-6030.5	77
1107	S[811]	-4007.5	357	1167	S[871]	-5027.5	357	1227	S[931]	-6047.5	357
1108	S[812]	-4024.5	217	1168	S[872]	-5044.5	217	1228	S[932]	-6064.5	217
1109	S[813]	-4041.5	77	1169	S[873]	-5061.5	77	1229	S[933]	-6081.5	77
1110	S[814]	-4058.5	357	1170	S[874]	-5078.5	357	1230	S[934]	-6098.5	357
1111	S[815]	-4075.5	217	1171	S[875]	-5095.5	217	1231	S[935]	-6115.5	217
1112	S[816]	-4092.5	77	1172	S[876]	-5112.5	77	1232	S[936]	-6132.5	77
1113	S[817]	-4109.5	357	1173	S[877]	-5129.5	357	1233	S[937]	-6149.5	357
1114	S[818]	-4126.5	217	1174	S[878]	-5146.5	217	1234	S[938]	-6166.5	217
1115	S[819]	-4143.5	77	1175	S[879]	-5163.5	77	1235	S[939]	-6183.5	77
1116	S[820]	-4160.5	357	1176	S[880]	-5180.5	357	1236	S[940]	-6200.5	357
1117	S[821]	-4177.5	217	1177	S[881]	-5197.5	217	1237	S[941]	-6217.5	217
1118	S[822]	-4194.5	77	1178	S[882]	-5214.5	77	1238	S[942]	-6234.5	77
1119	S[823]	-4211.5	357	1179	S[883]	-5231.5	357	1239	S[943]	-6251.5	357
1120	S[824]	-4228.5	217	1180	S[884]	-5248.5	217	1240	S[944]	-6268.5	217
1121	S[825]	-4245.5	77	1181	S[885]	-5265.5	77	1241	S[945]	-6285.5	77
1122	S[826]	-4262.5	357	1182	S[886]	-5282.5	357	1242	S[946]	-6302.5	357
1123	S[827]	-4279.5	217	1183	S[887]	-5299.5	217	1243	S[947]	-6319.5	217
1124	S[828]	-4296.5	77	1184	S[888]	-5316.5	77	1244	S[948]	-6336.5	77
1125	S[829]	-4313.5	357	1185	S[889]	-5333.5	357	1245	S[949]	-6353.5	357
1126	S[830]	-4330.5	217	1186	S[890]	-5350.5	217	1246	S[950]	-6370.5	217
1127	S[831]	-4347.5	77	1187	S[891]	-5367.5	77	1247	S[951]	-6387.5	77
1128	S[832]	-4364.5	357	1188	S[892]	-5384.5	357	1248	S[952]	-6404.5	357
1129	S[833]	-4381.5	217	1189	S[893]	-5401.5	217	1249	S[953]	-6421.5	217
1130	S[834]	-4398.5	77	1190	S[894]	-5418.5	77	1250	S[954]	-6438.5	77
1131	S[835]	-4415.5	357	1191	S[895]	-5435.5	357	1251	S[955]	-6455.5	357
1132	S[836]	-4432.5	217	1192	S[896]	-5452.5	217	1252	S[956]	-6472.5	217
1133	S[837]	-4449.5	77	1193	S[897]	-5469.5	77	1253	S[957]	-6489.5	77
1134	S[838]	-4466.5	357	1194	S[898]	-5486.5	357	1254	S[958]	-6506.5	357
1135	S[839]	-4483.5	217	1195	S[899]	-5503.5	217	1255	S[959]	-6523.5	217
1136	S[840]	-4500.5	77	1196	S[900]	-5520.5	77	1256	S[960]	-6540.5	77
1137	S[841]	-4517.5	357	1197	S[901]	-5537.5	357	1257	S[961]	-6557.5	357
1138	S[842]	-4534.5	217	1198	S[902]	-5554.5	217	1258	S[962]	-6574.5	217
1139	S[843]	-4551.5	77	1199	S[903]	-5571.5	77	1259	S[963]	-6591.5	77
1140	S[844]	-4568.5	357	1200	S[904]	-5588.5	357	1260	S[964]	-6608.5	357

number	pad name	x	y
1261	S[965]	-6625.5	217

number	pad name	x	y
1321	S[1025]	-7645.5	217

number	pad name	x	y
1381	S[1085]	-8665.5	217



1262	S[966]	-6642.5	77	1322	S[1026]	-7662.5	77	1382	S[1086]	-8682.5	77
1263	S[967]	-6659.5	357	1323	S[1027]	-7679.5	357	1383	S[1087]	-8699.5	357
1264	S[968]	-6676.5	217	1324	S[1028]	-7696.5	217	1384	S[1088]	-8716.5	217
1265	S[969]	-6693.5	77	1325	S[1029]	-7713.5	77	1385	S[1089]	-8733.5	77
1266	S[970]	-6710.5	357	1326	S[1030]	-7730.5	357	1386	S[1090]	-8750.5	357
1267	S[971]	-6727.5	217	1327	S[1031]	-7747.5	217	1387	S[1091]	-8767.5	217
1268	S[972]	-6744.5	77	1328	S[1032]	-7764.5	77	1388	S[1092]	-8784.5	77
1269	S[973]	-6761.5	357	1329	S[1033]	-7781.5	357	1389	S[1093]	-8801.5	357
1270	S[974]	-6778.5	217	1330	S[1034]	-7798.5	217	1390	S[1094]	-8818.5	217
1271	S[975]	-6795.5	77	1331	S[1035]	-7815.5	77	1391	S[1095]	-8835.5	77
1272	S[976]	-6812.5	357	1332	S[1036]	-7832.5	357	1392	S[1096]	-8852.5	357
1273	S[977]	-6829.5	217	1333	S[1037]	-7849.5	217	1393	S[1097]	-8869.5	217
1274	S[978]	-6846.5	77	1334	S[1038]	-7866.5	77	1394	S[1098]	-8886.5	77
1275	S[979]	-6863.5	357	1335	S[1039]	-7883.5	357	1395	S[1099]	-8903.5	357
1276	S[980]	-6880.5	217	1336	S[1040]	-7900.5	217	1396	S[1100]	-8920.5	217
1277	S[981]	-6897.5	77	1337	S[1041]	-7917.5	77	1397	S[1101]	-8937.5	77
1278	S[982]	-6914.5	357	1338	S[1042]	-7934.5	357	1398	S[1102]	-8954.5	357
1279	S[983]	-6931.5	217	1339	S[1043]	-7951.5	217	1399	S[1103]	-8971.5	217
1280	S[984]	-6948.5	77	1340	S[1044]	-7968.5	77	1400	S[1104]	-8988.5	77
1281	S[985]	-6965.5	357	1341	S[1045]	-7985.5	357	1401	S[1105]	-9005.5	357
1282	S[986]	-6982.5	217	1342	S[1046]	-8002.5	217	1402	S[1106]	-9022.5	217
1283	S[987]	-6999.5	77	1343	S[1047]	-8019.5	77	1403	S[1107]	-9039.5	77
1284	S[988]	-7016.5	357	1344	S[1048]	-8036.5	357	1404	S[1108]	-9056.5	357
1285	S[989]	-7033.5	217	1345	S[1049]	-8053.5	217	1405	S[1109]	-9073.5	217
1286	S[990]	-7050.5	77	1346	S[1050]	-8070.5	77	1406	S[1110]	-9090.5	77
1287	S[991]	-7067.5	357	1347	S[1051]	-8087.5	357	1407	S[1111]	-9107.5	357
1288	S[992]	-7084.5	217	1348	S[1052]	-8104.5	217	1408	S[1112]	-9124.5	217
1289	S[993]	-7101.5	77	1349	S[1053]	-8121.5	77	1409	S[1113]	-9141.5	77
1290	S[994]	-7118.5	357	1350	S[1054]	-8138.5	357	1410	S[1114]	-9158.5	357
1291	S[995]	-7135.5	217	1351	S[1055]	-8155.5	217	1411	S[1115]	-9175.5	217
1292	S[996]	-7152.5	77	1352	S[1056]	-8172.5	77	1412	S[1116]	-9192.5	77
1293	S[997]	-7169.5	357	1353	S[1057]	-8189.5	357	1413	S[1117]	-9209.5	357
1294	S[998]	-7186.5	217	1354	S[1058]	-8206.5	217	1414	S[1118]	-9226.5	217
1295	S[999]	-7203.5	77	1355	S[1059]	-8223.5	77	1415	S[1119]	-9243.5	77
1296	S[1000]	-7220.5	357	1356	S[1060]	-8240.5	357	1416	S[1120]	-9260.5	357
1297	S[1001]	-7237.5	217	1357	S[1061]	-8257.5	217	1417	S[1121]	-9277.5	217
1298	S[1002]	-7254.5	77	1358	S[1062]	-8274.5	77	1418	S[1122]	-9294.5	77
1299	S[1003]	-7271.5	357	1359	S[1063]	-8291.5	357	1419	S[1123]	-9311.5	357
1300	S[1004]	-7288.5	217	1360	S[1064]	-8308.5	217	1420	S[1124]	-9328.5	217
1301	S[1005]	-7305.5	77	1361	S[1065]	-8325.5	77	1421	S[1125]	-9345.5	77
1302	S[1006]	-7322.5	357	1362	S[1066]	-8342.5	357	1422	S[1126]	-9362.5	357
1303	S[1007]	-7339.5	217	1363	S[1067]	-8359.5	217	1423	S[1127]	-9379.5	217
1304	S[1008]	-7356.5	77	1364	S[1068]	-8376.5	77	1424	S[1128]	-9396.5	77
1305	S[1009]	-7373.5	357	1365	S[1069]	-8393.5	357	1425	S[1129]	-9413.5	357
1306	S[1010]	-7390.5	217	1366	S[1070]	-8410.5	217	1426	S[1130]	-9430.5	217
1307	S[1011]	-7407.5	77	1367	S[1071]	-8427.5	77	1427	S[1131]	-9447.5	77
1308	S[1012]	-7424.5	357	1368	S[1072]	-8444.5	357	1428	S[1132]	-9464.5	357
1309	S[1013]	-7441.5	217	1369	S[1073]	-8461.5	217	1429	S[1133]	-9481.5	217
1310	S[1014]	-7458.5	77	1370	S[1074]	-8478.5	77	1430	S[1134]	-9498.5	77
1311	S[1015]	-7475.5	357	1371	S[1075]	-8495.5	357	1431	S[1135]	-9515.5	357
1312	S[1016]	-7492.5	217	1372	S[1076]	-8512.5	217	1432	S[1136]	-9532.5	217
1313	S[1017]	-7509.5	77	1373	S[1077]	-8529.5	77	1433	S[1137]	-9549.5	77
1314	S[1018]	-7526.5	357	1374	S[1078]	-8546.5	357	1434	S[1138]	-9566.5	357
1315	S[1019]	-7543.5	217	1375	S[1079]	-8563.5	217	1435	S[1139]	-9583.5	217
1316	S[1020]	-7560.5	77	1376	S[1080]	-8580.5	77	1436	S[1140]	-9600.5	77
1317	S[1021]	-7577.5	357	1377	S[1081]	-8597.5	357	1437	S[1141]	-9617.5	357
1318	S[1022]	-7594.5	217	1378	S[1082]	-8614.5	217	1438	S[1142]	-9634.5	217
1319	S[1023]	-7611.5	77	1379	S[1083]	-8631.5	77	1439	S[1143]	-9651.5	77
1320	S[1024]	-7628.5	357	1380	S[1084]	-8648.5	357	1440	S[1144]	-9668.5	357

number	pad name	x	y	number	pad name	x	y	number	pad name	x	y
1441	S[1145]	-9685.5	217	1471	S[1175]	-10195.5	217	1501	XON_R	-10864	377
1442	S[1146]	-9702.5	77	1472	S[1176]	-10212.5	77	1502	XON_R	-10914	377

1443	S[1147]	-9719.5	357	1473	S[1177]	-10229.5	357	1503	F_CTRL_R	-11179	397
1444	S[1148]	-9736.5	217	1474	S[1178]	-10246.5	217	1504	SHIELDING[74]	-11049	357
1445	S[1149]	-9753.5	77	1475	S[1179]	-10263.5	77	1505	OE_V_R	-11179	317
1446	S[1150]	-9770.5	357	1476	S[1180]	-10280.5	357	1506	SHIELDING[75]	-11049	277
1447	S[1151]	-9787.5	217	1477	S[1181]	-10297.5	217	1507	UD_R	-11179	237
1448	S[1152]	-9804.5	77	1478	S[1182]	-10314.5	77	1508	SHIELDING[76]	-11049	197
1449	S[1153]	-9821.5	357	1479	S[1183]	-10331.5	357	1509	CKV_R	-11179	157
1450	S[1154]	-9838.5	217	1480	S[1184]	-10348.5	217	1510	SHIELDING[77]	-11049	117
1451	S[1155]	-9855.5	77	1481	S[1185]	-10365.5	77	1511	STV1_R	-11179	77
1452	S[1156]	-9872.5	357	1482	S[1186]	-10382.5	357	1512	SHIELDING[78]	-11049	37
1453	S[1157]	-9889.5	217	1483	S[1187]	-10399.5	217	1513	STV2_R	-11179	-3
1454	S[1158]	-9906.5	77	1484	S[1188]	-10416.5	77	1514	SHIELDING[79]	-11049	-43
1455	S[1159]	-9923.5	357	1485	S[1189]	-10433.5	357	1515	STV1_R	-11179	-83
1456	S[1160]	-9940.5	217	1486	S[1190]	-10450.5	217	1516	SHIELDING[80]	-11049	-123
1457	S[1161]	-9957.5	77	1487	S[1191]	-10467.5	77	1517	TP[9]	-11179	-163
1458	S[1162]	-9974.5	357	1488	S[1192]	-10484.5	357	1518	SHIELDING[81]	-11049	-203
1459	S[1163]	-9991.5	217	1489	S[1193]	-10501.5	217	1519	STBN_R	-11179	-243
1460	S[1164]	-10008.5	77	1490	S[1194]	-10518.5	77	1520	SHIELDING[82]	-11049	-283
1461	S[1165]	-10025.5	357	1491	S[1195]	-10535.5	357	1521	TP[10]	-11179	-323
1462	S[1166]	-10042.5	217	1492	S[1196]	-10552.5	217	1522	TP[11]	-11049	-363
1463	S[1167]	-10059.5	77	1493	S[1197]	-10569.5	77				
1464	S[1168]	-10076.5	357	1494	S[1198]	-10586.5	357				
1465	S[1169]	-10093.5	217	1495	S[1199]	-10603.5	217				
1466	S[1170]	-10110.5	77	1496	S[1200]	-10620.5	77				
1467	S[1171]	-10127.5	357	1497	SHIELDING[72]	-10664	377				
1468	S[1172]	-10144.5	217	1498	COM1_T	-10714	377				
1469	S[1173]	-10161.5	77	1499	COM1_T	-10764	377				
1470	S[1174]	-10178.5	357	1500	SHIELDING[73]	-10814	377				

Note: IC Pads Coordination values that concern thermal shift issue (After bonding Process)!!

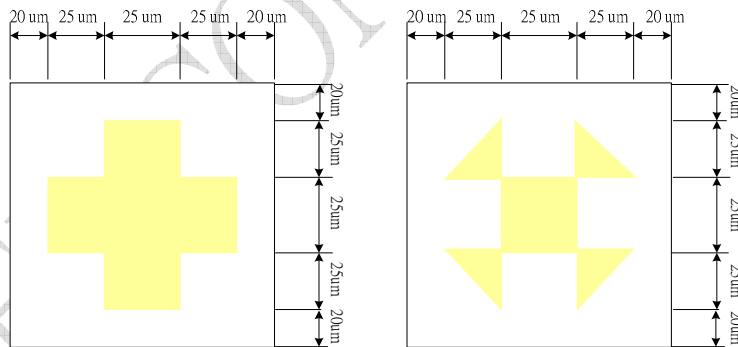
**Alignment Mark**

--Alignment mark coordinate

Left (-10773, 93)

Right (10773, 93)

--Alignment Mark size



Alignment Mark: Left

Alignment Mark: Right

### 15. Revision History

Version No.	Date	Page	Description
V0.01	2011/06/16	All	New creat

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