



EK73215BCGA

Rev. 1.0

DATA SHEET

1200/1152/1080/960-Output
TFT LCD Gate Driver

fitipower integrated technology Inc.

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1200/1152/1080/960-Output TFT LCD Gate Driver

1. GENERAL DESCRIPTION

The EK73215 is a 1200/1152/1080/960-Output gate driver used for driving the gate electrode of TFT LCD panel. It is designed for 2-level output with maximum +40V output driving voltage.

2. FEATURES

- 2-level output gate driver for TFT LCD panel
- 1200/1152/1080/960-Output gate driver with 2 dummy outputs which are fixed to VGL
- Maximum +40V output driving voltage
- Logic operating voltage (VCC): 1.7 ~ 3.6V
- Bi-directional data shift capability
- 200 KHz maximum operation frequency
- High voltage CMOS process technology
- COG package
- Chip size=23650*670 μ m
- Output bump pitch=18 μ m

3. BLOCK DIAGRAM

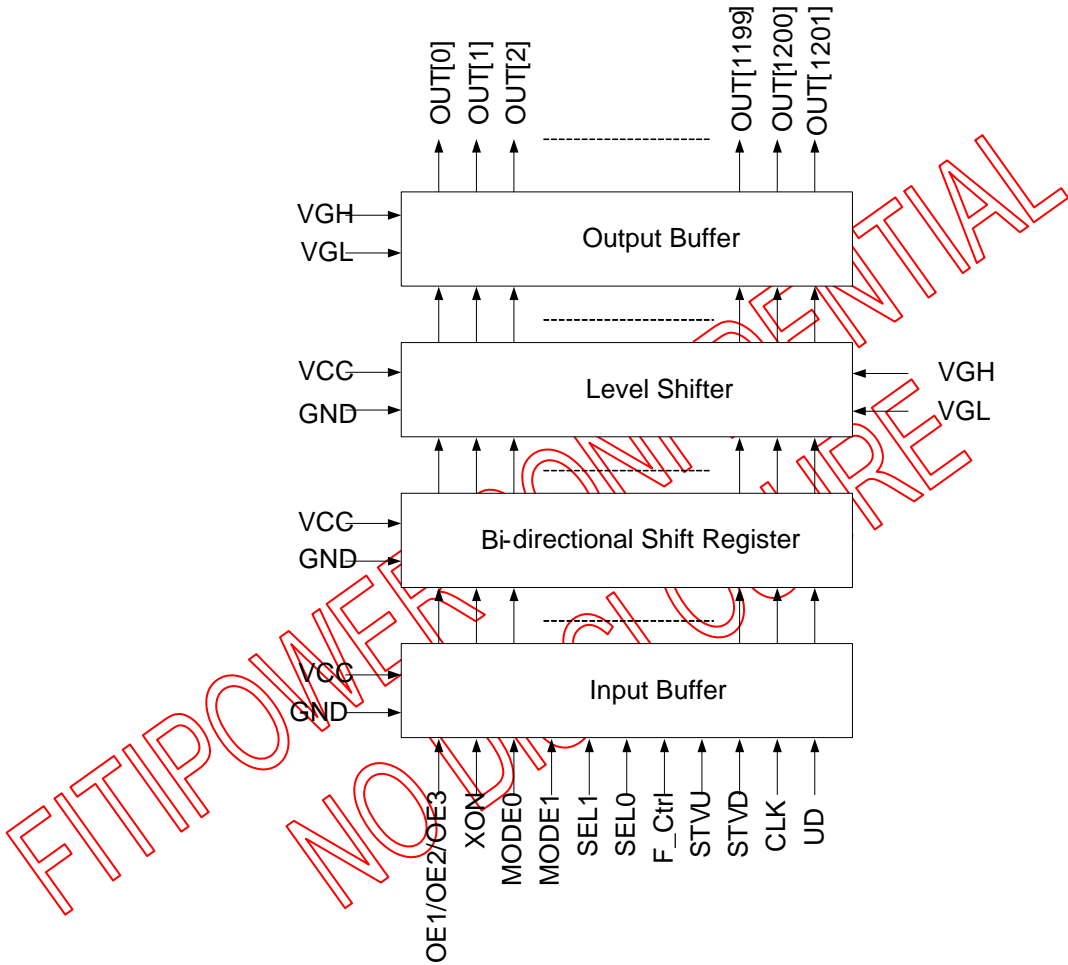


Figure 1. Block Diagram

4. PIN DESCRIPTION

Pin Name	Pin Type	Description									
CLKR/CLKL	I	This is the clock input for chip internal shift register. Data is shifted at each rising edge of this clock.									
UDR/UDL	I	This pin controls the output shifting direction as listed below. UD = H: STVD(input)→OUT[1]→OUT[2]→...→OUT[1200]→STVU UD = L: STVU(input)→OUT[1200]→...→OUT[2]→OUT[1]→STVD									
STVD STVU	I/O	These two pins are the device start pulse input or output pin. The function of these two pins depends on the status of UD pin. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th></th> <th>STVD</th> <th>STVU</th> </tr> </thead> <tbody> <tr> <td>UD = H</td> <td>input</td> <td>output</td> </tr> <tr> <td>UD = L</td> <td>output</td> <td>input</td> </tr> </tbody> </table>		STVD	STVU	UD = H	input	output	UD = L	output	input
	STVD	STVU									
UD = H	input	output									
UD = L	output	input									
OE1R/OE1L	I	The OE1 signal controls the OUT1, OUT4, OUT7...OUT1195, OUT1198 output enable. OE1,2,3="H": outputs are fixed to VGL regardless of CLK, However, the content of shift register is not cleared. OE1,2,3="L": Normal operation.									
OE2R/OE2L	I	The OE1 signal controls the OUT2, OUT5, OUT8...OUT1196, OUT1199 output enable. OE1,2,3="H": outputs are fixed to VGL regardless of CLK, However, the content of shift register is not cleared. OE1,2,3="L": Normal operation.									
OE3R/OE3L	I	The OE1 signal controls the OUT3, OUT6, OUT9...OUT1197, OUT1200 output enable. OE1,2,3="H": outputs are fixed to VGL regardless of CLK, However, the content of shift register is not cleared. OE1,2,3="L": Normal operation.									
XONR/XONL	IPH	When XON input pin is L, all the output pins are forced to VGH level. Note that this pin has higher priority than OE1/OE2/OE3. Also it has an internal pull high resistor, keep it to VCC is preferred when unused. The chip internal shift register is not cleared when XON input is active.									

MODE0R MODE0L MODE1R MODE1L	IPH	<p>Output channels select input. MODE0/MODE1 are internally pulled high.</p> <p>Note: This pin should be connected to either "VCC" or "GND".</p> <table border="1"> <thead> <tr> <th>MODE1</th> <th>MODE0</th> <th>Output Channels</th> <th>Disable channel</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> <td>1200</td> <td>-</td> </tr> <tr> <td>1</td> <td>0</td> <td>1152</td> <td>OUT[577] ~ OUT[624]</td> </tr> <tr> <td>0</td> <td>1</td> <td>1080</td> <td>OUT[541] ~ OUT[660]</td> </tr> <tr> <td>0</td> <td>0</td> <td>960</td> <td>OUT[481] ~ OUT[720]</td> </tr> </tbody> </table>	MODE1	MODE0	Output Channels	Disable channel	1	1	1200	-	1	0	1152	OUT[577] ~ OUT[624]	0	1	1080	OUT[541] ~ OUT[660]	0	0	960	OUT[481] ~ OUT[720]
MODE1	MODE0	Output Channels	Disable channel																			
1	1	1200	-																			
1	0	1152	OUT[577] ~ OUT[624]																			
0	1	1080	OUT[541] ~ OUT[660]																			
0	0	960	OUT[481] ~ OUT[720]																			
SEL0R SEL0L SEL1R SEL1L	IPL	<p>Output sequence control inputs. These two pins control the driver output sequence. Internally pulled low.</p> <table border="1"> <thead> <tr> <th>SEL1</th> <th>SEL0</th> <th>Scan Type</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> <td>Z+ Bow</td> </tr> <tr> <td>0</td> <td>1</td> <td>Bow</td> </tr> <tr> <td>X</td> <td>0</td> <td>Z</td> </tr> </tbody> </table>	SEL1	SEL0	Scan Type	1	1	Z+ Bow	0	1	Bow	X	0	Z								
SEL1	SEL0	Scan Type																				
1	1	Z+ Bow																				
0	1	Bow																				
X	0	Z																				
F_CtrlL F_CtrlR	IPL	<p>Frame control input. This pin decides to inverse the output sequence or not in odd or even frame. Internally pulled low.</p>																				
OUT[1] ~ OUT[1200]	O	<p>The output voltage is either VGH or VGL for driving the gate electrode of TFT LCD panel depending on the data stored in shift register and the state of OE.</p>																				
OUT[0] OUT[1201]	O	<p>LCD panel auxiliary pins, these pins always output VGL level.</p>																				

Pin Name	Pin Type	Description
VCC	P	Digital power
GND	P	Digital ground
VGH	P	Power supply for OUT[1] ~ OUT[1200] drive output High
VGL	P	Power supply for OUT[1] ~ OUT[1200] drive output Low.
PATH1R,PATH1L PATH2R,PATH2L PATH3R,PATH3L	-	Linked together internal.
DUM2~DUM220	-	This pin is connected to GND internally. Not connected.

Note:

I: Input, IPH: Input with internal pull high, IPL: Input with internal low, O: Output, P: Power.

Pass line name

Pass line No.	Pad name	
1	OE1R	OE1L
2	OE2R	OE2L
3	OE3R	OE3L
4	UDR	UDL
5	CLKR	CLKL
6	PATH1R	PATH1L
7	PATH2R	PATH2L
8	PATH3R	PATH3L
9	VGH	VGH
10	VGL	VGL
11	VCC	VCC
12	GND	GND
13	MODE0R	MODE0L
14	MODE1R	MODE0L
15	SEL0R	SEL0L
16	SEL1R	SEL1L
17	F_CtrlR	F_CtrlL
18	XONR	XONL

5. FUNCTION DESCRIPTION

5.1. Device operation

In the condition of UD=H, the STVD start pulse input is sensed at the rising edge of CLK and stored in the first stage of shift register, which causes the first scan signal is output from the X1 output pin. While stored data is transferred to the next stage shift register at the rising edge of next CLK, new data of STVD is sensed and stored simultaneously.

The output pin (OUT[1] to OUT[1200]) supplies VGH voltage or VGL voltage to the LCD panel depending on the data stored in the shift register. For normal operation, a VGH voltage is output one by one from OUT[1] to OUT[1200] in sync with CLK pulse.

After 1200 CLK rising edge are past, the STVU goes up to high level at the 1200th falling edge of CLK and goes down to low level at the 1201th falling edge of CLK. This STVU output signal becomes the STVD start pulse input of next cascaded gate driver device.

During any "H" state of OE, the corresponding output channels are forced to VGL level regardless of CLK. The channel output returns to normal status as soon as OE go back to "L".

5.2. Device power supply

The EK73215 must be used by the following conditions.

* $VGH - VGL = 40V$ (max.)

* $VGH - GND = 7 \sim 35V$

Example:

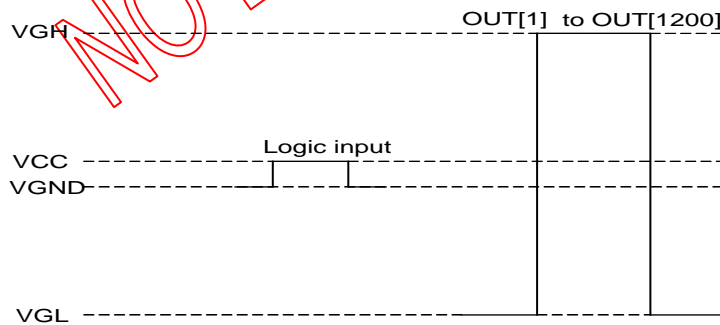


Figure 2. Device power supply

The input signal level of CLK, UD, OE, STVD, STVU, MODE0, MODE1, SEL1, SEL0, and F_ctrl have to swing between VCC and GND. The signal output level of start pulse (STVU or STVD) to the next stage cascaded device is VCC for "H" and GND for "L".

5.3. Power ON/OFF sequence

To prevent the device from damage due to latch up, the power ON/OFF sequence shown below must be followed.

When power on: VCC→VGL→VGH

When power off: VGH→VGL→VCC

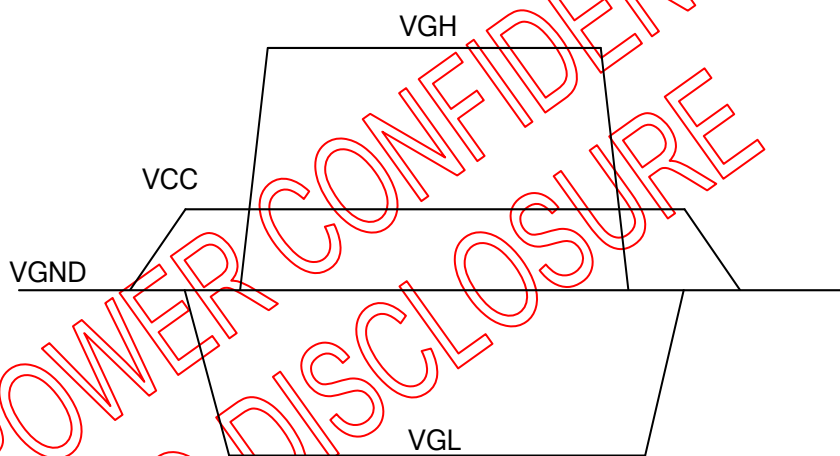


Figure 3. Power ON/OFF sequence

5.4. Start Pulse LIMITATION

The available start pulse is in the following diagram.

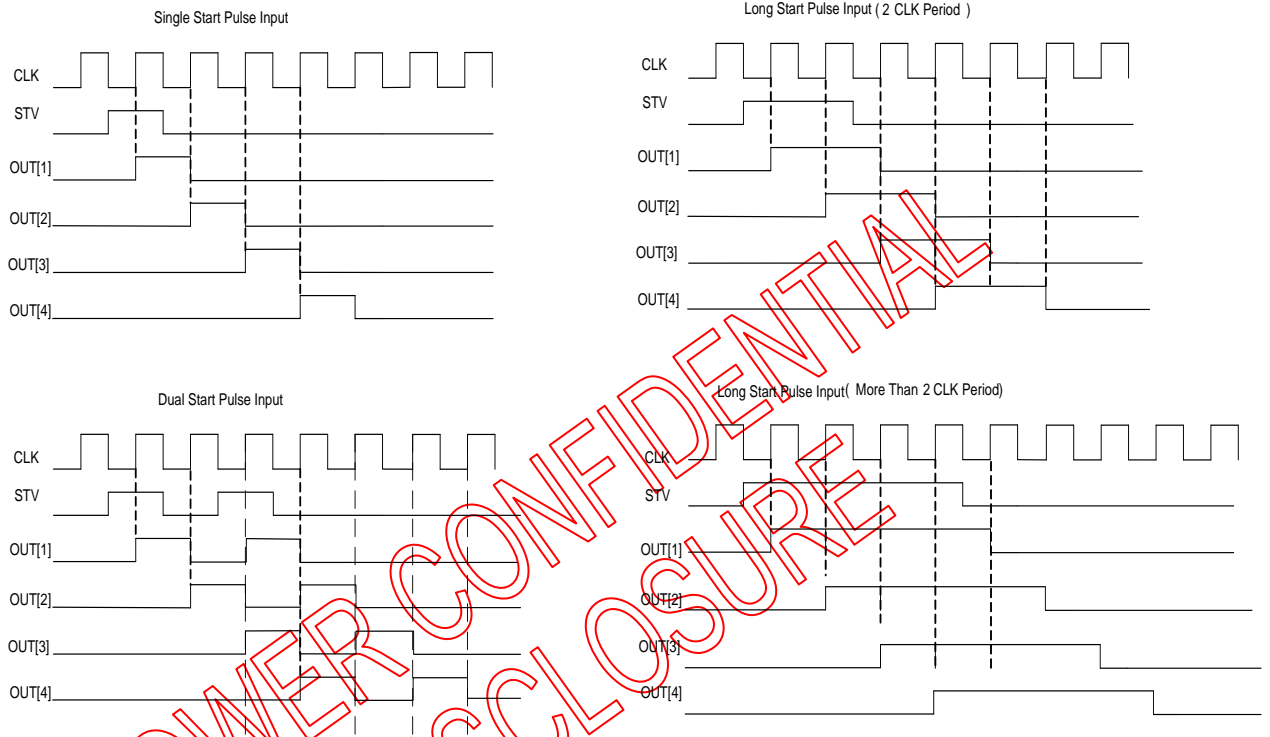
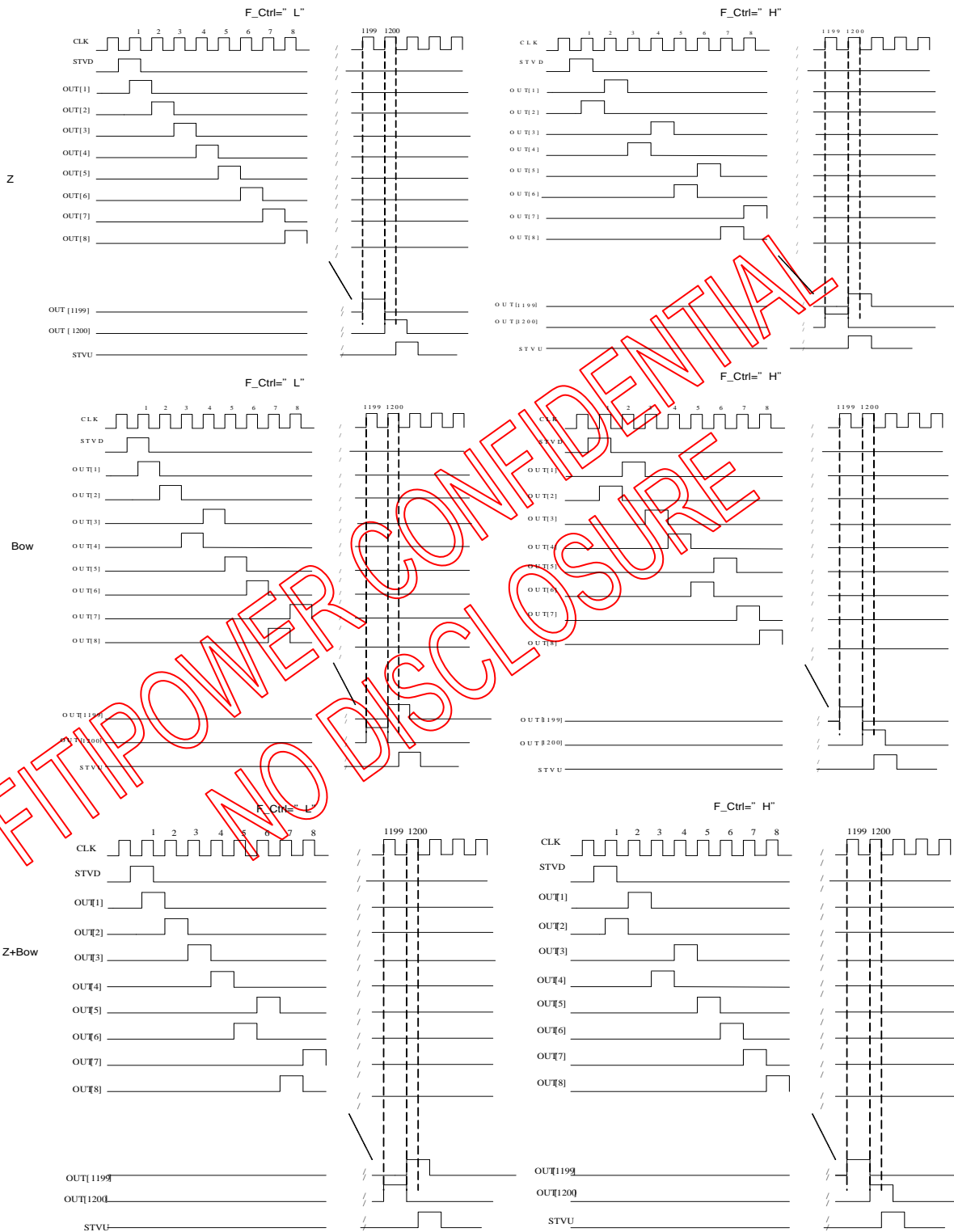


Figure 4. Start pulse Input limitation

Note: However the start pulse form changes, gate output keeps output sequentially.

5.5. Output Sequence and Frame Control

UD = H				
SEL0	SEL1	F_Ctrl	Scan Type	Output Sequence
1	1	0	Z + BOW	1→2→3→4→6→5→8→7→... (Note1)
		1	Inverse (Z+BOW)	2→1→4→3→5→6→7→8→...
1	0	0	BOW	1→2→4→3→5→6→8→7→... (Note2)
		1	Inverse BOW	2→1→3→4→6→5→7→8→...
0	X	0	Z	1→2→3→4→5→6→7→8→... (Note 3)
		1	Inverse Z	2→1→4→3→6→5→8→7→... (Note 4)
UD = L				
SEL0	SEL1	F_Ctrl	Scan Type	Output Sequence
1	1	0	Z + BOW	...8→7→6→5→3→4→1→2
		1	Inverse (Z+BOW)	...7→8→5→6→4→3→2→1
1	0	0	BOW	...8→7→5→6→4→3→1→2
		1	Inverse BOW	...7→8→6→5→3→4→2→1
0	X	0	Z	...8→7→6→5→4→3→2→1
		1	Inverse Z	...7→8→5→6→3→4→1→2



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6. ELECTRICAL SPECIFICATION

6.1. Absolute Maximum Ratings

Absolute Maximum Ratings (GND = 0 V)

Parameter	Symbol	Rating	Unit
Power supply voltage (1)	VGH	-0.3 to +42.0	V
Power supply voltage (2)	VCC	-0.3 to +7.0	V
Power supply voltage (3)	VGL	-20 to +0.3	V
Power supply voltage (4)	VGH - VGL	-0.3 to +40	V
Input voltage	V _{IN}	-0.3 to VCC+0.3	V
Storage temperature	T _{STG}	-55 to +125	°C

Note 1: All of the voltages listed above are with respect to GND = 0V.

Note 2: Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

6.2. Recommended Operating Range

Recommended Operating Range (VGND = 0V)

Parameter	Symbol	Conditions	Rating			Unit
			Min.	Typ.	Max.	
Power supply voltage (1)	VGH	-	7	-	VGL+40	V
Power supply voltage (2)	VCC	-	1.7	-	3.6	V
Power supply voltage (3)	VGL	VCC=1.7V~2.3V	-10	-	-5	V
		VCC=2.3V~3.6V	-10	-	-3	V
Power supply voltage (4)	VGH - VGL	-	15	-	40	V
Operation frequency	FCLK	-	-	-	200	KHz
Operation temperature	Ta	-	-20	-	+85	°C

6.3. DC Characteristics

DC Characteristic (VGH = 25V, VGL = -15V, VCC = 3.3V/1.8V, GND = 0V, Ta = 25°C)

Parameter	Symbol	Condition	Rating			Unit	Application pin
			Min.	Typ.	Max.		
Input H voltage	V _{IH}	-	0.7VCC	-	VCC	V	All input
Input L voltage	V _{IL}	-	0	-	0.3VCC	V	All input
Output H voltage	V _{OH}	I _{OH} =40μA	VCC-0.4	-	VCC	V	STVU,D
Output L voltage	V _{OL}	I _{OL} =40μA	0	-	0.4	V	STVU,D
Output H resistance	R _{OH}	V _X = VGH -0.5V	-	-	1000	Ω	OUT[1] ~ OUT[1200]
Output L resistance	R _{OL}	V _X = VGL +0.5V	-	-	1000	Ω	OUT[1] ~ OUT[1200]
Input leakage current	I _{IN}	-	-1.0	-	+1.0	μA	Note ⁽²⁾
Pull high / low resistance	R _{PHL}	VCC=3.3V V _{IN} =VGND V _{IN} =VCC	50	-	330	kΩ	XON, SEL1, SEL0, F_CTRL
		VCC=1.8V V _{IN} =VGND V _{IN} =VCC	220	-	1080	kΩ	
VGH Power consumption	I _{VGH}	Note ⁽¹⁾	-	50	250	μA	-
VGL Power consumption	I _{VGH}	Note ⁽¹⁾	-	-50	-250	μA	-
VCC Power consumption	I _{VCC}	Note ⁽¹⁾	-	15	100	μA	-

Note 1: Power consumption with the following condition: Output no load, VGH=25V, VGL=-15V, VCC=3.3V, V_{IH} =VCC, V_{IL}=GND, F_{clk} = 50 KHz, OE = VIL, XON= VIH.

Note 2: All input except XON, SEL1, SEL0, FCTRL

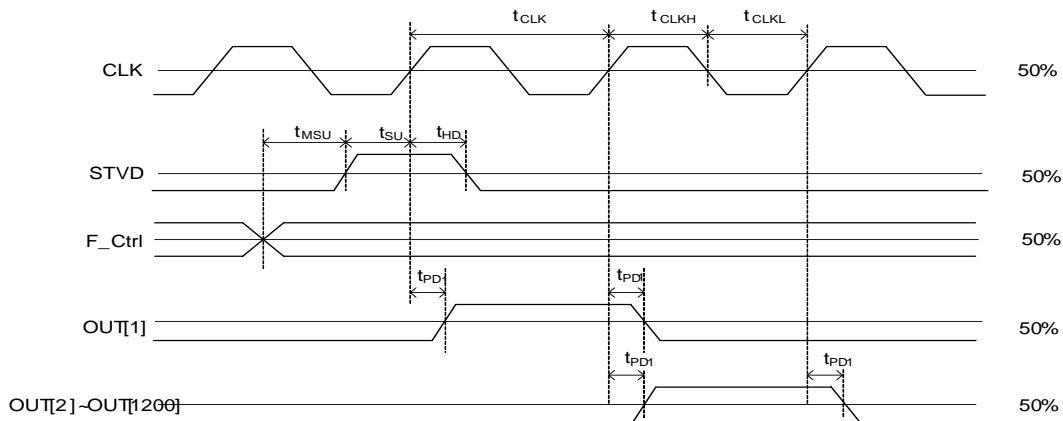
6.4. AC Characteristics

AC Characteristics (VGH = 25V, VGL = -15V, VCC = 3.3V/1.8V, VGND = 0V, Ta = 25°C)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
CLK period	t_{CLK}	-	5	-	-	μs
CLK pulse width	t_{CLKH}, t_{CLKL}	50% duty cycle	2.5	-	-	μs
OE pulse width	t_{WOE}	VCC=1.7V~2.3V	1.3	-	-	μs
		VCC=2.3V~3.6V	1	-	-	μs
XON pulse width	t_{WXAO}	-	100	-	-	μs
Data setup time	t_{SU}	-	0.7	-	-	μs
Data hold time	t_{HD}	-	0.7	-	-	μs
CLK to output delay time	t_{PD1}	CL=300pF, VCC=1.7V~2.3V	-	-	1.5	μs
		CL=300pF, VCC=2.3V~3.6V	-	-	1.2	μs
Start pulse output delay time	t_{PD2}	CL=30pF, VCC=1.7V~2.3V	-	-	1.3	μs
		CL=30pF, VCC=2.3V~3.6V	-	-	1	μs
OE to output delay time	t_{PD3}	CL=300pF, VCC=1.7V~2.3V	-	-	1.3	μs
		CL=300pF, VCC=2.3V~3.6V	-	-	1	μs
XON to output delay time	t_{PD4}	CL=300pF	-	-	100	μs
F_Ctrl setup time	t_{MSU}	-	1.0	-	-	μs
F_Ctrl hold time	t_{MHD}	-	1.0	-	-	μs

Note 1: The measurement point for all of above signals is at 50% of input/output amplitude.

6.5. Timing Waveform



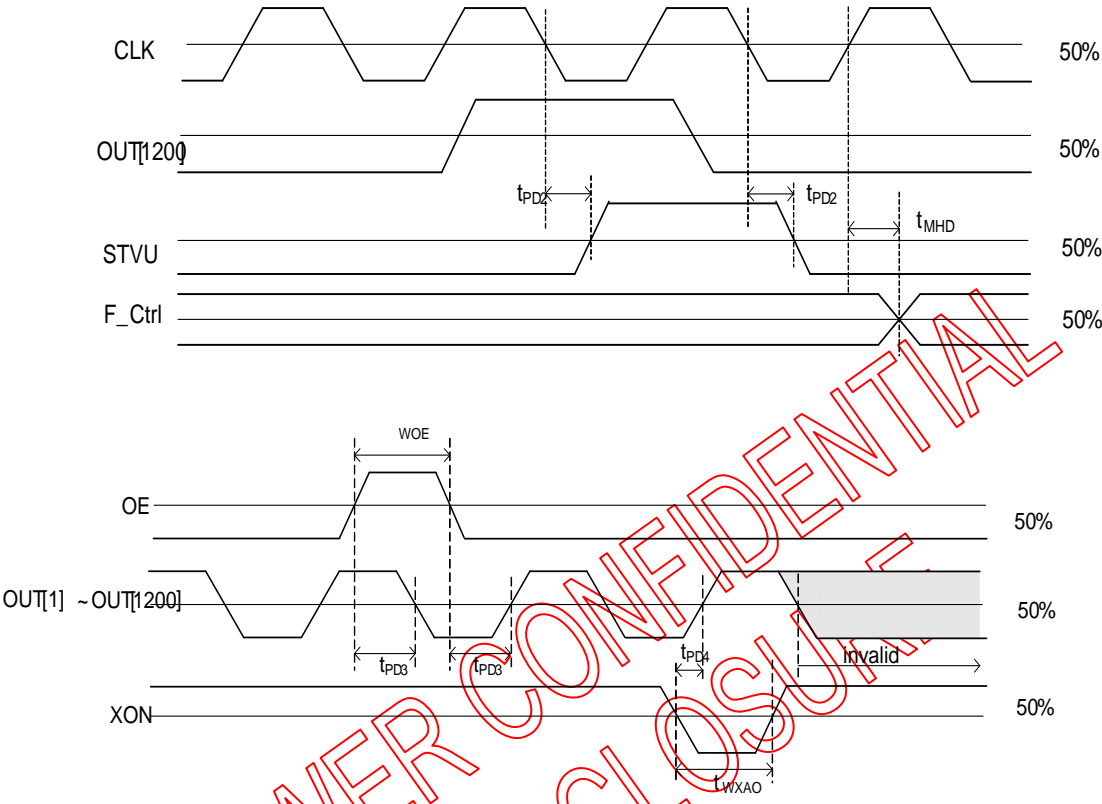


Figure 5. timing waveform

6.6. Operation Timing

UD="H"



Figure 6. Example of input/output timing (UD = H with OE and XON)

UD="L"

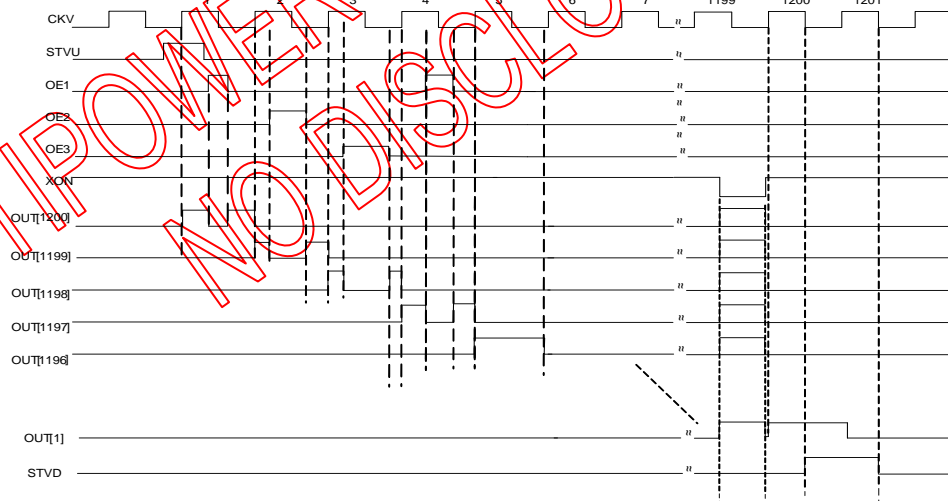
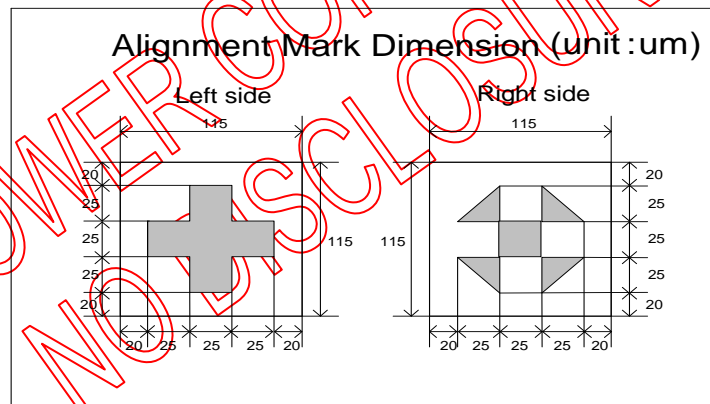
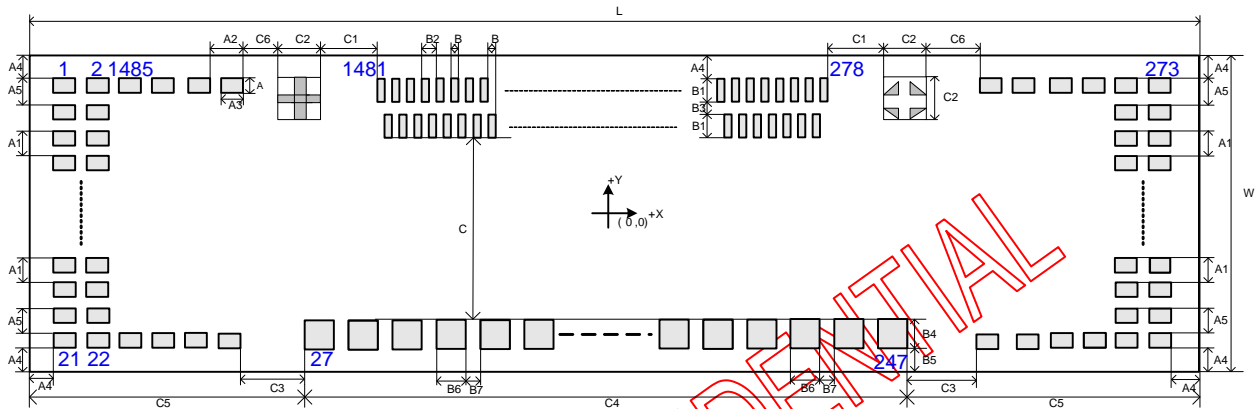


Figure 7. Example of input/output timing (UD = H with OE and XON)

7. CHIP OUTLINE DIMENSIONS AND ALIGNMENT MARK



Symbol	Dimensions	Symbol	Dimensions	Symbol	Dimensions
A	32	B2	36	C2	115
A1	52	B3	25	C3	208
A2	90	B4	70	C4	22080
A3	70	B5	57	C5	785
A4	57	B6	80	C6	89
A5	54	B7	20	L	23650
B	18	C	291	W	670
B1	85	C1	199	Unit : um	

Pad #	Pad Name	Pad Coordinate	
		X	Y
1441	OUT[1162]	-10116	235.5
1442	OUT[1163]	-10134	125.5
1443	OUT[1164]	-10152	235.5
1444	OUT[1165]	-10170	125.5
1445	OUT[1166]	-10188	235.5
1446	OUT[1167]	-10206	125.5
1447	OUT[1168]	-10224	235.5
1448	OUT[1169]	-10242	125.5
1449	OUT[1170]	-10260	235.5
1450	OUT[1171]	-10278	125.5
1451	OUT[1172]	-10296	235.5
1452	OUT[1173]	-10314	125.5
1453	OUT[1174]	-10332	235.5
1454	OUT[1175]	-10350	125.5
1455	OUT[1176]	-10368	235.5
1456	OUT[1177]	-10386	125.5
1457	OUT[1178]	-10404	235.5
1458	OUT[1179]	-10422	125.5
1459	OUT[1180]	-10440	235.5
1460	OUT[1181]	-10458	125.5
1461	OUT[1182]	-10476	235.5
1462	OUT[1183]	-10494	125.5
1463	OUT[1184]	-10512	235.5
1464	OUT[1185]	-10530	125.5
1465	OUT[1186]	-10548	235.5
1466	OUT[1187]	-10566	125.5
1467	OUT[1188]	-10584	235.5
1468	OUT[1189]	-10602	125.5
1469	OUT[1190]	-10620	235.5
1470	OUT[1191]	-10638	125.5
1471	OUT[1192]	-10656	235.5
1472	OUT[1193]	-10674	125.5
1473	OUT[1194]	-10692	235.5
1474	OUT[1195]	-10710	125.5
1475	OUT[1196]	-10728	235.5
1476	OUT[1197]	-10746	125.5
1477	OUT[1198]	-10764	235.5
1478	OUT[1199]	-10782	125.5
1479	OUT[1200]	-10800	235.5
1480	OUT[1201]	-10818	125.5
1481	PATN3L	-10836	235.5
1482	XONL	-11283	262
1483	XONL	-11373	262
1484	F_CTRLL	-11463	262
1485	F_CTRLL	-11553	262
1486	AL_MARK_L	-11101.5	280.5
1487	AL_MARK_R	11101.5	280.5

9. DEFINITIONS

9.1 Data Sheet Status

Preliminary Data Sheet	This data sheet contains preliminary data; supplementary data may be published later.
Data Sheet	This data sheet contains final product specifications.

Contents in the document are subject to change without notice.

9.2 Life Support Application

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. fitipower customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify fitipower for any damages resulting from such improper use or sale.

10 REVISION HISTORY

Revision	Content	Page	Date
1.0	New Issue		2012/11/07
1.1	(1) Add VCC Rating = 1.7~2.3V application (2) Modify ELECTRICAL SPECIFICATION (VGL Operating Range) (3) Modify DC Characteristics (Pull high / low resistance) (4) Modify AC Characteristics (t_{CLK} , t_{WOE} , t_{PD1} , t_{PD2} , t_{PD3} , t_{PD4})	2,12,13,14	2013/05/30