DATA SHEET

(DOC No. HX8238-D-DS)

HX8238-D

960 x 240 TFT LCD Single Chip Digital Driver

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List of Contents

List of Figures

1. General Description

The HX8238-D is a single chip controller and driver LSI that integrates the power circuit. It can drive a maximum 960x240 dot graphics on a-TFT panel displays in 16M colors with dithering.

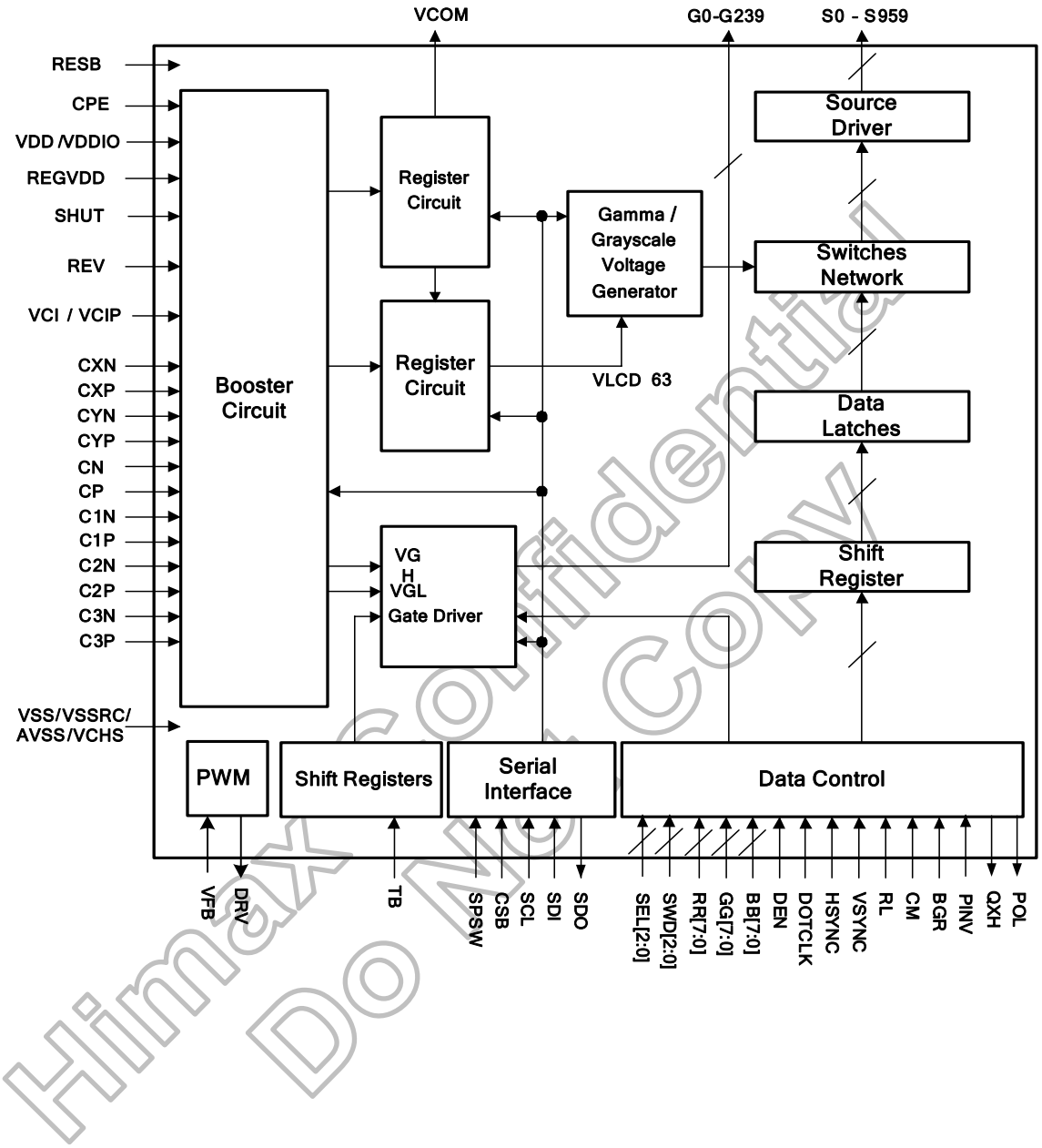
The HX8238-D has a low-voltage operation, 1.6 min voltage. In addition, The HX8238-D is equipped with a DC-DC converter control circuit that generates the supply voltage for source and gate drivers with minimum external components. A common voltage generation circuit is included to drive the TFT-display counter electrode. An integrated gamma control circuit is also included that can be adjusted by software commands to provide maximum flexibility and optimal display quality.

The HX8238-D is suitable for any medium-sized or small portable battery-driven product requiring long-term driving capabilities, such as Digital Still Cameras.

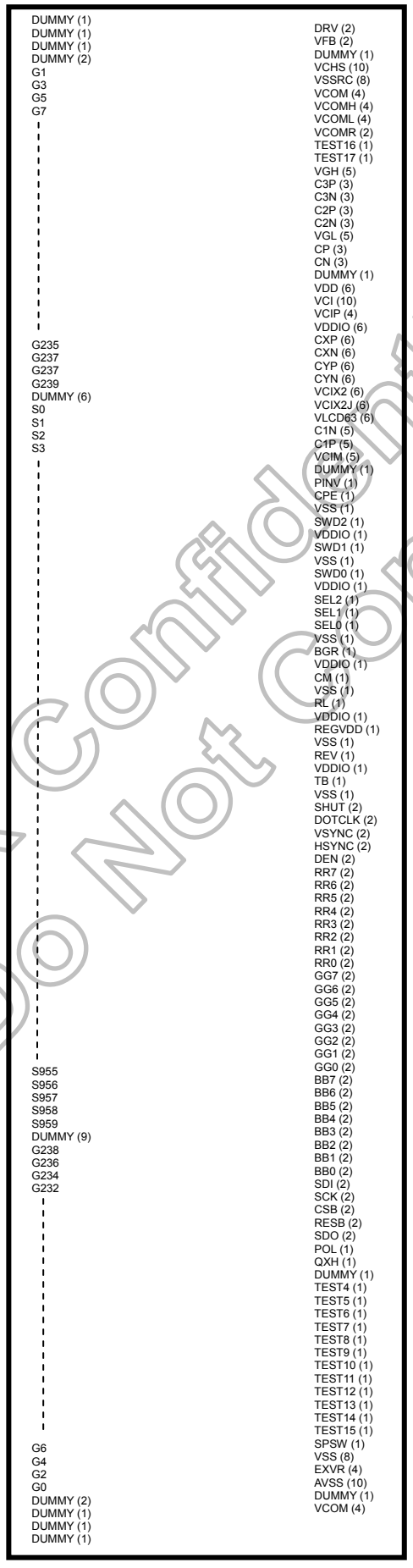
2. Features

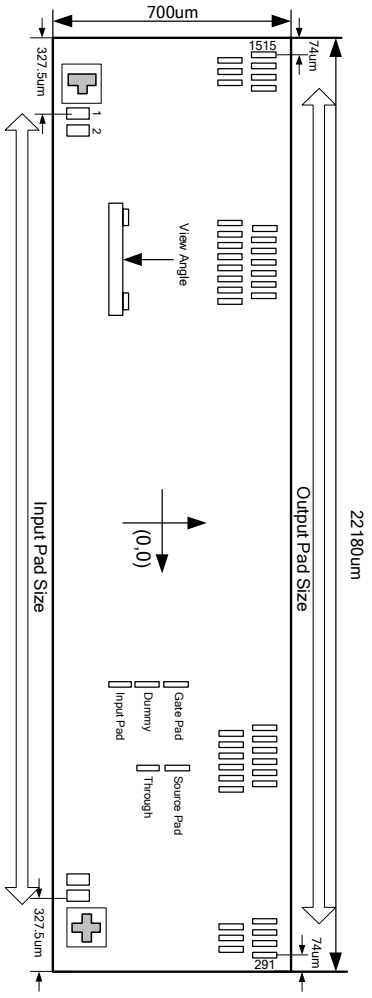
- 960 x 240 graphics display a-TFT panel controller/driver for 16M colors with dithering
- Support digital 8-bit serial/24-bit parallel RGB and CCIR601/656 input mode
- Power supply:
  - VDD=1.8V to 2.5V (non-regulated input for logic)
  - VDDIO=1.8V to 3.6V (regulated input for logic)
  - VCI=2.5V to 3.6V (power supply for internal analog circuit)
- Maximum gate driving output voltage: 30Vp-p
- Source driving output voltage: 0V to 5V
- Low current sleep mode and 8-color display mode for power saving
- Display size: 960 x 240
- Support Line and Frame inversion
- Support Contrast/Brightness control
- Source and gate scan direction control
- On-chip voltage generator
- On-chip DC-DC converter up to 6x / -6x
- Programmable gamma correction curve
- Non-Volatile Memory (OTP) for VCOM calibration
- Programmable common electrode voltage amplitude and level for Cs on common structure only
- PWM function to generate power for backlight control
- COG package

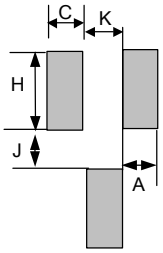
3. Block Diagram

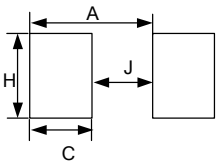


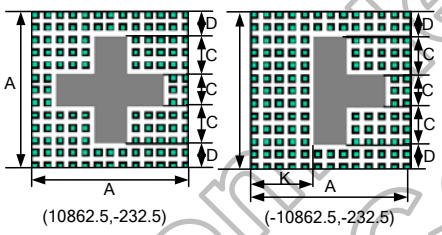
4. Pin Assignment











Output Pad	Symbol	Size
Bump pitch	A	18um
Bump width	C	18um
Bump height	H	85um
Bump gap 1 (Vertical)	J	45um
Bump gap 2 (Horizontal)	K	18um
Bump area	C x H	1530um^2

Input Pad	Symbol	Size
Bump pitch	A	75um
Bump width	C	50um
Bump height	H	80um
Bump gap 1 (Vertical)	J	25um
Bump area	C x H	4000um^2

Alignment Mark	Symbol	Size
Alignment mark size	A	105um
Clearance gap 1	D	15um
Clearance gap 2	K	40um
Alignment mark width	C	25um
Alignment area	A x A	11025um^2

Die Size approximately: 22180x700um^2
Bump Height : 15um +/- 3 um or 9um +/- 2 um
Bump Height Co-palanarity within Die: < 2µm
Bump Roughness:< 2µm with Rim
Hardness: 60 ± 15 Hv
Shear Stress: >4.5 g/mil2

Figure 4. 1: HX8238-D die floor plan (Bump face up)

5. Pin Description

Name	I/O	Function	Description
CM	Input	Logic Control	Input pin to select 16M-colors with dithering or 8-color display mode. After entered 8-color display mode, the driver will switch to Frame-Inversion-Mode, and only MSB of the data Red, Green and Blue will be considered. -Connect to VDDIO for 8-color display mode. -Connect to VSS for 16M-color with dithering display mode.
RR [7:0] GG [7:0] BB [7:0]	Input	Graphic Display Data	Graphic Data Input Pins. Internal pull low. -RR [7:0]: Red Data - 8-bit. -GG [7:0]: Green Data - 8-bit. -BB [7:0]: Blue Data - 8-bit. For 8 bit interface, only RR[7:0] are used. For unused pins, please connect to VSS or floating.
DEN	Input	Display Timing Signals	Display enable pin from controller. Internal pull high. Connect to VDDIO or floating if not used.
VSYNC			Frame synchronization signal. Internal pull high. -Fixed to VDDIO or floating if not used.
HSYNC			Line synchronization signal. Internal pull high. -Fixed to VDDIO or floating if not used.
DOTCLK			Dot-clock signal and oscillator source. A non-stop external clock must be provided to that pin even at front or black porch non-display period.
SHUT	Input	Logic Control	Display shut down pin to put the driver into sleep mode. A sharp falling edge must be provided to such pin when IC power on. Internal pull low. -Connect to VDDIO for sleep mode. -Connect to VSS for normal operating mode. (Refer to Power Up Sequence.)
RL	Input	Panel Mapping Control	Input pin to select the Source driver data shift direction. -Connect to VDDIO for display first RGB data at S0-S2. -Connect to VSS for display first RGB data at S959-S957.
TB			Input pin to select the Gate driver scan direction. -Connect to VSS for Gate scan from G239 to G0 (reverse scan). -Connect to VDDIO for Gate scan from G0 to G239 (normal scan).
BGR			Input pin to select the color mapping. Only for parallel RGB. -Connect to VDDIO for Blue-Green-Red mapping. -Connect to VSS for Red-Green-Blue mapping. (See S0-S959 pin description for details.)
REV			Input pin to select the display reversion. -Connect to VDDIO mapping data '0' to maximum pixel voltage for normally white panel. -Connect to VSS for mapping data '0' to minimum pixel voltage for normally black panel.
SWD[2:0]			Input pin to define color filter type. References register R04h.
SEL[2:0]			Input pin to select input interface mode. References register R04h. These pins are internal pull low.
CPE			Input pin to enable internal charge pump circuit. Internal pull high. -Connect to VDDIO to enable internal charge pump VCIM, VGH, VGL, VCIX2 and VCOM. -Connect to VSS to disable internal charge pump VGH, VGL, VCIX2 and VCOM.
QXH	Output		Data sequence control pin, this pin toggle each line under delta panel, keep floating if not used.
POL			Polarity signal to monitor VCOM signal, keep floating if not used.
PINV	Input	POL Control	Control the polarity of POL signal. Internal pull low. -Connect to VDDIO, POL phase is reversed with internal VCOM signal. -Connect to VSS, POL phase is same with internal VCOM signal.

Name	I/O	Function	Description
REGVDD	Input	Logic Control	Input pin to enable internal voltage regulation. -Connect to VDDIO if System Vdd > 2.5V. -Connect to VSS if 2.5V ≧ System Vdd ≧ 1.8V, internal regulator will be disabled.
RESB	Input	System Reset	System reset pin. Internal pull high. -Connect to VDDIO when not used. (Refer to Power Up Sequence.)
SPSW	Input	SPI Select	SPI table select. Internal pull high. -Connect to VSS for Secondary SPI Register. -Connect to VDDIO for Primary SPI Register.
CSB	Input	Serial Interface	Chip select pin of serial interface. Internal pull high. -Leave it OPEN when not used. (Refer to Serial Interface block.)
SCK			Clock pin of serial interface. Internal pull high. -Leave it OPEN when not used. (Refer to Serial Interface block.)
SDI			Data input pin in serial mode. Internal pull high. -Leave it OPEN when not used. (Refer to Serial Interface block.)
SDO	Output		Data output pin in serial mode. -Leave it OPEN when not used. (Refer to Serial Interface block.)
VDDIO	Power	Power Supply for Logic Circuits	Voltage input pin for I/O logic. -Connect to system Vdd.
VDD			Voltage input pin for internal logic. (a) REGVDD=VDDIO. Internal regulator will be on for 3.6V ≧ System Vdd ≧ 2.5V. VDD ~2V. (b) REGVDD=VSS. Internal regulator will be off for 2.5V ≧ System Vdd ≧ 1.8V. VDD=System Vdd.
VSS	Power	Ground of the Power Supply	System ground pin of the IC. -Connect to system ground.
AVSS			Grounding for analog circuit. -Connect to system ground.
VSSRC			Grounding for analog circuit. This pin requires a noise free path for providing accurate LCD driving voltages. -Connect to system ground.
VCHS			Grounding for booster circuit. -Connect to system ground.
VCI	Power	Power Supply for Analog Circuits	Booster input voltage pin. -Connect to voltage source between 2.5V to 3.6V.
VCIP			Voltage supply pin for analog circuit. This pin requires a noise free path for providing accurate LCD driving voltages. -Connect to same source of VCI.
VCIM	Output	Booster Voltages	Negative voltage of VCI. -Connect a capacitor for stabilization.
VCIX2			Equals to 2 x VCI. -Connect a capacitor for stabilization.
VCIX2J	Power	Voltage for Analog	This is the power supply used by on chip analog blocks and VGH/VGL dcdc.
EXVR	Input	External Reference	External reference of internal Gamma resistor. -Connect to VSS.
VCOMR			This pin provides voltage reference for internal voltage regulator when register VDV[6:0] of Power Control 3 set to “01111XX”. -Connect to an external voltage source for reference.
VCOMH	Output	Voltages for VCOM Signal	This pin indicates a HIGH level of VCOM generated in driving the VCOM alternation. -Connect a capacitor for stabilization.
VCOML			This pin indicates a LOW level of VCOM generated in driving the VCOM alternation. -Connect a capacitor for stabilization.

Name	I/O	Function	Description
VLCD63	Output	LCD Driving Voltages	Internal generated power for source driver. -Connect a capacitor for stabilization.
VGH			A positive power output pin for gate driver. -Connect a capacitor for stabilization.
VGL			A negative power output pin for gate driver. -Connect a capacitor for stabilization.
CP	Input	Booster and Stabilization Capacitors	-Connect a capacitor to CN.
CXP			-Connect a capacitor to CXN.
CYP			-Connect a capacitor to CYN.
C1P			-Connect a capacitor to C1N.
C2P			-Connect a capacitor to C2N.
C3P			-Connect a capacitor to C3N.
CN			-Connect a capacitor to CP.
CXN			-Connect a capacitor to CXP.
CYN			-Connect a capacitor to CYP.
C1N			-Connect a capacitor to C1P.
C2N			-Connect a capacitor to C2P.
C3N			-Connect a capacitor to C3P.
DRV	Output	PWM control	Power transistor gate signal for the boost converter, keep floating if not used.
VFB	Input		Main boost regulator feedback input. Connect feedback resistive divider to GND. FB threshold is 0.6 V nominal.
TEST4~5	Input	IC Testing Signal	Test pin of the internal circuit. Leave it connect to ground.
TEST6~17	Output	IC Testing Signal	Test pin of the internal circuit. Leave it OPEN.
VCOM	Output	LCD Driving Signals	A power supply for the TFT-display common electrode, keep floating if not used.
G0-G239			Gate driver output pins, keep floating if not used. These pins output VGH, VGL level.
S0-S959			Source driver output pins, keep floating if not used. S (3n): display Red if BGR=LOW, Blue if BGR=HIGH. S (3n+1): display Green. S (3n+2): display Blue if BGR=LOW, Red if BGR=HIGH.
DUMMY	-	-	Floating pins and no connection inside the IC. These pins can be shorted together or connect to any signal.

6. Block Function Description

6.1 Serial interface

The SPI is available through the chip select line (CSB), serial transfer clock line (SCK), serial data input (SDI), and serial data output (SDO).

The Driver IC recognizes the start of data transfer at the falling edge of CSB input to initiate the transfer of start byte. It recognizes the end of data transfer at the rising edge of CSB input. The Driver IC is selected when the 6-bit chip address in the start byte transferred from the transmission device and the 6-bit device identification code assigned to the Driver IC are compared and both 6-bit data correspond. The identification code must be 011100(Primary SPI Register) or 011101(Secondary SPI Register). Two different chip addresses must be assigned to the Driver IC because the seventh bit of the start byte is assigned to a register select bit (RS). When RS = 0, index register write or status read is executed. When the RS=1, instruction write. The eighth bit of the start byte is to specify read or write (R/W bit). The data are received when the R/W bit is 0, and are transmitted when the R/W bit is 1.

After receiving the start byte, the Driver IC starts to transmit or receive data by byte. The data transmission adopts a format by which the MSB is first transmitted (9th SCK started). All Driver IC instructions consist of 16 bits and they are executed internally after two bytes are transmitted with the MSB first (IB15 to 0---9th ~24th SCK).

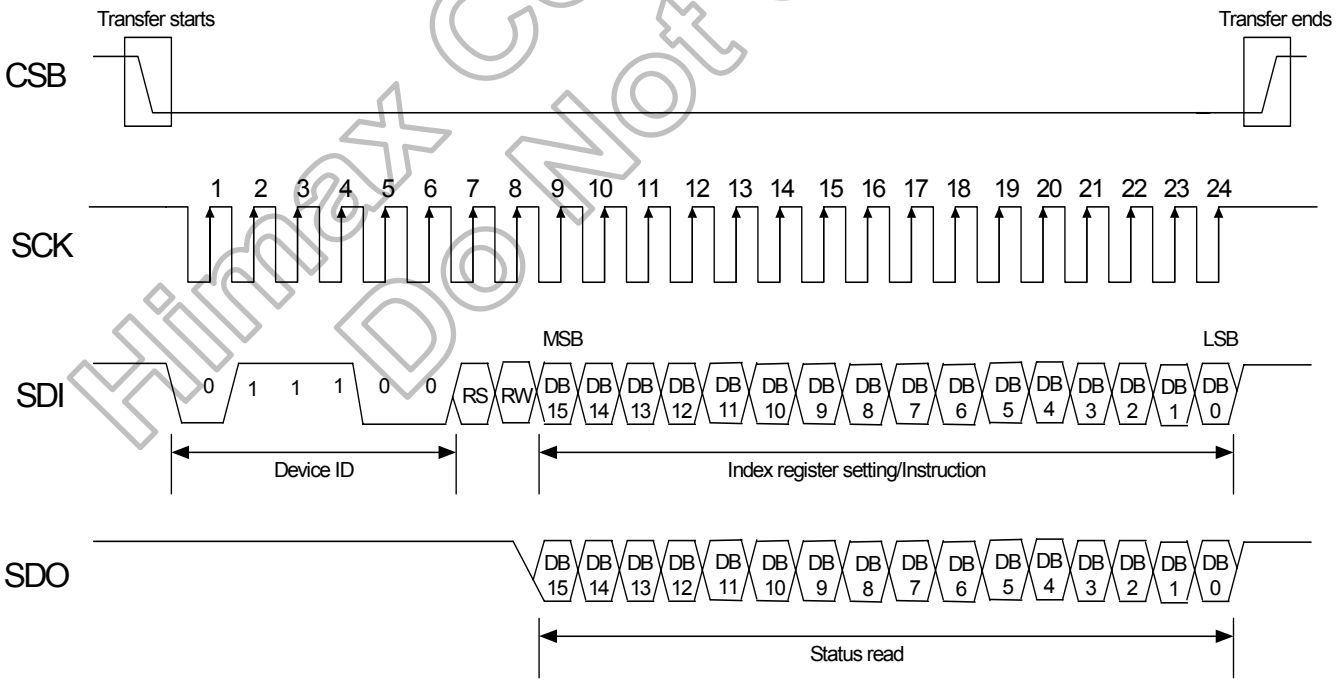


Figure 6. 1: SPI timing

6.2 Data control

The display data and frame position information from the controller is synchronized with the Gate Drive circuit and shift registered for the Source Driver circuit.

6.3 Gamma/Grayscale voltage generator

The grayscale voltage circuit generates a LCD driver circuit that corresponds to the grayscale levels as specified in the grayscale gamma-adjusting resistor. 16M colors with dithering possible colors can be displayed.

6.4 Boost and regulator circuit

These two functional blocks generate the voltage of VGH, VGL, VCOMH, VCOML and VLCD63, which are necessary for operating a TFT LCD.

6.5 PWM boost converter

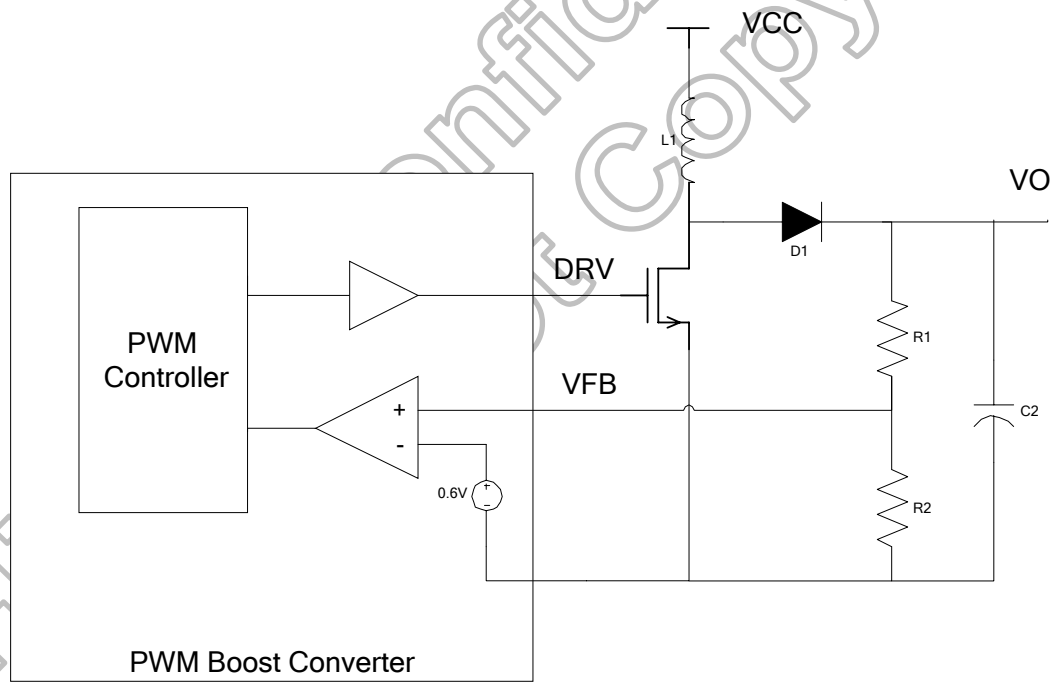


Figure 6. 2

When set PWMS=0, internal PWM function is enabled. The internal reference voltage is adjustable by FB[2:0] in R05h. By adjusting the voltage, you can get different VO to meet your system application.

When set PWMS=1, HX8238-D will send the enable signal from DRV pin to control external LED driver. The enable control signal can be adjusted the duty cycle by DUTY[7:0] in R08h, the duty cycle range is from 1/256 to 256/256. And it also can be adjustable the frequency by PWMF[3:0] in R08h, the frequency range is from 100Hz to 100 KHz.

6.6 Shift register

The shift registers control the direction of line scanning of source.

6.7 Data latches

This block is a series of latches carrying the display signal information. These latches hold the data, which will be fed to the Source Driver to output the required voltage level.

6.8 Aging mode

If only DOTCLK is sent into driver IC without VSYNC, HSYNC, and DEN signals, HX8238-D will enter Aging Mode after power on. In Aging Mode, the display will show Black, White, Red, Green, and Blue images in series automatically.

6.9 Reset circuit

This block is integrated into the Interface Logic which includes Power on Reset circuitry and the hardware reset pin, /RES. Both of these having the same reset function. Once the /RES pin receives a negative reset pulse, all internal circuitry will start to initialize. The minimum pulse width for completing the reset sequence is 10μs. The status of the chip after reset is given by.

7. 3-Wire Serial Port Interface

7.1 Primary register command table

Reg#	Register	R/W	R/S	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
SR	Status Read	1	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0
R01h	Driver output control	0	1	0	RL	REV	PINV	BGR	SM	TB	CPE	0	0	0	0	0	0	0	0
R02h	LCD driver AC control	0	1	0	0	0	0	0	0	B/C	0	0	0	0	0	0	0	0	0
R03h	Power control (1)	0	1	DCT3	DCT2	DCT1	DCT0	BTF	BT2	BT1	BT0	DC3	DC2	DC1	DC0	AP2	AP1	AP0	0
R04h	Data and color filter control	0	1	0	0	0	0	0	PALM	BLT1	BLT0	OEA1	OEA0	SEL2	SEL1	SEL0	SWD2	SWD1	SWD0
R05h	Function control	0	1	GHN	XDK	GDIS	LPF	DEP	CKP	VSP	HSP	DEO	DIT	0	PWM	0	FB2	FB1	FB0
R06h	Reserved	Reserved																	
R08h	LED control	0	1	0	0	0	PWMS	PWMF3	PWMF2	PWMF1	PWMF0	DUTY7	DUTY6	DUTY5	DUTY4	DUTY3	DUTY2	DUTY1	DUTY0
R0Ah	Contrast/ Brightness control	0	1	0	BR6	BR5	BR4	BR3	BR2	BR1	BR0	0	0	0	CON4	CON3	CON2	CON1	CON0
R0Bh	Frame cycle control	0	1	NO1	NO0	SDT1	SDT0	0	EQ2	EQ1	EQ0	0	0	0	0	0	0	0	0
R0Dh	Power control (2)	0	1	0	VRC2	VRC1	VRC0	0	0	VDS1	VDS0	0	0	VRH5	VRH4	VRH3	VRH2	VRH1	VRH0
R0Eh	Power control (3)	0	1	0	0	1	VDV6	VDV5	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0
R0Fh	Gate scan starting Position	0	1	0	0	0	0	0	0	0	0	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
R16h	Horizontal Porch	0	1	XLIM8	XLIM7	XLIM6	XLIM5	XLIM4	XLIM3	XLIM2	XLIM1	XLIM0	0	0	0	0	0	0	0
R17h	Vertical Porch	0	1	STH1	STH0	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0
R1Eh	Power control (4)	0	1	0	0	0	0	0	0	0	0	nOTP	VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
R27h	Reserved	Reserved																	
R28h	Reserved	Reserved																	
R29h	Reserved	Reserved																	
R2Bh	Reserved	Reserved																	
R30h	γ control (1)	0	1	0	0	0	0	0	PKP 12	PKP 11	PKP 10	0	0	0	0	0	PKP 02	PKP 01	PKP 00
R31h	γ control (2)	0	1	0	0	0	0	0	PKP 32	PKP 31	PKP 30	0	0	0	0	0	PKP 22	PKP 21	PKP 20
R32h	γ control (3)	0	1	0	0	0	0	0	PKP 52	PKP 51	PKP 50	0	0	0	0	0	PKP 42	PKP 41	PKP 40
R33h	γ control (4)	0	1	0	0	0	0	0	PRP 12	PRP 11	PRP 10	0	0	0	0	0	PRP 02	PRP 01	PRP 00
R34h	γ control (5)	0	1	0	0	0	0	0	PKN 12	PKN 11	PKN 10	0	0	0	0	0	PKN 02	PKN 01	PKN 00
R35h	γ control (6)	0	1	0	0	0	0	0	PKN 32	PKN 31	PKN 30	0	0	0	0	0	PKN 22	PKN 21	PKN 20
R36h	γ control (7)	0	1	0	0	0	0	0	PKN 52	PKN 51	PKN 50	0	0	0	0	0	PKN 42	PKN 41	PKN 40
R37h	γ control (8)	0	1	0	0	0	0	0	PRN 12	PRN 11	PRN 10	0	0	0	0	0	PRN 02	PRN 01	PRN 00
R3Ah	γ control (9)	0	1	0	0	0	VRP 14	VRP 13	VRP 12	VRP 11	VRP 10	0	0	0	0	VRP 03	VRP 02	VRP 01	VRP 00
R3Bh	γ control (10)	0	1	0	0	0	VRN 14	VRN 13	VRN 12	VRN 11	VRN 10	0	0	0	0	VRN 03	VRN 02	VRN 01	VRN 00

Note: * means don't care
Software settings will override hardware pin (eg, BGR bits override BGR pin definition)

Table 7. 1: Command table (Primary register map)

7.2 Primary register default value

Reg#	Hex dode	Register bit value
R01h	XX00	RL=X, REV=X, PINV=X, BGR=X, SM="0", TB=X, CPE=X
R02h	0200	B/C="1"
R03h	6464	DCT="0110", BT="100", BTF="0", DC="0110", AP="010"
R04h	04XX	PALM="1", BLT="00", OEA=**Note**(2), SEL= X, SWD=X
R05h		GHN="1", XDK="0", GDIS="1", LPF="1", DEP="0", CKP="1", VSP=**Note**(2), HSP="0", DEO="1", DIT="1", PWM="0", FB="100"
R08h	06FF	PWMS="0", PWMF="0110", DUTY="11111111"
R0Ah	4008	BR="1000000", CON="01000"
R0Bh	D400	NO="11", SDT="01", EQ="100"
R0Dh	3229	VRC="011", VDS="10", VRH="101001"
R0Eh	1200	VDV="1001000"
R0Fh	0000	SCN="00000000"
R16h	9F80	XLIM="100111111"
R17h		STH="00", HBP=**Note**(2), VBP=**Note**(2)
R1Eh	005F	nOTP="0", VCM="1011111"
R30h	0000	PKP1="000", PKP0="000"
R31h	0407	PKP3="100", PKP2="111"
R32h	0202	PKP5="010", PKP4="010"
R33h	0000	PRP1="000", PRP0="000"
R34h	0505	PKN1="101", PKN0="101"
R35h	0003	PKN3="000", PKN2="011"
R36h	0707	PKN5="111", PKN4="111"
R37h	0000	PRN1="000", PRN0="000"
R3Ah	0904	VRP1="01001", VRP0="0100"
R3Bh	0904	VRN1="01001", VRN0="0100"

Note: (1) X means the bit is refer to the logic stage of the corresponding hardware pin
(2) The default values of the VSP、OEA、HBP、VBP are automatically set by SEL

Default Value auto setting			VSP	OEA[1:0]	HBP[6:0]	VBP[6:0]
SEL[2:0] = 000	NTSC		0	01	1000100	0010010
	PAL	PALM=0	0	01	1000100	0010010
		PALM=1				0010010
SEL[2:0] = 001	NTSC		0	01	1000100	0010010
	PAL	PALM=0	0	01	1000100	0010010
		PALM=1				0010010
SEL[2:0] = 010	NTSC		0	01	1000101	0010110
	PAL	PALM=0	0	10	1000101	0011100
		PALM=1				0011000
SEL[2:0] = 011	NTSC		0	01	1000100	0010110
	PAL	PALM=0	0	10	1000111	0011100
		PALM=1				0011000
SEL[2:0] = 100	NTSC		1	10	1000110	0010001
	PAL	PALM=0	1	10	1000110	0011000
		PALM=1				0010100
SEL[2:0] = 101	NTSC		1	10	1000101	0010001
	PAL	PALM=0	1	10	1001000	0011000
		PALM=1				0010100
SEL[2:0] = 110	NTSC		1	10	1000101	0010001
	PAL	PALM=0	1	10	1001000	0011000
		PALM=1				0010100
SEL[2:0] = 111	NTSC		1	10	1000110	0010001
	PAL	PALM=0	1	10	1000110	0011000
		PALM=1				0010100

Table 7. 2: Registers default value (Primary register map)

7.3 Primary register command description

Status read

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0

Figure 7. 1: Status read

The status read instruction reads the internal status of the HX8238-D.

L7–0: Indicate the driving raster-row position where the liquid crystal display is being driven.

Driver output control (R01h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	R L	REV	PINV	BGR	S M	T B	CPE	0	0	0	0	0	0	0	0

Figure 7. 2: Driver output control

CPE: When CPE=0, Vcim is not shut down, but VGH, VGL, VCOM and Vcix2 are shut down. When CPE=1, internal charge pump Vcim, VGH, VGL, VCOM and Vcix2 are enabled.

REV: Displays all character and graphics display sections with reversal when REV="0". Since the grayscale level can be reversed, display of the same data is enabled on normally white and normally black panels. Source output level is indicated below.

REV	RGB data	Source output level	
		VCOM="L"	VCOM="H"
1	00000H : 3FFFFH	V0 : V63	V63 : V0
0	00000H : 3FFFFH	V63 : V0	V0 : V63

Table 7. 3: Source output level

PINV: When PINV=0, POL output is same phase with internal VCOM signal. When PINV=1, POL output phase is reversed with VCOM signal.

BGR: Selects the <R><G><B> arrangement. When BGR="0" <R><G><B> color is assigned from S0.When BGR="1" <B><G><R> color is assigned from S0. Only for parallel RGB.

SM: Change the division of gate driver. When SM = "0", odd/even division (interlace mode) is selected. When SM="1", upper/lower division is selected. Select the division mode according to the mounting method.

TB: Selects the output shift direction of the gate driver. When TB="1", G0 shifts to G239. When TB = "0", G239 shifts to G0.

RL: Selects the output shift direction of the source driver. When RL="1", S0 shifts to S959 and <R><G><B> color is assigned from S0. When RL="0", S959 shifts to S0 and <R><G><B> color is assigned from S959. Set RL bit and BGR bit when changing the dot order of R, G and B.

Note: The default setting of register bits **REV**, **BGR**, **TB** and **RL** are defined by the logic stage of corresponding hardware pins. These bits will override the hardware setting once software command was sent to set the bits.

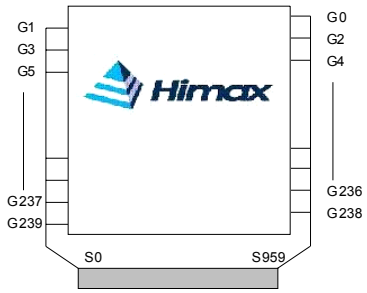
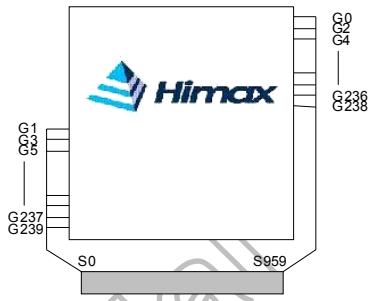
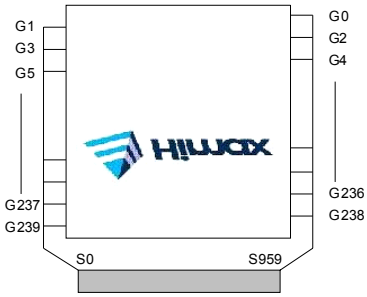
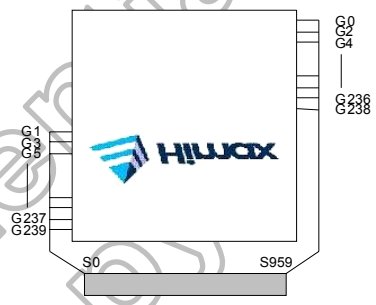
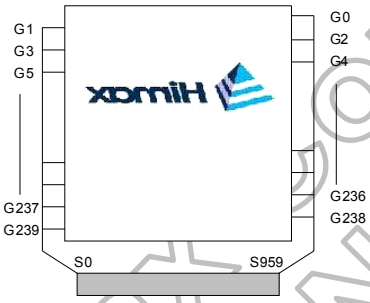
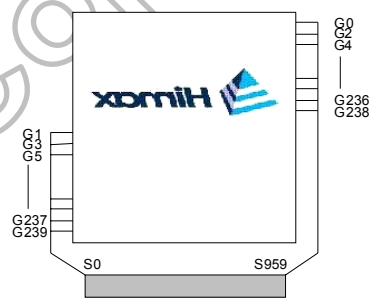
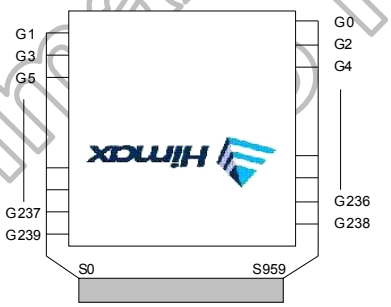
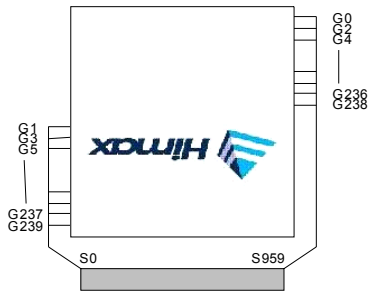
	SM=0	SM=1
TB=1 RL=1		
TB=0 RL=1		
TB=1 RL=0		
TB=0 RL=0		

Figure 7. 3: Scan direction & display

LCD-driving-waveform control (R02h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	B/C	0	0	0	0	0	0	0	0	0

Figure 7. 4 :LCD-driving-waveform control

B/C: When B/C=0, frame inversion of the LCD driving signal is enabled. When B/C=1, line inversion waveform is generated.

Power control 1 (R03h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	DCT3	DCT2	DCT1	DCT0	BTF	BT2	BT1	BT0	DC3	DC2	DC1	DC0	AP2	AP1	AP0	0

Figure 7. 5: Power control 1

DCT3-0: Set the step-up cycle of the step-up circuit for 8-color mode (CM=VDDIO). When the cycle is accelerated, the Vcim and Vcix2 be increased both driving ability of the step-up circuit and current consumption. Adjust the cycle taking into account the display quality and power consumption.
VGH and VGL are always fixed at the step-up cycle of Fline x 0.5.

DCT3	DCT2	DCT1	DCT0	Step-up cycle
0	0	0	0	Fline x 14
0	0	0	1	Fline x 12
0	0	1	0	Fline x 10
0	0	1	1	Fline x 8
0	1	0	0	Fline x 7
0	1	0	1	Fline x 6
0	1	1	0	Fline x 5
0	1	1	1	Fline x 4
1	0	0	0	Fline x 3
1	0	0	1	Fline x 2
1	0	1	0	Fline x 1
1	0	1	1	Fline x 0.5
1	1	0	0	Fline x 0.25
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

Note: Fline=horizontal frequency (Fline typ. 15KHz)

Table 7. 4: Step-up cycle

BT2-0 & BTF: Control the step-up factor of the step-up circuit. Adjust the step-up factor according to the power supply voltage to be used.

BTF	BT2	BT1	BT0	VGH output	VGL output
0	0	0	0	VCIX2j X 3	- (VCIX2j X 3) + VCI
0	0	0	1	VCIX2j X 3	- (VCIX2j X 2)
0	0	1	0	VCIX2 j X 3	- (VCIX2j X 3)
0	0	1	1	VCIX2j X 2 + VCI	- (VCIX2j X 2) - VCI
0	1	0	0	VCIX2j X 2 + VCI	- (VCIX2j X 2)
0	1	0	1	VCIX2j X 2 + VCI	- (VCIX2j X 2) + VCI
0	1	1	0	VCIX2j X 2	- (VCIX2j X 2)
0	1	1	1	VCIX2j X 2	- (VCIX2j X 2) + VCI
1	X	X	X	VCIX2j X 3	- VCIX2j

Table 7. 5: VGH and VGL booster ratio

DC3-0: Set the step-up cycle of the step-up circuit for 16M-colors with dithering mode (CM=VSS).
When the cycle is accelerated, the Vcim and Vcix2 be increased both driving ability of the step-up circuit and current consumption. Adjust the cycle taking into account the display quality and power consumption. VGH and VGL are always fixed at the step-up cycle of Fline x 0.5.

DC3	DC2	DC1	DC0	Step-up cycle
0	0	0	0	Fline x 14
0	0	0	1	Fline x 12
0	0	1	0	Fline x 10
0	0	1	1	Fline x 8
0	1	0	0	Fline x 7
0	1	0	1	Fline x 6
0	1	1	0	Fline x 5
0	1	1	1	Fline x 4
1	0	0	0	Fline x 3
1	0	0	1	Fline x 2
1	0	1	0	Fline x 1
1	0	1	1	Fline x 0.5
1	1	0	0	Fline x 0.25
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

Note: Fline=horizontal frequency (Fline Typ. 15KHz)

Table 7. 6: Step-up cycle

AP2-0: Adjust the amount of current from the stable-current source in the internal operational amplifier circuit. When the amount of current becomes large, the driving ability of the operational-amplifier circuits increase. Adjust the current taking into account the power consumption. During times when there is no display, such as when the system is in a sleep mode, set AP2-0="000" to halt the operational amplifier circuit and the step-up circuits to reduce current consumption.

AP2	AP1	AP0	Op-amp power
0	0	0	Least
0	0	1	Small
0	1	0	Small to medium
0	1	1	Medium
1	0	0	Medium to large
1	0	1	Large
1	1	0	Large to maximum
1	1	1	Maximum

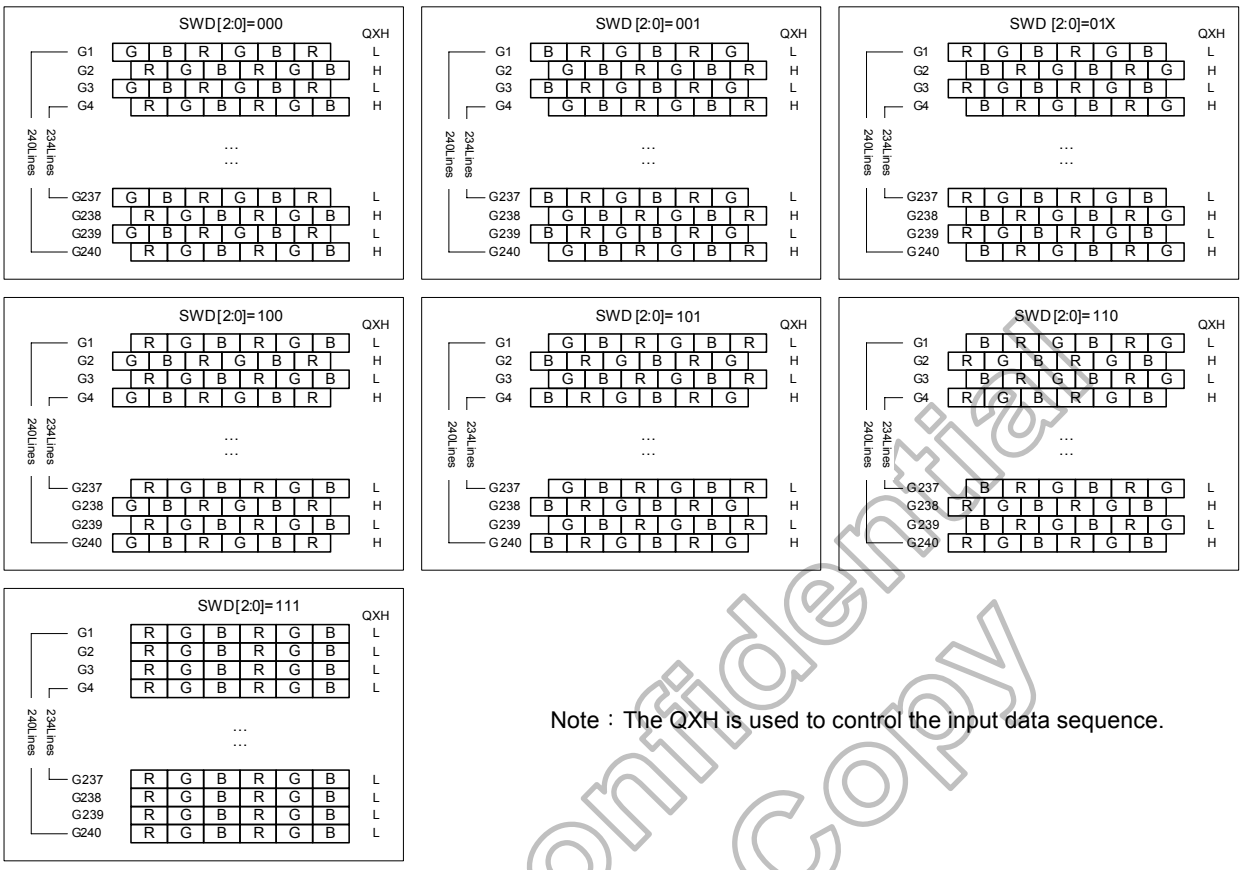
Table 7. 7: Op-amp power

Input data and color filter control (R04h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PALM	BLT1	BLT0	OEA1	OEA0	SEL2	SEL1	SEL0	SWD2	SWD1	SWD0

Figure 7. 6: Input data and color filter control

SWD2-0: Control and switch the relationship between the R, G, B data and color filter type.



Note：The QXH is used to control the input data sequence.

Table 7. 8: Color filter type

SEL2-0: Define the input interface mode.

SEL2	SEL1	SEL0	Format	Operating frequency
0	0	0	Parallel-RGB data format (only support stripe type color filter)	6.5MHz
0	0	1	Serial-RGB data format	19.5MHz
0	1	0	CCIR 656 data format (640RGB)	24.54MHz
0	1	1	CCIR 656 data format (720RGB)	27MHz
1	0	0	YUV mode A data format (Cr-Y-Cb-Y)	24.54MHz
1	0	1	YUV mode A data format (Cr-Y-Cb-Y)	27MHz
1	1	0	YUV mode B data format (Cb-Y-Cr-Y)	27MHz
1	1	1	YUV mode B data format (Cb-Y-Cr-Y)	24.54MHz

Input format	DOTCLK Freq (MHz)	Display data	Active area (DOTCLK)
YUV mode	24.54	640	1280
	27	720	1440

Table 7. 9: Interface type

OEA1-0: Odd/Even field advanced function.

OEA1	OEA0	
0	0	Display Start @ VBP delay for Odd field and @ ***VBP-1*** for Even field.
0	1	Display Start @ VBP delay for Odd field and @ ***VBP*** for Even field.
1	0	Display Start @ VBP delay for Odd field and @ ***VBP+1*** for Even field.
1	1	No use

Table 7. 10: Odd/Even field advanced function

BLT[1:0]: Set the initial power on black image insertion time.
00: 10 fields
01: 20 fields
10: 40 fields
11: 80 fields

PALM: Set the input data line number in PAL mode.
0: 280 lines
1: 288 lines

Function control (R05h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	GHN	XDK	GDIS	LPF	DEP	CKP	VSP	HSP	DEO	DIT	0	PWM	0	FB2	FB1	FB0

Figure 7. 7: Function control

FB2-0: Set PWM feedback level adjustment when PWMS=0.
000: 0.4V
001: 0.45V
010: 0.5V
011: 0.55V
100: 0.6V
101: 0.65V
110: 0.7V
111: 0.75V

PWM: When PWM=0, PWM function is disabled. When PWM=1, PWM function is enabled.

DIT: When DIT=0, dithering function is turned off. When DIT=1, dithering function is enabled.

DEO: When DEO=0, VSYNC/HSYNC are also needed in DE mode. Under this condition, vertical back porch is defined by VBP[6:0] and the horizontal first valid data is defined by DE signal. When DEO=1, only DEN signal is needed in DE mode.

HSP: When HSP=0, HSYNC is negative polarity. When HSP=1, HSYNC is positive polarity.

VSP: When VSP=0, VSYNC is negative polarity. When VSP=1, VSYNC is positive polarity.

CKP: When CKP=0, data is latched in CLK falling edge. When CKP=1, data is latched by CLK rising edge.

DEP: When DEP=0, DEN is negative polarity active. When DEP=1, DEN is positive polarity active.

LPF: When LPF=0, the low pass filter function in YUV mode is disabled. When LPF=1, the low pass filter function is YUV mode is enabled.

GDIS: When GDIS=0, VGL has no discharge path to VSS in standby mode. When GDIS=1, VGL will discharge to VSS in standby mode. When CPE=0, GDIS is fixed to 0, and you can't change it by SPI.

XDK: When XDK=0, VCIX2 is 2 stage pumping from VCI. (VCIX2=3 x VCI) When XDK=1, VCIX2 is 2 phase pumping from VCI. (VCIX2=2 x VCI)

GHN: When GHN=0, all gate outputs are forced to VGH. When GHN=1, gate driver is normal operation.

PWM control (R08h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	PWMS	PWMF3	PWMF2	PWMF1	PWMF0	DUTY7	DUTY6	DUTY5	DUTY4	DUTY3	DUTY2	DUTY1	DUTY0

Figure 7. 8: PWM for external LED driver control

PWMS: Select PWM function.
When PWMS=0, use internal PWM circuit. (Default)
When PWMS=1, use external LED driver, DRV pin outputs control signal.

PWMF3-0: Select control signal frequency when set PWMS=1. Adjust range from 100Hz to 100KHz. Default value=0110.

PWMF3	PWMF2	PWMF1	PWMF0	Enable signal frequency		
				Parallel RGB 6.5MHz	Serial RGB 19.5MHz	YUV/CCIR656 24.54/27MHz
0	0	0	0	DCLK / 2^8	DCLK / 3 / 2^8	DCLK / 2^8
0	0	0	1	DCLK / 2^8	DCLK / 3 / 2^8	DCLK / 2^9
0	0	1	0	DCLK / 2^8	DCLK / 3 / 2^8	DCLK / 2^{10}
0	0	1	1	DCLK / 2^9	DCLK / 3 / 2^9	DCLK / 2^{11}
0	1	0	0	DCLK / 2^{10}	DCLK / 3 / 2^{10}	DCLK / 2^{12}
0	1	0	1	DCLK / 2^{11}	DCLK / 3 / 2^{11}	DCLK / 2^{13}
0	1	1	0	DCLK / 2^{12}	DCLK / 3 / 2^{12}	DCLK / 2^{14}
0	1	1	1	DCLK / 2^{13}	DCLK / 3 /2^{13}	DCLK / 2^{15}
1	0	0	0	DCLK / 2^{14}	DCLK / 3 / 2^{14}	DCLK / 2^{16}
1	0	0	1	DCLK / 2^{15}	DCLK / 3 / 2^{15}	DCLK / 2^{17}
1	0	1	0	DCLK / 2^{16}	DCLK / 3 / 2^{16}	DCLK / 2^{18}
1	0	1	1	Reserved	Reserved	Reserved
1	1	0	0	Reserved	Reserved	Reserved
1	1	0	1	Reserved	Reserved	Reserved
1	1	1	0	Reserved	Reserved	Reserved
1	1	1	1	Reserved	Reserved	Reserved

Table 7. 11: LED driver control signal frequency

DUTY7-0: Select control signal duty cycle when set PWMS=1. Adjust range from 00h(duty cycle=1/256) to FFh(duty cycle=256/256). Default value is FFh.

Contrast/Brightness control (R0Ah)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	BR6	BR5	BR4	BR3	BR2	BR1	BR0	0	0	0	CON4	CON3	CON2	CON1	CON0

Figure 7. 9: Contrast/Brightness control

CON4-0: Display Contrast level adjustment. (0.125/step) Adjust range from 00h (level=0) to 1Fh (level=3.875). Default value is 08h (level=1).

BR6-0: Display Brightness level adjustment. (2/step) Adjust range from 00h (level=-128) to 7Fh(level=+126). Default value is 40h(level=0).

Frame cycle control (R0Bh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	NO1	NO0	SDT1	SDT0	0	EQ2	EQ1	EQ0	0	0	0	0	0	0	0	0

Figure 7. 10: Frame cycle control

NO1-0: Sets amount of non-overlap of the gate output.

NO1	NO0	Amount of non-overlap
0	0	1.5µs
0	1	3.0µs
1	0	4.5µs
1	1	6.0µs

Table 7. 12: Amount of non-overlap

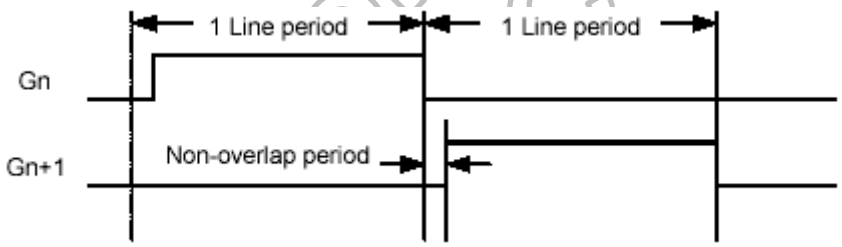


Figure 7. 11: NO timing diagram

SDT1-0: Set delay amount from the gate output signal falling edge to the source outputs.

SDT1	SDT0	Delay amount of the source output
0	0	1µs
0	1	3µs
1	0	5µs
1	1	7µs

Table 7. 13: Delay amount of source output

EQ2-0: Set the equalizing period.

EQ2	EQ1	EQ0	EQ period
0	0	0	No EQ
0	0	1	3µs
0	1	0	4µs
0	1	1	5µs
1	0	0	6µs
1	0	1	7µs
1	1	0	8µs
1	1	1	9µs

Table 7. 14: EQ period

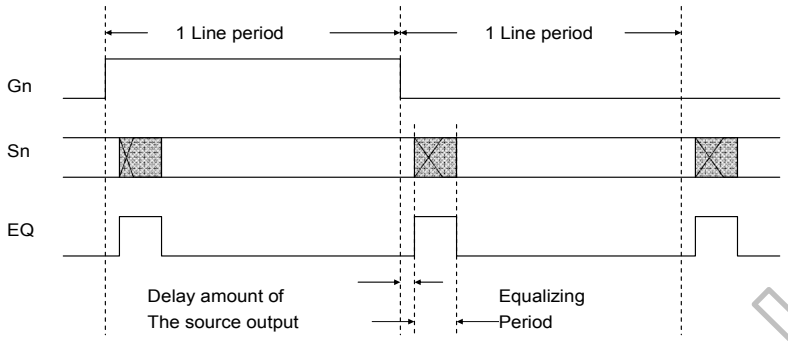


Figure 7. 12: EQ timing diagram

Power control 2 (R0Dh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	VRC2	VRC1	VRC0	0	0	VDS1	VDS0	0	0	VRH5	VRH4	VRH3	VRH2	VRH1	VRH0

Figure 7. 13 Power control 2

VRC[2:0]: Set the VCIX2 charge pump voltage clamp.
VRC[2:0]=000, 5.1V
VRC[2:0]=001, 5.3V
VRC[2:0]=010, 5.5V
VRC[2:0]=011, 5.7V
VRC[2:0]=100, 5.9V
VRC[2:0]=101, reserved
VRC[2:0]=110, reserved
VRC[2:0]=111, reserved

VDS[1:0]: Set the VDD regulator voltage if pin “REGVDD” is set to VDDIO.
VDS[1:0]=00, 1.8V
VDS[1:0]=01, 2V
VDS[1:0]=10, 2.2V
VDS[1:0]=11, 2.5V

VRH5-0: Set amplitude magnification of VLCD63. These bits amplify the VLCD63 voltage 2.464 to 4.456 times the Vref voltage set by VRH5-0.

VRH5	VRH4	VRH3	VRH2	VRH1	VRH0	VLCD63 voltage
0	0	0	0	0	0	Vref x 2.456
0	0	0	0	0	1	Vref x 2.488
0	0	0	0	1	0	Vref x 2.520
0	0	0	0	1	1	Vref x 2.552
0	0	0	1	0	0	Vref x 2.584
0	0	0	1	0	1	Vref x 2.616
0	0	0	1	1	0	Vref x 2.648
0	0	0	1	1	1	Vref x 2.680
0	0	1	0	0	0	Vref x 2.712
0	0	1	0	0	1	Vref x 2.744
0	0	1	0	1	0	Vref x 2.776
0	0	1	0	1	1	Vref x 2.808
0	0	1	1	0	0	Vref x 2.840
0	0	1	1	0	1	Vref x 2.872
0	0	1	1	1	0	Vref x 2.904
0	0	1	1	1	1	Vref x 2.936
0	1	0	0	0	0	Vref x 2.968
0	1	0	0	0	1	Vref x 3.000
0	1	0	0	1	0	Vref x 3.032
0	1	0	0	1	1	Vref x 3.064
0	1	0	1	0	0	Vref x 3.096
0	1	0	1	0	1	Vref x 3.128
0	1	0	1	1	0	Vref x 3.160
0	1	0	1	1	1	Vref x 3.192
0	1	1	0	0	0	Vref x 3.224
0	1	1	0	0	1	Vref x 3.256
0	1	1	0	1	0	Vref x 3.288
0	1	1	0	1	1	Vref x 3.320
0	1	1	1	0	0	Vref x 3.352
0	1	1	1	0	1	Vref x 3.384
0	1	1	1	1	0	Vref x 3.416
0	1	1	1	1	1	Vref x 3.448

VRH5	VRH4	VRH3	VRH2	VRH1	VRH0	VLCD63 voltage
1	0	0	0	0	0	Vref x 3.480
1	0	0	0	0	1	Vref x 3.512
1	0	0	0	1	0	Vref x 3.544
1	0	0	0	1	1	Vref x 3.576
1	0	0	1	0	0	Vref x 3.608
1	0	0	1	0	1	Vref x 3.640
1	0	0	1	1	0	Vref x 3.672
1	0	0	1	1	1	Vref x 3.704
1	0	1	0	0	0	Vref x 3.736
1	0	1	0	0	1	Vref x 3.768
1	0	1	0	1	0	Vref x 3.800
1	0	1	0	1	1	Vref x 3.832
1	0	1	1	0	0	Vref x 3.864
1	0	1	1	0	1	Vref x 3.896
1	0	1	1	1	0	Vref x 3.928
1	0	1	1	1	1	Vref x 3.960
1	1	0	0	0	0	Vref x 3.992
1	1	0	0	0	1	Vref x 4.024
1	1	0	0	1	0	Vref x 4.056
1	1	0	0	1	1	Vref x 4.088
1	1	0	1	0	0	Vref x 4.120
1	1	0	1	0	1	Vref x 4.152
1	1	0	1	1	0	Vref x 4.184
1	1	0	1	1	1	Vref x 4.216
1	1	1	0	0	0	Vref x 4.248
1	1	1	0	0	1	Vref x 4.280
1	1	1	0	1	0	Vref x 4.312
1	1	1	0	1	1	Vref x 4.344
1	1	1	1	0	0	Vref x 4.376
1	1	1	1	0	1	Vref x 4.408
1	1	1	1	1	0	Vref x 4.440
1	1	1	1	1	1	Vref x 4.472

Note: Vref is the internal reference voltage equals to 1.25V.

Table 7. 15: VLCD63 voltage

Power control 3 (R0Eh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	VDV6	VDV5	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0

Figure 7. 14: Power control 3

VDV6-0: Set the alternating amplitudes of VCOM at the VCOM alternating drive. These bits amplify VCOM amplitude 0.6 to 1.2525 times the VLCD63 voltage. External voltage at VCOMR is referenced when VDV="01111xx". The maximum voltage of VCOMR is VCIX2.

VDV6	VDV5	VDV4	VDV3	VDV2	VDV1	VDV0	VCOM amplitude
0	0	0	0	0	0	0	VLCD63 x 0.6000
0	0	0	0	0	0	1	VLCD63 x 0.6075
0	0	0	0	0	1	0	VLCD63 x 0.6150
0	0	0	0	0	1	1	VLCD63 x 0.6225
0	0	0	0	1	0	0	VLCD63 x 0.6300
			:				: Step = 0.0075 :
0	1	1	1	0	1	0	VLCD63 x 1.0350
0	1	1	1	0	1	1	VLCD63 x 1.0425
0	1	1	1	1	*	*	Reference from external voltage (VCOMR)
1	0	0	0	0	0	0	VLCD63 x 1.0500
1	0	0	0	0	0	1	VLCD63 x 1.0575
			:				: Step = 0.0075 :
1	0	1	1	0	1	0	VLCD63 x 1.2450
1	0	1	1	0	1	1	VLCD63 x 1.2525
1	0	1	1	1	*	*	Reserved
1	1	*	*	*	*	*	Reserved

Table 7. 16: VCOM amplitude

Gate scan position (R0Fh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0

Figure 7. 15: Gate scan position

SCN7-0: Set the scanning starting position of the gate driver.

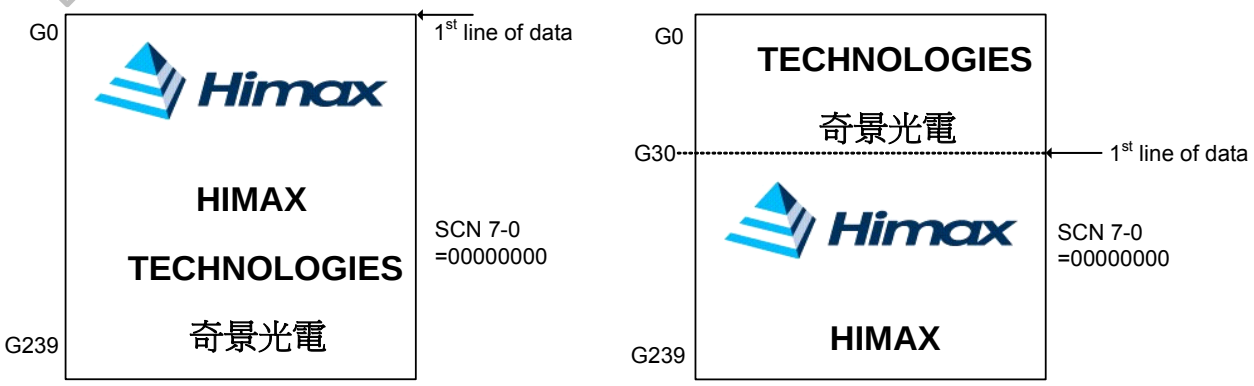


Figure 7. 16: Gate scan display position

Horizontal porch (R16h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	XLIM8	XLIM7	XLIM6	XLIM5	XLIM4	XLIM3	XLIM2	XLIM1	XLIM0	0	0	0	0	0	0	0

Figure 7. 17: Horizontal porch

XLIM8-0: Set the number of valid pixel per line.

XLIM8	XLIM7	XLIM6	XLIM5	XLIM4	XLIM3	XLIM2	XLIM1	XLIM0	No. of pixel per line
0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	0	1	0	3
				:					: Step=1 :
1	0	0	1	1	1	1	1	0	319
1	0	0	1	1	1	1	1	1	320
1	0	1	*	*	*	*	*	*	Reserved
1	1	*	*	*	*	*	*	*	Reserved

Table 7. 17: No. of pixel per line

Vertical porch (R17h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	STH1	STH0	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0

Figure 7. 18: Vertical porch

HBP6-0: Set the delay period from falling edge of HSYNC signal to first valid data. The pixel data exceed the range set by XLIM8-0 and before the first valid data will be treated as dummy data. The setting is only effective in SYNC mode timing.

HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	No. of clock cycle
0	0	0	0	0	0	0	Can't set.
0	0	0	0	0	0	1	Can't set.
0	0	0	0	0	1	0	Can't set.
0	0	0	0	0	1	1	Can't set.
0	0	0	0	1	0	0	Can't set.
0	0	0	0	1	0	1	Can't set.
0	0	0	0	1	1	0	Can't set.
0	0	0	0	1	1	1	Can't set.
0	0	0	1	0	0	0	Can't set.
0	0	0	1	0	0	1	9
			⋮				⋮ Step=1 ⋮
1	1	1	1	1	1	0	126
1	1	1	1	1	1	1	127

Table 7. 18: No. of clock cycle of clock

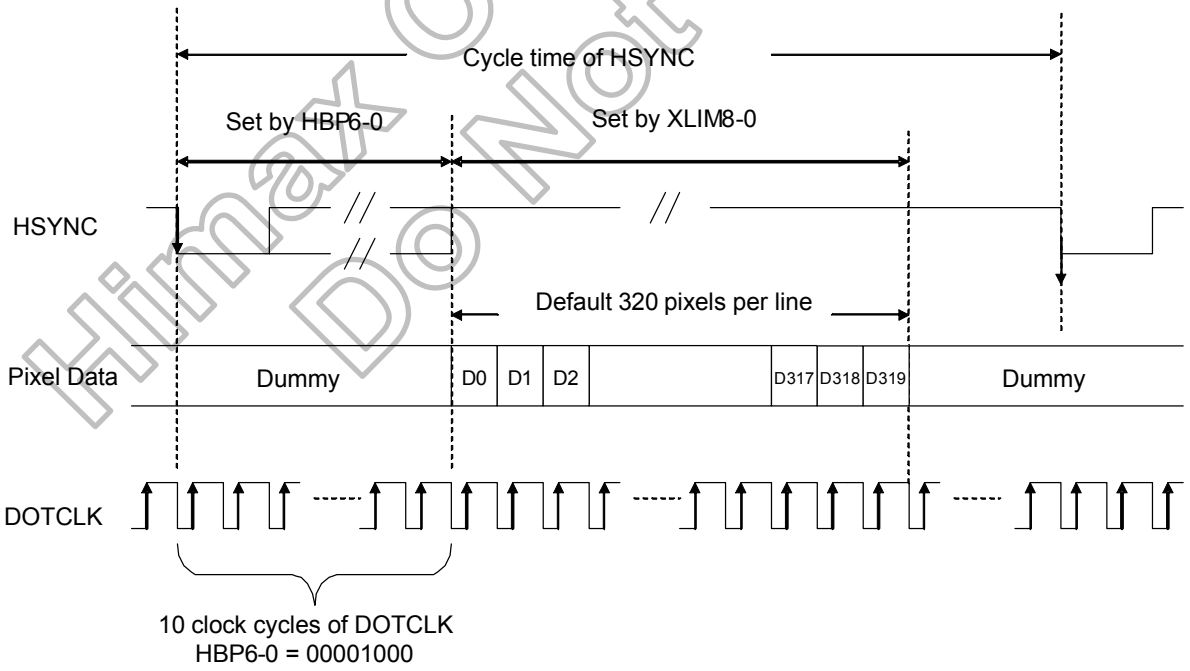


Figure 7. 19: No. of clock cycle of clock

STH1-0: Adjust the first valid data by dot clock. This setting is not valid in parallel RGB input interface.
STH=00: +0 dot clock
STH=01: +1 dot clock
STH=10: +2 dot clock
STH=11: +3 dot clock

VBP6-0: Set the delay period from falling edge of VSYNC to first valid line. The line data within this delay period will be treated as dummy line. The setting is only effective in SYNC mode timing.

VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	No. of clock cycle of HSYNC
0	0	0	0	0	0	0	Can't set.
0	0	0	0	0	0	1	Can't set.
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
0	0	0	0	1	0	0	4
			:				: Step=1 :
1	1	1	1	1	0	0	124
1	1	1	1	1	0	1	125
1	1	1	1	1	1	0	126
1	1	1	1	1	1	1	127

Table 7. 19: No. of clock cycle of HSYNC

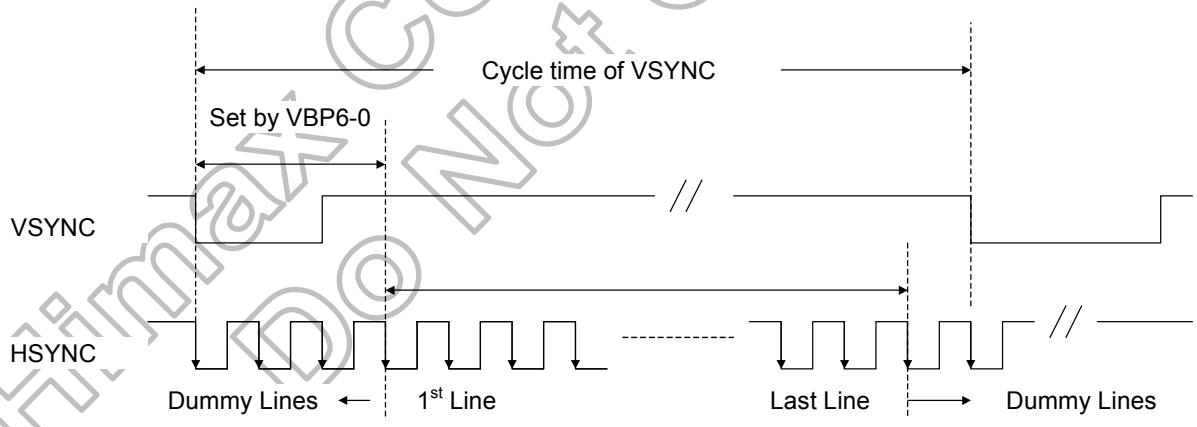


Figure 7. 20: No. of clock cycle of HSYNC

Power control 4 (R1Eh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	nOTP	VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0

Figure 7. 21: Power control 4

nOTP: nOTP=0, VCOM6-0 value is controlled by OTP memory. (Default)
nOTP=1, VCOM6-0 value is controlled by SPI register.

Before OTP programming, no matter what's nOTP setting, VCOMH voltage decided by SPI VCOM6-0. User can adjust the VCOMH voltage by setting VCOMH6-0.

After programmed OTP, VCOMH voltage is decided by nOTP setting. When power on reset, nOTP default value is 0, VCOMH voltage equals to programmed OTP value. If nOTP set to "1", setting of VCM6-0 becomes valid and voltage of VCOMH can be adjusted.

VCM6-0: Set the VCOMH voltage if nOTP="1". These bits amplify the VCOMH voltage 0.36 to 0.995 times the VLCD63 voltage.

VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH
0	0	0	0	0	0	0	VLCD63 x 0.360
0	0	0	0	0	0	1	VLCD63 x 0.365
0	0	0	0	0	1	0	VLCD63 x 0.370
0	0	0	0	0	1	1	VLCD63 x 0.375
0	0	0	0	1	0	0	VLCD63 x 0.380
:	:	:	:	:	:	:	: Step=0.005 :
1	1	1	1	1	0	0	VLCD63 x 0.980
1	1	1	1	1	0	1	VLCD63 x 0.985
1	1	1	1	1	1	0	VLCD63 x 0.990
1	1	1	1	1	1	1	VLCD63 x 0.995

Note: 2V < VCOMH < VLCD63

Table 7. 20: VCOMH

Gamma control 1 (R30h to R37h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PKP1	PKP1	PKP1	0	0	0	0	0	PKP0	PKP0	PKP0
W	1	0	0	0	0	0	PKP3	PKP3	PKP3	0	0	0	0	0	PKP2	PKP2	PKP2
W	1	0	0	0	0	0	PKP5	PKP5	PKP5	0	0	0	0	0	PKP4	PKP4	PKP4
W	1	0	0	0	0	0	PRP1	PRP1	PRP1	0	0	0	0	0	PRP0	PRP0	PRP0
W	1	0	0	0	0	0	PKN1	PKN1	PKN1	0	0	0	0	0	PKN0	PKN0	PKN0
W	1	0	0	0	0	0	PKN3	PKN3	PKN3	0	0	0	0	0	PKN2	PKN2	PKN2
W	1	0	0	0	0	0	PKN5	PKN5	PKN5	0	0	0	0	0	PKN4	PKN4	PKN4
W	1	0	0	0	0	0	PRN1	PRN1	PRN1	0	0	0	0	0	PRN0	PRN0	PRN0

Figure 7. 22: Gamma control 1

PKP52–00: Gamma micro adjustment registers for the positive polarity output.
PRP12-00: Gradient adjustment registers for the positive polarity output.
PKN52-00: Gamma micro adjustment registers for the negative polarity output.
PRN12-00: Gradient adjustment registers for the negative polarity output.

Gamma control 2 (R3Ah to R3Bh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	0	VRP03	VRP02	VRP01	VRP00
W	1	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	0	VRN03	VRN02	VRN01	VRN00

Figure 7. 23: Gamma control 2

VRP14-00: Adjustment registers for amplification adjustment of the positive polarity output.
VRN14-00: Adjustment registers for the amplification adjustment of the negative polarity output.
(Refer to gamma adjustment function for details.)

7.4 Secondary register command table

Reg No.	Register	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
01h	DISPLAY INTERFACE	IM	0	0	0	0	0	0	0	REV	0	0	0	0	0	0	0
02h	DISPLAY DATA CONTROL	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
03h	ENTER MODE	VPL	HPL	DPL	EPL	0	0	0	SS	0	0	0	0	0	0	STB	0
04h	GATE CONTROL 1	0	0	CLW1	CLW0	0	0	0	0	0	0	GAON	0	0	0	0	0
05h	GATE CONTROL 2	0	NW	0	DSC	0	0	0	0	0	0	0	0	0	0	0	0
06h	DISPLAY CONTROL 1	0	0	0	0	0	0	0	0	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0
07h	DISPLAY CONTROL 2	0	0	0	0	0	0	HBP9	HBP8	HBP7	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0
08h	SOURCE OUTPUT TIMING CONTROL	0	0	0	0	SDT1	SDT0	0	0	0	0	0	EQ2	EQ1	EQ0	0	0
09h	POWER CONTROL 1	MSEL	EXM	0	0	GON	0	POC	0	0	SAP2	SAP1	SAP0	0	0	0	0
0ah	POWER CONTROL 2	0	0	0	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	VCM4	VCM3	VCM2	VCM1	VCM0
10h	GAMMA CONTROL(1)	0	0	0	0	0	PRP12	PRP11	PRP10	0	0	0	0	0	PRP02	PRP01	PRP00
11h	GAMMA CONTROL(1)	0	0	0	0	0	PRN12	PRN11	PRN10	0	0	0	0	0	PRN02	PRN01	PRN00
12h	GAMMA CONTROL(1)	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	0	VRP03	VRP02	VRP01	VRP00
13h	GAMMA CONTROL(1)	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	0	VRN03	VRN02	VRN01	VRN00
14h	GAMMA CONTROL(1)	0	0	0	0	0	PKP12	PKP11	PKP10	0	0	0	0	0	PKP02	PKP01	PKP00
15h	GAMMA CONTROL(1)	0	0	0	0	0	PKP32	PKP31	PKP30	0	0	0	0	0	PKP22	PKP21	PKP20
16h	GAMMA CONTROL(1)	0	0	0	0	0	PKP52	PKP51	PKP50	0	0	0	0	0	PKP42	PKP41	PKP40
17h	GAMMA CONTROL(1)	0	0	0	0	0	PKN12	PKN11	PKN10	0	0	0	0	0	PKN02	PKN01	PKN00
18h	GAMMA CONTROL(1)	0	0	0	0	0	PKN32	PKN31	PKN30	0	0	0	0	0	PKN22	PKN21	PKN20
19h	GAMMA CONTROL(1)	0	0	0	0	0	PKN52	PKN51	PKN50	0	0	0	0	0	PKN42	PKN41	PKN40
1ah	Function Control	0	0	0	0	0	0	0	OTD	PWM	OTF	FB2	FB1	FB0	0	nOTP	OTG
1bh	PWM Control	0	0	0	PWMS	PWMF3	PWMF2	PWMF1	PWMF0	DUTY7	DUTY6	DUTY5	DUTY4	DUTY3	DUTY2	DUTY1	DUTY0
1ch	Power Control 1	DCT3	DCT2	DCT1	DCT0	DC3	DC2	DC1	DC0	0	XDK	GDIS	0	BTF	BT2	BT1	BT0
1dh	Power Control 2	0	VRC2	VRC1	VRC0	0	0	VDS1	VDS0	0	0	VRH5	VRH4	VRH3	VRH2	VRH1	VRH0

Table 7. 21: Command table

7.5 Secondary register default value

Reg no.	Hex code	Register bit value
R01h	0000	IM="0", REV="0"
R02h	0000	-
R03h	0100	VPL="0", HPL="0", DPL="0", EPL="0", SS="1", STB="0"
R04h	3000	CLW1="1", CLW0="1", GAON="0"
R05h	5000	NW="1", DSC="1"
R06h	000A	VBP7="0", VBP6="0", VBP5="0", VBP4="0", VBP3="1", VBP2="0", VBP1="1", VBP0="0"
R07h	0021	HBP9="0", HBP8="0", HBP7="0", HBP6="0", HBP5="1", HBP4="0", HBP3="0", HBP2="0", HBP1="0", HBP0="1"
R08h	0410	SDT1="0", SDT0="1", EQ2="1", EQ1="0", EQ0="0"
R09h	0A00	MSEL="0", EXM="0", GON="1", POC="1", SAP2="0", SAP1="0", SAP0="0"
R0Ah	040F	VDV4="0", VDV3="0", VDV2="1", VDV1="0", VDV0="0",VCM4="0", VCM3="1", VCM2="1", VCM1="1", VCM0="1"
R10h	0000	PRP12="0", PRP11="0", PRP10="0", PRP02="0", PRP01="0", PRP00="0"
R11h	0000	PRN12="0", PRN11="0", PRN10="0", PRN02="0", PRN01="0", PRN00="0"
R12h	0904	VRP14="0", VRP13="1", VRP12="0", VRP11="0", VRP10="1", VRP03="0", VRP02="1", VRP01="0", VRP00="0"
R13h	0904	VRN14="0", VRN13="1", VRN12="0", VRN11="0", VRN10="1", VRN03="0", VRN02="1", VRN01="0", VRN00="0"
R14h	0000	PKP12="0", PKP11="0", PKP10="0", PKP02="0", PKP01="0", PKP00="0"
R15h	0407	PKP32="1", PKP31="0", PKP30="0", PKP22="1", PKP21="1", PKP20="1"
R16h	0202	PKP52="0", PKP51="1", PKP50="0", PKP42="0", PKP41="1", PKP40="0"
R17h	0505	PKN12="1", PKN11="0", PKN10="1", PKN02="1", PKN01="0", PKN00="1"
R18h	0003	PKN32="0", PKN31="0", PKN30="0", PKN32="0", PKN31="1", PKN30="1"
R19h	0707	PKN52="1", PKN51="1", PKN50="1", PKN42="0", PKN41="1", PKN40="1"
R1Ah	0020	OTD="0", PWM="0", OTF="0", FB2="1", FB1="0", FB0="0", nOTP="0", OTG="0"
R1Bh	06FF	PWMS="0", PWMF3="0", PWMF2="1", PWMF1="1", PWMF0="0", DUTY7="1", DUTY6="1", DUTY5="1", DUTY4="1", DUTY3="1", DUTY2="1", DUTY1="1", DUTY0="1"
R1Ch	6624	DCT3="0", DCT2="1", DCT1="1", DCT0="0", DC3="0", DC2="1", DC1="1", DC0="0", XDK="0", GDIS="1", BTF="0", BT2="1", BT1="0", BT0="0"
R1Dh	3229	VRC2="0", VRC1="1", VRC0="1", VDS1="1", VDS0="0", VRH5="1", VRH4="0", VRH3="1", VRH2="0", VRH1="0", VRH0="1"

Table 7. 22: Registers default value (Secondary register map)

7.6 Secondary regsiter command description

Display interface control (R01H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	I M	0	0	0	0	0	0	0	REV	0	0	0	0	0	0	0

Figure 7. 24: Display interface control instruction

IM: Specify the PD data weight.
IM="0": 24bits interface.
IM="1": 8bits interface.

REV: Reverses all character and graphics display sections.
REV="0": Normally White Panel.
REV="1": Normally Black Panel.

REV	Data	Source output level of displayed area	
		Positive polarity	Negative polarity
0	6'b000000 : : 6'b111111	V0 : : V63	V63 : : V0
1	6'b000000 : : 6'b111111	V63 : : V0	V0 : : V63

Table 7. 23: REV bit and source output level of displayed area

Entry mode (R03H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	VPL	HPL	DPL	EPL	0	0	0	S S	0	0	0	0	0	0	STB	0

Figure 7. 25: Entry mode instruction

VPL: Reverses the polarity of the VSYNC signal.
VPL="0": VSYNC is low active.
VPL="1": VSYNC is high active.

HPL: Reverses the polarity of the HSYNC signal.
HPL="0": HSYNC is low active.
HPL="1": HSYNC is high active.

DPL: Reverses the polarity of the DOTCLK signal.
DPL="0": Display data is fetched at rising edge of DOTCLK.
DPL="1": Display data is fetched at falling edge of DOTCLK.

EPL: Set the polarity of ENABLE pin while using DE interface mode.
EPL="0": DE=L write data, DE=H won't write data.
EPL="1": DE=H write data, DE=L won't write data.

SS: Selects the output shift direction of the source driver.
SS="0": S960→S1.
SS="1": S1→S960.

STB: Standby mode.
STB="1": Standby mode (SD/GD/TCON/VCOM disable).
STB="0": Standby mode cancel.

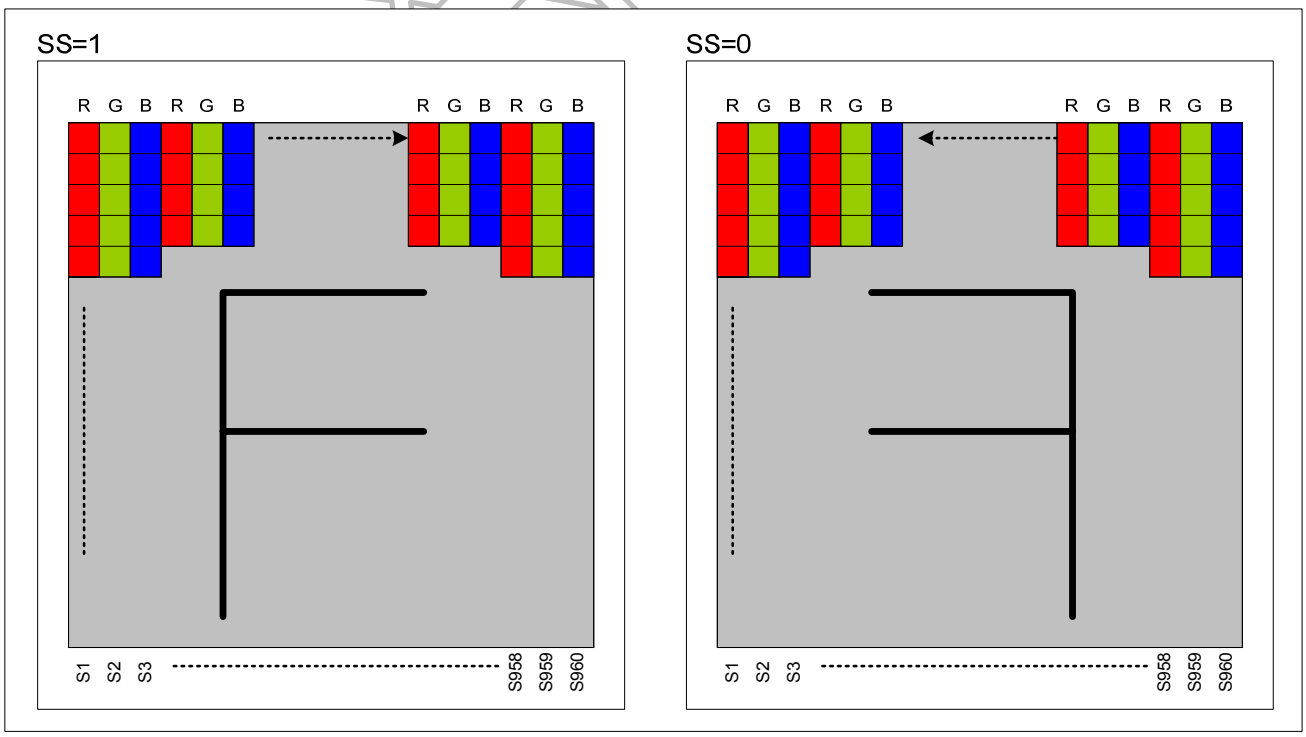


Figure 7. 26: Display direction according to SS

Gate control 1 (R04H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	CLW1	CLW0	0	0	0	0	0	0	GAON	0	0	0	0	0

Figure 7. 27 Gate control 1 instruction

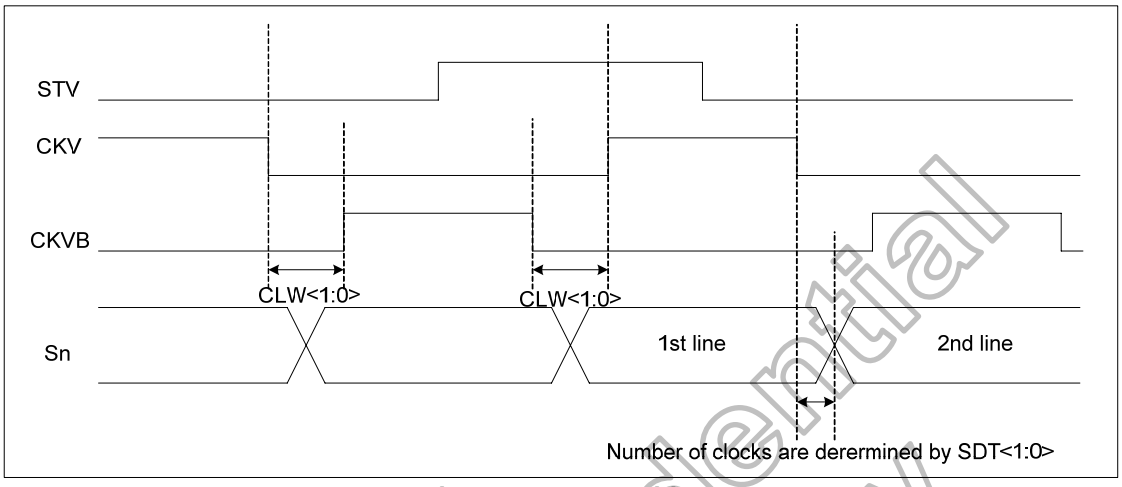


Figure 7. 28: CLW bits

CLW2-0: Specify the pulse output timing of the CKV and CKVB signal.

CLW1	CLW0	OEV
0	0	1.5μs
0	1	3.0μs
1	0	4.5μs
1	1	6.0μs

Note: The values indicate the number of clocks after the falling edge of CKV & CKVB.

Table 7. 24: CLW bits setting

GAON: Gate all on.
GAON="0", Gate all on disable.
GAON="1", Gate all on enable.

Gate control 2 (R05H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	NW	0	DSC	0	0	0	0	0	0	0	0	0	0	0	0

Figure 7. 29: Gate control2 instruction

NW: Frame or line inversion selection.
NW="0": Frame inversion.
NW="1": Line inversion.

DSC: Specify state of gate driver output signal.
DSC="0": Gate output disable, GOUT=VGL.
DSC="1": Gate output enable.

Display control 1 (R06H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0

Figure 7. 30: Display control1 instruction

VBP7-0: Vertical back porch. (4H < VBP < 255H)

VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	No. of clock cycle of HSYNC
0	0	0	0	0	0	0	0	Can't set.
0	0	0	0	0	0	0	1	Can't set.
0	0	0	0	0	0	1	0	Can't set.
0	0	0	0	0	0	1	1	Can't set.
0	0	0	0	0	1	0	0	4
:	:	:	:	:	:	:	:	: Step=1 :
1	1	1	1	1	1	0	0	252
1	1	1	1	1	1	0	1	253
1	1	1	1	1	1	1	0	254
1	1	1	1	1	1	1	1	255

Display control 2 (R07H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	HBP9	HBP8	HBP7	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0

Figure 7. 31: Display control2 instruction

HBP9-0: Horizontal back porch. (8clock < HBP < 1023clock)
8clock < HBP of the Parallel RGB < 255clock
8clock < HBP of the Serial RGB < 1023clock

HBP9	HBP8	HBP7	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	No. of clock cycle
0	0	0	0	0	0	0	0	0	0	Can't set.
0	0	0	0	0	0	0	0	0	1	Can't set.
0	0	0	0	0	0	0	0	1	0	Can't set.
0	0	0	0	0	0	0	0	1	1	Can't set.
0	0	0	0	0	0	0	1	0	0	Can't set.
0	0	0	0	0	0	0	1	0	1	Can't set.
0	0	0	0	0	0	0	1	1	0	Can't set.
0	0	0	0	0	0	0	1	1	1	Can't set.
0	0	0	0	0	0	1	0	0	0	8
0	0	0	0	0	0	1	0	0	1	9
				:						: Step=1 :
1	1	1	1	1	1	1	1	1	0	1022
1	1	1	1	1	1	1	1	1	1	1023

Source output timing control (R08H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	SDT1	SDT0	0	0	0	0	0	EQ2	EQ1	EQ0	0	0

Figure 7. 32: Source output timing control instruction

SDT1-0: Set delay amount from the gate output signal falling edge to the source output.

SDT1	SDT0	Delay amount of the source output (DOTCL)
0	0	5μs
0	1	5μs
1	0	1μs
1	1	3μs

Table 7. 25: SDT bits setting

EQ2-0: Sets the equalized period.

EQ2	EQ1	EQ0	Equalizing period (DOTCLK)
0	0	0	Not equalized
0	0	1	3μs
0	1	0	4μs
0	1	1	5μs
1	0	0	6μs
1	0	1	7μs
1	1	0	8μs
1	1	1	9μs

Table 7. 26: EQ bits setting

Power control 1 (R09H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	MSEL	EXM	0	0	GON	0	POC	0	0	SAP2	SAP1	SAP0	0	0	0	0

Figure 7. 33: Power control1 instruction

MSEL: Select the polarity of POL.
MSEL=”0”: POL is in phase with internal VCOM.
MSEL=”1”: POL is reverse with internal VCOM.

EXM: VCOM enable selection.
EXM=“0”: VCOM circuit enable.
EXM=“1”: VCOM circuit disable, VCOMOUT floating.

GON: VCOM enable selection.
GON=“0”: VCOM circuit disable, VCOMOUT floating.
GON=“1”: VCOM circuit enable.

POC: Power control.
POC=“0”: SD output the blanking data when CPE = L.
White display for normally white and black display for normally black.
POC=“1”: SD output the normal display.

SAP2-0: Set current amount of SD/Power circuit

SAP2	SAP1	SAP0	Amount of current in SD/power circuit
0	0	0	Standby mode(default)
0	0	1	Small
0	1	0	Small or medium
0	1	1	Medium
1	0	0	Medium or large
1	0	1	Large
1	1	0	Setting Inhibited
1	1	1	Setting Inhibited

Table 7. 27: SAP bits setting

Power control (R0Ah)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	VCM4	VCM3	VCM2	VCM1	VCM0

Figure 7. 34: Power control

VDV4-0: Set the alternating amplitudes of VCOM at the VCOM alternating drive. These bits amplify VCOM amplitude 0.7875 to 1.2525 times the VLCD63 voltage. External voltage at VCOMR is referenced when VDV="01111xx". The maximum voltage of VCOMR is VCIX2.

VDV4	VDV3	VDV2	VDV1	VDV0	VCOM amplitude
0	0	0	0	0	VLCD63 x 0.7875
0	0	0	0	1	VLCD63 x 0.8025
0	0	0	1	0	VLCD63 x 0.8175
0	0	0	1	1	VLCD63 x 0.8325
		:			: Step=0.0150 :
1	0	0	1	*	Setting inhibited
		:			: Step=0.0150 :
1	1	1	0	0	VLCD63 x 1.2225
1	1	1	1	0	VLCD63 x 1.2375
1	1	1	1	1	VLCD63 x 1.2525

Table 7. 28: VCOM amplitude

VCM4-0: Set the VCOMH voltage if nOTP="1". These bits amplify the VCOMH voltage 0.68 to 0.990 times the VLCD63 voltage.

VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH
0	0	0	0	0	VLCD63 x 0.680
0	0	0	0	1	VLCD63 x 0.690
0	0	0	1	0	VLCD63 x 0.700
0	0	0	1	1	VLCD63 x 0.710
0	0	1	0	0	VLCD63 x 0.720
		:			: Step=0.010 :
1	1	1	0	0	VLCD63 x 0.960
1	1	1	0	1	VLCD63 x 0.970
1	1	1	1	0	VLCD63 x 0.980
1	1	1	1	1	VLCD63 x 0.990

Note: 2V < VCOMH < VLCD63

Table 7. 29: VCOMH

Gamma control 1 (R10h to R11h and R14h to R19h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PRP12	PRP11	PRP10	0	0	0	0	0	PRP02	PRP01	PRP00
W	1	0	0	0	0	0	PRN12	PRN11	PRN10	0	0	0	0	0	PRN02	PRN01	PRN00
W	1	0	0	0	0	0	PKP12	PKP11	PKP10	0	0	0	0	0	PKP02	PKP01	PKP00
W	1	0	0	0	0	0	PKP32	PKP31	PKP30	0	0	0	0	0	PKP22	PKP21	PKP20
W	1	0	0	0	0	0	PKP52	PKP51	PKP50	0	0	0	0	0	PKP42	PKP41	PKP40
W	1	0	0	0	0	0	PKN12	PKN11	PKN10	0	0	0	0	0	PKN02	PKN01	PKN00
W	1	0	0	0	0	0	PKN32	PKN31	PKN30	0	0	0	0	0	PKN22	PKN21	PKN20
W	1	0	0	0	0	0	PKN52	PKN51	PKN50	0	0	0	0	0	PKN42	PKN41	PKN40

Figure 7. 35: Gamma control 1

PKP52-00: Gamma micro adjustment registers for the positive polarity output
PRP12-00: Gradient adjustment registers for the positive polarity output
PKN52-00: Gamma micro adjustment registers for the negative polarity output
PRN12-00: Gradient adjustment registers for the negative polarity output

Gamma control 2 (R12h to R13h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	0	VRP03	VRP02	VRP01	VRP00
W	1	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	0	VRN03	VRN02	VRN01	VRN00

Figure 7. 36: Gamma control 2

VRP14-00: Adjustment registers for amplification adjustment of the positive polarity output.
VRN14-00: Adjustment registers for the amplification adjustment of the negative polarity output.
(Refer to gamma adjustment function for details)

Function control (R1Ah)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	OTD	PWM	OTF	FB2	FB1	FB0	0	nOTP	OTG

Figure 7. 37: Function control

PWM: When PWM=0, PWM function is disabled.
When PWM=1, PWM function is enabled.

FB2-0: Set PWM feedback level adjustment when PWMS=0.
000: 0.4V 001: 0.45V 010: 0.5V
011: 0.55V 100: 0.6V 101: 0.65V
110: 0.7V 111: 0.75V

OTD: OTD=0, VDV4-0 value is controlled by OTP memory. (Default)
OTD=1, VDV4-0 value is controlled by SPI register.
Before OTP programming, no matter what's OTD setting, VCOMA voltage decided by SPI VDV4-0. User can adjust the VCOMA voltage by setting VDV4-0.

After programmed OTP, VCOMA voltage is decided by OTD setting. When power on reset, OTD default value is 0, VCOMA voltage equals to programmed OTP value. If OTD set to "1", setting of VDV4-0 becomes valid and voltage of VCOMA can be adjusted.

nOTP: nOTP=0, VCOM6-0 value is controlled by OTP memory. (Default)
nOTP=1, VCOM6-0 value is controlled by SPI register.
Before OTP programming, no matter what's nOTP setting, VCOMH voltage decided by SPI VCOM6-0. User can adjust the VCOMH voltage by setting VCOMH6-0.

After programmed OTP, VCOMH voltage is decided by nOTP setting. When power on reset, nOTP default value is 0, VCOMH voltage equals to programmed OTP value. If nOTP set to "1", setting of VCM6-0 becomes valid and voltage of VCOMH can be adjusted.

OTF: OTF=0, BTF and BT2-0 value are controlled by OTP memory. (Default)
OTF=1, BTF and BT2-0 value are controlled by SPI register.
Before OTP programming, no matter what's OTF setting, VGH/VGL pump voltage ratio voltage decided by SPI BTF and BT2-0. User can adjust the VGH/VGL pump voltage ratio by setting BTF and BT2-0.

After programmed OTP, VGH/VGL pump voltage ratio voltage is decided by OTF setting. When power on reset, BTF and BT2-0 default value is 0, VGH/VGL pump voltage ratio voltage equals to programmed OTP value. If OTF set to "1", setting of BTF and BT2-0 becomes valid and voltage of VGH/VGL pump voltage ratio can be adjusted.

OTG: Gamma voltage setting is controlled by OTP or SPI.
OTG=0, Gamma setting is controlled by OTP memory. (Default)
OTG=1, Gamma setting is controlled by SPI.

PWM control (R1Bh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	PWMS	PWMF3	PWMF2	PWMF1	PWMF0	DUTY7	DUTY6	DUTY5	DUTY4	DUTY3	DUTY2	DUTY1	DUTY0

Figure 7. 38: PWM for external LED driver control

PWMS: Select PWM function.
When PWMS=0, use internal PWM circuit. (Default)
When PWMS=1, use external LED driver, DRV pin outputs control signal.

PWMF3-0: Select control signal frequency when set PWMS=1. Adjust range from 100Hz to 100KHz. Default value = 0110.

PWMF3	PWMF2	PWMF1	PWMF0	Enable signal frequency	
				Parallel RGB 6.5MHz	Serial RGB 19.5MHz
0	0	0	0	DCLK / 2^8	DCLK / 3 / 2^8
0	0	0	1	DCLK / 2^8	DCLK / 3 / 2^8
0	0	1	0	DCLK / 2^8	DCLK / 3 / 2^8
0	0	1	1	DCLK / 2^9	DCLK / 3 / 2^9
0	1	0	0	DCLK / 2^{10}	DCLK / 3 / 2^{10}
0	1	0	1	DCLK / 2^{11}	DCLK / 3 / 2^{11}
0	1	1	0	DCLK / 2^{12}	DCLK / 3 / 2^{12}
0	1	1	1	DCLK / 2^{13}	DCLK / 3 /2^{13}
1	0	0	0	DCLK / 2^{14}	DCLK / 3 / 2^{14}
1	0	0	1	DCLK / 2^{15}	DCLK / 3 / 2^{15}
1	0	1	0	DCLK / 2^{16}	DCLK / 3 / 2^{16}
1	0	1	1	Reserved	Reserved
1	1	0	0	Reserved	Reserved
1	1	0	1	Reserved	Reserved
1	1	1	0	Reserved	Reserved
1	1	1	1	Reserved	Reserved

Table 7. 30: LED driver control signal frequency

DUTY7-0: Select control signal duty cycle when set PWMS=1. Adjust range from 00h (duty cycle=1/256) to FFh(duty cycle=256/256). Default value is FFh.

Power control 1 (R1Ch)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	DCT3	DCT2	DCT1	DCT0	DC3	DC2	DC1	DC0	0	XDK	GDIS	0	BTF	BT2	BT1	BT0

Figure 7. 39: Power control 1

DCT3-0: Set the step-up cycle of the step-up circuit for 8-color mode (CM=VDDIO). When the cycle is accelerated, the Vcim and Vcix2 driving ability are of the step-up circuit increase, but their current consumption increase, too. Adjust the cycle taking into account the display quality and power consumption.
VGH and VGL are always fixed at the step-up cycle of Fline x 0.5.

DCT3	DCT2	DCT1	DCT0	Step-up cycle
0	0	0	0	Fline x 14
0	0	0	1	Fline x 12
0	0	1	0	Fline x 10
0	0	1	1	Fline x 8
0	1	0	0	Fline x 7
0	1	0	1	Fline x 6
0	1	1	0	Fline x 5
0	1	1	1	Fline x 4
1	0	0	0	Fline x 3
1	0	0	1	Fline x 2
1	0	1	0	Fline x 1
1	0	1	1	Fline x 0.5
1	1	0	0	Fline x 0.25
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

Note: Fline = horizontal frequency (Fline Typ. 15KHz)

Table 7. 31: Step-up cycle

DC3-0: Set the step-up cycle of the step-up circuit for 16M-color with dithering mode (CM=VSS). When the cycle is accelerated, the Vcim and Vcix2 driving ability are of the step-up circuit increase, but their current consumption increase, too. Adjust the cycle taking into account the display quality and power consumption.
VGH and VGL are always fixed at the step-up cycle of Fline x 0.5.

DC3	DC2	DC1	DC0	Step-up cycle
0	0	0	0	Fline x 14
0	0	0	1	Fline x 12
0	0	1	0	Fline x 10
0	0	1	1	Fline x 8
0	1	0	0	Fline x 7
0	1	0	1	Fline x 6
0	1	1	0	Fline x 5
0	1	1	1	Fline x 4
1	0	0	0	Fline x 3
1	0	0	1	Fline x 2
1	0	1	0	Fline x 1
1	0	1	1	Fline x 0.5
1	1	0	0	Fline x 0.25
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

Note: Fline = horizontal frequency (Fline typ. 15KHz)

Table 7. 32: Step-up cycle

XDK: When XDK=0, VCIX2 is 2 stage pumping from VCI. (VCIX2=3 x VCI)
When XDK=1, VCIX2 is 2 phase pumping from VCI. (VCIX2=2 x VCI)

GDIS: When GDIS=0, VGL has no discharge path to VSS in standby mode. When GDIS=1, VGL will discharge to VSS in standby mode. When CPE=0, GDIS is fixed to 0, and you can't change it by SPI.

BT2-0 & BTF: Control the step-up factor of the step-up circuit. Adjust the step-up factor according to the power supply voltage to be used.

BTF	BT2	BT1	BT0	VGH output	VGL output
0	0	0	0	VCIX2j X 3	- (VCIX2j X 3) + VCI
0	0	0	1	VCIX2j X 3	- (VCIX2j X 2)
0	0	1	0	VCIX2j X 3	- (VCIX2j X 3)
0	0	1	1	VCIX2j X 2 + VCI	- (VCIX2j X 2) - VCI
0	1	0	0	VCIX2j X 2 + VCI	- (VCIX2j X 2)
0	1	0	1	VCIX2j X 2 + VCI	- VCIX2j 2 - VCI
0	1	1	0	VCIX2j X 2	- (VCIX2j X 2)
0	1	1	1	VCIX2j X 2	- (VCIX2j X 2) + VCI
1	X	X	X	VCIX2j X 3	- VCIX2j

Table 7. 33: VGH and VGL booster ratio

Power control 2 (R1Dh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	VRC2	VRC1	VRC0	0	0	VDS1	VDS0	0	0	VRH5	VRH4	VRH3	VRH2	VRH1	VRH0

Figure 7. 40: Power control 2

VRC[2:0]: Set the VCIX2 charge pump voltage clamp.
VRC[2:0]=000, 5.1V
VRC[2:0]=001, 5.3V
VRC[2:0]=010, 5.5V
VRC[2:0]=011, 5.7V
VRC[2:0]=100, 5.9V
VRC[2:0]=101, reserved
VRC[2:0]=110, reserved
VRC[2:0]=111, reserved

VDS[1:0]: Set the VDD regulator voltage if pin “REGVDD” is set to VDDIO.
VDS[1:0]=00, 1.8V
VDS[1:0]=01, 2.0V
VDS[1:0]=10, 2.2V
VDS[1:0]=11, 2.5V

VRH5-0: Set amplitude magnification of VLCD63. These bits amplify the VLCD63 voltage 2.464 to 4.456 times the Vref voltage set by VRH5-0.

VRH5	VRH4	VRH3	VRH2	VRH1	VRH0	VLCD63 voltage
0	0	0	0	0	0	Vref x 2.456
0	0	0	0	0	1	Vref x 2.488
0	0	0	0	1	0	Vref x 2.520
0	0	0	0	1	1	Vref x 2.552
0	0	0	1	0	0	Vref x 2.584
0	0	0	1	0	1	Vref x 2.616
0	0	0	1	1	0	Vref x 2.648
0	0	0	1	1	1	Vref x 2.680
0	0	1	0	0	0	Vref x 2.712
0	0	1	0	0	1	Vref x 2.744
0	0	1	0	1	0	Vref x 2.776
0	0	1	0	1	1	Vref x 2.808
0	0	1	1	0	0	Vref x 2.840
0	0	1	1	0	1	Vref x 2.872
0	0	1	1	1	0	Vref x 2.904
0	0	1	1	1	1	Vref x 2.936
0	1	0	0	0	0	Vref x 2.968
0	1	0	0	0	1	Vref x 3.000
0	1	0	0	1	0	Vref x 3.032
0	1	0	0	1	1	Vref x 3.064
0	1	0	1	0	0	Vref x 3.096
0	1	0	1	0	1	Vref x 3.128
0	1	0	1	1	0	Vref x 3.160
0	1	0	1	1	1	Vref x 3.192
0	1	1	0	0	0	Vref x 3.224
0	1	1	0	0	1	Vref x 3.256
0	1	1	0	1	0	Vref x 3.288
0	1	1	0	1	1	Vref x 3.320
0	1	1	1	0	0	Vref x 3.352
0	1	1	1	0	1	Vref x 3.384
0	1	1	1	1	0	Vref x 3.416
0	1	1	1	1	1	Vref x 3.448

VRH5	VRH4	VRH3	VRH2	VRH1	VRH0	VLCD63 voltage
1	0	0	0	0	0	Vref x 3.480
1	0	0	0	0	1	Vref x 3.512
1	0	0	0	1	0	Vref x 3.544
1	0	0	0	1	1	Vref x 3.576
1	0	0	1	0	0	Vref x 3.608
1	0	0	1	0	1	Vref x 3.640
1	0	0	1	1	0	Vref x 3.672
1	0	0	1	1	1	Vref x 3.704
1	0	1	0	0	0	Vref x 3.736
1	0	1	0	0	1	Vref x 3.768
1	0	1	0	1	0	Vref x 3.800
1	0	1	0	1	1	Vref x 3.832
1	0	1	1	0	0	Vref x 3.864
1	0	1	1	0	1	Vref x 3.896
1	0	1	1	1	0	Vref x 3.928
1	0	1	1	1	1	Vref x 3.960
1	1	0	0	0	0	Vref x 3.992
1	1	0	0	0	1	Vref x 4.024
1	1	0	0	1	0	Vref x 4.056
1	1	0	0	1	1	Vref x 4.088
1	1	0	1	0	0	Vref x 4.120
1	1	0	1	0	1	Vref x 4.152
1	1	0	1	1	0	Vref x 4.184
1	1	0	1	1	1	Vref x 4.216
1	1	1	0	0	0	Vref x 4.248
1	1	1	0	0	1	Vref x 4.280
1	1	1	0	1	0	Vref x 4.312
1	1	1	0	1	1	Vref x 4.344
1	1	1	1	0	0	Vref x 4.376
1	1	1	1	0	1	Vref x 4.408
1	1	1	1	1	0	Vref x 4.440
1	1	1	1	1	1	Vref x 4.472

Note: Vref is the internal reference voltage equals to 1.25V.

Table 7. 34: VLCD63 voltage

7.7 Power up/down sequence of the secondary register command

When set to Secondary Register command and CPE=VSS, the charge pump circuit will not enable and the VCIX2, VGH, VGL need to external input.

VCOM can be selected to internal generation or external input by setting register R09h EXM or GON, it needs set both EXM=0 and GON=1, VCOM will be internal generated. If each EXM=1 or GON=0, then VCOM circuit will be disabled, and VCOM need to be external input.

Please follow the recommend power up/down sequence as below steps:
(Set VCOM is external inputted.)

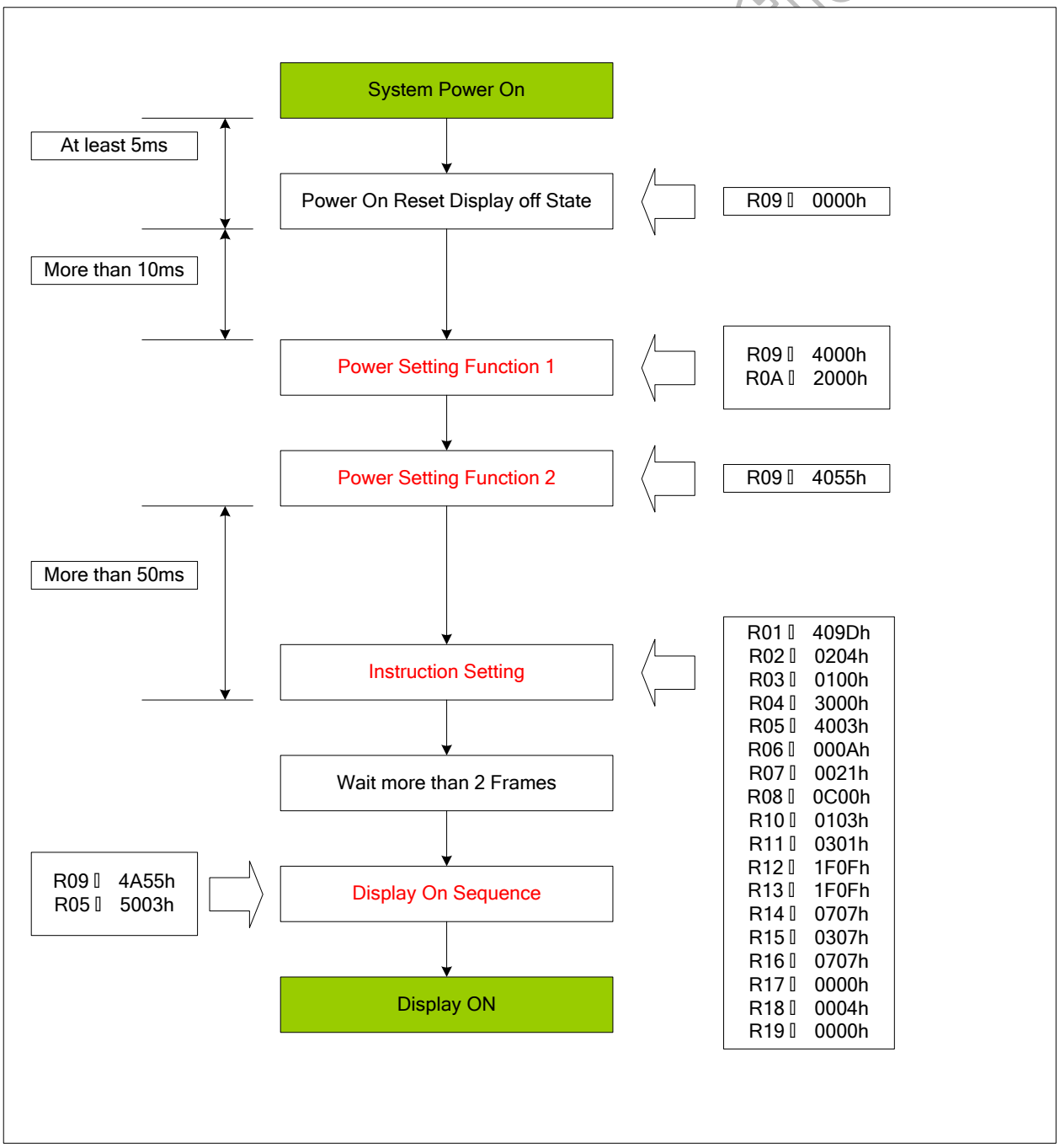


Figure 7. 41: Power up sequence when SPSW connect to VSS (CPE=VSS)

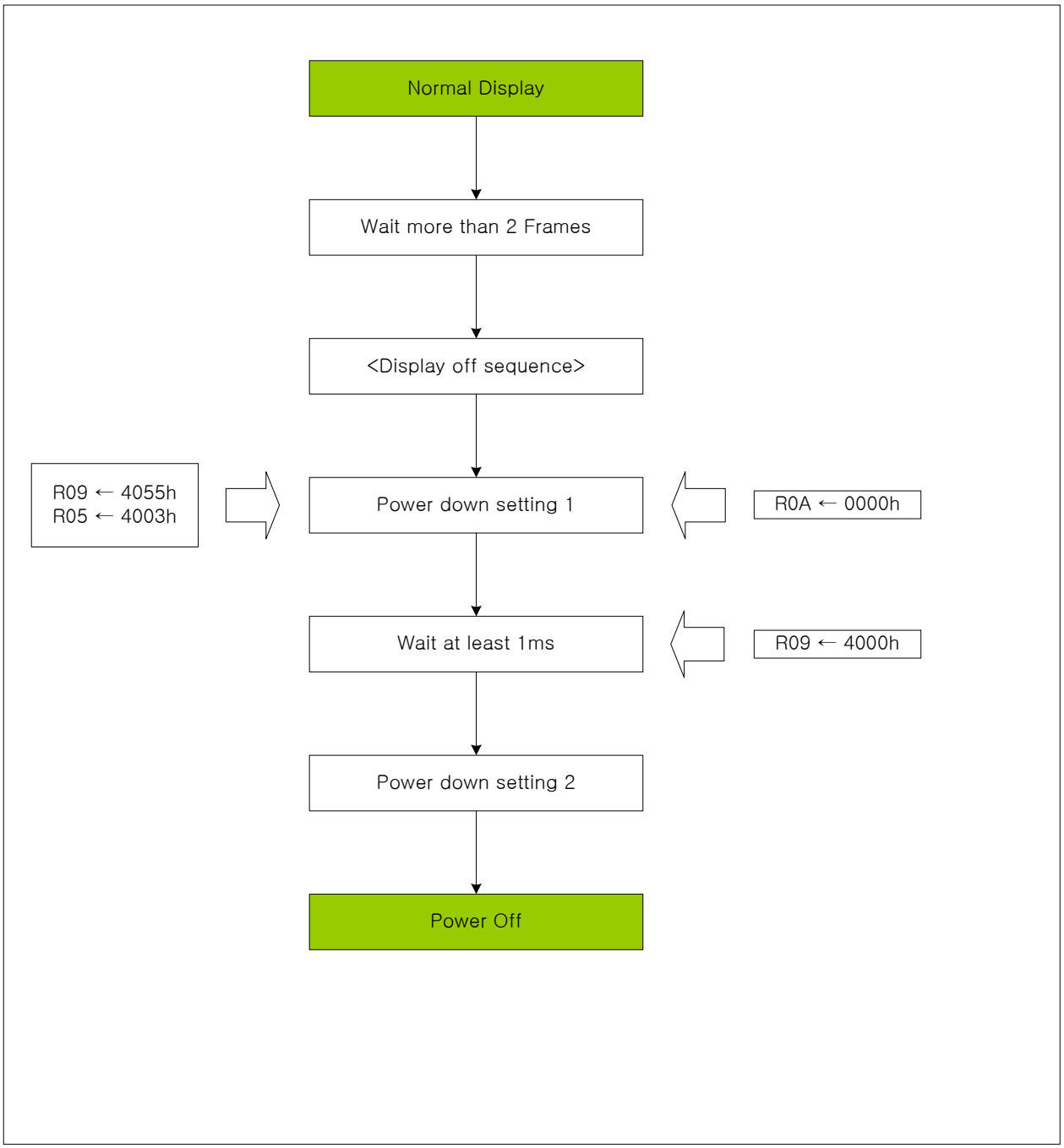


Figure 7. 42: Power down sequence when SPSW connect to VSS (CPE=VSS)

When set to Secondary register command and CPE=VDDIO, the charge pump circuit will enable and the VCIX2, VGH, VGL, VCOM will internal generation.

Please follow the power up/down sequence as Figure 12.10 and Figure 12.11.

8. OTP Programming

OTP write sequence

Step	Operation
1	Power up the module. Set nOTP=1 and find out the appropriate value of VCM[6:0] and power off the system.
2	Power up the system with VDD=VDDIO=2.5V. If REGVDD=1, set R0Dh=16'h0324.
3	Set appropriate values found from step 1 to register of VCOM (R1Eh).
4	Set R06h=16'h2820 to stop VGH/VGL pumping. Wait 0.5s.
5	Set R60h=16'h8000.
6	Set R60h=16'hC000.
7	Connect 7.25~7.75V to VGH and 0V to VGL. (Note1)
8	Set R60h=16'hC200.
9	Set R60h=16'hC280.
10	Wait 350μs for completing this program.
11	Set R60h=16'hC200.
12	Remove 7.25V ~ 7.75V from VGH and 0V from VGL.
13	Set R60h=16'h8200.
14	Set R60h=16'h0200.
15	Set R60h=16'h0040.
16	Set R60h=16'h0000.

Note: VGH is connected to 7.25~7.75V

Table 8. 1: OTP programming sequence

You can use above programming sequence to set VCM[6:0] value to OTP cell twice. If you want to check if the OTP cell is still available for programming, you can read the status from R61h shown below.

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	1	IND[2]	VCM6[2]	VCM5[2]	VCM4[2]	VCM3[2]	VCM2[2]	VCM1[2]	VCM0[2]	IND[1]	VCM6[1]	VCM5[1]	VCM4[1]	VCM3[1]	VCM2[1]	VCM1[1]	VCM0[1]

Figure 8. 1: OTP read table

You can check the IND[2] bit to see if the VCM[6:0] is still programmable or not. If IND[2]=0, you can program new VCM[6:0] value to OTP. If IND[2]=1, it means that the OTP cell have already programmed twice and you can't program it any more. IB6~IB0 indicate the currently effective VCM[6:0] setting in OTP cell.

OTP programming circuitry

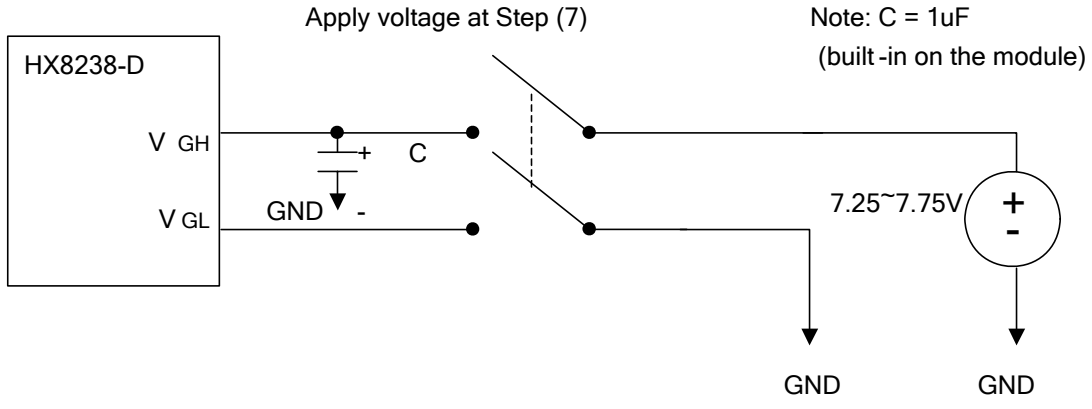


Figure 8. 2: OTP programming circuitry

9. Gamma Adjustment Function

The HX8238-D incorporates gamma adjustment function for the 16M-colors with dithering display. Gamma adjustment is implemented by deciding the 8-grayscale levels with angle adjustment and micro adjustment register. Also, angle adjustment and micro adjustment is fixed for each of the internal positive and negative polarity. Set up by the liquid crystal panel's specification.

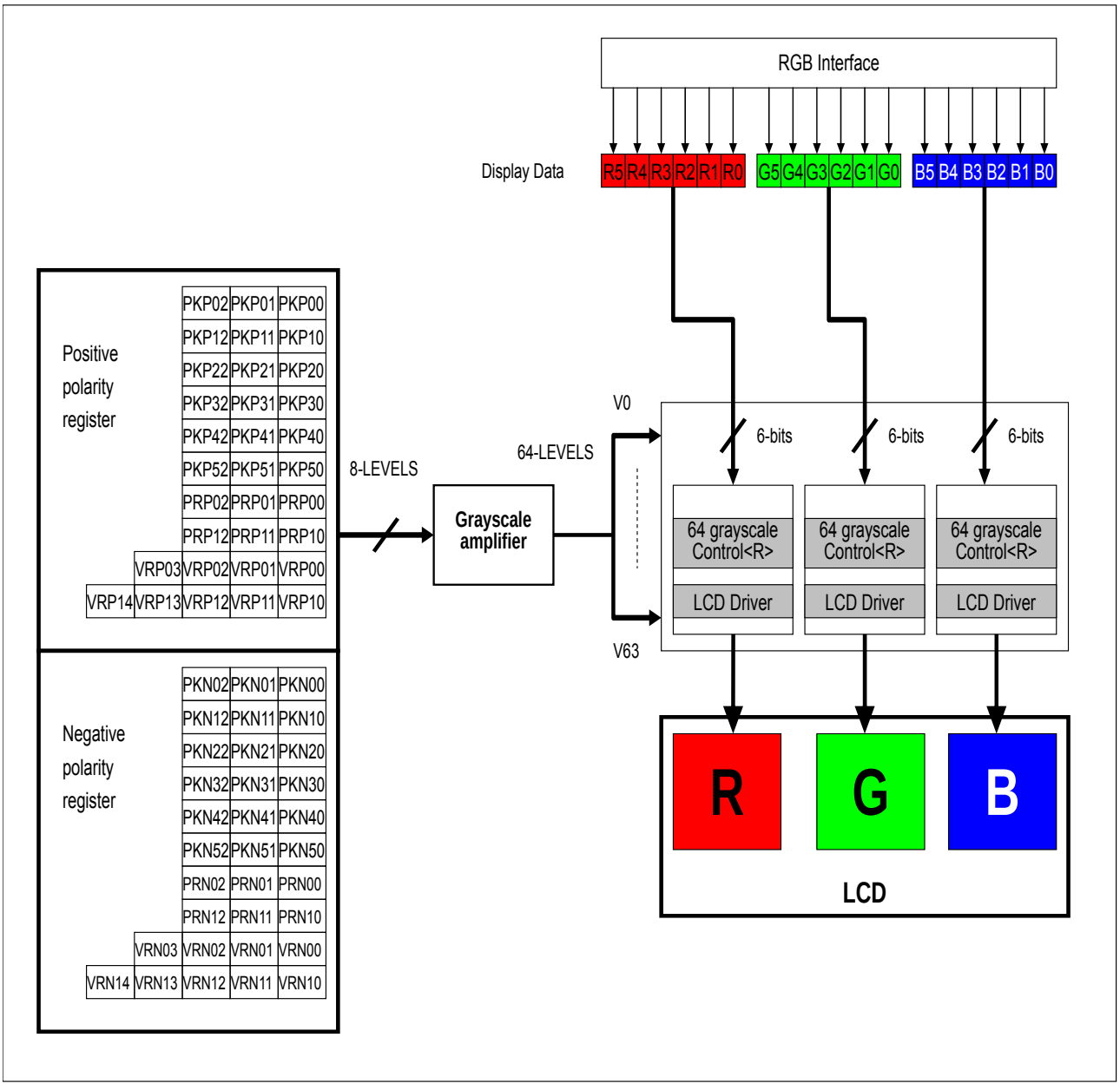


Figure 9. 1: Grayscale control block

9.1 Structure of grayscale amplifier

Below figure indicates the structure of the grayscale amplifier. It determines 8 levels (VIN0-VIN7) by the gradient adjuster and the micro adjustment register. Also, dividing these levels with ladder resistors generates V0 to V63.

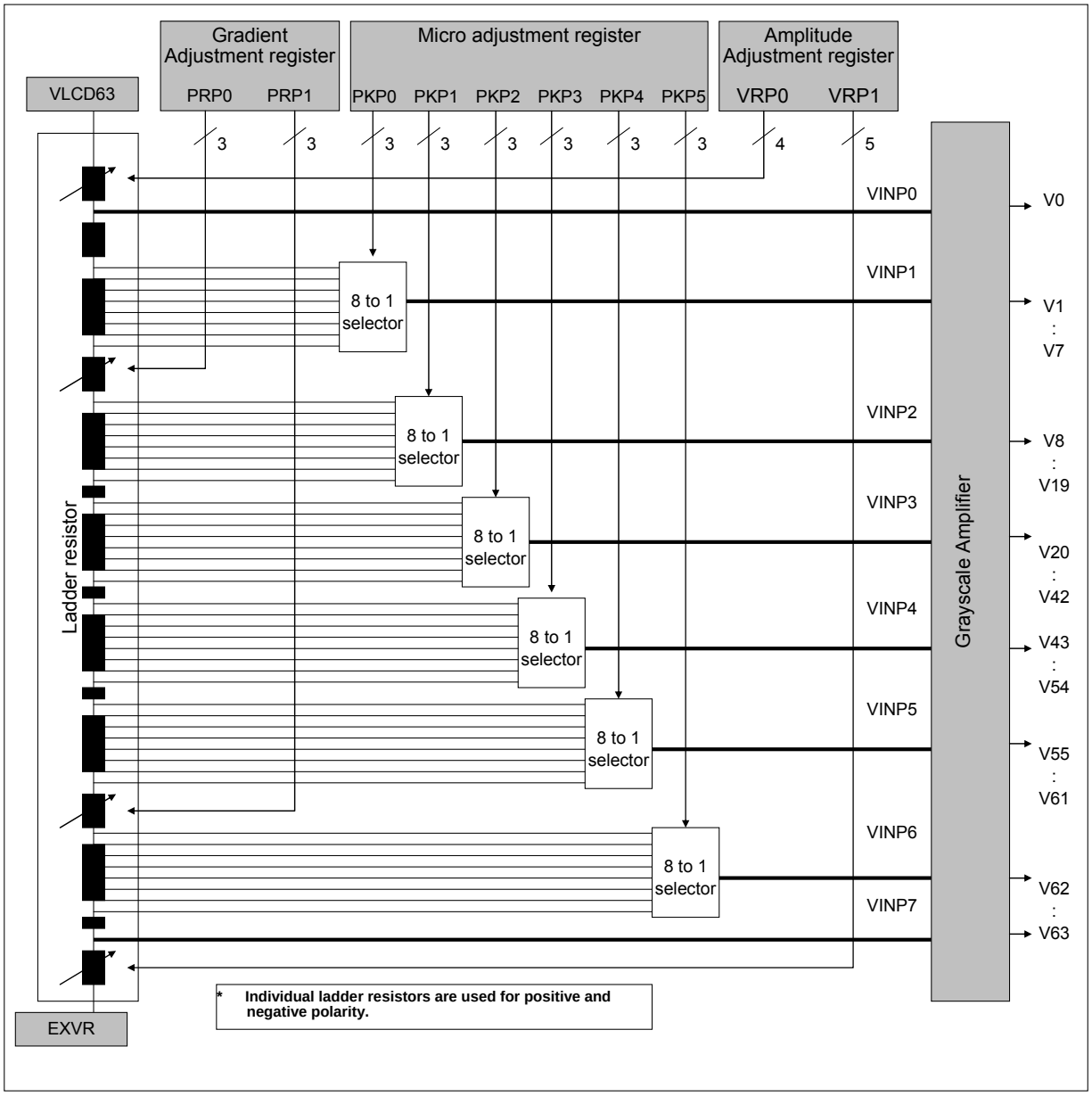


Figure 9. 2: Grayscale amplifier

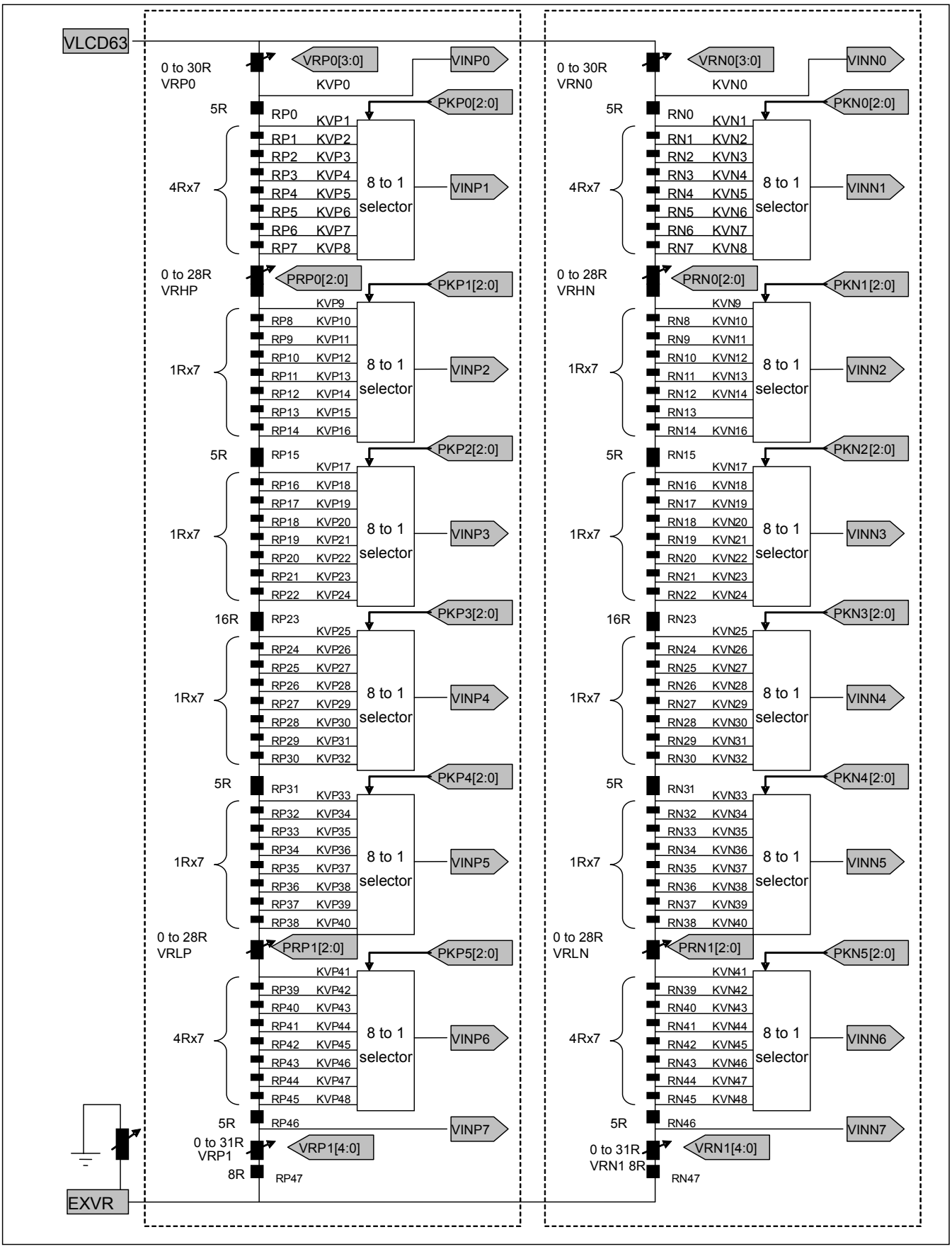


Figure 9. 3: Resistor ladder for gamma voltages generation

9.2 Gamma adjustment register

This block is the register to set up the grayscale voltage adjusting to the gamma specification of the LCD panel. This register can independent set up to positive/negative polarities and there are three types of register groups to adjust gradient, amplitude, and micro-adjustment on number of the grayscale, characteristics of the grayscale voltage. (Use the same setting of Reference-value and R.G. B.) Following graphics indicates the operation of each adjusting register.

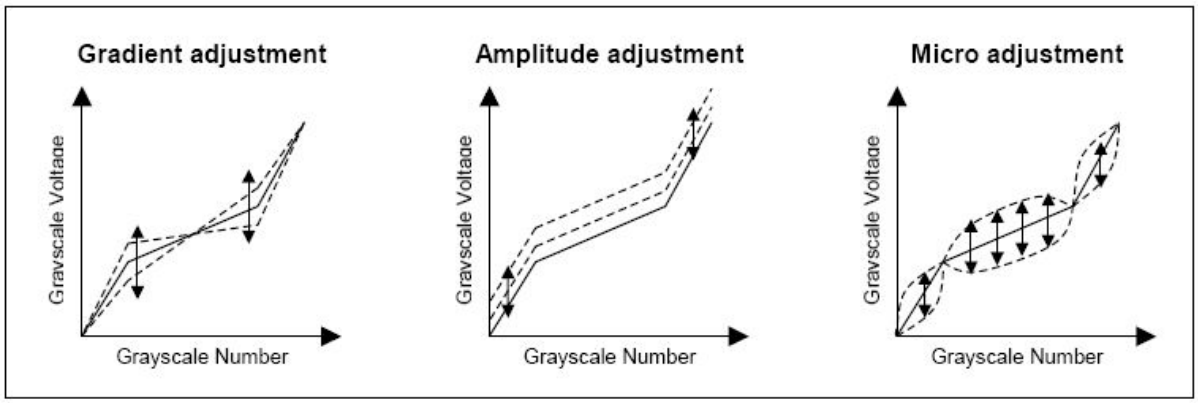


Figure 9. 4: Gamma adjustment function

9.2.1 Gradient adjusting register

The gradient-adjusting resistor is to adjust around middle gradient, specification of the grayscale number and the grayscale voltage without changing the dynamic range. To accomplish the adjustment, it controls the variable resistors in the middle of the ladder resistor by registers (PRP(N)0 / PRP(N)1) for the grayscale voltage generator. Also, there is an independent resistor on the positive/negative polarities in order for corresponding to asymmetry drive.

9.2.2 Amplitude adjusting register

The amplitude-adjusting resistor is to adjust amplitude of the grayscale voltage. To accomplish the adjustment, it controls the variable resistors in the boundary of the ladder resistor by registers (VRP(N)0 / VRP(N)1) for the grayscale voltage generator. Also, there is an independent resistor on the positive/negative polarities as well as the gradient-adjusting resistor.

9.2.3 Micro adjusting register

The micro-adjusting register is to make subtle adjustment of the grayscale voltage level. To accomplish the adjustment, it controls each reference voltage level by the 8 to 1 selector towards the 8-level reference voltage generated from the ladder resistor. Also, there is an independent resistor on the positive/negative polarities as well as other adjusting resistors.

9.3 Ladder resistor / 8 to 1 selector

This block outputs the reference voltage of the grayscale voltage. There are two ladder resistors including the variable resistor and the 8 to 1 selector selecting voltage generated by the ladder resistor. The gamma registers control the variable resistors and 8 to 1 selector resistors. Also, there has pin (EXVR) that can be connected to VSS or an external variable resistor for compensating the dispersion of length between both panels.

Variable resistor

There are 3 types of the variable resistors that are for the gradient and amplitude adjustment. The resistance is set by the resistor (PRP(N)0 / PRP(N)1) and (VRP(N)0 / VRP(N)1) as below.

PRP(N)[0:1]	Resistance
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Table 9. 1: PRP(N)

VRP(N)0	Resistance
0000	0R
0001	2R
0010	4R
: Step = 2R :	
1110	28R
1111	30R

Table 9. 2: VRP(N)0

VRP(N)1	Resistance
00000	0R
00001	1R
00010	2R
: Step = 1R :	
11110	30R
11111	31R

Table 9. 3: VRP(N)1

8 to 1 selector

In the 8 to 1 selector, a reference voltage VIN can be selected from the levels which are generated by the ladder resistors. There are six types of reference voltage (VIN1 to VIN6) and totally 48 divided voltages can be selected in one ladder resistor. Following figure explains the relationship between the micro adjusting register and the selecting voltage.

Positive polarity							Negative polarity						
Register	Selected voltage						Register	Selected voltage					
PKP[2:0]	VINP1	VINP2	VINP3	VINP4	VINP5	VINP6	PKN[2:0]	VINN1	VINN2	VINN3	VINN4	VINN5	VINN6
000	KVP1	KVP9	KVP17	KVP25	KVP33	KVP41	000	KVN1	KVN9	KVN17	KVN25	KVN33	KVN41
001	KVP2	KVP10	KVP18	KVP26	KVP34	KVP42	001	KVN2	KVN10	KVN18	KVN26	KVN34	KVN42
010	KVP3	KVP11	KVP19	KVP27	KVP35	KVP43	010	KVN3	KVN11	KVN19	KVN27	KVN35	KVN43
011	KVP4	KVP12	KVP20	KVP28	KVP36	KVP44	011	KVN4	KVN12	KVN20	KVN28	KVN36	KVN44
100	KVP5	KVP13	KVP21	KVP29	KVP37	KVP45	100	KVN5	KVN13	KVN21	KVN29	KVN37	KVN45
101	KVP6	KVP14	KVP22	KVP30	KVP38	KVP46	101	KVN6	KVN14	KVN22	KVN30	KVN38	KVN46
110	KVP7	KVP15	KVP23	KVP31	KVP39	KVP47	110	KVN7	KVN15	KVN23	KVN31	KVN39	KVN47
111	KVP8	KVP16	KVP24	KVP32	KVP40	KVP48	111	KVN8	KVN16	KVN24	KVN32	KVN40	KVN48

Table 9. 4: PKP and PKN

Grayscale voltage	Positive polarity	Negative polarity
V0	VINP0	VINN7
V1	VINP1	VINN6
V2	V8+(V1-V8)*(2241/2703)	V1+(V8-V1)*(462/2703)
V3	V8+(V1-V8)*(1671/2703)	V1+(V8-V1)*(1032/2703)
V4	V8+(V1-V8)*(1209/2703)	V1+(V8-V1)*(1494/2703)
V5	V8+(V1-V8)*(849/2703)	V1+(V8-V1)*(1854/2703)
V6	V8+(V1-V8)*(567/2703)	V1+(V8-V1)*(2136/2703)
V7	V8+(V1-V8)*(294/2703)	V1+(V8-V1)*(2409/2703)
V8	VINP2	VINN5
V9	V20+(V8-V20)*(1533/1767)	V8+(V20-V8)*(234/1767)
V10	V20+(V8-V20)*(1356/1767)	V8+(V20-V8)*(411/1767)
V11	V20+(V8-V20)*(1188/1767)	V8+(V20-V8)*(579/1767)
V12	V20+(V8-V20)*(993/1767)	V8+(V20-V8)*(774/1767)
V13	V20+(V8-V20)*(843/1767)	V8+(V20-V8)*(924/1767)
V14	V20+(V8-V20)*(693/1767)	V8+(V20-V8)*(1074/1767)
V15	V20+(V8-V20)*(543/1767)	V8+(V20-V8)*(1224/1767)
V16	V20+(V8-V20)*(441/1767)	V8+(V20-V8)*(1326/1767)
V17	V20+(V8-V20)*(336/1767)	V8+(V20-V8)*(1431/1767)
V18	V20+(V8-V20)*(213/1767)	V8+(V20-V8)*(1554/1767)
V19	V20+(V8-V20)*(81/1767)	V8+(V20-V8)*(1686/1767)
V20	VINP3	VINN4
V21	V43+(V20-V43)*(1887/1965)	V20+(V43-V20)*(78/1965)
V22	V43+(V20-V43)*(1779/1965)	V20+(V43-V20)*(186/1965)
V23	V43+(V20-V43)*(1653/1965)	V20+(V43-V20)*(312/1965)
V24	V43+(V20-V43)*(1536/1965)	V20+(V43-V20)*(429/1965)
V25	V43+(V20-V43)*(1437/1965)	V20+(V43-V20)*(528/1965)
V26	V43+(V20-V43)*(1362/1965)	V20+(V43-V20)*(603/1965)
V27	V43+(V20-V43)*(1278/1965)	V20+(V43-V20)*(687/1965)
V28	V43+(V20-V43)*(1191/1965)	V20+(V43-V20)*(774/1965)
V29	V43+(V20-V43)*(1098/1965)	V20+(V43-V20)*(867/1965)
V30	V43+(V20-V43)*(1008/1965)	V20+(V43-V20)*(957/1965)
V31	V43+(V20-V43)*(927/1965)	V20+(V43-V20)*(1038/1965)
V32	V43+(V20-V43)*(843/1965)	V20+(V43-V20)*(1122/1965)
V33	V43+(V20-V43)*(750/1965)	V20+(V43-V20)*(1215/1965)
V34	V43+(V20-V43)*(678/1965)	V20+(V43-V20)*(1287/1965)
V35	V43+(V20-V43)*(612/1965)	V20+(V43-V20)*(1353/1965)
V36	V43+(V20-V43)*(528/1965)	V20+(V43-V20)*(1437/1965)
V37	V43+(V20-V43)*(450/1965)	V20+(V43-V20)*(1515/1965)
V38	V43+(V20-V43)*(375/1965)	V20+(V43-V20)*(1590/1965)
V39	V43+(V20-V43)*(303/1965)	V20+(V43-V20)*(1662/1965)
V40	V43+(V20-V43)*(222/1965)	V20+(V43-V20)*(1743/1965)
V41	V43+(V20-V43)*(147/1965)	V20+(V43-V20)*(1818/1965)
V42	V43+(V20-V43)*(87/1965)	V20+(V43-V20)*(1878/1965)
V43	VINP4	VINN3
V44	V55+(V43-V55)*(936/1014)	V43+(V55-V43)*(78/1014)
V45	V55+(V43-V55)*(867/1014)	V43+(V55-V43)*(147/1014)
V46	V55+(V43-V55)*(792/1014)	V43+(V55-V43)*(222/1014)
V47	V55+(V43-V55)*(723/1014)	V43+(V55-V43)*(291/1014)
V48	V55+(V43-V55)*(648/1014)	V43+(V55-V43)*(366/1014)
V49	V55+(V43-V55)*(561/1014)	V43+(V55-V43)*(453/1014)
V50	V55+(V43-V55)*(465/1014)	V43+(V55-V43)*(549/1014)
V51	V55+(V43-V55)*(387/1014)	V43+(V55-V43)*(627/1014)
V52	V55+(V43-V55)*(291/1014)	V43+(V55-V43)*(723/1014)
V53	V55+(V43-V55)*(201/1014)	V43+(V55-V43)*(813/1014)
V54	V55+(V43-V55)*(111/1014)	V43+(V55-V43)*(903/1014)
V55	VINP5	VINN2
V56	V62+(V55-V62)*(1218/1317)	V55+(V62-V55)*(99/1317)
V57	V62+(V55-V62)*(1092/1317)	V55+(V62-V55)*(225/1317)
V58	V62+(V55-V62)*(936/1317)	V55+(V62-V55)*(381/1317)
V59	V62+(V55-V62)*(774/1317)	V55+(V62-V55)*(543/1317)
V60	V62+(V55-V62)*(579/1317)	V55+(V62-V55)*(738/1317)
V61	V62+(V55-V62)*(324/1317)	V55+(V62-V55)*(993/1317)
V62	VINP6	VINN1
V63	VINP7	VINN0

Table 9. 5: Grayscale voltages formulas

Reference	Formula	Micro-adjusting register	Reference voltage
KVP0	VLCD63 - ΔV x VRP0 / SUMRP	-	VINP0
KVP1	VLCD63 - ΔV x (VRP0 + 5R) / SUMRP	PKP0[2:0] = ”000”	VINP1
KVP2	VLCD63 - ΔV x (VRP0 + 9R) / SUMRP	PKP0[2:0] = ”001”	
KVP3	VLCD63 - ΔV x (VRP0 + 13R) / SUMRP	PKP0[2:0] = ”010”	
KVP4	VLCD63 - ΔV x (VRP0 + 17R) / SUMRP	PKP0[2:0] = ”011”	
KVP5	VLCD63 - ΔV x (VRP0 + 21R) / SUMRP	PKP0[2:0] = ”100”	
KVP6	VLCD63 - ΔV x (VRP0 + 25R) / SUMRP	PKP0[2:0] = ”101”	
KVP7	VLCD63 - ΔV x (VRP0 + 29R) / SUMRP	PKP0[2:0] = ”110”	
KVP8	VLCD63 - ΔV x (VRP0 + 33R) / SUMRP	PKP0[2:0] = ”111”	
KVP9	VLCD63 - ΔV x (VRP0 + 33R + VRHP) / SUMRP	PKP1[2:0] = ”000”	VINP2
KVP10	VLCD63 - ΔV x (VRP0 + 34R + VRHP) / SUMRP	PKP1[2:0] = ”001”	
KVP11	VLCD63 - ΔV x (VRP0 + 35R + VRHP) / SUMRP	PKP1[2:0] = ”010”	
KVP12	VLCD63 - ΔV x (VRP0 + 36R + VRHP) / SUMRP	PKP1[2:0] = ”011”	
KVP13	VLCD63 - ΔV x (VRP0 + 37R + VRHP) / SUMRP	PKP1[2:0] = ”100”	
KVP14	VLCD63 - ΔV x (VRP0 + 38R + VRHP) / SUMRP	PKP1[2:0] = ”101”	
KVP15	VLCD63 - ΔV x (VRP0 + 39R + VRHP) / SUMRP	PKP1[2:0] = ”110”	
KVP16	VLCD63 - ΔV x (VRP0 + 40R + VRHP) / SUMRP	PKP1[2:0] = ”111”	
KVP17	VLCD63 - ΔV x (VRP0 + 45R + VRHP) / SUMRP	PKP2[2:0] = ”000”	VINP3
KVP18	VLCD63 - ΔV x (VRP0 + 46R + VRHP) / SUMRP	PKP2[2:0] = ”001”	
KVP19	VLCD63 - ΔV x (VRP0 + 47R + VRHP) / SUMRP	PKP2[2:0] = ”010”	
KVP20	VLCD63 - ΔV x (VRP0 + 48R + VRHP) / SUMRP	PKP2[2:0] = ”011”	
KVP21	VLCD63 - ΔV x (VRP0 + 49R + VRHP) / SUMRP	PKP2[2:0] = ”100”	
KVP22	VLCD63 - ΔV x (VRP0 + 50R + VRHP) / SUMRP	PKP2[2:0] = ”101”	
KVP23	VLCD63 - ΔV x (VRP0 + 51R + VRHP) / SUMRP	PKP2[2:0] = ”110”	
KVP24	VLCD63 - ΔV x (VRP0 + 52R + VRHP) / SUMRP	PKP2[2:0] = ”111”	
KVP25	VLCD63 - ΔV x (VRP0 + 68R + VRHP) / SUMRP	PKP3[2:0] = ”000”	VINP4
KVP26	VLCD63 - ΔV x (VRP0 + 69R + VRHP) / SUMRP	PKP3[2:0] = ”001”	
KVP27	VLCD63 - ΔV x (VRP0 + 70R + VRHP) / SUMRP	PKP3[2:0] = ”010”	
KVP28	VLCD63 - ΔV x (VRP0 + 71R + VRHP) / SUMRP	PKP3[2:0] = ”011”	
KVP29	VLCD63 - ΔV x (VRP0 + 72R + VRHP) / SUMRP	PKP3[2:0] = ”100”	
KVP30	VLCD63 - ΔV x (VRP0 + 73R + VRHP) / SUMRP	PKP3[2:0] = ”101”	
KVP31	VLCD63 - ΔV x (VRP0 + 74R + VRHP) / SUMRP	PKP3[2:0] = ”110”	
KVP32	VLCD63 - ΔV x (VRP0 + 75R + VRHP) / SUMRP	PKP3[2:0] = ”111”	
KVP33	VLCD63 - ΔV x (VRP0 + 80R + VRHP) / SUMRP	PKP4[2:0] = ”000”	VINP5
KVP34	VLCD63 - ΔV x (VRP0 + 81R + VRHP) / SUMRP	PKP4[2:0] = ”001”	
KVP35	VLCD63 - ΔV x (VRP0 + 82R + VRHP) / SUMRP	PKP4[2:0] = ”010”	
KVP36	VLCD63 - ΔV x (VRP0 + 83R + VRHP) / SUMRP	PKP4[2:0] = ”011”	
KVP37	VLCD63 - ΔV x (VRP0 + 84R + VRHP) / SUMRP	PKP4[2:0] = ”100”	
KVP38	VLCD63 - ΔV x (VRP0 + 85R + VRHP) / SUMRP	PKP4[2:0] = ”101”	
KVP39	VLCD63 - ΔV x (VRP0 + 86R + VRHP) / SUMRP	PKP4[2:0] = ”110”	
KVP40	VLCD63 - ΔV x (VRP0 + 87R + VRHP) / SUMRP	PKP4[2:0] = ”111”	
KVP41	VLCD63 - ΔV x (VRP0 + 87R + VRHP + VRLP) / SUMRP	PKP5[2:0] = ”000”	VINP6
KVP42	VLCD63 - ΔV x (VRP0 + 91R + VRHP + VRLP) / SUMRP	PKP5[2:0] = ”001”	
KVP43	VLCD63 - ΔV x (VRP0 + 95R + VRHP + VRLP) / SUMRP	PKP5[2:0] = ”010”	
KVP44	VLCD63 - ΔV x (VRP0 + 99R + VRHP + VRLP) / SUMRP	PKP5[2:0] = ”011”	
KVP45	VLCD63 - ΔV x (VRP0 + 103R + VRHP + VRLP) / SUMRP	PKP5[2:0] = ”100”	
KVP46	VLCD63 - ΔV x (VRP0 + 107R + VRHP + VRLP) / SUMRP	PKP5[2:0] = ”101”	
KVP47	VLCD63 - ΔV x (VRP0 + 111R + VRHP + VRLP) / SUMRP	PKP5[2:0] = ”110”	
KVP48	VLCD63 - ΔV x (VRP0 + 115R + VRHP + VRLP) / SUMRP	PKP5[2:0] = ”111”	
KVP49	VLCD63 - ΔV x (VRP0 + 120R + VRHP + VRLP) / SUMRP	-	VINP7

Note: (1) SUMRP: Total of the positive polarity ladder resistance = 128R + VRHP + VRLP + VRP0 + VRP1
(2) ΔV: Voltage difference between VLCD63 and of EXVR.

Table 9. 6: Reference voltages of positive polarity

Reference	Formula	Micro-adjusting register	Reference voltage
KVN0	VLCD63 - ΔV x VRN0 / SUMRN	-	VINN0
KVN1	VLCD63 - ΔV x (VRN0 + 5R) / SUMRN	PKN0[2:0] = ”000”	VINN1
KVN2	VLCD63 - ΔV x (VRN0 + 9R) / SUMRN	PKN0[2:0] = ”001”	
KVN3	VLCD63 - ΔV x (VRN0 + 13R) / SUMRN	PKN0[2:0] = ”010”	
KVN4	VLCD63 - ΔV x (VRN0 + 17R) / SUMRN	PKN0[2:0] = ”011”	
KVN5	VLCD63 - ΔV x (VRN0 + 21R) / SUMRN	PKN0[2:0] = ”100”	
KVN6	VLCD63 - ΔV x (VRN0 + 25R) / SUMRN	PKN0[2:0] = ”101”	
KVN7	VLCD63 - ΔV x (VRN0 + 29R) / SUMRN	PKN0[2:0] = ”110”	
KVN8	VLCD63 - ΔV x (VRN0 + 33R) / SUMRN	PKN0[2:0] = ”111”	
KVN9	VLCD63 - ΔV x (VRN0 + 33R + VRHN) / SUMRN	PKN1[2:0] = ”000”	VINN2
KVN10	VLCD63 - ΔV x (VRN0 + 34R + VRHN) / SUMRN	PKN1[2:0] = ”001”	
KVN11	VLCD63 - ΔV x (VRN0 + 35R + VRHN) / SUMRN	PKN1[2:0] = ”010”	
KVN12	VLCD63 - ΔV x (VRN0 + 36R + VRHN) / SUMRN	PKN1[2:0] = ”011”	
KVN13	VLCD63 - ΔV x (VRN0 + 37R + VRHN) / SUMRN	PKN1[2:0] = ”100”	
KVN14	VLCD63 - ΔV x (VRN0 + 38R + VRHN) / SUMRN	PKN1[2:0] = ”101”	
KVN15	VLCD63 - ΔV x (VRN0 + 39R + VRHN) / SUMRN	PKN1[2:0] = ”110”	
KVN16	VLCD63 - ΔV x (VRN0 + 40R + VRHN) / SUMRN	PKN1[2:0] = ”111”	
KVN17	VLCD63 - ΔV x (VRN0 + 45R + VRHN) / SUMRN	PKN2[2:0] = ”000”	VINN3
KVN18	VLCD63 - ΔV x (VRN0 + 46R + VRHN) / SUMRN	PKN2[2:0] = ”001”	
KVN19	VLCD63 - ΔV x (VRN0 + 47R + VRHN) / SUMRN	PKN2[2:0] = ”010”	
KVN20	VLCD63 - ΔV x (VRN0 + 48R + VRHN) / SUMRN	PKN2[2:0] = ”011”	
KVN21	VLCD63 - ΔV x (VRN0 + 49R + VRHN) / SUMRN	PKN2[2:0] = ”100”	
KVN22	VLCD63 - ΔV x (VRN0 + 50R + VRHN) / SUMRN	PKN2[2:0] = ”101”	
KVN23	VLCD63 - ΔV x (VRN0 + 51R + VRHN) / SUMRN	PKN2[2:0] = ”110”	
KVN24	VLCD63 - ΔV x (VRN0 + 52R + VRHN) / SUMRN	PKN2[2:0] = ”111”	
KVN25	VLCD63 - ΔV x (VRN0 + 68R + VRHN) / SUMRN	PKN3[2:0] = ”000”	VINN4
KVN26	VLCD63 - ΔV x (VRN0 + 69R + VRHN) / SUMRN	PKN3[2:0] = ”001”	
KVN27	VLCD63 - ΔV x (VRN0 + 70R + VRHN) / SUMRN	PKN3[2:0] = ”010”	
KVN28	VLCD63 - ΔV x (VRN0 + 71R + VRHN) / SUMRN	PKN3[2:0] = ”011”	
KVN29	VLCD63 - ΔV x (VRN0 + 72R + VRHN) / SUMRN	PKN3[2:0] = ”100”	
KVN30	VLCD63 - ΔV x (VRN0 + 73R + VRHN) / SUMRN	PKN3[2:0] = ”101”	
KVN31	VLCD63 - ΔV x (VRN0 + 74R + VRHN) / SUMRN	PKN3[2:0] = ”110”	
KVN32	VLCD63 - ΔV x (VRN0 + 75R + VRHN) / SUMRN	PKN3[2:0] = ”111”	
KVN33	VLCD63 - ΔV x (VRN0 + 80R + VRHN) / SUMRN	PKN4[2:0] = ”000”	VINN5
KVN34	VLCD63 - ΔV x (VRN0 + 81R + VRHN) / SUMRN	PKN4[2:0] = ”001”	
KVN35	VLCD63 - ΔV x (VRN0 + 82R + VRHN) / SUMRN	PKN4[2:0] = ”010”	
KVN36	VLCD63 - ΔV x (VRN0 + 83R + VRHN) / SUMRN	PKN4[2:0] = ”011”	
KVN37	VLCD63 - ΔV x (VRN0 + 84R + VRHN) / SUMRN	PKN4[2:0] = ”100”	
KVN38	VLCD63 - ΔV x (VRN0 + 85R + VRHN) / SUMRN	PKN4[2:0] = ”101”	
KVN39	VLCD63 - ΔV x (VRN0 + 86R + VRHN) / SUMRN	PKN4[2:0] = ”110”	
KVN40	VLCD63 - ΔV x (VRN0 + 87R + VRHN) / SUMRN	PKN4[2:0] = ”111”	
KVN41	VLCD63 - ΔV x (VRN0 + 87R + VRHN + VRLN) / SUMRN	PKN5[2:0] = ”000”	VINN6
KVN42	VLCD63 - ΔV x (VRN0 + 91R + VRHN + VRLN) / SUMRN	PKN5[2:0] = ”001”	
KVN43	VLCD63 - ΔV x (VRN0 + 95R + VRHN + VRLN) / SUMRN	PKN5[2:0] = ”010”	
KVN44	VLCD63 - ΔV x (VRN0 + 99R + VRHN + VRLN) / SUMRN	PKN5[2:0] = ”011”	
KVN45	VLCD63 - ΔV x (VRN0 + 103R + VRHN + VRLN) / SUMRN	PKN5[2:0] = ”100”	
KVN46	VLCD63 - ΔV x (VRN0 + 107R + VRHN + VRLN) / SUMRN	PKN5[2:0] = ”101”	
KVN47	VLCD63 - ΔV x (VRN0 + 111R + VRHN + VRLN) / SUMRN	PKN5[2:0] = ”110”	
KVN48	VLCD63 - ΔV x (VRN0 + 115R + VRHN + VRLN) / SUMRN	PKN5[2:0] = ”111”	
KVN49	VLCD63 - ΔV x (VRN0 + 120R + VRHN + VRLN) / SUMRN	-	VINN7

Note: (1) SUMRN: Total of the negative polarity ladder resistance = 128R + VRHN + VRLN + VRN0 + VRN1
(2) ΔV: Voltage difference between VLCD63 and of EXVR.

Table 9. 7: Reference voltages of negative polarity

10. Maximum Rating

Maximum ratings (Voltage referenced to VSS)

Symbol	Parameter	Spec.			Unit
		Min.	Typ.	Max.	
VDD	Supply Voltage	-0.3	-	2.7	V
VDDIO		-0.3	-	4.0	V
VCI	Input Voltage	VSS-0.3	-	3.96	V
I	Current Drain Per Pin Excluding VDD and VSS	-	25	-	mA
TA	Operating Temperature	-30	-	85	℃
Tstg	Storage Temperature	-65	-	150	℃

Table 10. 1: Maximum ratings

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that VCI and VOUT be constrained to the range VSS < VDDIO ≤VCI < VOUT.

Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either VSS or VDDIO).

Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

11. DC Characteristics

DC characteristics

(Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DDIO} = 2.2V, T_A = 25℃)

Symbol	Parameter	Test condition	Spec.			Unit
			Min.	Typ.	Max.	
V_{DD}	System power supply pins of the logic block	Recommend Operating Voltage Possible Operating Voltage	1.8	-	2.50	V
V_{DDIO}	Power supply pin of IO pins	Recommend Operating Voltage Possible Operating Voltage	1.8	-	3.6	V
V_{CI}	Booster Reference Supply Voltage Range	Recommend Operating Voltage Possible Operating Voltage	2.5 or VDDIO	-	3.6	V
I_{sleep}	Sleep mode current	-	-	50	-	μA
I_{dp}	Operating mode current	VCI=3.3V	-	10	12	mA
V_{CIM}	Negative V_{CI} Output Voltage	No panel loading	- VCI	-	- VCI+0.7	V
V_{CIX2}	V_{CIX2} primary booster efficiency(1)	No panel loading, ITO for V_{CIX2}, V_{CI} and V_{CHS} = 10 Ohm	83	90	-	%
V_{GH}	Gate driver High Output Voltage Booster efficiency(2)	No panel loading; 4x booster; ITO for C_{YP}, C_{YN}, V_{CIX2}, V_{CI} and V_{CHS} = 10 Ohm	84	89.5	-	%
		No panel loading; 5x booster; ITO for C_{YP}, C_{YN}, V_{CIX2}, V_{CI} and V_{CHS} = 10 Ohm	80	88.5	-	%
		No panel loading; 6x booster; ITO for C_{YP}, C_{YN}, V_{CIX2}, V_{CI} and V_{CHS} = 10 Ohm	72	80	-	%
V_{GL}	Gate driver Low Output Voltage	-	- V_{GH}		-5.1	V
V_{COMH}	VCOM High Output Voltage	-	-	-	5.54	V
V_{COML}	VCOM Low Output Voltage	-	V_{CIM}+0.5	-	-	V
V_{COMA}	VCOM Amplitude	-	-	-	6	V
V_{LCD63}	V_{LCD63} Output Voltage	-	-	-	5.57	V
△V_{LCD63}	Max. Source Voltage Variation	-	-2	-	2	%
V_{OH1}	Logic High Output Voltage	Iout = -100μA	0.9V_{DDIO}	-	V_{DD}	V
V_{VD}	Source Output Voltage Deviation	-	-	±20	-	mV
V_{OS}	Source Output Voltage Offset	-	-	-	±30	mV
V_{OL1}	Logic Low Output Voltage	Iout = 100μA	0	-	0.1V_{DDIO}	V
V_{IH1}	Logic High Input voltage	-	0.8V_{DDIO}	-	V_{DDIO}	V
V_{IL1}	Logic Low Input voltage	-	0	-	0.2V_{DDIO}	V
I_{OH}	Logic High Output Current Source	V out = VDD – 0.4V	50	-	-	μA
I_{OL}	Logic Low Output Current Drain	V out = 0.4V	-	-	-50	μA
I_{OZ}	Logic Output Tri-state Current Drain Source	-	-1	-	1	μA
$I_{IL/I\ IH}$	Logic Input Current	-	-1	-	1	μA
C_{IN}	Logic Pins Input Capacitance	-	-	5	7.5	pF
R_{SON}	Source drivers output resistance	-	-	1	-	kΩ
R_{GON}	Gate drivers output resistance	-	-	500	-	Ω
R_{CON}	VCOM output resistance	-	-	200	-	Ω

Note : (1) VCIX2 efficiency=VCIX2 / (2 x VCI) x 100%
(2) VGH efficiency=VGH / (VCI x n) x 100% (where n=booster factor)

Table 11. 1: DC Characteristics

12. AC Characteristics

AC characteristics

(Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DDIO} = 2.2V, T_A = 25℃)

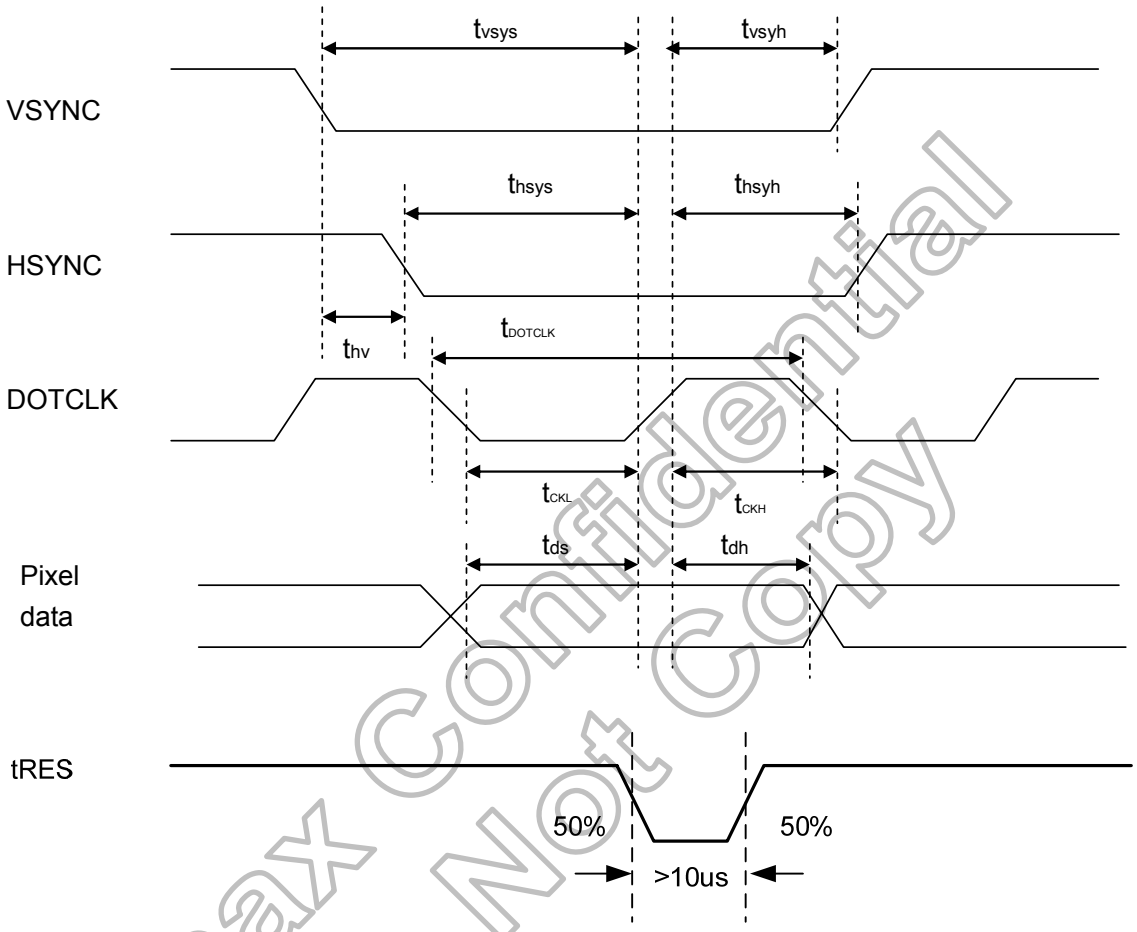


Figure 12. 1: Pixel timing

Characteristics	Symbol	Min.		Typ.		Max.		Unit
		24-bit	8-bit	24- bit	8-bit	24-bit	8-bit	
DOTCLK Frequency	fDOTCLK	-	-	6.5	19.5	10	30	MHz
DOTCLK Period	tDOTCLK	100	33.3	154	51.3	-	-	ns
Vertical Sync Setup Time	tvsys	20	10	-	-	-	-	ns
Vertical Sync Hold Time	tvsyh	20	10	-	-	-	-	ns
Horizontal Sync Setup Time	thsys	20	10	-	-	-	-	ns
Horizontal Sync Hold Time	thsyh	20	10	-	-	-	-	ns
Phase difference of Sync Signal Falling Edge	thv	1		-		240		tDOTCLK
DOTCLK Low Period	tCKL	50	15	-	-	-	-	ns
DOTCLK High Period	tCKH	50	15	-	-	-	-	ns
Data Setup Time	tds	12	10	-	-	-	-	ns
Data hold Time	tdh	12	10	-	-	-	-	ns
Reset pulse width	tRES	10		-		-		μs

Note: External clock source must be provided to DOTCLK pin of HX8238-D. The driver will not operate if absent of the clocking signal.

Table 12. 1: Pixel timing

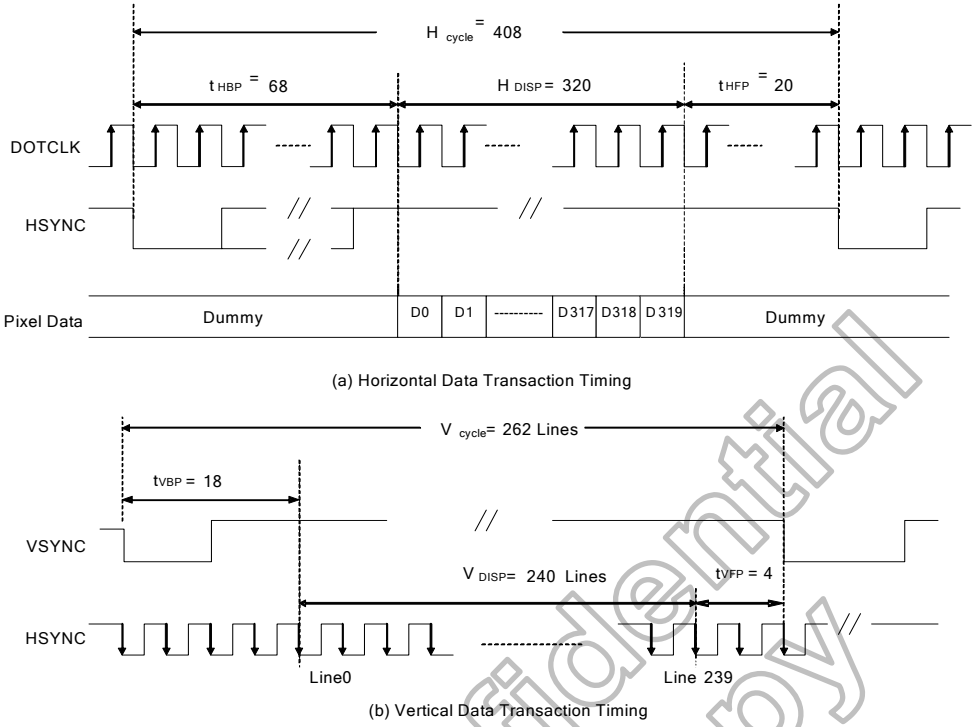


Figure 12. 2: Data transaction timing in parallel RGB (24-bit) interface (SYNC mode)

Characteristics		Symbol	Min.		Typ.		Max.		Unit
			24-bit	8-bit	24- bit	8-bit	24-bit	8-bit	
DOTCLK Frequency		fDOTCLK	-	-	6.5	19.5	10	30	MHz
DOTCLK Period		tDOTCLK	100	33.3	154	51.3	-	-	ns
Horizontal Frequency (Line)		fH	-		15.75		22.35		KHz
Vertical Frequency (Refresh)		fV	-		60		90		Hz
Horizontal Back Porch		tHBP	-	-	68	204	-	-	tDOTCLK
Horizontal Front Porch		tHFP	-	-	20	60	-	-	tDOTCLK
Hsync LOW Pulse Width		tWH	2		32				tDOTCLK
Horizontal Data Start Point		tHBP	9	27	68	204	127	381	tDOTCLK
Horizontal Blanking Period		tHBP + tHFP	52	146	88	264	180	960	tDOTCLK
Horizontal Display Area		HDISP	-	-	320	960	-	-	tDOTCLK
Horizontal Cycle		Hcycle	350	1106	408	1224	500	1500	tDOTCLK
VSYNC Low Pulse Width		tWV	2		4				Lines
Vertical Back Porch		tVBP	2		18		127		Lines
Vertical Front Porch		tVFP	-		4		-		Lines
Vertical Data Start Point		tVBP	-		18		-		Lines
Vertical Blanking Period	NTSC	tVBP + tVFP	10		22		47		Lines
	PAL		20		33		120		
	PAL		12		25		112		
Vertical Display Area	NTSC	VDISP	-		240		-		Lines
	PAL				280(PALM=0)				
	PAL				288(PALM=1)				
Vertical Cycle	NTSC	Vcycle	250		262		287		Lines
	PAL		300		313		400		

Table 12. 2: Data transaction timing in normal operating mode

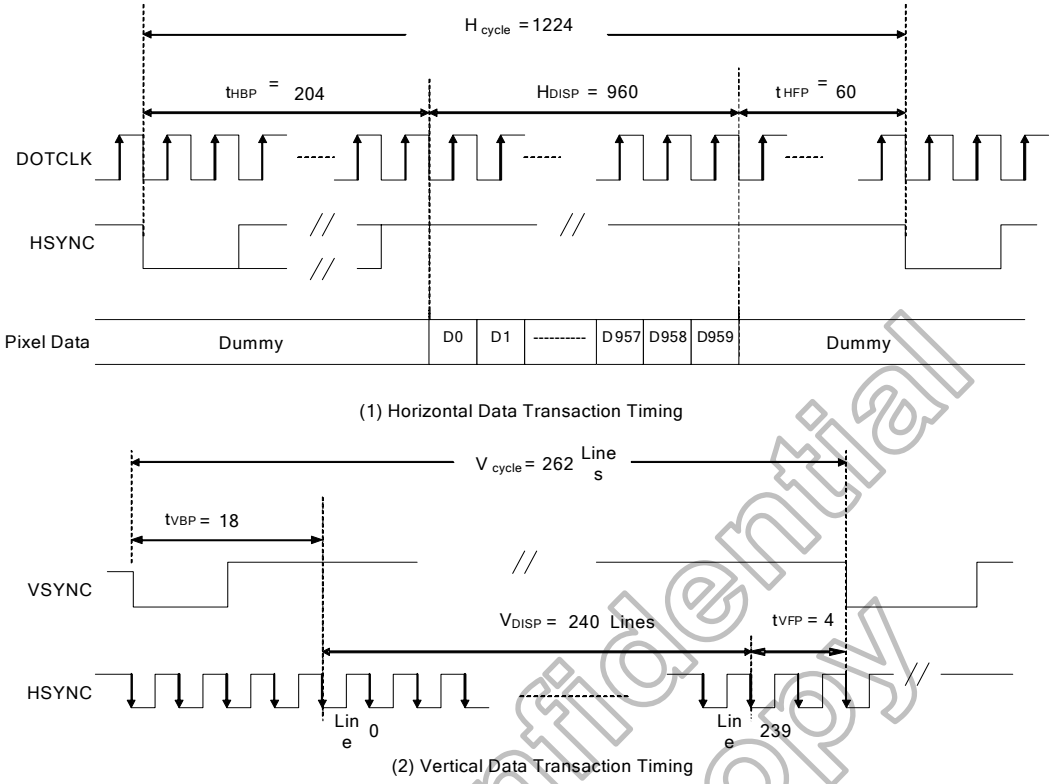


Figure 12. 3: Data transaction timing in serial RGB (8-bit) interface (SYNC mode)

Characteristics	Symbol	Min.		Typ.		Max.		Unit
		24-bit	8-bit	24- bit	8-bit	24-bit	8-bit	
DOTCLK Frequency	fDOTCLK	-	-	6.5	19.5	10	30	MHz
DOTCLK Period	tDOTCLK	100	33.3	154	51.3	-	-	ns
Horizontal Blanking Period	tHBP + tHFP	52	146	88	264	180	960	tDOTCLK
Horizontal Display Area	HDISP	-	-	320	960	-	-	tDOTCLK
Horizontal Cycle	Hcycle	372	1106	408	1224	500	1920	tDOTCLK
Vertical Blanking Period	tVBP + tVFP	2		-		47		Lines
Vertical Display Area	VDISP	-		240		-		Lines
Vertical Cycle	Vcycle	242		-		287		Lines

Table 12. 3: Data transaction timing in DE only operating mode

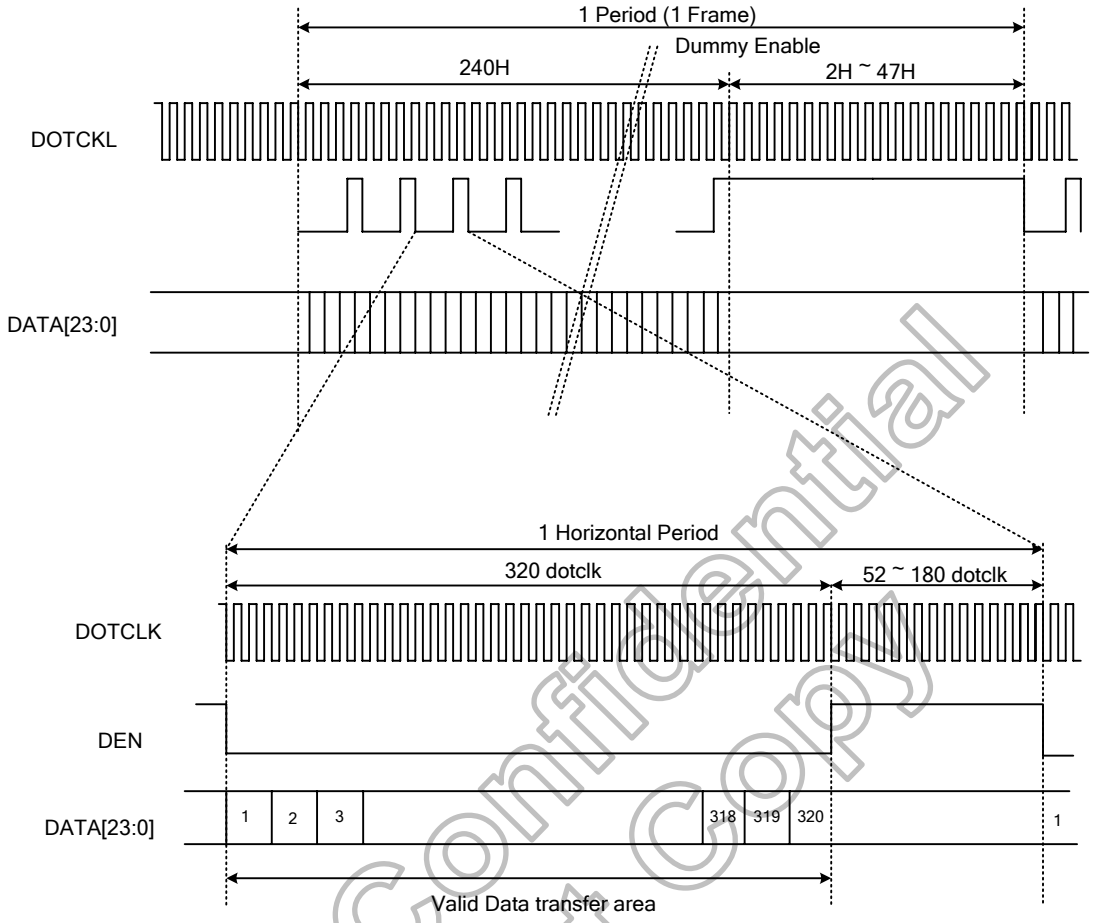
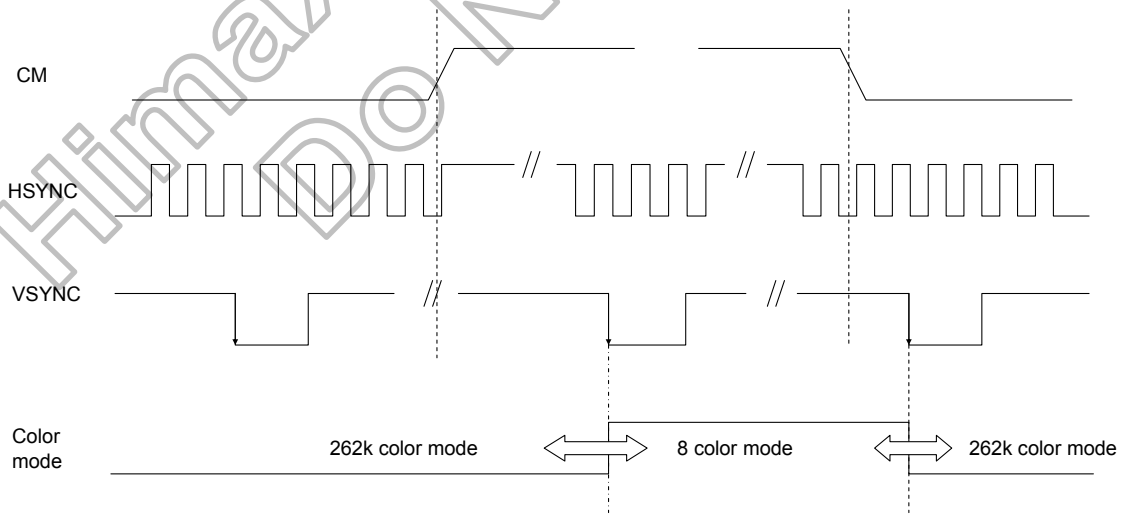


Figure 12. 4: Signal timing in DE only mode



Note: The color mode conversion starts at the first falling edge of VSYNC after stage change of CM.

Figure 12. 5: Color mode conversion timing

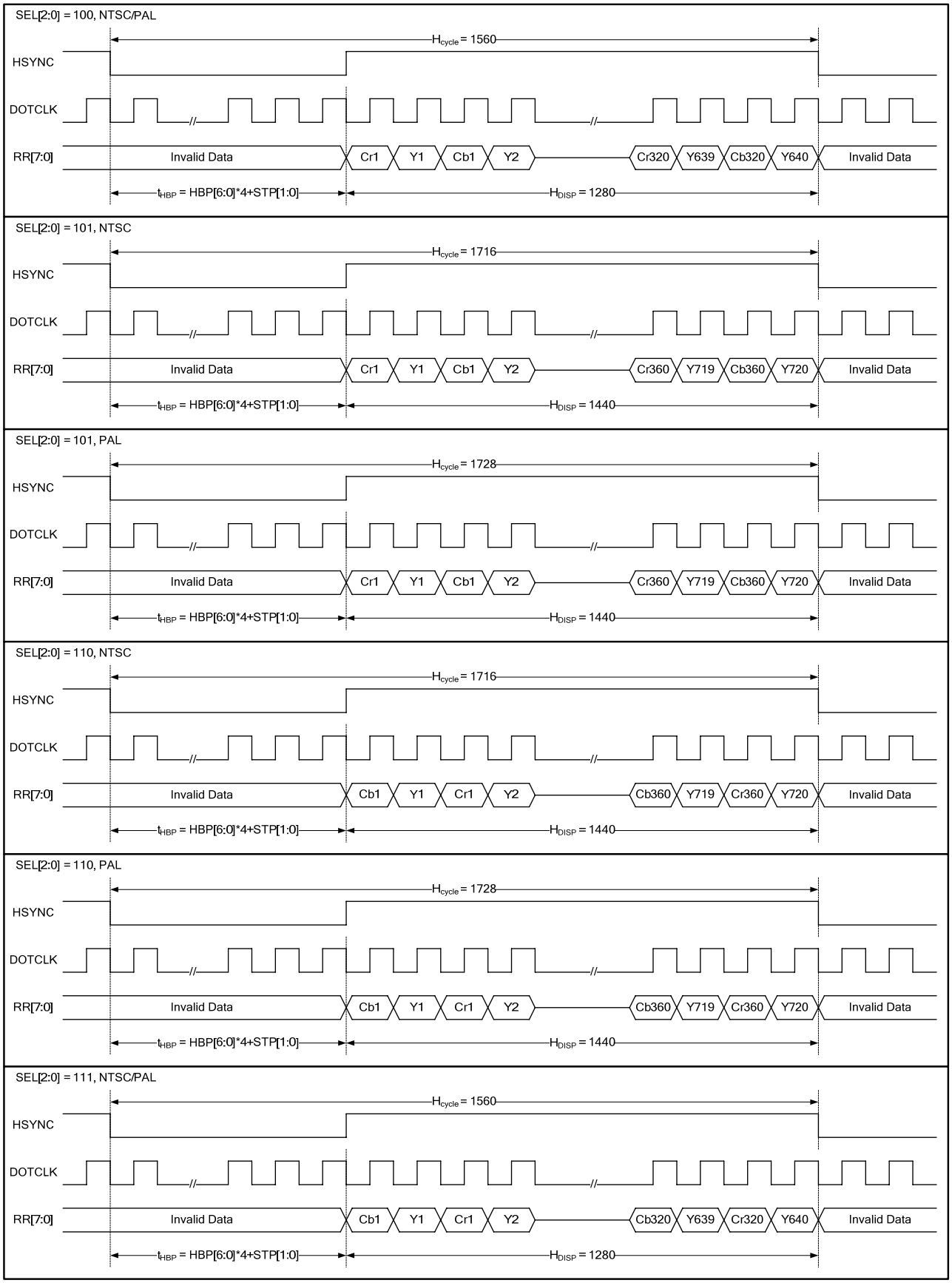


Figure 12. 6: CCIR601 horizontal timing

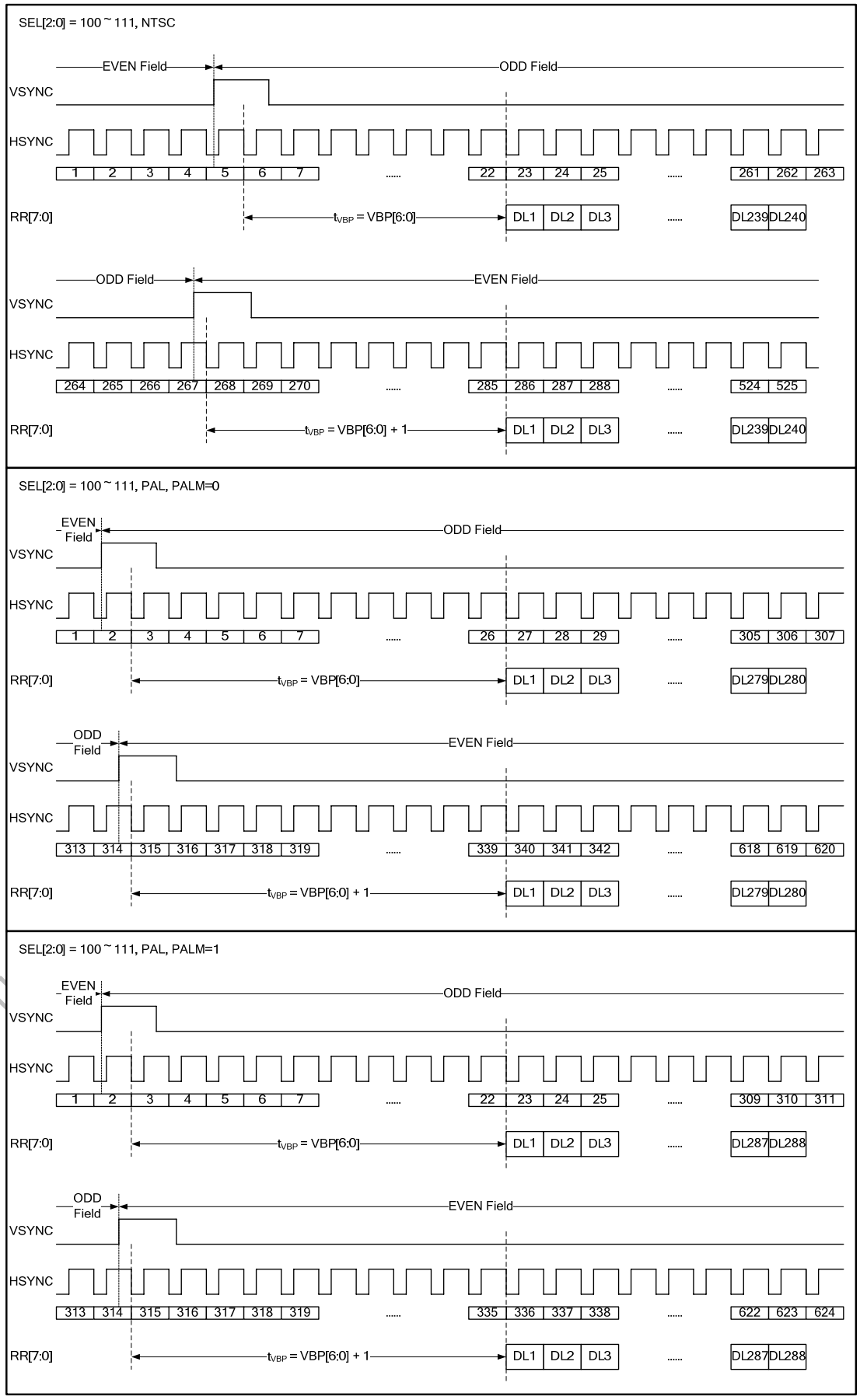


Figure 12. 7: CCIR601 vertical timing

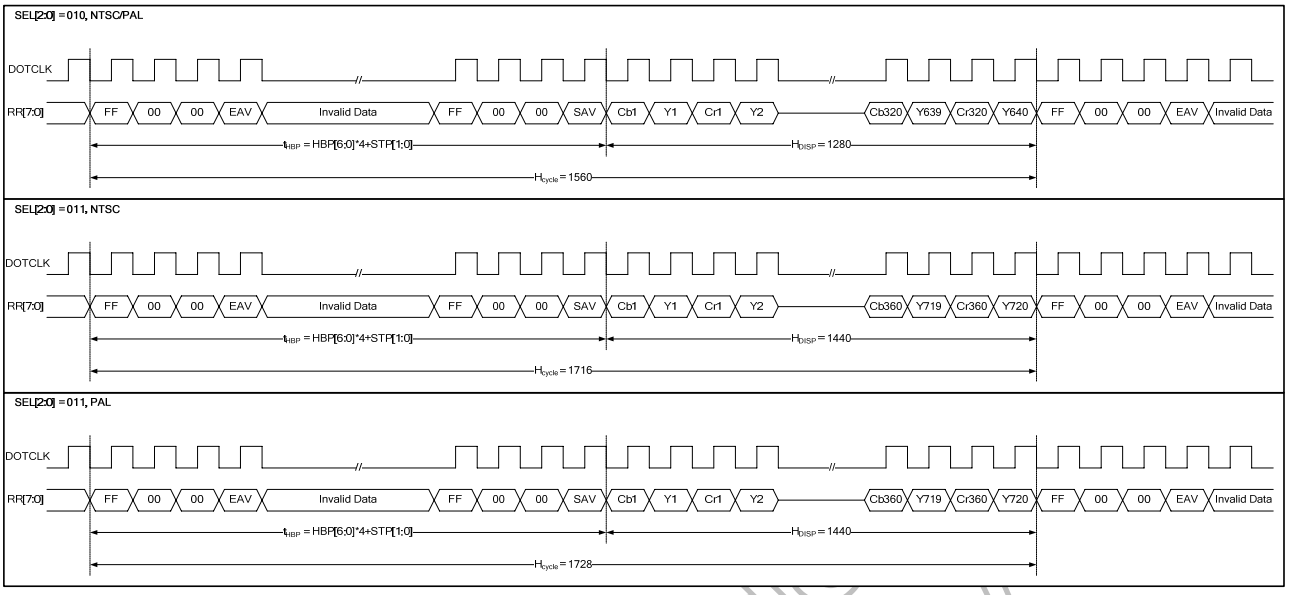


Figure 12. 8: CCIR656 horizontal timing

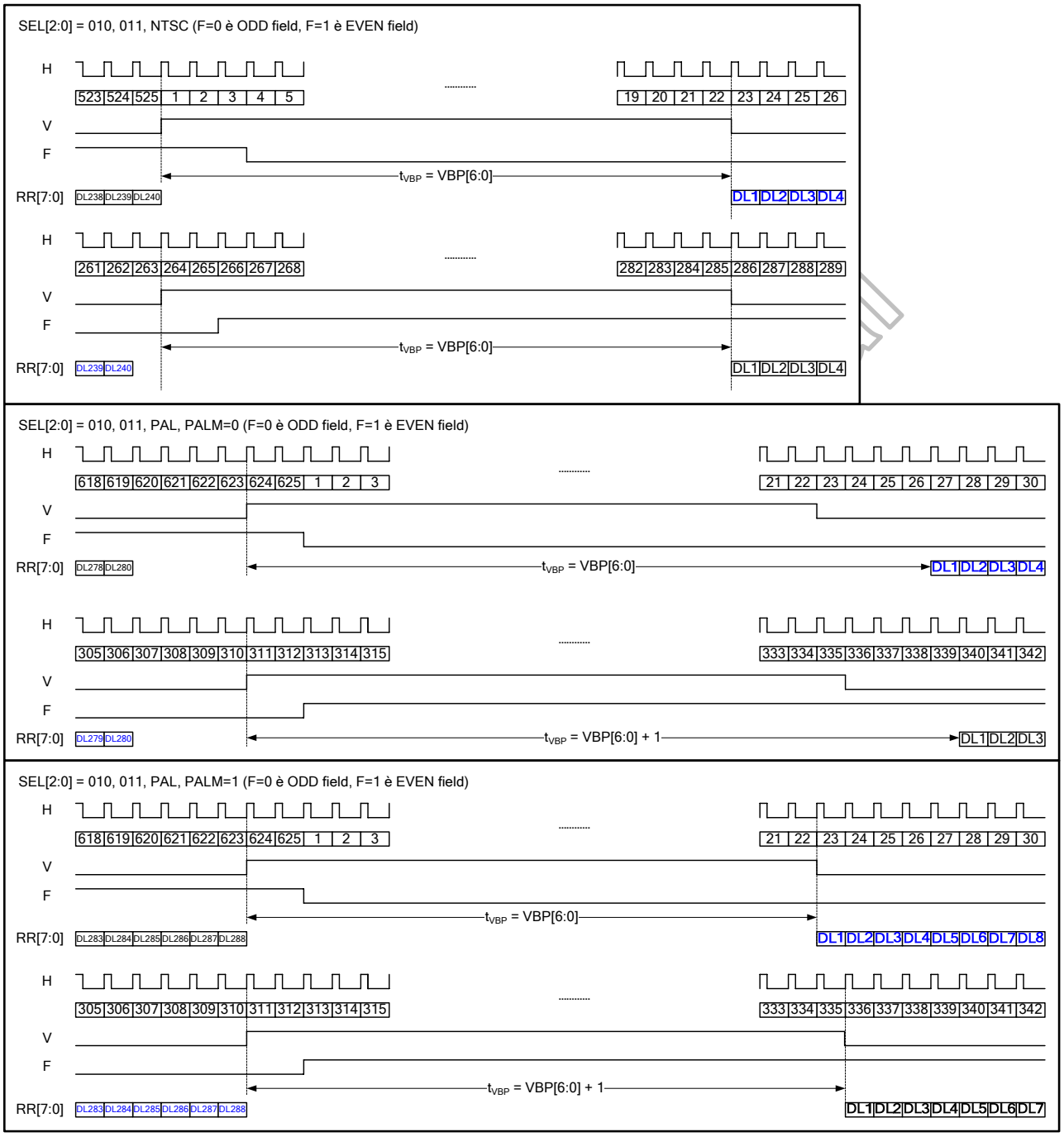


Figure 12. 9: CCIR656 vertical timing

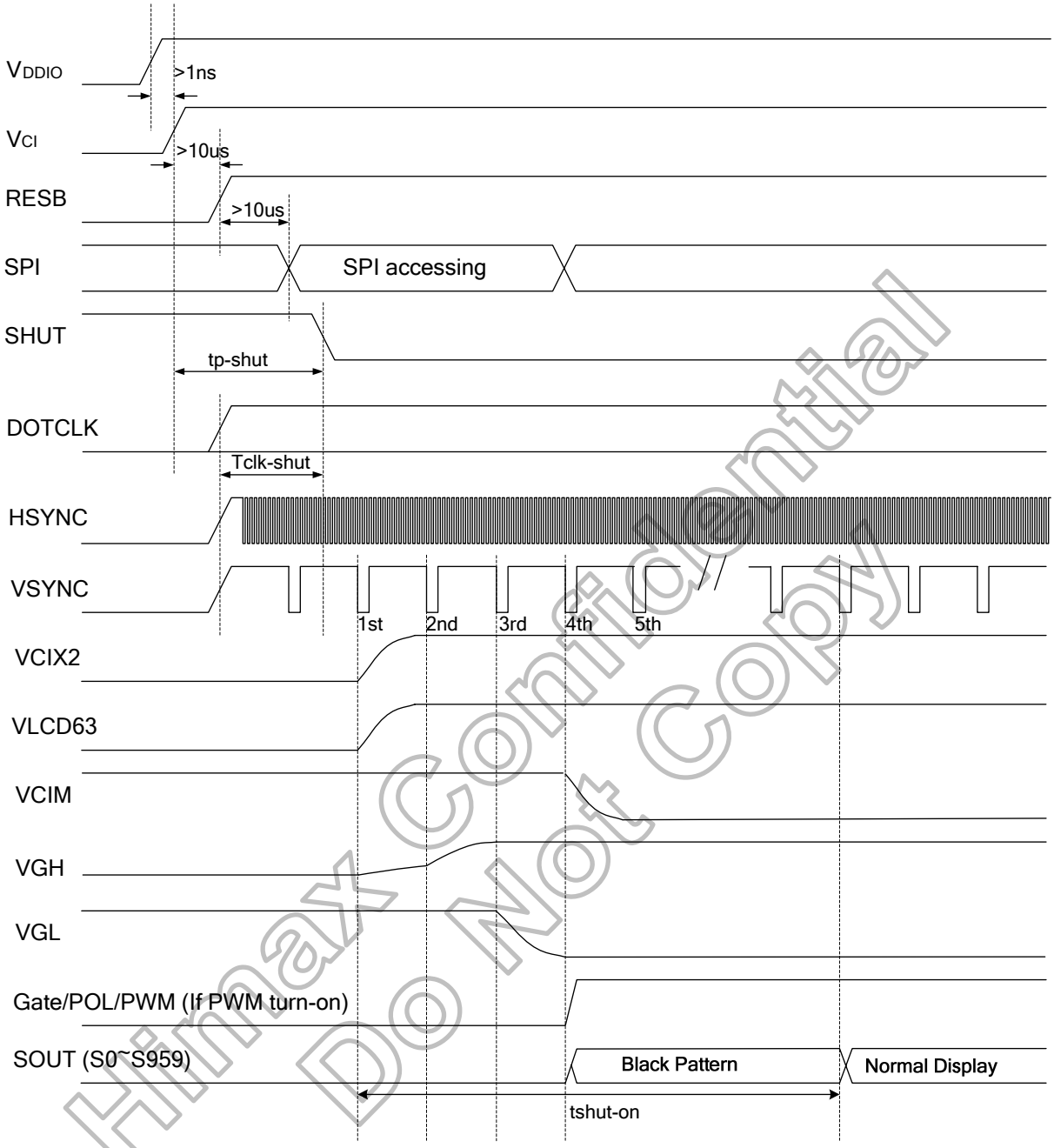


Figure 12. 10: Power up sequence

Characteristics	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
VCI / VDDIO on to falling edge of SHUT	tp-shut	1	-	-	µs
DOTCLK to falling edge of SHUT	tclk-shut (Note 1)	1	-	-	clk
Falling edge of SHUT to display start -1 line: 408 clk -1 frame: 262 line -DOTCLK = 6.5MHz	tshut-on (Note 2)	-	-	14	frame

Note: (1) It is necessary to input DOTCLK before the falling edge of SHUT.
(2) Display starts at 14th falling edge of VSTNC after the falling edge of SHUT. The display starts at the falling edge of VSYNC which is determined by BLT[1:0] of R04h.

Table 12. 4: Power up sequence with SHUT

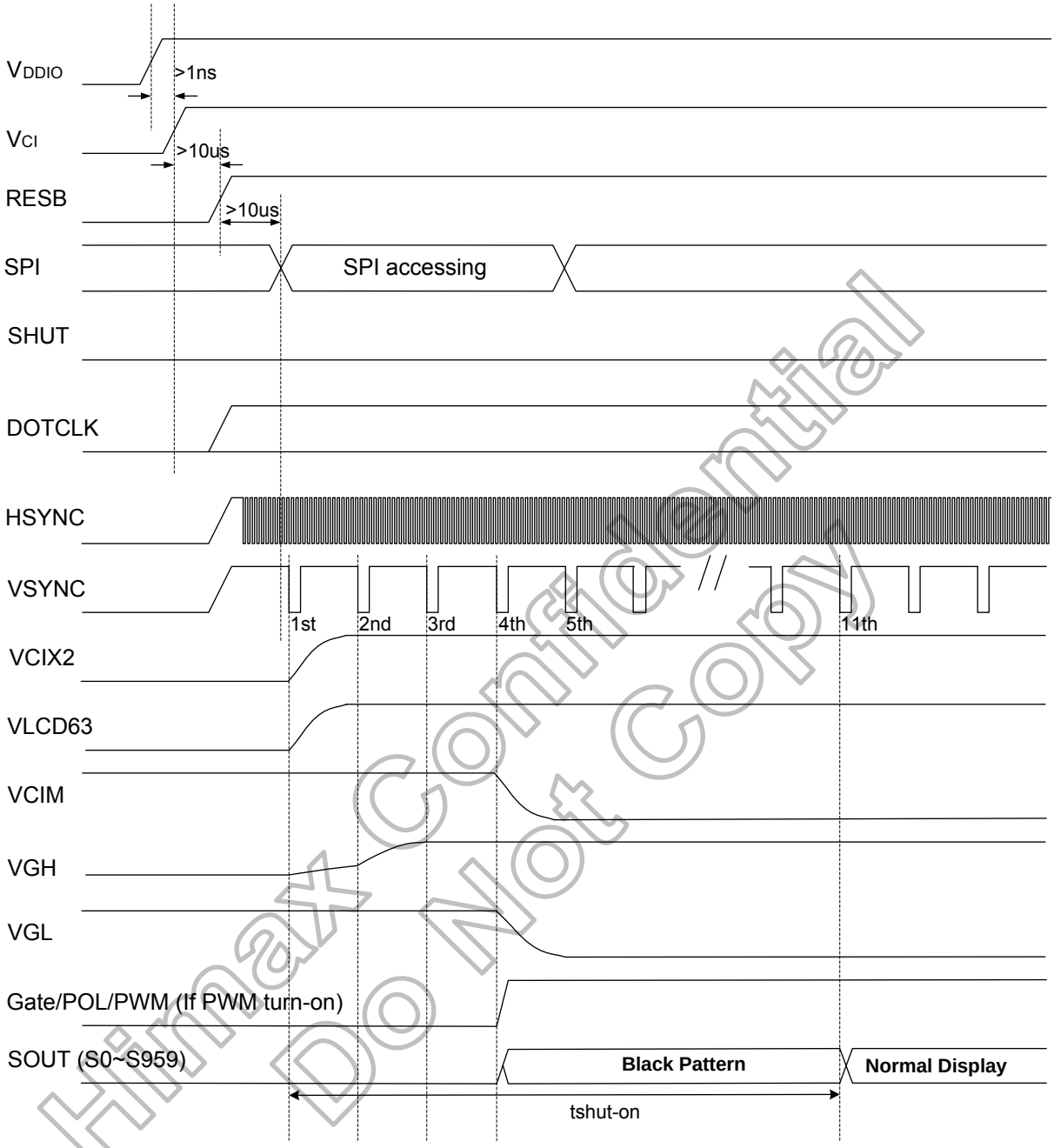


Figure 12. 11: Power up sequence without SHUT

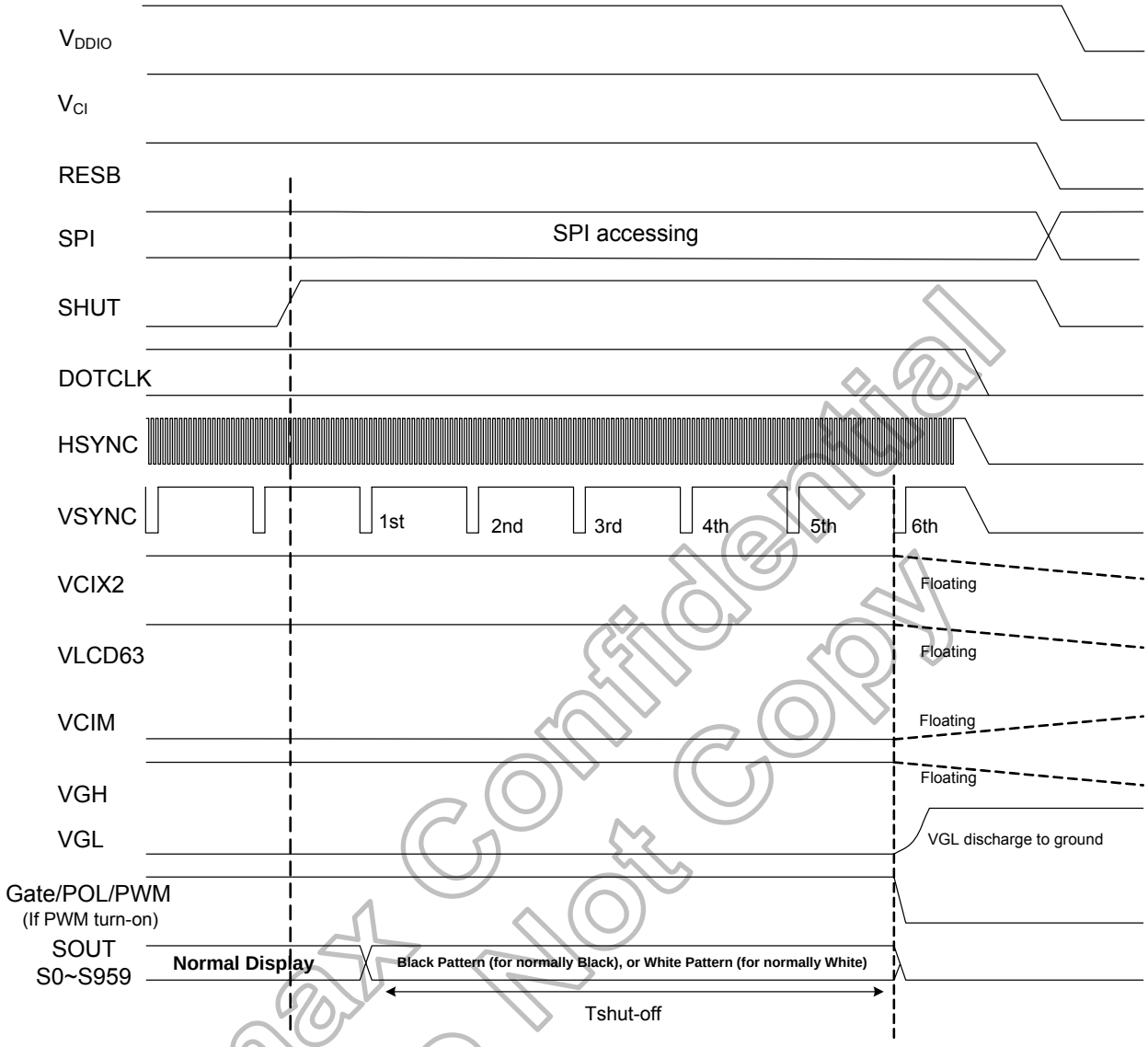


Figure 12. 12: Power down sequence

Characteristics	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Rising edge of SHUT to display off -1 line: 408 clk -1 frame: 262 line -DOTCLK=6.5MHz	tshut-off	-	-	6	frame

Note: DOTCLK must be maintained at lease 6 frames after the rising edge of SHUT.
Display become off at the 6th falling edge of VSYNC after the rising edge of SHUT.
If RESET signal is necessary for power down, provide it after the 6-frames-cycle of the SHUT period.

Table 12. 5: Power down sequence with SHUT

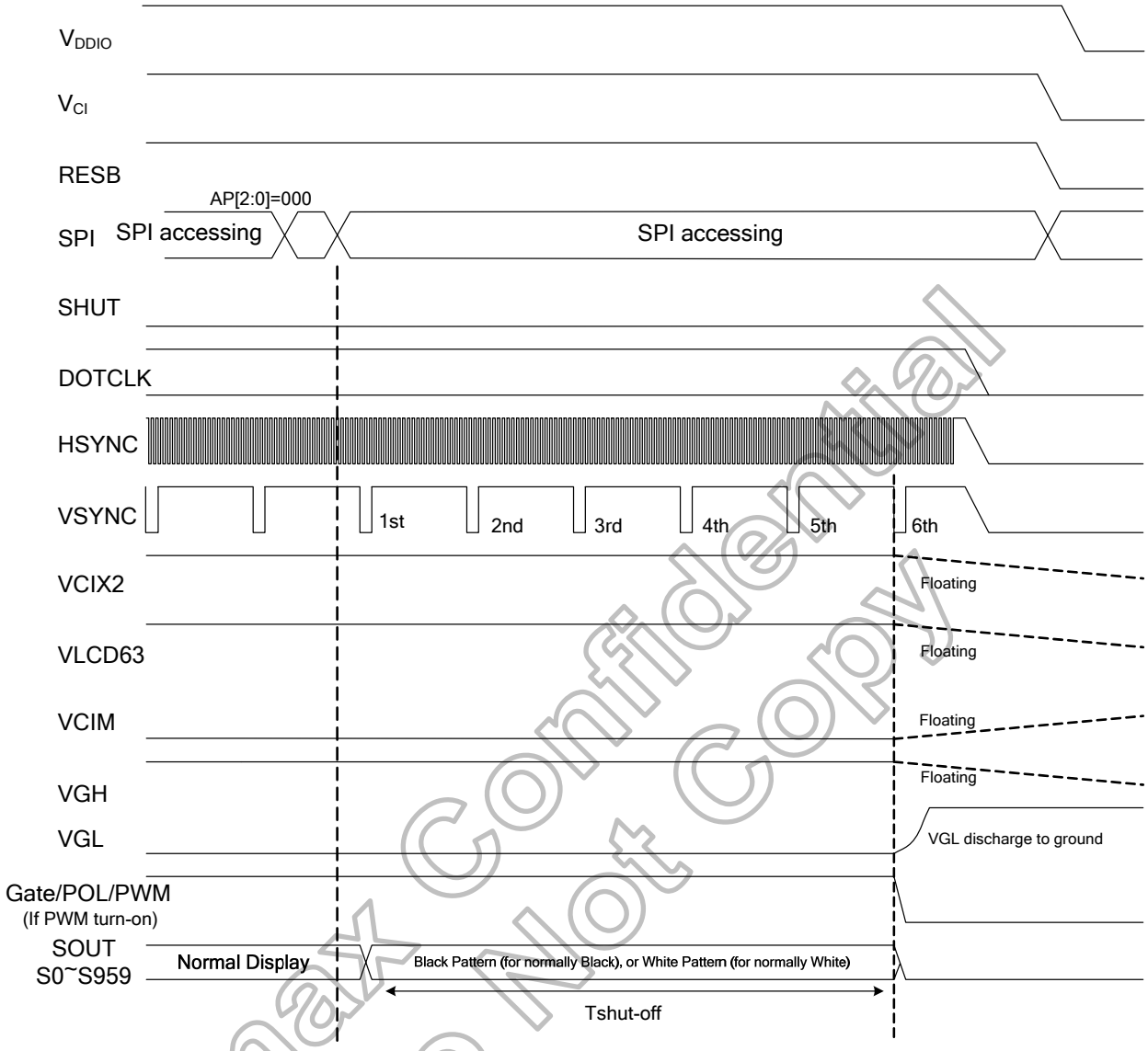
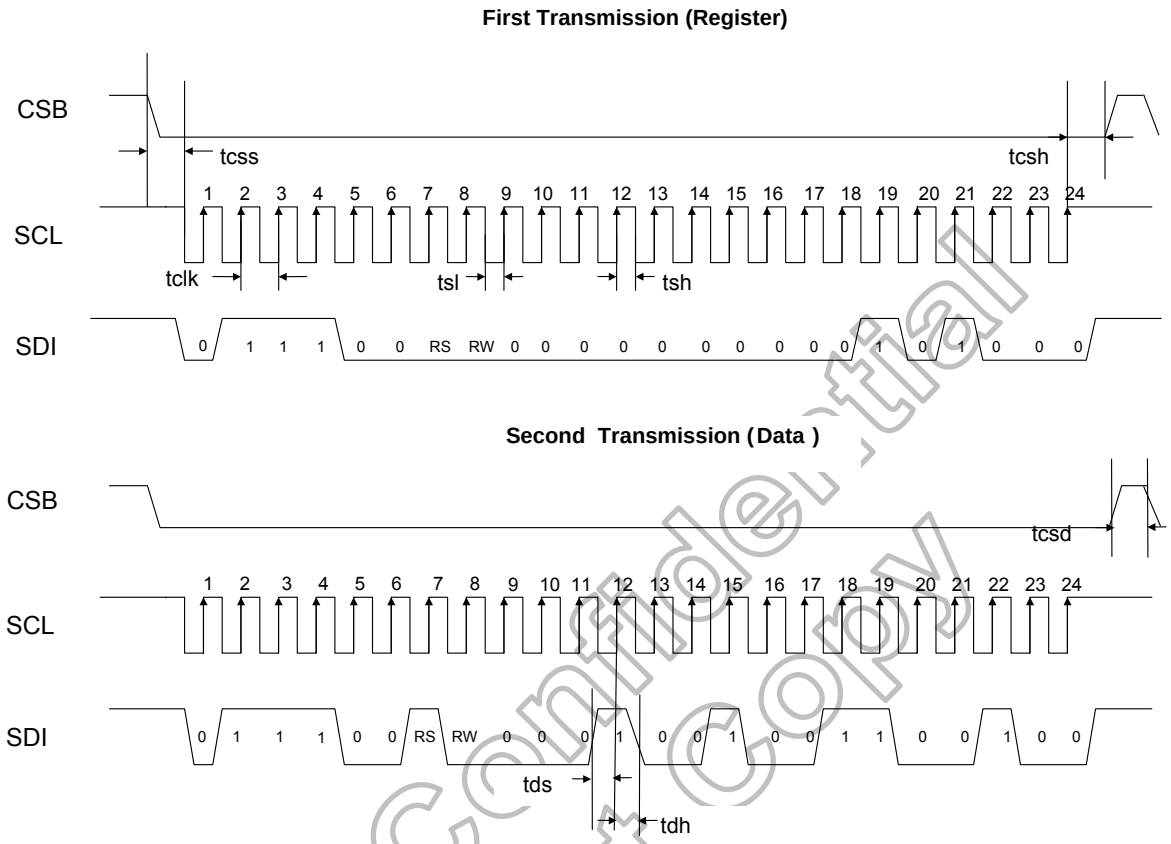


Figure 12. 13: Power down sequence without SHUT

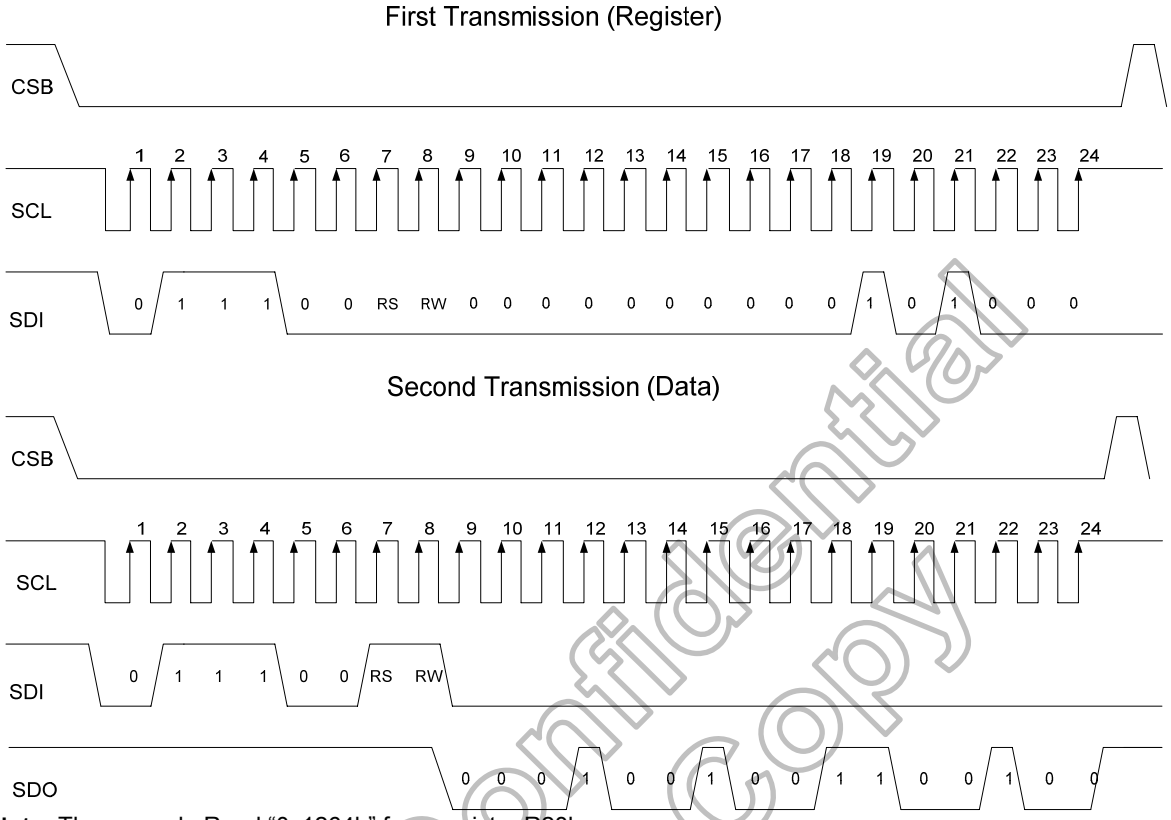
- Write SPI



Note: The example writes “0x1264h” to register R28h.
SPID connected to VSS.

Figure 12. 14: (a) SPI interface timing diagram & write SPI example

- Read SPI



Note: The example Read “0x1264h” from register R28h.

Figure 12. 15: (b) SPI interface timing diagram & read SPI example

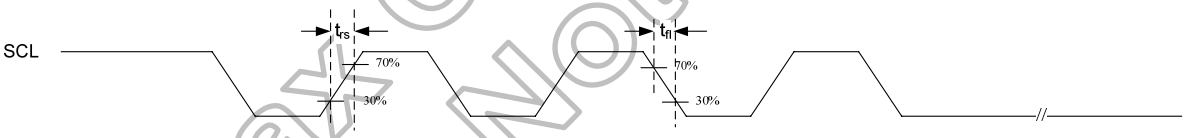
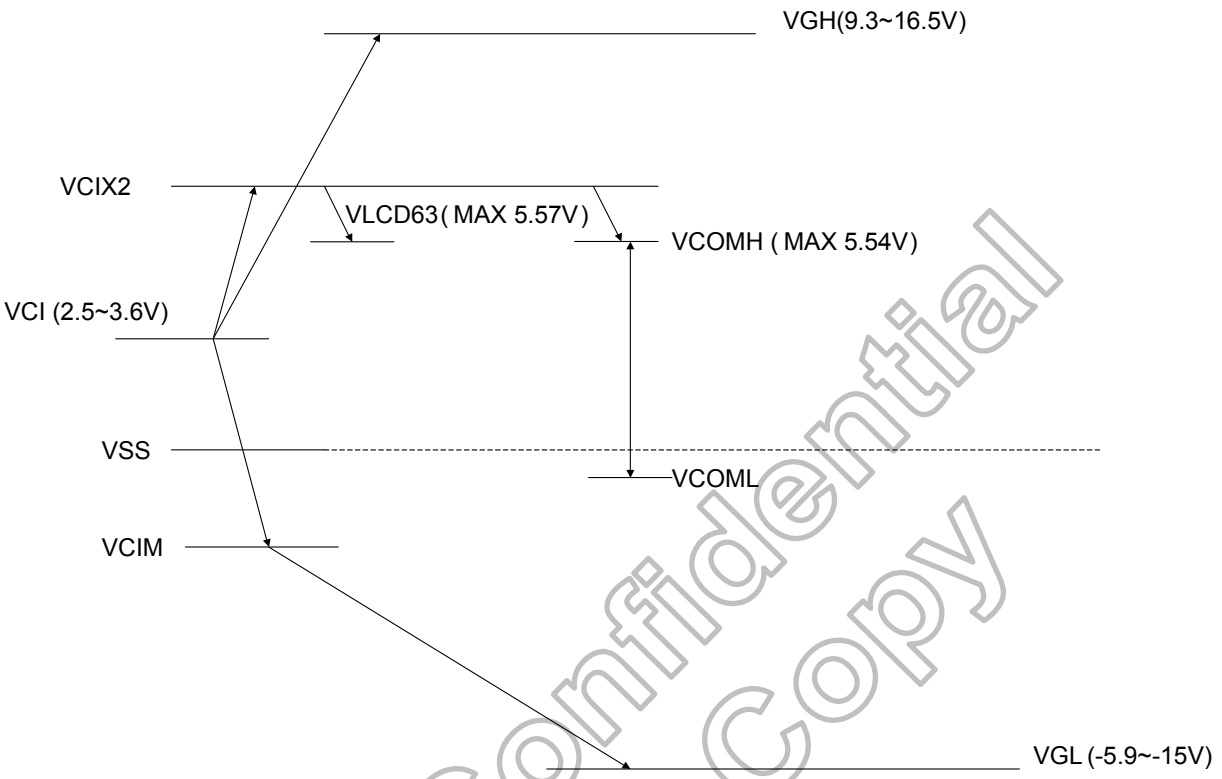


Figure 12. 16: Rising/Falling time

Characteristics	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Serial Clock Frequency	fclk	-	-	20	MHz
Serial Clock Cycle Time	tclk	50	-	-	ns
Clock Low Width	tsl	25	-	-	ns
Clock High Width	tsh	25	-	-	ns
Clock Rising Time	trs	-	-	30	ns
Clock Falling Time	tfl	-	-	30	ns
Chip Select Hold Time	tcsh	10	-	-	ns
Chip Select High Delay Time	tcsd	20	-	-	ns
Data Setup Time	tds	5	-	-	ns
Data Hold Time	tdh	10	-	-	ns

Table 12. 6: SPI timing

13. HX8238-D Output Voltage Relationship



Note: The above voltages level assumed 100% efficiency of the internal booster. There has no voltage drop due to resistance from ITO trace of the panel.

Figure 13. 1: LCD driving voltage relationship

14. Application Circuit

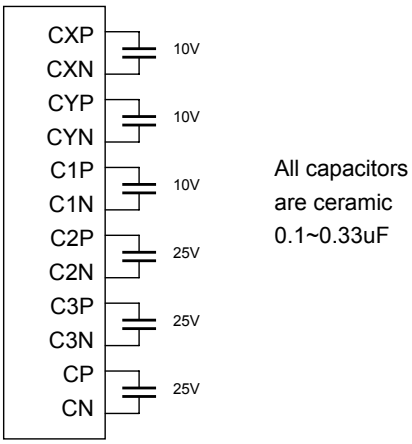


Figure 14. 1: Booster capacitors

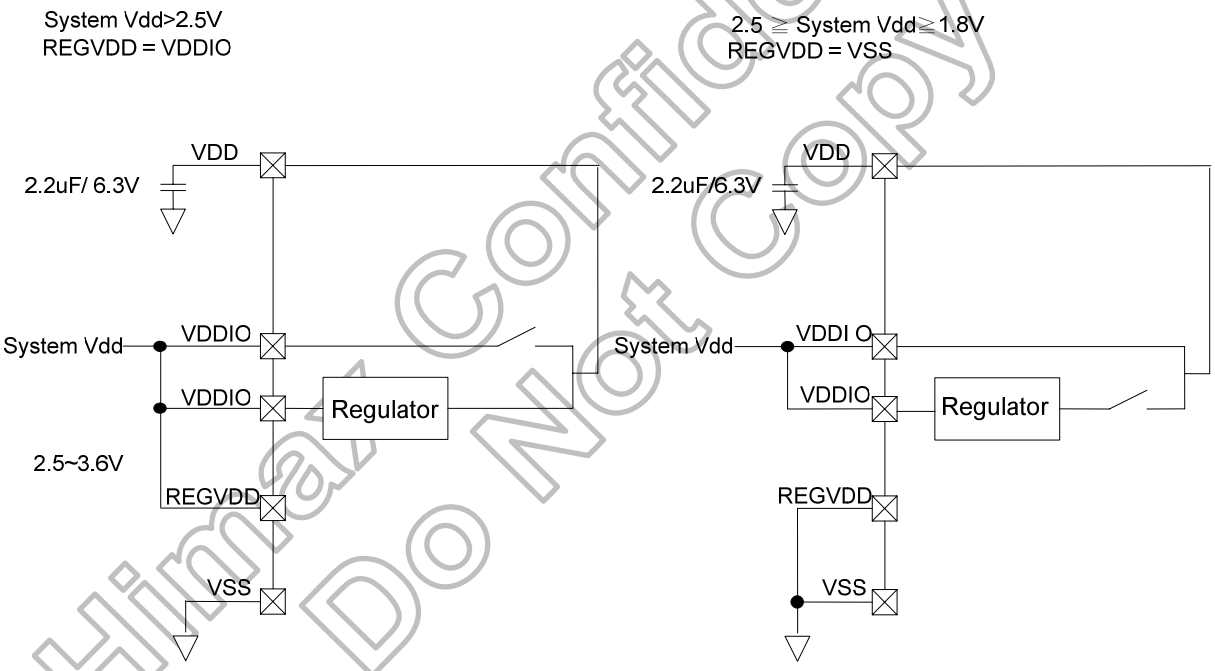


Figure 14. 2: Power supply pins connections

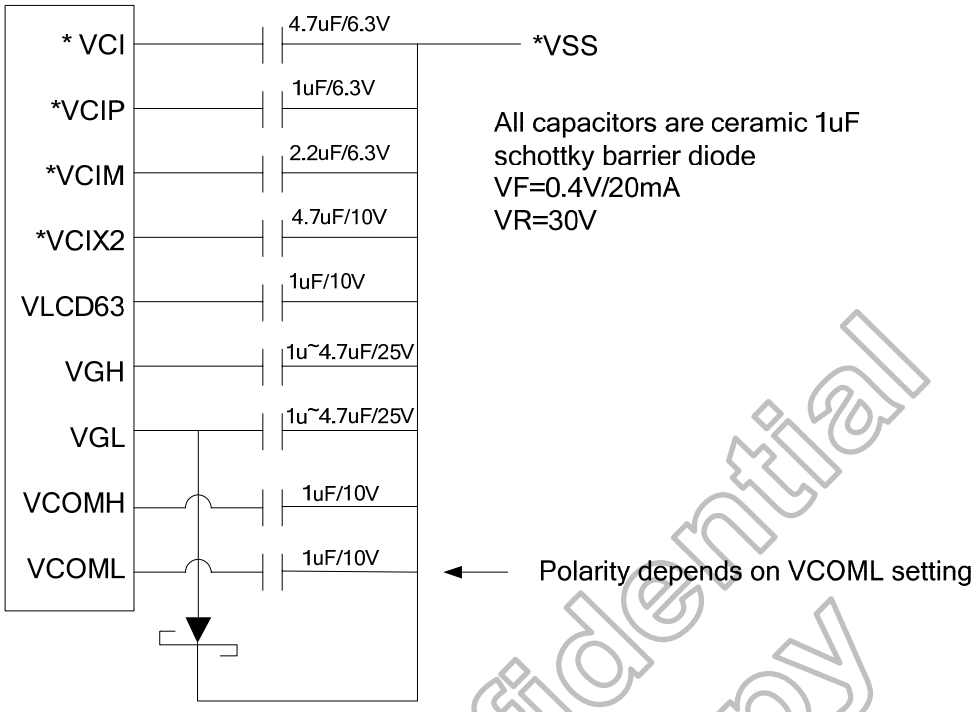


Figure 14. 3: Filtering and charge sharing capacitors

(1) Capacitors on VCI should be 4.7μF.
(2) Capacitors on VCIM should be 2.2μF.
(3) Capacitors on VCIX2 should be 4.7μF.
(4) Capacitors on VGH, VGL should be 1~4.7μF.
(5) Other capacitors should be 1μF.

* VCI should be separate with VCIP at ITO layout to provide noise free path
* VSS, VCHS, AVSS, and VSSRC should be separated at ITO layout to provide noise free path

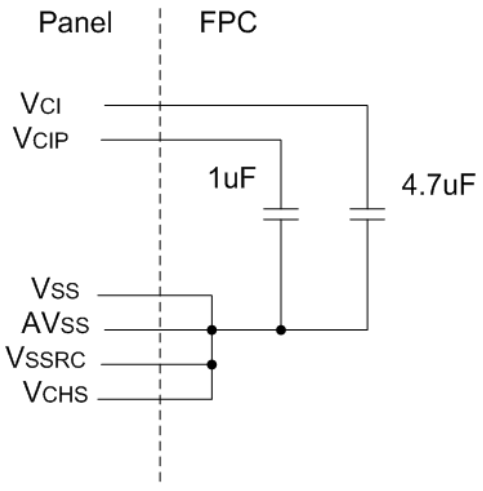


Figure 14. 4: Panel and FPC connection

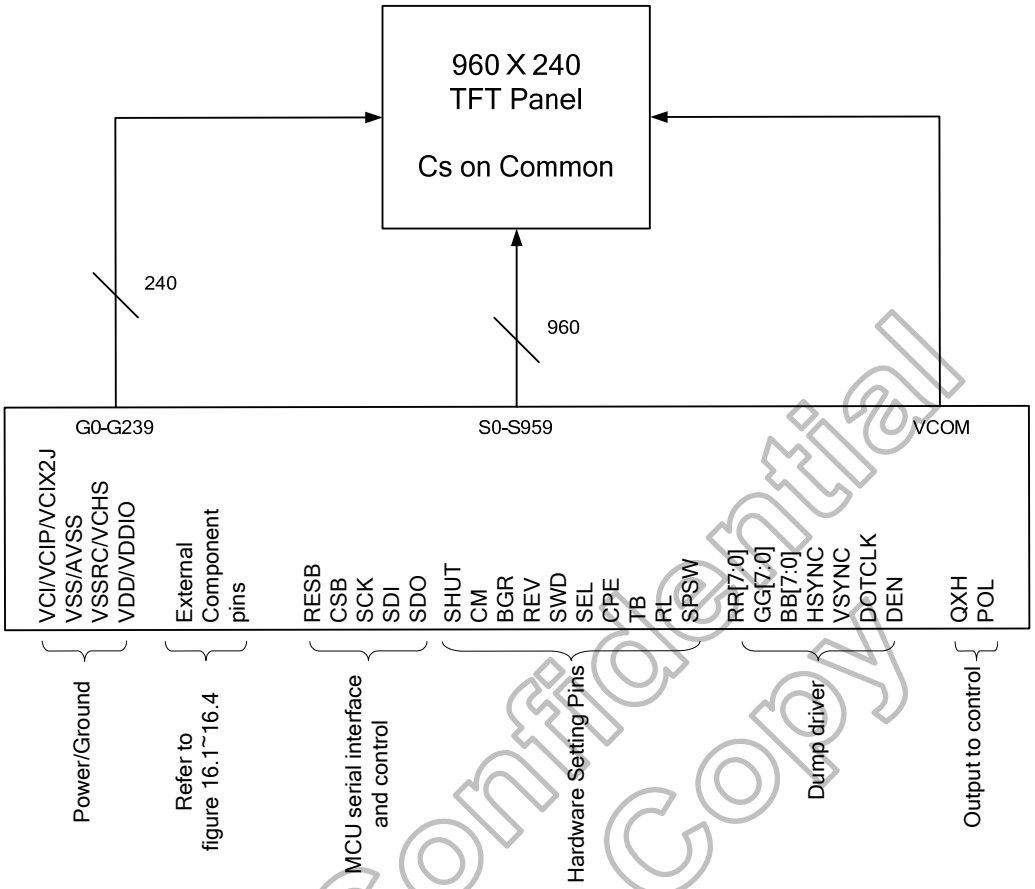


Figure 14. 5: Panel connection example

15. Pad Coordinates

No.	Name	X	Y	Bump size
1	VCOM	-10762.5	-245	50 x 80
2	VCOM	-10687.5	-245	50 x 80
3	VCOM	-10612.5	-245	50 x 80
4	VCOM	-10537.5	-245	50 x 80
5	DUMMY	-10462.5	-245	50 x 80
6	AVSS	-10387.5	-245	50 x 80
7	AVSS	-10312.5	-245	50 x 80
8	AVSS	-10237.5	-245	50 x 80
9	AVSS	-10162.5	-245	50 x 80
10	AVSS	-10087.5	-245	50 x 80
11	AVSS	-10012.5	-245	50 x 80
12	AVSS	-9937.5	-245	50 x 80
13	AVSS	-9862.5	-245	50 x 80
14	AVSS	-9787.5	-245	50 x 80
15	AVSS	-9712.5	-245	50 x 80
16	EXVR	-9637.5	-245	50 x 80
17	EXVR	-9562.5	-245	50 x 80
18	EXVR	-9487.5	-245	50 x 80
19	EXVR	-9412.5	-245	50 x 80
20	VSS	-9337.5	-245	50 x 80
21	VSS	-9262.5	-245	50 x 80
22	VSS	-9187.5	-245	50 x 80
23	VSS	-9112.5	-245	50 x 80
24	VSS	-9037.5	-245	50 x 80
25	VSS	-8962.5	-245	50 x 80
26	VSS	-8887.5	-245	50 x 80
27	VSS	-8812.5	-245	50 x 80
28	SPSW	-8737.5	-245	50 x 80
29	TEST15	-8662.5	-245	50 x 80
30	TEST14	-8587.5	-245	50 x 80
31	TEST13	-8512.5	-245	50 x 80
32	TEST12	-8437.5	-245	50 x 80
33	TEST11	-8362.5	-245	50 x 80
34	TEST10	-8287.5	-245	50 x 80
35	TEST9	-8212.5	-245	50 x 80
36	TEST8	-8137.5	-245	50 x 80
37	TEST7	-8062.5	-245	50 x 80
38	TEST6	-7987.5	-245	50 x 80
39	TEST5	-7912.5	-245	50 x 80
40	TEST4	-7837.5	-245	50 x 80
41	DUMMY	-7762.5	-245	50 x 80
42	QXH	-7687.5	-245	50 x 80
43	POL	-7612.5	-245	50 x 80
44	SDO	-7537.5	-245	50 x 80
45	SDO	-7462.5	-245	50 x 80
46	RESB	-7387.5	-245	50 x 80
47	RESB	-7312.5	-245	50 x 80
48	CSB	-7237.5	-245	50 x 80
49	CSB	-7162.5	-245	50 x 80
50	SCK	-7087.5	-245	50 x 80

No.	Name	X	Y	Bump size
51	SCK	-7012.5	-245	50 x 80
52	SDI	-6937.5	-245	50 x 80
53	SDI	-6862.5	-245	50 x 80
54	BB0	-6787.5	-245	50 x 80
55	BB0	-6712.5	-245	50 x 80
56	BB1	-6637.5	-245	50 x 80
57	BB1	-6562.5	-245	50 x 80
58	BB2	-6487.5	-245	50 x 80
59	BB2	-6412.5	-245	50 x 80
60	BB3	-6337.5	-245	50 x 80
61	BB3	-6262.5	-245	50 x 80
62	BB4	-6187.5	-245	50 x 80
63	BB4	-6112.5	-245	50 x 80
64	BB5	-6037.5	-245	50 x 80
65	BB5	-5962.5	-245	50 x 80
66	BB6	-5887.5	-245	50 x 80
67	BB6	-5812.5	-245	50 x 80
68	BB7	-5737.5	-245	50 x 80
69	BB7	-5662.5	-245	50 x 80
70	GG0	-5587.5	-245	50 x 80
71	GG0	-5512.5	-245	50 x 80
72	GG1	-5437.5	-245	50 x 80
73	GG1	-5362.5	-245	50 x 80
74	GG2	-5287.5	-245	50 x 80
75	GG2	-5212.5	-245	50 x 80
76	GG3	-5137.5	-245	50 x 80
77	GG3	-5062.5	-245	50 x 80
78	GG4	-4987.5	-245	50 x 80
79	GG4	-4912.5	-245	50 x 80
80	GG5	-4837.5	-245	50 x 80
81	GG5	-4762.5	-245	50 x 80
82	GG6	-4687.5	-245	50 x 80
83	GG6	-4612.5	-245	50 x 80
84	GG7	-4537.5	-245	50 x 80
85	GG7	-4462.5	-245	50 x 80
86	RR0	-4387.5	-245	50 x 80
87	RR0	-4312.5	-245	50 x 80
88	RR1	-4237.5	-245	50 x 80
89	RR1	-4162.5	-245	50 x 80
90	RR2	-4087.5	-245	50 x 80
91	RR2	-4012.5	-245	50 x 80
92	RR3	-3937.5	-245	50 x 80
93	RR3	-3862.5	-245	50 x 80
94	RR4	-3787.5	-245	50 x 80
95	RR4	-3712.5	-245	50 x 80
96	RR5	-3637.5	-245	50 x 80
97	RR5	-3562.5	-245	50 x 80
98	RR6	-3487.5	-245	50 x 80
99	RR6	-3412.5	-245	50 x 80
100	RR7	-3337.5	-245	50 x 80

No.	Name	X	Y	Bump size
101	RR7	-3262.5	-245	50 x 80
102	DEN	-3187.5	-245	50 x 80
103	DEN	-3112.5	-245	50 x 80
104	HSYNC	-3037.5	-245	50 x 80
105	HSYNC	-2962.5	-245	50 x 80
106	VSYNC	-2887.5	-245	50 x 80
107	VSYNC	-2812.5	-245	50 x 80
108	DOTCLK	-2737.5	-245	50 x 80
109	DOTCLK	-2662.5	-245	50 x 80
110	SHUT	-2587.5	-245	50 x 80
111	SHUT	-2512.5	-245	50 x 80
112	VSS	-2437.5	-245	50 x 80
113	TB	-2362.5	-245	50 x 80
114	VDDIO	-2287.5	-245	50 x 80
115	REV	-2212.5	-245	50 x 80
116	VSS	-2137.5	-245	50 x 80
117	REGVDD	-2062.5	-245	50 x 80
118	VDDIO	-1987.5	-245	50 x 80
119	RL	-1912.5	-245	50 x 80
120	VSS	-1837.5	-245	50 x 80
121	CM	-1762.5	-245	50 x 80
122	VDDIO	-1687.5	-245	50 x 80
123	BGR	-1612.5	-245	50 x 80
124	VSS	-1537.5	-245	50 x 80
125	SEL0	-1462.5	-245	50 x 80
126	SEL1	-1387.5	-245	50 x 80
127	SEL2	-1312.5	-245	50 x 80
128	VDDIO	-1237.5	-245	50 x 80
129	SWD0	-1162.5	-245	50 x 80
130	VSS	-1087.5	-245	50 x 80
131	SWD1	-1012.5	-245	50 x 80
132	VDDIO	-937.5	-245	50 x 80
133	SWD2	-862.5	-245	50 x 80
134	VSS	-787.5	-245	50 x 80
135	CPE	-712.5	-245	50 x 80
136	PINV	-637.5	-245	50 x 80
137	DUMMY	-562.5	-245	50 x 80
138	VCIM	-487.5	-245	50 x 80
139	VCIM	-412.5	-245	50 x 80
140	VCIM	-337.5	-245	50 x 80
141	VCIM	-262.5	-245	50 x 80
142	VCIM	-187.5	-245	50 x 80
143	C1P	-112.5	-245	50 x 80
144	C1P	-37.5	-245	50 x 80
145	C1P	37.5	-245	50 x 80
146	C1P	112.5	-245	50 x 80
147	C1P	187.5	-245	50 x 80
148	C1N	262.5	-245	50 x 80
149	C1N	337.5	-245	50 x 80
150	C1N	412.5	-245	50 x 80

No.	Name	X	Y	Bump size
151	C1N	487.5	-245	50 x 80
152	C1N	562.5	-245	50 x 80
153	VLCD63	637.5	-245	50 x 80
154	VLCD63	712.5	-245	50 x 80
155	VLCD63	787.5	-245	50 x 80
156	VLCD63	862.5	-245	50 x 80
157	VLCD63	937.5	-245	50 x 80
158	VLCD63	1012.5	-245	50 x 80
159	VCIX2J	1087.5	-245	50 x 80
160	VCIX2J	1162.5	-245	50 x 80
161	VCIX2J	1237.5	-245	50 x 80
162	VCIX2J	1312.5	-245	50 x 80
163	VCIX2J	1387.5	-245	50 x 80
164	VCIX2J	1462.5	-245	50 x 80
165	VCIX2	1537.5	-245	50 x 80
166	VCIX2	1612.5	-245	50 x 80
167	VCIX2	1687.5	-245	50 x 80
168	VCIX2	1762.5	-245	50 x 80
169	VCIX2	1837.5	-245	50 x 80
170	VCIX2	1912.5	-245	50 x 80
171	CYN	1987.5	-245	50 x 80
172	CYN	2062.5	-245	50 x 80
173	CYN	2137.5	-245	50 x 80
174	CYN	2212.5	-245	50 x 80
175	CYN	2287.5	-245	50 x 80
176	CYN	2362.5	-245	50 x 80
177	CYP	2437.5	-245	50 x 80
178	CYP	2512.5	-245	50 x 80
179	CYP	2587.5	-245	50 x 80
180	CYP	2662.5	-245	50 x 80
181	CYP	2737.5	-245	50 x 80
182	CYP	2812.5	-245	50 x 80
183	CXN	2887.5	-245	50 x 80
184	CXN	2962.5	-245	50 x 80
185	CXN	3037.5	-245	50 x 80
186	CXN	3112.5	-245	50 x 80
187	CXN	3187.5	-245	50 x 80
188	CXN	3262.5	-245	50 x 80
189	CXP	3337.5	-245	50 x 80
190	CXP	3412.5	-245	50 x 80
191	CXP	3487.5	-245	50 x 80
192	CXP	3562.5	-245	50 x 80
193	CXP	3637.5	-245	50 x 80
194	CXP	3712.5	-245	50 x 80
195	VDDIO	3787.5	-245	50 x 80
196	VDDIO	3862.5	-245	50 x 80
197	VDDIO	3937.5	-245	50 x 80
198	VDDIO	4012.5	-245	50 x 80
199	VDDIO	4087.5	-245	50 x 80
200	VDDIO	4162.5	-245	50 x 80

No.	Name	X	Y	Bump size
201	VCIP	4237.5	-245	50 x 80
202	VCIP	4312.5	-245	50 x 80
203	VCIP	4387.5	-245	50 x 80
204	VCIP	4462.5	-245	50 x 80
205	VCI	4537.5	-245	50 x 80
206	VCI	4612.5	-245	50 x 80
207	VCI	4687.5	-245	50 x 80
208	VCI	4762.5	-245	50 x 80
209	VCI	4837.5	-245	50 x 80
210	VCI	4912.5	-245	50 x 80
211	VCI	4987.5	-245	50 x 80
212	VCI	5062.5	-245	50 x 80
213	VCI	5137.5	-245	50 x 80
214	VCI	5212.5	-245	50 x 80
215	VDD	5287.5	-245	50 x 80
216	VDD	5362.5	-245	50 x 80
217	VDD	5437.5	-245	50 x 80
218	VDD	5512.5	-245	50 x 80
219	VDD	5587.5	-245	50 x 80
220	VDD	5662.5	-245	50 x 80
221	DUMMY	5737.5	-245	50 x 80
222	CN	5812.5	-245	50 x 80
223	CN	5887.5	-245	50 x 80
224	CN	5962.5	-245	50 x 80
225	CP	6037.5	-245	50 x 80
226	CP	6112.5	-245	50 x 80
227	CP	6187.5	-245	50 x 80
228	VGL	6262.5	-245	50 x 80
229	VGL	6337.5	-245	50 x 80
230	VGL	6412.5	-245	50 x 80
231	VGL	6487.5	-245	50 x 80
232	VGL	6562.5	-245	50 x 80
233	C2N	6637.5	-245	50 x 80
234	C2N	6712.5	-245	50 x 80
235	C2N	6787.5	-245	50 x 80
236	C2P	6862.5	-245	50 x 80
237	C2P	6937.5	-245	50 x 80
238	C2P	7012.5	-245	50 x 80
239	C3N	7087.5	-245	50 x 80
240	C3N	7162.5	-245	50 x 80
241	C3N	7237.5	-245	50 x 80
242	C3P	7312.5	-245	50 x 80
243	C3P	7387.5	-245	50 x 80
244	C3P	7462.5	-245	50 x 80
245	VGH	7537.5	-245	50 x 80
246	VGH	7612.5	-245	50 x 80
247	VGH	7687.5	-245	50 x 80
248	VGH	7762.5	-245	50 x 80
249	VGH	7837.5	-245	50 x 80
250	TEST17	7912.5	-245	50 x 80

No.	Name	X	Y	Bump size
251	TEST16	7987.5	-245	50 x 80
252	VCOMR	8062.5	-245	50 x 80
253	VCOMR	8137.5	-245	50 x 80
254	VCOML	8212.5	-245	50 x 80
255	VCOML	8287.5	-245	50 x 80
256	VCOML	8362.5	-245	50 x 80
257	VCOML	8437.5	-245	50 x 80
258	VCOMH	8512.5	-245	50 x 80
259	VCOMH	8587.5	-245	50 x 80
260	VCOMH	8662.5	-245	50 x 80
261	VCOMH	8737.5	-245	50 x 80
262	VCOM	8812.5	-245	50 x 80
263	VCOM	8887.5	-245	50 x 80
264	VCOM	8962.5	-245	50 x 80
265	VCOM	9037.5	-245	50 x 80
266	VSSRC	9112.5	-245	50 x 80
267	VSSRC	9187.5	-245	50 x 80
268	VSSRC	9262.5	-245	50 x 80
269	VSSRC	9337.5	-245	50 x 80
270	VSSRC	9412.5	-245	50 x 80
271	VSSRC	9487.5	-245	50 x 80
272	VSSRC	9562.5	-245	50 x 80
273	VSSRC	9637.5	-245	50 x 80
274	VCHS	9712.5	-245	50 x 80
275	VCHS	9787.5	-245	50 x 80
276	VCHS	9862.5	-245	50 x 80
277	VCHS	9937.5	-245	50 x 80
278	VCHS	10012.5	-245	50 x 80
279	VCHS	10087.5	-245	50 x 80
280	VCHS	10162.5	-245	50 x 80
281	VCHS	10237.5	-245	50 x 80
282	VCHS	10312.5	-245	50 x 80
283	VCHS	10387.5	-245	50 x 80
284	DUMMY	10462.5	-245	50 x 80
285	VFB	10537.5	-245	50 x 80
286	VFB	10612.5	-245	50 x 80
287	DRV	10687.5	-245	50 x 80
288	DRV	10762.5	-245	50 x 80
289	DUMMY	11016	242.5	18 x 85
290	DUMMY	10998	112.5	18 x 85
291	DUMMY	10980	242.5	18 x 85
292	DUMMY	10962	112.5	18 x 85
293	DUMMY	10944	242.5	18 x 85
294	G1	10926	112.5	18 x 85
295	G3	10908	242.5	18 x 85
296	G5	10890	112.5	18 x 85
297	G7	10872	242.5	18 x 85
298	G9	10854	112.5	18 x 85
299	G11	10836	242.5	18 x 85
300	G13	10818	112.5	18 x 85

No.	Name	X	Y	Bump size
301	G15	10800	242.5	18 x 85
302	G17	10782	112.5	18 x 85
303	G19	10764	242.5	18 x 85
304	G21	10746	112.5	18 x 85
305	G23	10728	242.5	18 x 85
306	G25	10710	112.5	18 x 85
307	G27	10692	242.5	18 x 85
308	G29	10674	112.5	18 x 85
309	G31	10656	242.5	18 x 85
310	G33	10638	112.5	18 x 85
311	G35	10620	242.5	18 x 85
312	G37	10602	112.5	18 x 85
313	G39	10584	242.5	18 x 85
314	G41	10566	112.5	18 x 85
315	G43	10548	242.5	18 x 85
316	G45	10530	112.5	18 x 85
317	G47	10512	242.5	18 x 85
318	G49	10494	112.5	18 x 85
319	G51	10476	242.5	18 x 85
320	G53	10458	112.5	18 x 85
321	G55	10440	242.5	18 x 85
322	G57	10422	112.5	18 x 85
323	G59	10404	242.5	18 x 85
324	G61	10386	112.5	18 x 85
325	G63	10368	242.5	18 x 85
326	G65	10350	112.5	18 x 85
327	G67	10332	242.5	18 x 85
328	G69	10314	112.5	18 x 85
329	G71	10296	242.5	18 x 85
330	G73	10278	112.5	18 x 85
331	G75	10260	242.5	18 x 85
332	G77	10242	112.5	18 x 85
333	G79	10224	242.5	18 x 85
334	G81	10206	112.5	18 x 85
335	G83	10188	242.5	18 x 85
336	G85	10170	112.5	18 x 85
337	G87	10152	242.5	18 x 85
338	G89	10134	112.5	18 x 85
339	G91	10116	242.5	18 x 85
340	G93	10098	112.5	18 x 85
341	G95	10080	242.5	18 x 85
342	G97	10062	112.5	18 x 85
343	G99	10044	242.5	18 x 85
344	G101	10026	112.5	18 x 85
345	G103	10008	242.5	18 x 85
346	G105	9990	112.5	18 x 85
347	G107	9972	242.5	18 x 85
348	G109	9954	112.5	18 x 85
349	G111	9936	242.5	18 x 85
350	G113	9918	112.5	18 x 85

No.	Name	X	Y	Bump size
351	G115	9900	242.5	18 x 85
352	G117	9882	112.5	18 x 85
353	G119	9864	242.5	18 x 85
354	G121	9846	112.5	18 x 85
355	G123	9828	242.5	18 x 85
356	G125	9810	112.5	18 x 85
357	G127	9792	242.5	18 x 85
358	G129	9774	112.5	18 x 85
359	G131	9756	242.5	18 x 85
360	G133	9738	112.5	18 x 85
361	G135	9720	242.5	18 x 85
362	G137	9702	112.5	18 x 85
363	G139	9684	242.5	18 x 85
364	G141	9666	112.5	18 x 85
365	G143	9648	242.5	18 x 85
366	G145	9630	112.5	18 x 85
367	G147	9612	242.5	18 x 85
368	G149	9594	112.5	18 x 85
369	G151	9576	242.5	18 x 85
370	G153	9558	112.5	18 x 85
371	G155	9540	242.5	18 x 85
372	G157	9522	112.5	18 x 85
373	G159	9504	242.5	18 x 85
374	G161	9486	112.5	18 x 85
375	G163	9468	242.5	18 x 85
376	G165	9450	112.5	18 x 85
377	G167	9432	242.5	18 x 85
378	G169	9414	112.5	18 x 85
379	G171	9396	242.5	18 x 85
380	G173	9378	112.5	18 x 85
381	G175	9360	242.5	18 x 85
382	G177	9342	112.5	18 x 85
383	G179	9324	242.5	18 x 85
384	G181	9306	112.5	18 x 85
385	G183	9288	242.5	18 x 85
386	G185	9270	112.5	18 x 85
387	G187	9252	242.5	18 x 85
388	G189	9234	112.5	18 x 85
389	G191	9216	242.5	18 x 85
390	G193	9198	112.5	18 x 85
391	G195	9180	242.5	18 x 85
392	G197	9162	112.5	18 x 85
393	G199	9144	242.5	18 x 85
394	G201	9126	112.5	18 x 85
395	G203	9108	242.5	18 x 85
396	G205	9090	112.5	18 x 85
397	G207	9072	242.5	18 x 85
398	G209	9054	112.5	18 x 85
399	G211	9036	242.5	18 x 85
400	G213	9018	112.5	18 x 85

No.	Name	X	Y	Bump size
401	G215	9000	242.5	18 x 85
402	G217	8982	112.5	18 x 85
403	G219	8964	242.5	18 x 85
404	G221	8946	112.5	18 x 85
405	G223	8928	242.5	18 x 85
406	G225	8910	112.5	18 x 85
407	G227	8892	242.5	18 x 85
408	G229	8874	112.5	18 x 85
409	G231	8856	242.5	18 x 85
410	G233	8838	112.5	18 x 85
411	G235	8820	242.5	18 x 85
412	G237	8802	112.5	18 x 85
413	G239	8784	242.5	18 x 85
414	DUMMY	8766	112.5	18 x 85
415	DUMMY	8748	242.5	18 x 85
416	DUMMY	8730	112.5	18 x 85
417	DUMMY	8712	242.5	18 x 85
418	DUMMY	8694	112.5	18 x 85
419	DUMMY	8676	242.5	18 x 85
420	S0	8658	112.5	18 x 85
421	S1	8640	242.5	18 x 85
422	S2	8622	112.5	18 x 85
423	S3	8604	242.5	18 x 85
424	S4	8586	112.5	18 x 85
425	S5	8568	242.5	18 x 85
426	S6	8550	112.5	18 x 85
427	S7	8532	242.5	18 x 85
428	S8	8514	112.5	18 x 85
429	S9	8496	242.5	18 x 85
430	S10	8478	112.5	18 x 85
431	S11	8460	242.5	18 x 85
432	S12	8442	112.5	18 x 85
433	S13	8424	242.5	18 x 85
434	S14	8406	112.5	18 x 85
435	S15	8388	242.5	18 x 85
436	S16	8370	112.5	18 x 85
437	S17	8352	242.5	18 x 85
438	S18	8334	112.5	18 x 85
439	S19	8316	242.5	18 x 85
440	S20	8298	112.5	18 x 85
441	S21	8280	242.5	18 x 85
442	S22	8262	112.5	18 x 85
443	S23	8244	242.5	18 x 85
444	S24	8226	112.5	18 x 85
445	S25	8208	242.5	18 x 85
446	S26	8190	112.5	18 x 85
447	S27	8172	242.5	18 x 85
448	S28	8154	112.5	18 x 85
449	S29	8136	242.5	18 x 85
450	S30	8118	112.5	18 x 85

No.	Name	X	Y	Bump size
451	S31	8100	242.5	18 x 85
452	S32	8082	112.5	18 x 85
453	S33	8064	242.5	18 x 85
454	S34	8046	112.5	18 x 85
455	S35	8028	242.5	18 x 85
456	S36	8010	112.5	18 x 85
457	S37	7992	242.5	18 x 85
458	S38	7974	112.5	18 x 85
459	S39	7956	242.5	18 x 85
460	S40	7938	112.5	18 x 85
461	S41	7920	242.5	18 x 85
462	S42	7902	112.5	18 x 85
463	S43	7884	242.5	18 x 85
464	S44	7866	112.5	18 x 85
465	S45	7848	242.5	18 x 85
466	S46	7830	112.5	18 x 85
467	S47	7812	242.5	18 x 85
468	S48	7794	112.5	18 x 85
469	S49	7776	242.5	18 x 85
470	S50	7758	112.5	18 x 85
471	S51	7740	242.5	18 x 85
472	S52	7722	112.5	18 x 85
473	S53	7704	242.5	18 x 85
474	S54	7686	112.5	18 x 85
475	S55	7668	242.5	18 x 85
476	S56	7650	112.5	18 x 85
477	S57	7632	242.5	18 x 85
478	S58	7614	112.5	18 x 85
479	S59	7596	242.5	18 x 85
480	S60	7578	112.5	18 x 85
481	S61	7560	242.5	18 x 85
482	S62	7542	112.5	18 x 85
483	S63	7524	242.5	18 x 85
484	S64	7506	112.5	18 x 85
485	S65	7488	242.5	18 x 85
486	S66	7470	112.5	18 x 85
487	S67	7452	242.5	18 x 85
488	S68	7434	112.5	18 x 85
489	S69	7416	242.5	18 x 85
490	S70	7398	112.5	18 x 85
491	S71	7380	242.5	18 x 85
492	S72	7362	112.5	18 x 85
493	S73	7344	242.5	18 x 85
494	S74	7326	112.5	18 x 85
495	S75	7308	242.5	18 x 85
496	S76	7290	112.5	18 x 85
497	S77	7272	242.5	18 x 85
498	S78	7254	112.5	18 x 85
499	S79	7236	242.5	18 x 85
500	S80	7218	112.5	18 x 85

No.	Name	X	Y	Bump size
501	S81	7200	242.5	18 x 85
502	S82	7182	112.5	18 x 85
503	S83	7164	242.5	18 x 85
504	S84	7146	112.5	18 x 85
505	S85	7128	242.5	18 x 85
506	S86	7110	112.5	18 x 85
507	S87	7092	242.5	18 x 85
508	S88	7074	112.5	18 x 85
509	S89	7056	242.5	18 x 85
510	S90	7038	112.5	18 x 85
511	S91	7020	242.5	18 x 85
512	S92	7002	112.5	18 x 85
513	S93	6984	242.5	18 x 85
514	S94	6966	112.5	18 x 85
515	S95	6948	242.5	18 x 85
516	S96	6930	112.5	18 x 85
517	S97	6912	242.5	18 x 85
518	S98	6894	112.5	18 x 85
519	S99	6876	242.5	18 x 85
520	S100	6858	112.5	18 x 85
521	S101	6840	242.5	18 x 85
522	S102	6822	112.5	18 x 85
523	S103	6804	242.5	18 x 85
524	S104	6786	112.5	18 x 85
525	S105	6768	242.5	18 x 85
526	S106	6750	112.5	18 x 85
527	S107	6732	242.5	18 x 85
528	S108	6714	112.5	18 x 85
529	S109	6696	242.5	18 x 85
530	S110	6678	112.5	18 x 85
531	S111	6660	242.5	18 x 85
532	S112	6642	112.5	18 x 85
533	S113	6624	242.5	18 x 85
534	S114	6606	112.5	18 x 85
535	S115	6588	242.5	18 x 85
536	S116	6570	112.5	18 x 85
537	S117	6552	242.5	18 x 85
538	S118	6534	112.5	18 x 85
539	S119	6516	242.5	18 x 85
540	S120	6498	112.5	18 x 85
541	S121	6480	242.5	18 x 85
542	S122	6462	112.5	18 x 85
543	S123	6444	242.5	18 x 85
544	S124	6426	112.5	18 x 85
545	S125	6408	242.5	18 x 85
546	S126	6390	112.5	18 x 85
547	S127	6372	242.5	18 x 85
548	S128	6354	112.5	18 x 85
549	S129	6336	242.5	18 x 85
550	S130	6318	112.5	18 x 85

No.	Name	X	Y	Bump size
551	S131	6300	242.5	18 x 85
552	S132	6282	112.5	18 x 85
553	S133	6264	242.5	18 x 85
554	S134	6246	112.5	18 x 85
555	S135	6228	242.5	18 x 85
556	S136	6210	112.5	18 x 85
557	S137	6192	242.5	18 x 85
558	S138	6174	112.5	18 x 85
559	S139	6156	242.5	18 x 85
560	S140	6138	112.5	18 x 85
561	S141	6120	242.5	18 x 85
562	S142	6102	112.5	18 x 85
563	S143	6084	242.5	18 x 85
564	S144	6066	112.5	18 x 85
565	S145	6048	242.5	18 x 85
566	S146	6030	112.5	18 x 85
567	S147	6012	242.5	18 x 85
568	S148	5994	112.5	18 x 85
569	S149	5976	242.5	18 x 85
570	S150	5958	112.5	18 x 85
571	S151	5940	242.5	18 x 85
572	S152	5922	112.5	18 x 85
573	S153	5904	242.5	18 x 85
574	S154	5886	112.5	18 x 85
575	S155	5868	242.5	18 x 85
576	S156	5850	112.5	18 x 85
577	S157	5832	242.5	18 x 85
578	S158	5814	112.5	18 x 85
579	S159	5796	242.5	18 x 85
580	S160	5778	112.5	18 x 85
581	S161	5760	242.5	18 x 85
582	S162	5742	112.5	18 x 85
583	S163	5724	242.5	18 x 85
584	S164	5706	112.5	18 x 85
585	S165	5688	242.5	18 x 85
586	S166	5670	112.5	18 x 85
587	S167	5652	242.5	18 x 85
588	S168	5634	112.5	18 x 85
589	S169	5616	242.5	18 x 85
590	S170	5598	112.5	18 x 85
591	S171	5580	242.5	18 x 85
592	S172	5562	112.5	18 x 85
593	S173	5544	242.5	18 x 85
594	S174	5526	112.5	18 x 85
595	S175	5508	242.5	18 x 85
596	S176	5490	112.5	18 x 85
597	S177	5472	242.5	18 x 85
598	S178	5454	112.5	18 x 85
599	S179	5436	242.5	18 x 85
600	S180	5418	112.5	18 x 85

No.	Name	X	Y	Bump size
601	S181	5400	242.5	18 x 85
602	S182	5382	112.5	18 x 85
603	S183	5364	242.5	18 x 85
604	S184	5346	112.5	18 x 85
605	S185	5328	242.5	18 x 85
606	S186	5310	112.5	18 x 85
607	S187	5292	242.5	18 x 85
608	S188	5274	112.5	18 x 85
609	S189	5256	242.5	18 x 85
610	S190	5238	112.5	18 x 85
611	S191	5220	242.5	18 x 85
612	S192	5202	112.5	18 x 85
613	S193	5184	242.5	18 x 85
614	S194	5166	112.5	18 x 85
615	S195	5148	242.5	18 x 85
616	S196	5130	112.5	18 x 85
617	S197	5112	242.5	18 x 85
618	S198	5094	112.5	18 x 85
619	S199	5076	242.5	18 x 85
620	S200	5058	112.5	18 x 85
621	S201	5040	242.5	18 x 85
622	S202	5022	112.5	18 x 85
623	S203	5004	242.5	18 x 85
624	S204	4986	112.5	18 x 85
625	S205	4968	242.5	18 x 85
626	S206	4950	112.5	18 x 85
627	S207	4932	242.5	18 x 85
628	S208	4914	112.5	18 x 85
629	S209	4896	242.5	18 x 85
630	S210	4878	112.5	18 x 85
631	S211	4860	242.5	18 x 85
632	S212	4842	112.5	18 x 85
633	S213	4824	242.5	18 x 85
634	S214	4806	112.5	18 x 85
635	S215	4788	242.5	18 x 85
636	S216	4770	112.5	18 x 85
637	S217	4752	242.5	18 x 85
638	S218	4734	112.5	18 x 85
639	S219	4716	242.5	18 x 85
640	S220	4698	112.5	18 x 85
641	S221	4680	242.5	18 x 85
642	S222	4662	112.5	18 x 85
643	S223	4644	242.5	18 x 85
644	S224	4626	112.5	18 x 85
645	S225	4608	242.5	18 x 85
646	S226	4590	112.5	18 x 85
647	S227	4572	242.5	18 x 85
648	S228	4554	112.5	18 x 85
649	S229	4536	242.5	18 x 85
650	S230	4518	112.5	18 x 85

No.	Name	X	Y	Bump size
651	S231	4500	242.5	18 x 85
652	S232	4482	112.5	18 x 85
653	S233	4464	242.5	18 x 85
654	S234	4446	112.5	18 x 85
655	S235	4428	242.5	18 x 85
656	S236	4410	112.5	18 x 85
657	S237	4392	242.5	18 x 85
658	S238	4374	112.5	18 x 85
659	S239	4356	242.5	18 x 85
660	S240	4338	112.5	18 x 85
661	S241	4320	242.5	18 x 85
662	S242	4302	112.5	18 x 85
663	S243	4284	242.5	18 x 85
664	S244	4266	112.5	18 x 85
665	S245	4248	242.5	18 x 85
666	S246	4230	112.5	18 x 85
667	S247	4212	242.5	18 x 85
668	S248	4194	112.5	18 x 85
669	S249	4176	242.5	18 x 85
670	S250	4158	112.5	18 x 85
671	S251	4140	242.5	18 x 85
672	S252	4122	112.5	18 x 85
673	S253	4104	242.5	18 x 85
674	S254	4086	112.5	18 x 85
675	S255	4068	242.5	18 x 85
676	S256	4050	112.5	18 x 85
677	S257	4032	242.5	18 x 85
678	S258	4014	112.5	18 x 85
679	S259	3996	242.5	18 x 85
680	S260	3978	112.5	18 x 85
681	S261	3960	242.5	18 x 85
682	S262	3942	112.5	18 x 85
683	S263	3924	242.5	18 x 85
684	S264	3906	112.5	18 x 85
685	S265	3888	242.5	18 x 85
686	S266	3870	112.5	18 x 85
687	S267	3852	242.5	18 x 85
688	S268	3834	112.5	18 x 85
689	S269	3816	242.5	18 x 85
690	S270	3798	112.5	18 x 85
691	S271	3780	242.5	18 x 85
692	S272	3762	112.5	18 x 85
693	S273	3744	242.5	18 x 85
694	S274	3726	112.5	18 x 85
695	S275	3708	242.5	18 x 85
696	S276	3690	112.5	18 x 85
697	S277	3672	242.5	18 x 85
698	S278	3654	112.5	18 x 85
699	S279	3636	242.5	18 x 85
700	S280	3618	112.5	18 x 85

No.	Name	X	Y	Bump size
701	S281	3600	242.5	18 x 85
702	S282	3582	112.5	18 x 85
703	S283	3564	242.5	18 x 85
704	S284	3546	112.5	18 x 85
705	S285	3528	242.5	18 x 85
706	S286	3510	112.5	18 x 85
707	S287	3492	242.5	18 x 85
708	S288	3474	112.5	18 x 85
709	S289	3456	242.5	18 x 85
710	S290	3438	112.5	18 x 85
711	S291	3420	242.5	18 x 85
712	S292	3402	112.5	18 x 85
713	S293	3384	242.5	18 x 85
714	S294	3366	112.5	18 x 85
715	S295	3348	242.5	18 x 85
716	S296	3330	112.5	18 x 85
717	S297	3312	242.5	18 x 85
718	S298	3294	112.5	18 x 85
719	S299	3276	242.5	18 x 85
720	S300	3258	112.5	18 x 85
721	S301	3240	242.5	18 x 85
722	S302	3222	112.5	18 x 85
723	S303	3204	242.5	18 x 85
724	S304	3186	112.5	18 x 85
725	S305	3168	242.5	18 x 85
726	S306	3150	112.5	18 x 85
727	S307	3132	242.5	18 x 85
728	S308	3114	112.5	18 x 85
729	S309	3096	242.5	18 x 85
730	S310	3078	112.5	18 x 85
731	S311	3060	242.5	18 x 85
732	S312	3042	112.5	18 x 85
733	S313	3024	242.5	18 x 85
734	S314	3006	112.5	18 x 85
735	S315	2988	242.5	18 x 85
736	S316	2970	112.5	18 x 85
737	S317	2952	242.5	18 x 85
738	S318	2934	112.5	18 x 85
739	S319	2916	242.5	18 x 85
740	S320	2898	112.5	18 x 85
741	S321	2880	242.5	18 x 85
742	S322	2862	112.5	18 x 85
743	S323	2844	242.5	18 x 85
744	S324	2826	112.5	18 x 85
745	S325	2808	242.5	18 x 85
746	S326	2790	112.5	18 x 85
747	S327	2772	242.5	18 x 85
748	S328	2754	112.5	18 x 85
749	S329	2736	242.5	18 x 85
750	S330	2718	112.5	18 x 85

No.	Name	X	Y	Bump size
751	S331	2700	242.5	18 x 85
752	S332	2682	112.5	18 x 85
753	S333	2664	242.5	18 x 85
754	S334	2646	112.5	18 x 85
755	S335	2628	242.5	18 x 85
756	S336	2610	112.5	18 x 85
757	S337	2592	242.5	18 x 85
758	S338	2574	112.5	18 x 85
759	S339	2556	242.5	18 x 85
760	S340	2538	112.5	18 x 85
761	S341	2520	242.5	18 x 85
762	S342	2502	112.5	18 x 85
763	S343	2484	242.5	18 x 85
764	S344	2466	112.5	18 x 85
765	S345	2448	242.5	18 x 85
766	S346	2430	112.5	18 x 85
767	S347	2412	242.5	18 x 85
768	S348	2394	112.5	18 x 85
769	S349	2376	242.5	18 x 85
770	S350	2358	112.5	18 x 85
771	S351	2340	242.5	18 x 85
772	S352	2322	112.5	18 x 85
773	S353	2304	242.5	18 x 85
774	S354	2286	112.5	18 x 85
775	S355	2268	242.5	18 x 85
776	S356	2250	112.5	18 x 85
777	S357	2232	242.5	18 x 85
778	S358	2214	112.5	18 x 85
779	S359	2196	242.5	18 x 85
780	S360	2178	112.5	18 x 85
781	S361	2160	242.5	18 x 85
782	S362	2142	112.5	18 x 85
783	S363	2124	242.5	18 x 85
784	S364	2106	112.5	18 x 85
785	S365	2088	242.5	18 x 85
786	S366	2070	112.5	18 x 85
787	S367	2052	242.5	18 x 85
788	S368	2034	112.5	18 x 85
789	S369	2016	242.5	18 x 85
790	S370	1998	112.5	18 x 85
791	S371	1980	242.5	18 x 85
792	S372	1962	112.5	18 x 85
793	S373	1944	242.5	18 x 85
794	S374	1926	112.5	18 x 85
795	S375	1908	242.5	18 x 85
796	S376	1890	112.5	18 x 85
797	S377	1872	242.5	18 x 85
798	S378	1854	112.5	18 x 85
799	S379	1836	242.5	18 x 85
800	S380	1818	112.5	18 x 85

No.	Name	X	Y	Bump size
801	S381	1800	242.5	18 x 85
802	S382	1782	112.5	18 x 85
803	S383	1764	242.5	18 x 85
804	S384	1746	112.5	18 x 85
805	S385	1728	242.5	18 x 85
806	S386	1710	112.5	18 x 85
807	S387	1692	242.5	18 x 85
808	S388	1674	112.5	18 x 85
809	S389	1656	242.5	18 x 85
810	S390	1638	112.5	18 x 85
811	S391	1620	242.5	18 x 85
812	S392	1602	112.5	18 x 85
813	S393	1584	242.5	18 x 85
814	S394	1566	112.5	18 x 85
815	S395	1548	242.5	18 x 85
816	S396	1530	112.5	18 x 85
817	S397	1512	242.5	18 x 85
818	S398	1494	112.5	18 x 85
819	S399	1476	242.5	18 x 85
820	S400	1458	112.5	18 x 85
821	S401	1440	242.5	18 x 85
822	S402	1422	112.5	18 x 85
823	S403	1404	242.5	18 x 85
824	S404	1386	112.5	18 x 85
825	S405	1368	242.5	18 x 85
826	S406	1350	112.5	18 x 85
827	S407	1332	242.5	18 x 85
828	S408	1314	112.5	18 x 85
829	S409	1296	242.5	18 x 85
830	S410	1278	112.5	18 x 85
831	S411	1260	242.5	18 x 85
832	S412	1242	112.5	18 x 85
833	S413	1224	242.5	18 x 85
834	S414	1206	112.5	18 x 85
835	S415	1188	242.5	18 x 85
836	S416	1170	112.5	18 x 85
837	S417	1152	242.5	18 x 85
838	S418	1134	112.5	18 x 85
839	S419	1116	242.5	18 x 85
840	S420	1098	112.5	18 x 85
841	S421	1080	242.5	18 x 85
842	S422	1062	112.5	18 x 85
843	S423	1044	242.5	18 x 85
844	S424	1026	112.5	18 x 85
845	S425	1008	242.5	18 x 85
846	S426	990	112.5	18 x 85
847	S427	972	242.5	18 x 85
848	S428	954	112.5	18 x 85
849	S429	936	242.5	18 x 85
850	S430	918	112.5	18 x 85

No.	Name	X	Y	Bump size
851	S431	900	242.5	18 x 85
852	S432	882	112.5	18 x 85
853	S433	864	242.5	18 x 85
854	S434	846	112.5	18 x 85
855	S435	828	242.5	18 x 85
856	S436	810	112.5	18 x 85
857	S437	792	242.5	18 x 85
858	S438	774	112.5	18 x 85
859	S439	756	242.5	18 x 85
860	S440	738	112.5	18 x 85
861	S441	720	242.5	18 x 85
862	S442	702	112.5	18 x 85
863	S443	684	242.5	18 x 85
864	S444	666	112.5	18 x 85
865	S445	648	242.5	18 x 85
866	S446	630	112.5	18 x 85
867	S447	612	242.5	18 x 85
868	S448	594	112.5	18 x 85
869	S449	576	242.5	18 x 85
870	S450	558	112.5	18 x 85
871	S451	540	242.5	18 x 85
872	S452	522	112.5	18 x 85
873	S453	504	242.5	18 x 85
874	S454	486	112.5	18 x 85
875	S455	468	242.5	18 x 85
876	S456	450	112.5	18 x 85
877	S457	432	242.5	18 x 85
878	S458	414	112.5	18 x 85
879	S459	396	242.5	18 x 85
880	S460	378	112.5	18 x 85
881	S461	360	242.5	18 x 85
882	S462	342	112.5	18 x 85
883	S463	324	242.5	18 x 85
884	S464	306	112.5	18 x 85
885	S465	288	242.5	18 x 85
886	S466	270	112.5	18 x 85
887	S467	252	242.5	18 x 85
888	S468	234	112.5	18 x 85
889	S469	216	242.5	18 x 85
890	S470	198	112.5	18 x 85
891	S471	180	242.5	18 x 85
892	S472	162	112.5	18 x 85
893	S473	144	242.5	18 x 85
894	S474	126	112.5	18 x 85
895	S475	108	242.5	18 x 85
896	S476	90	112.5	18 x 85
897	S477	72	242.5	18 x 85
898	S478	54	112.5	18 x 85
899	S479	36	242.5	18 x 85
900	S480	18	112.5	18 x 85

No.	Name	X	Y	Bump size
901	S481	0	242.5	18 x 85
902	S482	-18	112.5	18 x 85
903	S483	-36	242.5	18 x 85
904	S484	-54	112.5	18 x 85
905	S485	-72	242.5	18 x 85
906	S486	-90	112.5	18 x 85
907	S487	-108	242.5	18 x 85
908	S488	-126	112.5	18 x 85
909	S489	-144	242.5	18 x 85
910	S490	-162	112.5	18 x 85
911	S491	-180	242.5	18 x 85
912	S492	-198	112.5	18 x 85
913	S493	-216	242.5	18 x 85
914	S494	-234	112.5	18 x 85
915	S495	-252	242.5	18 x 85
916	S496	-270	112.5	18 x 85
917	S497	-288	242.5	18 x 85
918	S498	-306	112.5	18 x 85
919	S499	-324	242.5	18 x 85
920	S500	-342	112.5	18 x 85
921	S501	-360	242.5	18 x 85
922	S502	-378	112.5	18 x 85
923	S503	-396	242.5	18 x 85
924	S504	-414	112.5	18 x 85
925	S505	-432	242.5	18 x 85
926	S506	-450	112.5	18 x 85
927	S507	-468	242.5	18 x 85
928	S508	-486	112.5	18 x 85
929	S509	-504	242.5	18 x 85
930	S510	-522	112.5	18 x 85
931	S511	-540	242.5	18 x 85
932	S512	-558	112.5	18 x 85
933	S513	-576	242.5	18 x 85
934	S514	-594	112.5	18 x 85
935	S515	-612	242.5	18 x 85
936	S516	-630	112.5	18 x 85
937	S517	-648	242.5	18 x 85
938	S518	-666	112.5	18 x 85
939	S519	-684	242.5	18 x 85
940	S520	-702	112.5	18 x 85
941	S521	-720	242.5	18 x 85
942	S522	-738	112.5	18 x 85
943	S523	-756	242.5	18 x 85
944	S524	-774	112.5	18 x 85
945	S525	-792	242.5	18 x 85
946	S526	-810	112.5	18 x 85
947	S527	-828	242.5	18 x 85
948	S528	-846	112.5	18 x 85
949	S529	-864	242.5	18 x 85
950	S530	-882	112.5	18 x 85

No.	Name	X	Y	Bump size
951	S531	-900	242.5	18 x 85
952	S532	-918	112.5	18 x 85
953	S533	-936	242.5	18 x 85
954	S534	-954	112.5	18 x 85
955	S535	-972	242.5	18 x 85
956	S536	-990	112.5	18 x 85
957	S537	-1008	242.5	18 x 85
958	S538	-1026	112.5	18 x 85
959	S539	-1044	242.5	18 x 85
960	S540	-1062	112.5	18 x 85
961	S541	-1080	242.5	18 x 85
962	S542	-1098	112.5	18 x 85
963	S543	-1116	242.5	18 x 85
964	S544	-1134	112.5	18 x 85
965	S545	-1152	242.5	18 x 85
966	S546	-1170	112.5	18 x 85
967	S547	-1188	242.5	18 x 85
968	S548	-1206	112.5	18 x 85
969	S549	-1224	242.5	18 x 85
970	S550	-1242	112.5	18 x 85
971	S551	-1260	242.5	18 x 85
972	S552	-1278	112.5	18 x 85
973	S553	-1296	242.5	18 x 85
974	S554	-1314	112.5	18 x 85
975	S555	-1332	242.5	18 x 85
976	S556	-1350	112.5	18 x 85
977	S557	-1368	242.5	18 x 85
978	S558	-1386	112.5	18 x 85
979	S559	-1404	242.5	18 x 85
980	S560	-1422	112.5	18 x 85
981	S561	-1440	242.5	18 x 85
982	S562	-1458	112.5	18 x 85
983	S563	-1476	242.5	18 x 85
984	S564	-1494	112.5	18 x 85
985	S565	-1512	242.5	18 x 85
986	S566	-1530	112.5	18 x 85
987	S567	-1548	242.5	18 x 85
988	S568	-1566	112.5	18 x 85
989	S569	-1584	242.5	18 x 85
990	S570	-1602	112.5	18 x 85
991	S571	-1620	242.5	18 x 85
992	S572	-1638	112.5	18 x 85
993	S573	-1656	242.5	18 x 85
994	S574	-1674	112.5	18 x 85
995	S575	-1692	242.5	18 x 85
996	S576	-1710	112.5	18 x 85
997	S577	-1728	242.5	18 x 85
998	S578	-1746	112.5	18 x 85
999	S579	-1764	242.5	18 x 85
1000	S580	-1782	112.5	18 x 85

No.	Name	X	Y	Bump size
1001	S581	-1800	242.5	18 x 85
1002	S582	-1818	112.5	18 x 85
1003	S583	-1836	242.5	18 x 85
1004	S584	-1854	112.5	18 x 85
1005	S585	-1872	242.5	18 x 85
1006	S586	-1890	112.5	18 x 85
1007	S587	-1908	242.5	18 x 85
1008	S588	-1926	112.5	18 x 85
1009	S589	-1944	242.5	18 x 85
1010	S590	-1962	112.5	18 x 85
1011	S591	-1980	242.5	18 x 85
1012	S592	-1998	112.5	18 x 85
1013	S593	-2016	242.5	18 x 85
1014	S594	-2034	112.5	18 x 85
1015	S595	-2052	242.5	18 x 85
1016	S596	-2070	112.5	18 x 85
1017	S597	-2088	242.5	18 x 85
1018	S598	-2106	112.5	18 x 85
1019	S599	-2124	242.5	18 x 85
1020	S600	-2142	112.5	18 x 85
1021	S601	-2160	242.5	18 x 85
1022	S602	-2178	112.5	18 x 85
1023	S603	-2196	242.5	18 x 85
1024	S604	-2214	112.5	18 x 85
1025	S605	-2232	242.5	18 x 85
1026	S606	-2250	112.5	18 x 85
1027	S607	-2268	242.5	18 x 85
1028	S608	-2286	112.5	18 x 85
1029	S609	-2304	242.5	18 x 85
1030	S610	-2322	112.5	18 x 85
1031	S611	-2340	242.5	18 x 85
1032	S612	-2358	112.5	18 x 85
1033	S613	-2376	242.5	18 x 85
1034	S614	-2394	112.5	18 x 85
1035	S615	-2412	242.5	18 x 85
1036	S616	-2430	112.5	18 x 85
1037	S617	-2448	242.5	18 x 85
1038	S618	-2466	112.5	18 x 85
1039	S619	-2484	242.5	18 x 85
1040	S620	-2502	112.5	18 x 85
1041	S621	-2520	242.5	18 x 85
1042	S622	-2538	112.5	18 x 85
1043	S623	-2556	242.5	18 x 85
1044	S624	-2574	112.5	18 x 85
1045	S625	-2592	242.5	18 x 85
1046	S626	-2610	112.5	18 x 85
1047	S627	-2628	242.5	18 x 85
1048	S628	-2646	112.5	18 x 85
1049	S629	-2664	242.5	18 x 85
1050	S630	-2682	112.5	18 x 85

No.	Name	X	Y	Bump size
1051	S631	-2700	242.5	18 x 85
1052	S632	-2718	112.5	18 x 85
1053	S633	-2736	242.5	18 x 85
1054	S634	-2754	112.5	18 x 85
1055	S635	-2772	242.5	18 x 85
1056	S636	-2790	112.5	18 x 85
1057	S637	-2808	242.5	18 x 85
1058	S638	-2826	112.5	18 x 85
1059	S639	-2844	242.5	18 x 85
1060	S640	-2862	112.5	18 x 85
1061	S641	-2880	242.5	18 x 85
1062	S642	-2898	112.5	18 x 85
1063	S643	-2916	242.5	18 x 85
1064	S644	-2934	112.5	18 x 85
1065	S645	-2952	242.5	18 x 85
1066	S646	-2970	112.5	18 x 85
1067	S647	-2988	242.5	18 x 85
1068	S648	-3006	112.5	18 x 85
1069	S649	-3024	242.5	18 x 85
1070	S650	-3042	112.5	18 x 85
1071	S651	-3060	242.5	18 x 85
1072	S652	-3078	112.5	18 x 85
1073	S653	-3096	242.5	18 x 85
1074	S654	-3114	112.5	18 x 85
1075	S655	-3132	242.5	18 x 85
1076	S656	-3150	112.5	18 x 85
1077	S657	-3168	242.5	18 x 85
1078	S658	-3186	112.5	18 x 85
1079	S659	-3204	242.5	18 x 85
1080	S660	-3222	112.5	18 x 85
1081	S661	-3240	242.5	18 x 85
1082	S662	-3258	112.5	18 x 85
1083	S663	-3276	242.5	18 x 85
1084	S664	-3294	112.5	18 x 85
1085	S665	-3312	242.5	18 x 85
1086	S666	-3330	112.5	18 x 85
1087	S667	-3348	242.5	18 x 85
1088	S668	-3366	112.5	18 x 85
1089	S669	-3384	242.5	18 x 85
1090	S670	-3402	112.5	18 x 85
1091	S671	-3420	242.5	18 x 85
1092	S672	-3438	112.5	18 x 85
1093	S673	-3456	242.5	18 x 85
1094	S674	-3474	112.5	18 x 85
1095	S675	-3492	242.5	18 x 85
1096	S676	-3510	112.5	18 x 85
1097	S677	-3528	242.5	18 x 85
1098	S678	-3546	112.5	18 x 85
1099	S679	-3564	242.5	18 x 85
1100	S680	-3582	112.5	18 x 85

No.	Name	X	Y	Bump size
1101	S681	-3600	242.5	18 x 85
1102	S682	-3618	112.5	18 x 85
1103	S683	-3636	242.5	18 x 85
1104	S684	-3654	112.5	18 x 85
1105	S685	-3672	242.5	18 x 85
1106	S686	-3690	112.5	18 x 85
1107	S687	-3708	242.5	18 x 85
1108	S688	-3726	112.5	18 x 85
1109	S689	-3744	242.5	18 x 85
1110	S690	-3762	112.5	18 x 85
1111	S691	-3780	242.5	18 x 85
1112	S692	-3798	112.5	18 x 85
1113	S693	-3816	242.5	18 x 85
1114	S694	-3834	112.5	18 x 85
1115	S695	-3852	242.5	18 x 85
1116	S696	-3870	112.5	18 x 85
1117	S697	-3888	242.5	18 x 85
1118	S698	-3906	112.5	18 x 85
1119	S699	-3924	242.5	18 x 85
1120	S700	-3942	112.5	18 x 85
1121	S701	-3960	242.5	18 x 85
1122	S702	-3978	112.5	18 x 85
1123	S703	-3996	242.5	18 x 85
1124	S704	-4014	112.5	18 x 85
1125	S705	-4032	242.5	18 x 85
1126	S706	-4050	112.5	18 x 85
1127	S707	-4068	242.5	18 x 85
1128	S708	-4086	112.5	18 x 85
1129	S709	-4104	242.5	18 x 85
1130	S710	-4122	112.5	18 x 85
1131	S711	-4140	242.5	18 x 85
1132	S712	-4158	112.5	18 x 85
1133	S713	-4176	242.5	18 x 85
1134	S714	-4194	112.5	18 x 85
1135	S715	-4212	242.5	18 x 85
1136	S716	-4230	112.5	18 x 85
1137	S717	-4248	242.5	18 x 85
1138	S718	-4266	112.5	18 x 85
1139	S719	-4284	242.5	18 x 85
1140	S720	-4302	112.5	18 x 85
1141	S721	-4320	242.5	18 x 85
1142	S722	-4338	112.5	18 x 85
1143	S723	-4356	242.5	18 x 85
1144	S724	-4374	112.5	18 x 85
1145	S725	-4392	242.5	18 x 85
1146	S726	-4410	112.5	18 x 85
1147	S727	-4428	242.5	18 x 85
1148	S728	-4446	112.5	18 x 85
1149	S729	-4464	242.5	18 x 85
1150	S730	-4482	112.5	18 x 85

No.	Name	X	Y	Bump size
1151	S731	-4500	242.5	18 x 85
1152	S732	-4518	112.5	18 x 85
1153	S733	-4536	242.5	18 x 85
1154	S734	-4554	112.5	18 x 85
1155	S735	-4572	242.5	18 x 85
1156	S736	-4590	112.5	18 x 85
1157	S737	-4608	242.5	18 x 85
1158	S738	-4626	112.5	18 x 85
1159	S739	-4644	242.5	18 x 85
1160	S740	-4662	112.5	18 x 85
1161	S741	-4680	242.5	18 x 85
1162	S742	-4698	112.5	18 x 85
1163	S743	-4716	242.5	18 x 85
1164	S744	-4734	112.5	18 x 85
1165	S745	-4752	242.5	18 x 85
1166	S746	-4770	112.5	18 x 85
1167	S747	-4788	242.5	18 x 85
1168	S748	-4806	112.5	18 x 85
1169	S749	-4824	242.5	18 x 85
1170	S750	-4842	112.5	18 x 85
1171	S751	-4860	242.5	18 x 85
1172	S752	-4878	112.5	18 x 85
1173	S753	-4896	242.5	18 x 85
1174	S754	-4914	112.5	18 x 85
1175	S755	-4932	242.5	18 x 85
1176	S756	-4950	112.5	18 x 85
1177	S757	-4968	242.5	18 x 85
1178	S758	-4986	112.5	18 x 85
1179	S759	-5004	242.5	18 x 85
1180	S760	-5022	112.5	18 x 85
1181	S761	-5040	242.5	18 x 85
1182	S762	-5058	112.5	18 x 85
1183	S763	-5076	242.5	18 x 85
1184	S764	-5094	112.5	18 x 85
1185	S765	-5112	242.5	18 x 85
1186	S766	-5130	112.5	18 x 85
1187	S767	-5148	242.5	18 x 85
1188	S768	-5166	112.5	18 x 85
1189	S769	-5184	242.5	18 x 85
1190	S770	-5202	112.5	18 x 85
1191	S771	-5220	242.5	18 x 85
1192	S772	-5238	112.5	18 x 85
1193	S773	-5256	242.5	18 x 85
1194	S774	-5274	112.5	18 x 85
1195	S775	-5292	242.5	18 x 85
1196	S776	-5310	112.5	18 x 85
1197	S777	-5328	242.5	18 x 85
1198	S778	-5346	112.5	18 x 85
1199	S779	-5364	242.5	18 x 85
1200	S780	-5382	112.5	18 x 85

No.	Name	X	Y	Bump size
1201	S781	-5400	242.5	18 x 85
1202	S782	-5418	112.5	18 x 85
1203	S783	-5436	242.5	18 x 85
1204	S784	-5454	112.5	18 x 85
1205	S785	-5472	242.5	18 x 85
1206	S786	-5490	112.5	18 x 85
1207	S787	-5508	242.5	18 x 85
1208	S788	-5526	112.5	18 x 85
1209	S789	-5544	242.5	18 x 85
1210	S790	-5562	112.5	18 x 85
1211	S791	-5580	242.5	18 x 85
1212	S792	-5598	112.5	18 x 85
1213	S793	-5616	242.5	18 x 85
1214	S794	-5634	112.5	18 x 85
1215	S795	-5652	242.5	18 x 85
1216	S796	-5670	112.5	18 x 85
1217	S797	-5688	242.5	18 x 85
1218	S798	-5706	112.5	18 x 85
1219	S799	-5724	242.5	18 x 85
1220	S800	-5742	112.5	18 x 85
1221	S801	-5760	242.5	18 x 85
1222	S802	-5778	112.5	18 x 85
1223	S803	-5796	242.5	18 x 85
1224	S804	-5814	112.5	18 x 85
1225	S805	-5832	242.5	18 x 85
1226	S806	-5850	112.5	18 x 85
1227	S807	-5868	242.5	18 x 85
1228	S808	-5886	112.5	18 x 85
1229	S809	-5904	242.5	18 x 85
1230	S810	-5922	112.5	18 x 85
1231	S811	-5940	242.5	18 x 85
1232	S812	-5958	112.5	18 x 85
1233	S813	-5976	242.5	18 x 85
1234	S814	-5994	112.5	18 x 85
1235	S815	-6012	242.5	18 x 85
1236	S816	-6030	112.5	18 x 85
1237	S817	-6048	242.5	18 x 85
1238	S818	-6066	112.5	18 x 85
1239	S819	-6084	242.5	18 x 85
1240	S820	-6102	112.5	18 x 85
1241	S821	-6120	242.5	18 x 85
1242	S822	-6138	112.5	18 x 85
1243	S823	-6156	242.5	18 x 85
1244	S824	-6174	112.5	18 x 85
1245	S825	-6192	242.5	18 x 85
1246	S826	-6210	112.5	18 x 85
1247	S827	-6228	242.5	18 x 85
1248	S828	-6246	112.5	18 x 85
1249	S829	-6264	242.5	18 x 85
1250	S830	-6282	112.5	18 x 85

No.	Name	X	Y	Bump size
1251	S831	-6300	242.5	18 x 85
1252	S832	-6318	112.5	18 x 85
1253	S833	-6336	242.5	18 x 85
1254	S834	-6354	112.5	18 x 85
1255	S835	-6372	242.5	18 x 85
1256	S836	-6390	112.5	18 x 85
1257	S837	-6408	242.5	18 x 85
1258	S838	-6426	112.5	18 x 85
1259	S839	-6444	242.5	18 x 85
1260	S840	-6462	112.5	18 x 85
1261	S841	-6480	242.5	18 x 85
1262	S842	-6498	112.5	18 x 85
1263	S843	-6516	242.5	18 x 85
1264	S844	-6534	112.5	18 x 85
1265	S845	-6552	242.5	18 x 85
1266	S846	-6570	112.5	18 x 85
1267	S847	-6588	242.5	18 x 85
1268	S848	-6606	112.5	18 x 85
1269	S849	-6624	242.5	18 x 85
1270	S850	-6642	112.5	18 x 85
1271	S851	-6660	242.5	18 x 85
1272	S852	-6678	112.5	18 x 85
1273	S853	-6696	242.5	18 x 85
1274	S854	-6714	112.5	18 x 85
1275	S855	-6732	242.5	18 x 85
1276	S856	-6750	112.5	18 x 85
1277	S857	-6768	242.5	18 x 85
1278	S858	-6786	112.5	18 x 85
1279	S859	-6804	242.5	18 x 85
1280	S860	-6822	112.5	18 x 85
1281	S861	-6840	242.5	18 x 85
1282	S862	-6858	112.5	18 x 85
1283	S863	-6876	242.5	18 x 85
1284	S864	-6894	112.5	18 x 85
1285	S865	-6912	242.5	18 x 85
1286	S866	-6930	112.5	18 x 85
1287	S867	-6948	242.5	18 x 85
1288	S868	-6966	112.5	18 x 85
1289	S869	-6984	242.5	18 x 85
1290	S870	-7002	112.5	18 x 85
1291	S871	-7020	242.5	18 x 85
1292	S872	-7038	112.5	18 x 85
1293	S873	-7056	242.5	18 x 85
1294	S874	-7074	112.5	18 x 85
1295	S875	-7092	242.5	18 x 85
1296	S876	-7110	112.5	18 x 85
1297	S877	-7128	242.5	18 x 85
1298	S878	-7146	112.5	18 x 85
1299	S879	-7164	242.5	18 x 85
1300	S880	-7182	112.5	18 x 85

No.	Name	X	Y	Bump size
1301	S881	-7200	242.5	18 x 85
1302	S882	-7218	112.5	18 x 85
1303	S883	-7236	242.5	18 x 85
1304	S884	-7254	112.5	18 x 85
1305	S885	-7272	242.5	18 x 85
1306	S886	-7290	112.5	18 x 85
1307	S887	-7308	242.5	18 x 85
1308	S888	-7326	112.5	18 x 85
1309	S889	-7344	242.5	18 x 85
1310	S890	-7362	112.5	18 x 85
1311	S891	-7380	242.5	18 x 85
1312	S892	-7398	112.5	18 x 85
1313	S893	-7416	242.5	18 x 85
1314	S894	-7434	112.5	18 x 85
1315	S895	-7452	242.5	18 x 85
1316	S896	-7470	112.5	18 x 85
1317	S897	-7488	242.5	18 x 85
1318	S898	-7506	112.5	18 x 85
1319	S899	-7524	242.5	18 x 85
1320	S900	-7542	112.5	18 x 85
1321	S901	-7560	242.5	18 x 85
1322	S902	-7578	112.5	18 x 85
1323	S903	-7596	242.5	18 x 85
1324	S904	-7614	112.5	18 x 85
1325	S905	-7632	242.5	18 x 85
1326	S906	-7650	112.5	18 x 85
1327	S907	-7668	242.5	18 x 85
1328	S908	-7686	112.5	18 x 85
1329	S909	-7704	242.5	18 x 85
1330	S910	-7722	112.5	18 x 85
1331	S911	-7740	242.5	18 x 85
1332	S912	-7758	112.5	18 x 85
1333	S913	-7776	242.5	18 x 85
1334	S914	-7794	112.5	18 x 85
1335	S915	-7812	242.5	18 x 85
1336	S916	-7830	112.5	18 x 85
1337	S917	-7848	242.5	18 x 85
1338	S918	-7866	112.5	18 x 85
1339	S919	-7884	242.5	18 x 85
1340	S920	-7902	112.5	18 x 85
1341	S921	-7920	242.5	18 x 85
1342	S922	-7938	112.5	18 x 85
1343	S923	-7956	242.5	18 x 85
1344	S924	-7974	112.5	18 x 85
1345	S925	-7992	242.5	18 x 85
1346	S926	-8010	112.5	18 x 85
1347	S927	-8028	242.5	18 x 85
1348	S928	-8046	112.5	18 x 85
1349	S929	-8064	242.5	18 x 85
1350	S930	-8082	112.5	18 x 85

No.	Name	X	Y	Bump size
1351	S931	-8100	242.5	18 x 85
1352	S932	-8118	112.5	18 x 85
1353	S933	-8136	242.5	18 x 85
1354	S934	-8154	112.5	18 x 85
1355	S935	-8172	242.5	18 x 85
1356	S936	-8190	112.5	18 x 85
1357	S937	-8208	242.5	18 x 85
1358	S938	-8226	112.5	18 x 85
1359	S939	-8244	242.5	18 x 85
1360	S940	-8262	112.5	18 x 85
1361	S941	-8280	242.5	18 x 85
1362	S942	-8298	112.5	18 x 85
1363	S943	-8316	242.5	18 x 85
1364	S944	-8334	112.5	18 x 85
1365	S945	-8352	242.5	18 x 85
1366	S946	-8370	112.5	18 x 85
1367	S947	-8388	242.5	18 x 85
1368	S948	-8406	112.5	18 x 85
1369	S949	-8424	242.5	18 x 85
1370	S950	-8442	112.5	18 x 85
1371	S951	-8460	242.5	18 x 85
1372	S952	-8478	112.5	18 x 85
1373	S953	-8496	242.5	18 x 85
1374	S954	-8514	112.5	18 x 85
1375	S955	-8532	242.5	18 x 85
1376	S956	-8550	112.5	18 x 85
1377	S957	-8568	242.5	18 x 85
1378	S958	-8586	112.5	18 x 85
1379	S959	-8604	242.5	18 x 85
1380	DUMMY	-8622	112.5	18 x 85
1381	DUMMY	-8640	242.5	18 x 85
1382	DUMMY	-8658	112.5	18 x 85
1383	DUMMY	-8676	242.5	18 x 85
1384	DUMMY	-8694	112.5	18 x 85
1385	DUMMY	-8712	242.5	18 x 85
1386	DUMMY	-8730	112.5	18 x 85
1387	DUMMY	-8748	242.5	18 x 85
1388	DUMMY	-8766	112.5	18 x 85
1389	G238	-8784	242.5	18 x 85
1390	G236	-8802	112.5	18 x 85
1391	G234	-8820	242.5	18 x 85
1392	G232	-8838	112.5	18 x 85
1393	G230	-8856	242.5	18 x 85
1394	G228	-8874	112.5	18 x 85
1395	G226	-8892	242.5	18 x 85
1396	G224	-8910	112.5	18 x 85
1397	G222	-8928	242.5	18 x 85
1398	G220	-8946	112.5	18 x 85
1399	G218	-8964	242.5	18 x 85
1400	G216	-8982	112.5	18 x 85

No.	Name	X	Y	Bump size
1401	G214	-9000	242.5	18 x 85
1402	G212	-9018	112.5	18 x 85
1403	G210	-9036	242.5	18 x 85
1404	G208	-9054	112.5	18 x 85
1405	G206	-9072	242.5	18 x 85
1406	G204	-9090	112.5	18 x 85
1407	G202	-9108	242.5	18 x 85
1408	G200	-9126	112.5	18 x 85
1409	G198	-9144	242.5	18 x 85
1410	G196	-9162	112.5	18 x 85
1411	G194	-9180	242.5	18 x 85
1412	G192	-9198	112.5	18 x 85
1413	G190	-9216	242.5	18 x 85
1414	G188	-9234	112.5	18 x 85
1415	G186	-9252	242.5	18 x 85
1416	G184	-9270	112.5	18 x 85
1417	G182	-9288	242.5	18 x 85
1418	G180	-9306	112.5	18 x 85
1419	G178	-9324	242.5	18 x 85
1420	G176	-9342	112.5	18 x 85
1421	G174	-9360	242.5	18 x 85
1422	G172	-9378	112.5	18 x 85
1423	G170	-9396	242.5	18 x 85
1424	G168	-9414	112.5	18 x 85
1425	G166	-9432	242.5	18 x 85
1426	G164	-9450	112.5	18 x 85
1427	G162	-9468	242.5	18 x 85
1428	G160	-9486	112.5	18 x 85
1429	G158	-9504	242.5	18 x 85
1430	G156	-9522	112.5	18 x 85
1431	G154	-9540	242.5	18 x 85
1432	G152	-9558	112.5	18 x 85
1433	G150	-9576	242.5	18 x 85
1434	G148	-9594	112.5	18 x 85
1435	G146	-9612	242.5	18 x 85
1436	G144	-9630	112.5	18 x 85
1437	G142	-9648	242.5	18 x 85
1438	G140	-9666	112.5	18 x 85
1439	G138	-9684	242.5	18 x 85
1440	G136	-9702	112.5	18 x 85
1441	G134	-9720	242.5	18 x 85
1442	G132	-9738	112.5	18 x 85
1443	G130	-9756	242.5	18 x 85
1444	G128	-9774	112.5	18 x 85
1445	G126	-9792	242.5	18 x 85
1446	G124	-9810	112.5	18 x 85
1447	G122	-9828	242.5	18 x 85
1448	G120	-9846	112.5	18 x 85
1449	G118	-9864	242.5	18 x 85
1450	G116	-9882	112.5	18 x 85

No.	Name	X	Y	Bump size
1451	G114	-9900	242.5	18 x 85
1452	G112	-9918	112.5	18 x 85
1453	G110	-9936	242.5	18 x 85
1454	G108	-9954	112.5	18 x 85
1455	G106	-9972	242.5	18 x 85
1456	G104	-9990	112.5	18 x 85
1457	G102	-10008	242.5	18 x 85
1458	G100	-10026	112.5	18 x 85
1459	G98	-10044	242.5	18 x 85
1460	G96	-10062	112.5	18 x 85
1461	G94	-10080	242.5	18 x 85
1462	G92	-10098	112.5	18 x 85
1463	G90	-10116	242.5	18 x 85
1464	G88	-10134	112.5	18 x 85
1465	G86	-10152	242.5	18 x 85
1466	G84	-10170	112.5	18 x 85
1467	G82	-10188	242.5	18 x 85
1468	G80	-10206	112.5	18 x 85
1469	G78	-10224	242.5	18 x 85
1470	G76	-10242	112.5	18 x 85
1471	G74	-10260	242.5	18 x 85
1472	G72	-10278	112.5	18 x 85
1473	G70	-10296	242.5	18 x 85
1474	G68	-10314	112.5	18 x 85
1475	G66	-10332	242.5	18 x 85
1476	G64	-10350	112.5	18 x 85
1477	G62	-10368	242.5	18 x 85
1478	G60	-10386	112.5	18 x 85
1479	G58	-10404	242.5	18 x 85
1480	G56	-10422	112.5	18 x 85
1481	G54	-10440	242.5	18 x 85
1482	G52	-10458	112.5	18 x 85
1483	G50	-10476	242.5	18 x 85
1484	G48	-10494	112.5	18 x 85
1485	G46	-10512	242.5	18 x 85
1486	G44	-10530	112.5	18 x 85
1487	G42	-10548	242.5	18 x 85
1488	G40	-10566	112.5	18 x 85
1489	G38	-10584	242.5	18 x 85
1490	G36	-10602	112.5	18 x 85
1491	G34	-10620	242.5	18 x 85
1492	G32	-10638	112.5	18 x 85
1493	G30	-10656	242.5	18 x 85
1494	G28	-10674	112.5	18 x 85
1495	G26	-10692	242.5	18 x 85
1496	G24	-10710	112.5	18 x 85
1497	G22	-10728	242.5	18 x 85
1498	G20	-10746	112.5	18 x 85
1499	G18	-10764	242.5	18 x 85
1500	G16	-10782	112.5	18 x 85

No.	Name	X	Y	Bump size
1501	G14	-10800	242.5	18 x 85
1502	G12	-10818	112.5	18 x 85
1503	G10	-10836	242.5	18 x 85
1504	G8	-10854	112.5	18 x 85
1505	G6	-10872	242.5	18 x 85
1506	G4	-10890	112.5	18 x 85
1507	G2	-10908	242.5	18 x 85
1508	G0	-10926	112.5	18 x 85
1509	DUMMY	-10944	242.5	18 x 85
1510	DUMMY	-10962	112.5	18 x 85
1511	DUMMY	-10980	242.5	18 x 85
1512	DUMMY	-10998	112.5	18 x 85
1513	DUMMY	-11016	242.5	18 x 85

Name	X	Y
Alignmark_R	10862.5	-232.5
Alignmark_L	-10862.5	-232.5

16. Ordering Information

Part NO.	Package
HX8238-D00BPDXXX	PD: means COG XXX: means chip thickness(μm), default 400μm

17. Revision History

Version	Date	Description of Changes
01	2007/06/08	New setup
	2007/07/05	1. Change Chip size. 2. Change pad location and alignment mark location.
	2007/07/31	1. Modify CPE pin and register definition on VCOM. 2. Add LED driver control function on register PWMS, PWMF[3:0], DUTY[7:0]. 3. Change OTP program time to twice on CTM's site.
	2007/08/02	1. Modify PWMF[3:0] setting 2. Change nOTP definition and default value.
	2007/08/07	1. Change nOTP definition and default value. 2. Change PWMS, PWMF[3:0], DUTY[7:0] from register R07 to R08.
	2007/08/10	1. Modify Fig 16.2 Power Supply Pin Connection. 2. Modify all R07 to R08. 3. Modify DUTY[7:0] default value = FF (Page 39)
	2007/08/22	1. Modify the Fig 14.9 Power up sequence 2. Modify the Fig 14.10 Power down sequence.
	2007/09/05	1. Modify the default value R1Eh Power Control VCM[6:0] from 1010010 to 1011111(Page 15)
	2007/10/12	1. Add the Secondary SPI Register. 2. Modify the default value BT[2:0] from 011 to 100.
	2007/11/15	1. Add the OTD and OTF in R1Ah of the Secondary SPI register.(Page 33) 2. Modify the description of the MSEL and POC.(Page 41) 3. Modify the value of the VCOM amplitude to control by VDV[4:0](Page 42) 4. Add the description of the VCOM in POWER ON/OFF sequence.(Page 50)
02	2008/03/11	1. Revised the SDT[1:0] definition in Secondary SPI.(Page 40) 2. Revised the Power Up Sequnce.(Page 71) 3. Change VDDIO range from 1.6V ~ 3.6V.(All page)
03	2008/06/05	1. Revised the SPSW description. (Page 10) 2. Modify the Capacitors on VCIX2 to 4.7μF. (Page 77)
	2008/09/19	1. Add the voltage of the VCOMR description. (Page 27, 41)
	2008/10/29	1. Add the description of the data transaction timing in normal operating mode.(Page 63) 2. Add the description of the data transaction timing in DE Only operating mode.(Page 64)
04	2010/04/15	3. Change VDDIO range from 1.8V ~ 3.6V.(All page)
05	2010/09/10	1. Revised the OTP programming voltage and waiting time.
06	2012/01/03	Page 10 1. Revised Bump Height spec.